

Article

Analysis of a Wide Voltage Hybrid Soft Switching Converter

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Abstract: A hybrid PWM converter is proposed and investigated to realize the benefits of wide zero-voltage switching (ZVS) operation, wide voltage input operation, and low circulating current for direct current (DC) wind power conversion and solar PV power conversion applications. Compared to the drawbacks of high freewheeling current and hard switching operation of active devices at the lagging-leg of conventional full bridge PWM converter, a three-leg PWM converter is studied to have wide input-voltage operation (120–600 V). For low input-voltage condition (120–270 V), two-leg full bridge converter with lower transformer turns ratio is activated to control load voltage. For high input-voltage case (270–600 V), PWM converter with higher transformer turns ratio is operated to regulate load voltage. The LLC resonant converter is connecting to the lagging-leg switches in order to achieve wide load range of soft switching turn-on operation. The high conduction losses at the freewheeling state on conventional full bridge converter are overcome by connecting the output voltage of resonant converter to the output rectified terminal of full bridge converter. Hence, a 5:1 (600–120 V) hybrid converter is realized to have less circulating current loss, wide input-voltage operation and wide soft switching characteristics. An 800 W prototype is set up and tested to validate the converter effectiveness.

Keywords: pulse-width modulation; DC converters; wide voltage variation; freewheeling current



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1. Introduction

For past years, clean and sustainable energy has received increased attention to reduce greenhouse gas emissions and fossil energy demand. Photovoltaic (PV) solar cell, fuel cell stacks, and DC wind power are attractive sustainable energy sources as they are cost-effective [1–4]. The main drawback of these sustainable energy sources is that the output DC or AC voltage is not constant. To solve this problem, the soft switching high-frequency DC-DC converters have been developed by using switching frequency modulation [5,6], pulse-width modulation (PWM) [7–10], active clamp PWM [11,12], and asymmetric PWM [13,14] schemes. The main drawbacks of active clamp PWM and asymmetric PWM schemes are the unbalance current and voltage stresses on the rectifier diodes. In resonant converters, the operating switching frequency depends on the load power and input voltage so that the load voltage is controlled by frequency modulation. However, the wide output-voltage variation of sustainable energy sources will result in wide switching frequency deviation in resonant converters. In PWM scheme, the duty ratio (or duty cycle) on active devices or input leg voltage of PWM converter depends on input voltage. Thus, the duty cycle of PWM converter can be regulated to counteract input voltage variation. Generally, the maximum (minimum) effective duty ratio $d_{eff,max}$ ($d_{eff,min}$) is related to minimum (maximum) input voltage $V_{in,min}$ ($V_{in,max}$). Due to duty loss problem at the freewheeling state on conventional phase-shift PWM converter, the effective duty ratio d_{eff} is usually designed to be greater than 0.15 and less than 0.45. Hence, input voltage variation will be limited at $V_{in,max}/V_{in,min} = d_{eff,max}/d_{eff,min} < 3$ on conventional phase-shift PWM operation. As the voltage deviation from PV panels and DC wind generator outputs may be greater than 3, the cascaded or parallel-connected circuit structures [15–17] have been developed to

overcome this problem. However, the low efficiency is the main problem of cascaded PWM converters. In serial- and parallel-connected circuit topology with wide voltage operation in [15,16], the component counts, high circulating current, and the complicated control algorithm are the main disadvantages. However, the maximum voltage deviation in [15–17] is still less than 4 ($V_{in,max}/V_{in,min} < 4$). The DC converters with more than 5 ($V_{in,max}/V_{in,min} > 5$) wide voltage capability are normally demanded for renewable energy.

A hybrid converter with a three-leg phase-shift PWM circuit and a LLC circuit are presented and realized to have benefits of wide load range of zero voltage switching (ZVS), less circulating current loss, and wide input voltage capability (120–600 V). On the basis of input voltage, two sub-circuits are selected to operate in order to overcome wide input-voltage deviation. One AC switch is adopted to select one of two sub-circuits under low or high input-voltage condition. Therefore, a 5:1 ($V_{in,max} = 5 V_{in,min}$) wide input voltage hybrid converter is achieved. The phase-shift PWM approach is used to control output voltage. Power devices at the leading leg can be easily turned on at ZVS because the output inductor energy is used to release energy stored on output capacitor of active devices. The hard switching disadvantage of lagging-leg active devices in conventional full bridge converter is overcome by connecting a LLC resonant circuit to the lagging-leg active devices. Therefore, the lagging-leg active devices are turned on at ZVS. In circuit implementation, a Schmitt comparator with a ± 30 V hysteresis range is adopted to select the appropriate sub-circuit under high or low voltage input operation. The control scheme can be easily implemented by using logic gates, comparator, and phase-shift PWM integrated circuit. The benefits of the studied hybrid zero-voltage switching (ZVS) converter are confirmed by an 800 W experimental prototype.

2. Structure of the Proposed Converter

The converter diagram of conventional full bridge PWM converter is given in Figure 1a. The main benefit of full bridge PWM converter is ZVS operation on S_1 and S_2 (leading-leg switches). However, the full bridge PWM converter has several drawbacks, such as hard switching operation on S_3 and S_4 (lagging-leg switches) and high primary current loss at the freewheeling state $v_{ab} = 0$ when S_1 and S_3 are ON or S_2 and S_4 are ON. Therefore, serious switching losses can be generated at the lagging leg and high conduction losses will be generated on the primary side under low duty cycle condition. To overcome hard switching loss, a LLC resonant circuit (L_r , T_2 , C_r , D_3 , D_4 , C_{LLC} and D_5) remark in red (Figure 1b) is adopted and connected to the lagging-leg switches. As LLC resonant circuit is operated at constant frequency ($f_{sw} = f_r$ resonant frequency of L_r and C_r), active devices S_3 and S_4 can achieve ZVS operation. The other drawback of conventional PWM converter in Figure 1a is the serious circulating current loss at the freewheeling state $v_{ab} = 0$. To solve this problem, diode D_5 is used to connect two voltage terminals $V_{o,LLC}$ and V_R on the secondary side. Therefore, the secondary rectified voltage V_R is positive in Figure 1b instead of $V_R = 0$ in Figure 1a during the freewheeling interval. During the forward power flow from V_{in} to V_o , the primary-side leg voltage $|v_{ab}| \approx V_{in}$ and the secondary rectified voltage $V_R \approx V_{in} n_s / n_{p1} > V_{o,LLC}$. Thus, diode D_5 is reverse biased. Diode D_5 is forward biased during the freewheeling interval ($v_{ab} = 0$). Because D_5 is conducting, the energy on C_{LLC} is transferred to V_o at the freewheeling state. In the freewheeling interval, the rectified voltage $V_R = V_{o,LLC} > 0$, the primary inductor voltage $V_{LR} = -(n_{p1}/n_{s1})V_{o,LLC}$, and the primary current i_{LR} are decreased. For some renewable energy power conversions for solar power or wind power applications, the DC converters with wide voltage operation capability are needed in order to counteract wide input voltage variation. Conventional full bridge PWM converter can operate well with narrow voltage variation, such as $V_{in,max}/V_{in,min} < 3$. For more wide voltage deviation, the conventional full bridge PWM circuit cannot achieve this demand. To achieve wide voltage deviation request, three leg PWM converter is adopted and shown in Figure 1c. Comparing the circuit diagrams in Figure 1b,c, it can be noted, one more switch leg with components S_1 , S_2 , and Q remark in blue is adopted in the presented

circuit. The transformer T_1 has four winding turns n_{p1} , n_{p1} , n_{s1} , and n_{s1} . Switch Q is used to control turns ratio of T_1 under the different input voltage regions.

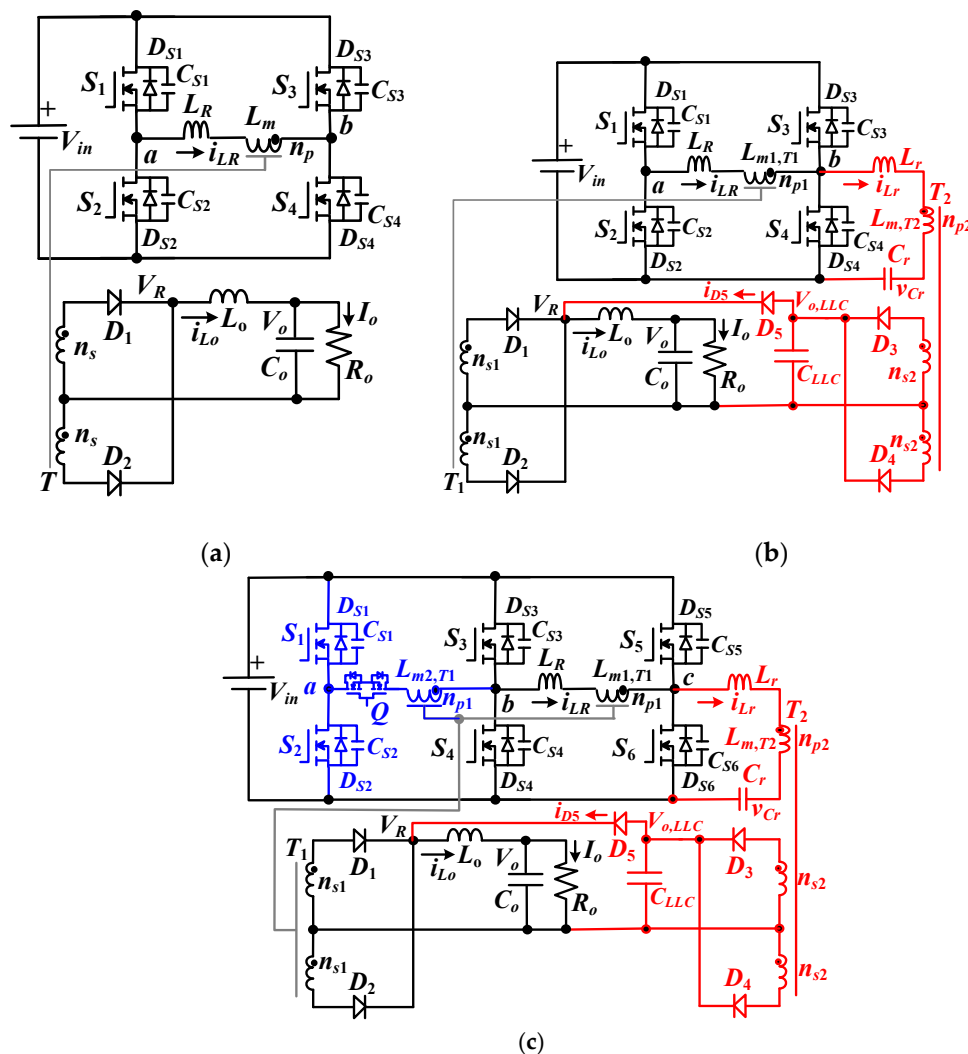


Figure 1. Circuit structure (a) conventional phase-shift PWM converter, (b) hybrid soft switching PWM converter with less primary current at the freewheeling state, (c) proposed hybrid soft switching PWM converter with wide input voltage operation and less primary current at the freewheeling state.

When $120\text{ V} \leq V_{in} < 270\text{ V}$ (low voltage region, $V_{in,L}$), the proposed converter with high voltage gain is requested to keep load voltage constant. Therefore, active devices Q , S_1 , and S_2 are OFF, as shown in Figure 2a. Only S_3 – S_6 are activated to regulate V_o . Circuit S_3 – S_6 , T_1 , L_R , D_1 , D_2 , and L_o are activated as the full bridge phase-shift PWM converter. The leading-leg active devices S_3 and S_4 can easily turn on at ZVS operation. The turns-ratio of T_1 is n_{p1}/n_{s1} under low voltage input range. Circuit structure with components S_5 , S_6 , T_2 , L_r , C_r , D_3 , D_4 , and C_{LLC} is operated as the LLC series resonant converter. Due to the resonant behavior, the lagging leg active devices S_5 and S_6 are turned on at ZVS. When $270\text{ V} \leq V_{in} < 600\text{ V}$ (high voltage region, $V_{in,H}$), Q is ON and S_3 and S_4 are OFF, as shown in Figure 2b. S_1 , S_2 , S_5 , and S_6 are activated to control load voltage V_o . Circuit structure with components S_1 , S_2 , S_5 , S_6 , T_1 , L_R , D_1 , D_2 , and L_o are activated as the full bridge phase-shift PWM circuit. The leading-leg active devices S_1 and S_2 turn on at ZVS. The turns-ratio of T_1 in Figure 2b is $2n_{p1}/n_{s1}$ under high voltage input range. Due to LLC circuit connected to the lagging leg, S_5 and S_6 are turned on at ZVS. From the previous discussion, it is clear that the presented hybrid converter has soft switching

operation, wide input-voltage operation ($V_{in,max}/V_{in,min} = 5$), and less primary current at the freewheeling state.

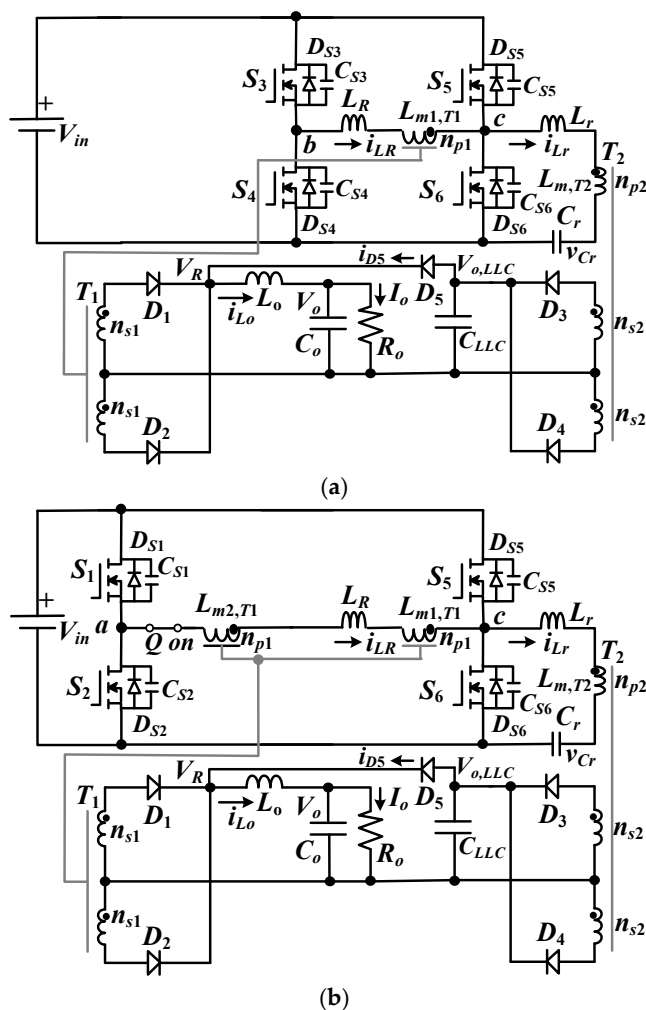


Figure 2. Proposed hybrid PWM converter (a) operated at low voltage operation, $120\text{ V} \leq V_{in} < 270\text{ V}$, (b) operated at high voltage operation, $270\text{ V} < V_{in} \leq 600\text{ V}$.

3. Principle of Operation

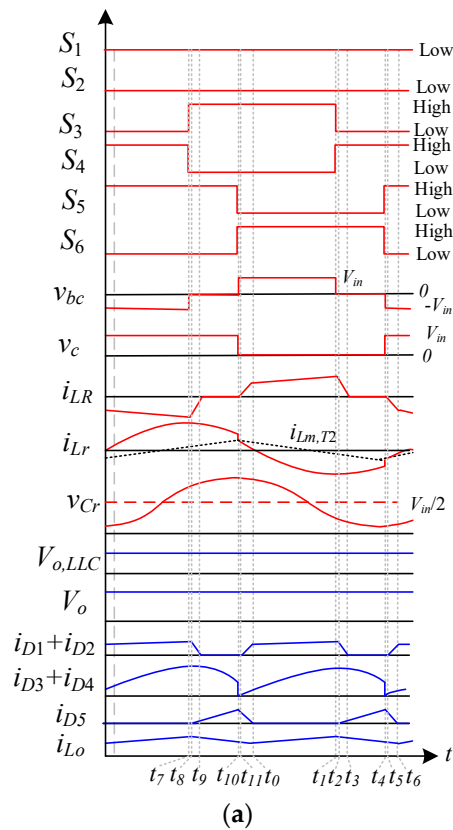
If V_{in} is in the low voltage region ($V_{in,L} = 120\text{--}270\text{ V}$), active devices Q , S_1 , and S_2 are all turned off. Power switches $S_3\text{--}S_6$ and passive components T_1 , L_R , D_1 , D_2 , and L_o are operated with PWM approach to control load voltage V_o . LLC resonant circuit with components S_5 , S_6 , T_2 , L_r , C_r , D_3 , D_4 , and C_{LLC} is operated with fixed switching frequency to achieve ZVS operation of S_5 and S_6 . It is assumed the inductances $L_{m1} = L_{m2} \gg L_R$ and capacitances $C_{S1} = \dots = C_{S6} = C_{oss}$. The PWM waveforms under the low input-voltage region are given in Figure 3a. One can observe that there are six states (Figure 3b–g) in each half switching cycle. The PWM waveforms are symmetrical in every half switching period. To simplify the system analysis, only the operating states in the first half switching period are stated in this section.

State 1 [$t_0 \leq t < t_1$]: In state 1, S_3 and S_6 are in the on-state and leg voltage $v_{bc} = V_{in}$. LLC converter is controlled at the resonant frequency. As S_6 is in the on-state, i_{Lr} decreases and $i_{Lr} < i_{Lm,T2}$. The secondary diodes D_1 and D_4 are forward biased. The drain voltages

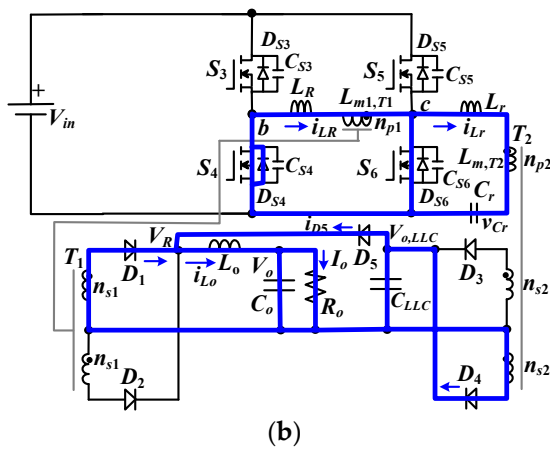
$v_{CS4} = v_{CS5} = V_{in}$ and the diode voltages $v_{D2} \approx 2 \times V_{in}/(n_p/n_{s1})$ and $v_{D3} \approx 2 V_{o,LLC}$. The currents i_{Lo} and i_{LR} are expressed in Equations (1) and (2):

$$i_{Lo}(t) \approx i_{Lo}(t_0) + \frac{\frac{V_{in}}{n_{p1}/n_{s1}} - V_o}{L_o}(t - t_0) \tag{1}$$

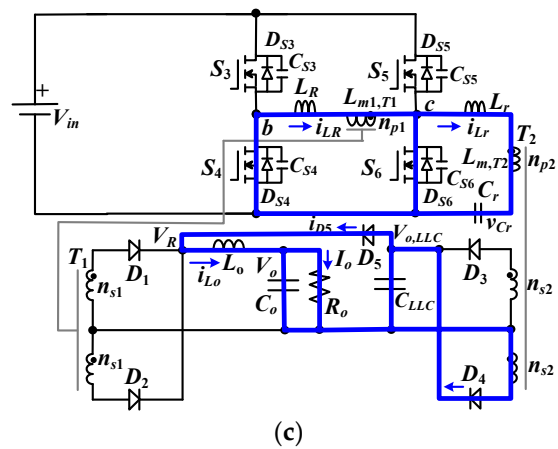
$$i_{LR}(t) \approx i_{LR}(t_0) + \frac{V_{in} - \frac{n_{p1}V_o}{n_{s1}}}{(n_{p1}/n_{s1})^2 L_o}(t - t_0) \tag{2}$$



(a)



(b)



(c)

Figure 3. Cont.

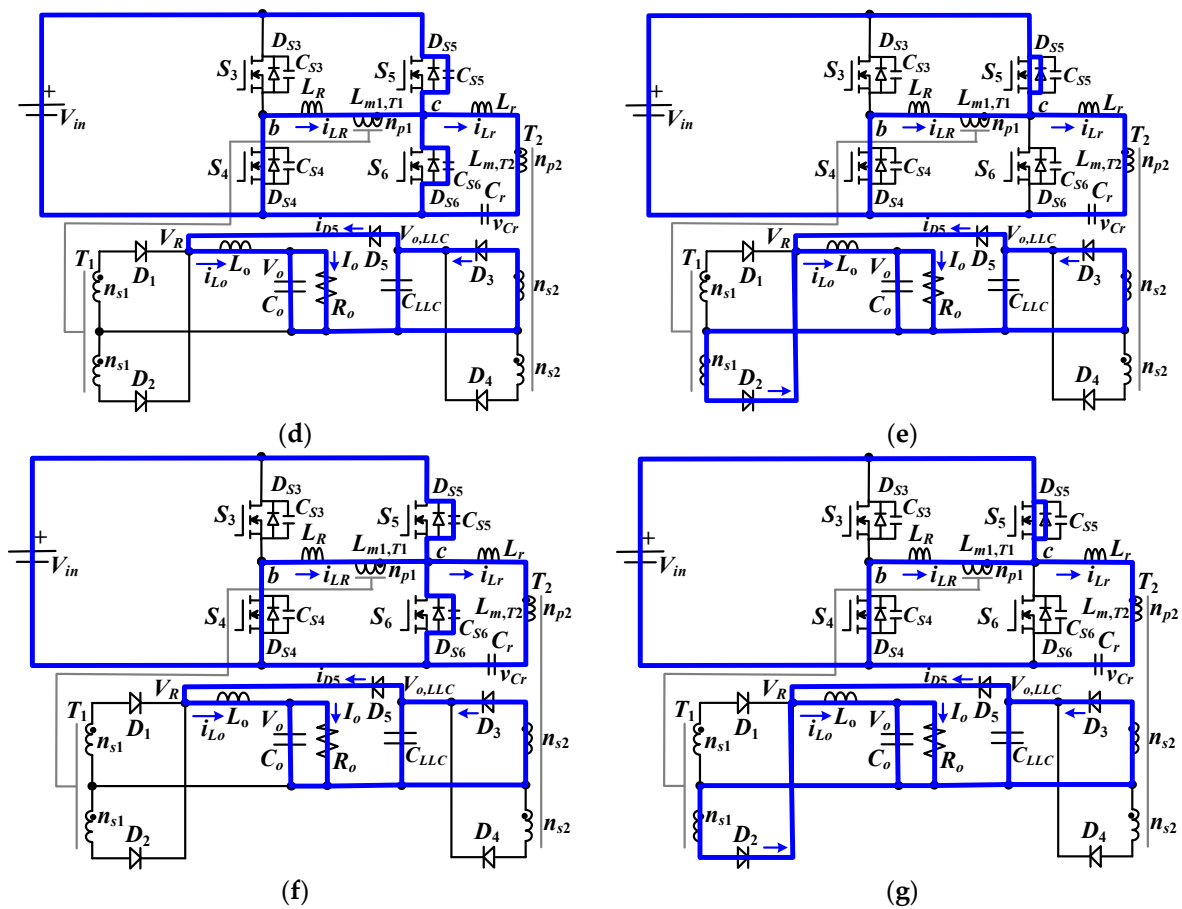


Figure 3. Low input-voltage region operation (a) PWM waveforms, (b) state 1, (c) state 2, (d) state 3, (e) state 4, (f) state 5, (g) state 6.

State 2 [$t_1 \leq t < t_2$]: At t_1 , S_3 turns off. As $i_{LR}(t_1) > 0$, C_{S4} is discharged by i_{LR} after time t_1 . If the inductor energy $[L_R + (n_{p1}/n_{s1})^2 L_o] i_{LR}^2(t_1) > 2C_{oss} V_{in}^2$, v_{CS4} is decreased and will be equal to 0 at t_2 . The discharged time of C_{S4} is expressed as:

$$\Delta t_{12} \approx (2V_{in} C_{oss} n_{p1}) / (I_o n_{s1}) \quad (3)$$

LLC converter is still controlled at the resonant mode to distribute power from V_{in} to $V_{o,LLC}$.

State 3 [$t_2 \leq t < t_3$]: At t_2 , v_{CS4} is decreased and equal to zero voltage. Since $i_{LR}(t_2) > 0$, D_{S4} is conducting and S_4 can turn on to have soft switching operation. Due to $v_{bc} = 0$, the diode D_5 becomes forward biased and the rectified voltage V_R is clamped at $V_{o,LLC}$. Therefore, the inductor voltages $v_{LR} = -n_{p1} V_{o,LLC} / n_{s1} < 0$ and $v_{L_o} = V_{o,LLC} - V_o < 0$. i_{LR} and i_{L_o} are decreased in this state.

$$i_{L_o}(t) \approx i_{L_o}(t_2) + \frac{V_{o,LLC} - V_o}{L_o} (t - t_2) \quad (4)$$

$$i_{LR}(t) \approx i_{LR}(t_2) - \frac{n_{p1} V_{o,LLC}}{n_{s1} L_R} (t - t_2) \quad (5)$$

However, the conventional full bridge converter has $v_{LR} \approx 0$ and $i_{LR} \approx$ constant in this state (freewheeling state). Therefore, the conventional full bridge PWM converter has more circulating current loss in this state. In Equation (5), one can observe the primary current i_{LR} is decreased at freewheeling state in the proposed converter. If the time interval

at freewheeling state is long enough, the diode current i_{D1} or the primary current i_{LR} can be declined to zero.

$$\Delta t_{i_{LR}=0} \approx L_R I_o / [(n_{p1}/n_{s1})^2 V_{o,LLC}] \quad (6)$$

The time $\Delta t_{i_{Lp}=0}$ is related to L_R , $V_{o,LLC}$, and I_o . Thus, more freewheeling time duration is required at full load to eliminate the circulating current.

State 4 [$t_3 \leq t < t_4$]: At t_3 , $i_{D1} = 0$ and $i_{LR} \approx 0$. The diode current $i_{D5} = i_{L_o}$. Thus, the circulating current of i_{LR} is almost removed at freewheeling state ($v_{bc} = 0$). The inductor voltage $v_{L_o} = V_{o,LLC} - V_o < 0$ so that i_{L_o} decreases.

State 5 [$t_4 \leq t < t_5$]: S_6 is turned off at t_4 . Since $i_{L_r}(t_4) - i_{LR}(t_4)$ is negative, C_{S5} will be discharged. In LLC converter, D_3 becomes forward biased as $i_{L_r} > i_{L_m,T2}$ after time t_4 . C_{S5} will be discharged to zero voltage at t_5 .

State 6 [$t_5 \leq t < t_6$]: State 6 starts at time t_5 when v_{CS5} is declined to zero. Due to $i_{LR}(t_5) - i_{L_r}(t_5) > 0$, D_{S5} becomes forward biased. Then, S_5 can be turned on after time t_5 to realize soft switching operation. In this state, $v_{bc} = -V_{in}$ and D_2 becomes forward biased. Owing to $i_{D2}(t_5) < i_{L_o}(t_5)$, D_5 is conducting and $V_R = V_{o,LLC}$. The inductor voltage $v_{LR} \approx n_{p1}V_{o,LLC}/n_{s1} - V_{in} < 0$ and the primary current i_{LR} decreases in this state. At the end of state 6, the diode current i_{D2} is equal to i_{L_o} so that D_5 becomes reverse biased and the primary current $i_{LR} \approx -n_{s1}i_{L_o}/n_{p1}$. The time duration of state 6 is obtained and expressed in Equation (7):

$$\Delta t_{56} \approx I_o L_R / [n_{p1}(V_{in} - n_{p1}V_{o,LLC}/n_{s1})/n_{s1}] \quad (7)$$

Since D_5 is forward biased, the duty loss in state 6 is calculated in Equation (8):

$$d_6 \approx f_{sw} I_o L_R / [n_{p1}(V_{in} - n_{p1}V_{o,LLC}/n_{s1})/n_{s1}] \quad (8)$$

In this state, $v_{L_o} = V_{o,LLC} - V_o < 0$ so that i_{L_o} decreases. At time t_6 , the converter goes to the next half switching period.

When V_{in} is in the high voltage region ($V_{in,L} = 270 \text{ V} - 600 \text{ V}$), Q is turned on and S_3 and S_4 are turned off. Switches S_1 , S_2 , S_5 , and S_6 and passive components T_1 , L_R , D_1 , D_2 , and L_o are controlled by phase shift PWM scheme. Components S_5 , S_6 , T_2 , L_r , C_r , D_3 , D_4 , and C_{LLC} are operated as the LLC resonant circuit to have ZVS operation of S_5 and S_6 . The turns ratio of full bridge converter under the high input-voltage region is $2n_{p1}/n_{s1}$ in Figure 2b. Figure 4a shows PWM waveforms for high voltage input region. Figure 4b–g provides the equivalent state circuits for first half switching period.

State 1 [$t_0 \leq t < t_1$]: In this state, switches S_1 and S_6 are ON and the leg voltage $v_{ac} = V_{in}$. LLC converter (S_6 , L_r , T_2 , C_r , D_4 , and C_{LLC}) is operated at the resonant frequency. On the secondary side, D_1 and D_4 are conducting. The drain voltages $v_{CS2} = v_{CS5} = V_{in}$ and the diode voltage stresses $v_{D2} \approx V_{in}n_{s1}/n_{p1}$ and $v_{D3} \approx 2V_{o,LLC}$. The inductor currents i_{L_o} and i_{LR} are increased and i_{L_r} is decreased in this state.

State 2 [$t_1 \leq t < t_2$]: At t_1 , switch S_1 is turned off. Owing to $i_{LR}(t_1) > 0$, i_{LR} discharges C_{S2} . If the inductor energy $[L_R + (2n_{p1}/n_{s1})^2 L_o]i_{LR}^2(t_1) > 2C_{oss}V_{in}^2$, then C_{S4} can be completely discharged to zero voltage.

State 3 [$t_2 \leq t < t_3$]: At t_2 , $v_{CS2} = 0$. Since $i_{LR}(t_2) > 0$, D_{S2} conducts and S_2 is turned on at ZVS. In this state, the leg voltage $v_{ac} = 0$ so that D_5 is forward biased. Therefore, the rectified voltage $V_R = V_{o,LLC}$, $v_{LR} = -2 \times n_{p1}V_{o,LLC}/n_{s1} < 0$ and $v_{L_o} = V_{o,LLC} - V_o < 0$. The inductor currents i_{L_r} , i_{L_o} , and i_{LR} are all decreased in state 3. If the primary currents i_{LR} or i_{D1} can be declined to zero, then the necessary time interval of the freewheeling state at the high input-voltage region is derived as:

$$\Delta t_{i_{LR}=0} \approx L_R I_o / [(2n_{p1}/n_{s1})^2 V_{o,LLC}] \quad (9)$$

If $i_{D1} = 0$ at t_3 , then the circuit operation goes to state 4. If i_{D1} is not equal to zero at the end of the freewheeling state, then the circuit goes to state 5.

State 4 [$t_3 \leq t < t_4$]: At t_3 , $i_{D1} = 0$. One can observe $i_{D5} = i_{Lo}$ and the primary current i_{LR} is approximately equal to zero when $v_{ac} = 0$ (freewheeling state). Since D_5 is conducting, power is delivered to V_o through LLC resonant converter in state 4.

State 5 [$t_4 \leq t < t_5$]: At t_4 , S_6 turns off. Owing to $i_{LR}(t_4) - i_{Lr}(t_4) > 0$, C_{S5} will be discharged. In LLC circuit, D_3 is conducting. At t_5 , v_{CS5} is decreased to zero voltage.

State 6 [$t_5 \leq t < t_6$]: At t_5 , $v_{CS5} = 0$. Owing to $i_{LR}(t_5) - i_{Lr}(t_5) > 0$, D_{S5} is conducting. Thus, S_5 is turned on at ZVS. In state 6, $v_{ac} = -V_{in}$ and D_2 is forward biased. Due to $i_{D2}(t_5) < i_{Lo}(t_5)$, D_5 is still conducting and $V_R = V_{o,LLC}$. The primary inductor voltage $v_{LR} \approx 2n_{p1}V_{o,LLC}/n_{s1} - V_{in} < 0$ and i_{LR} decreases. At the end of state 6, the diode current $i_{D2} = i_{Lo}$ so that D_5 is conducting. The duty loss at state 6 under the high input-voltage region is obtained as:

$$d_6 \approx f_{sw} I_o L_R / [2n_{p1} (V_{in} - 2n_{p1} V_{o,LLC} / n_{s1}) / n_{s1}] \tag{10}$$

At time t_6 , the converter goes to the next half switching period.

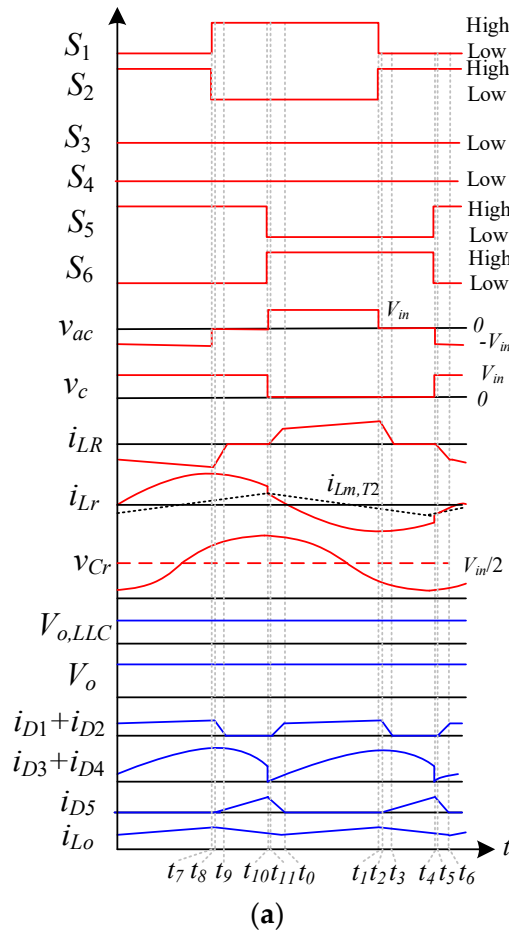


Figure 4. Cont.

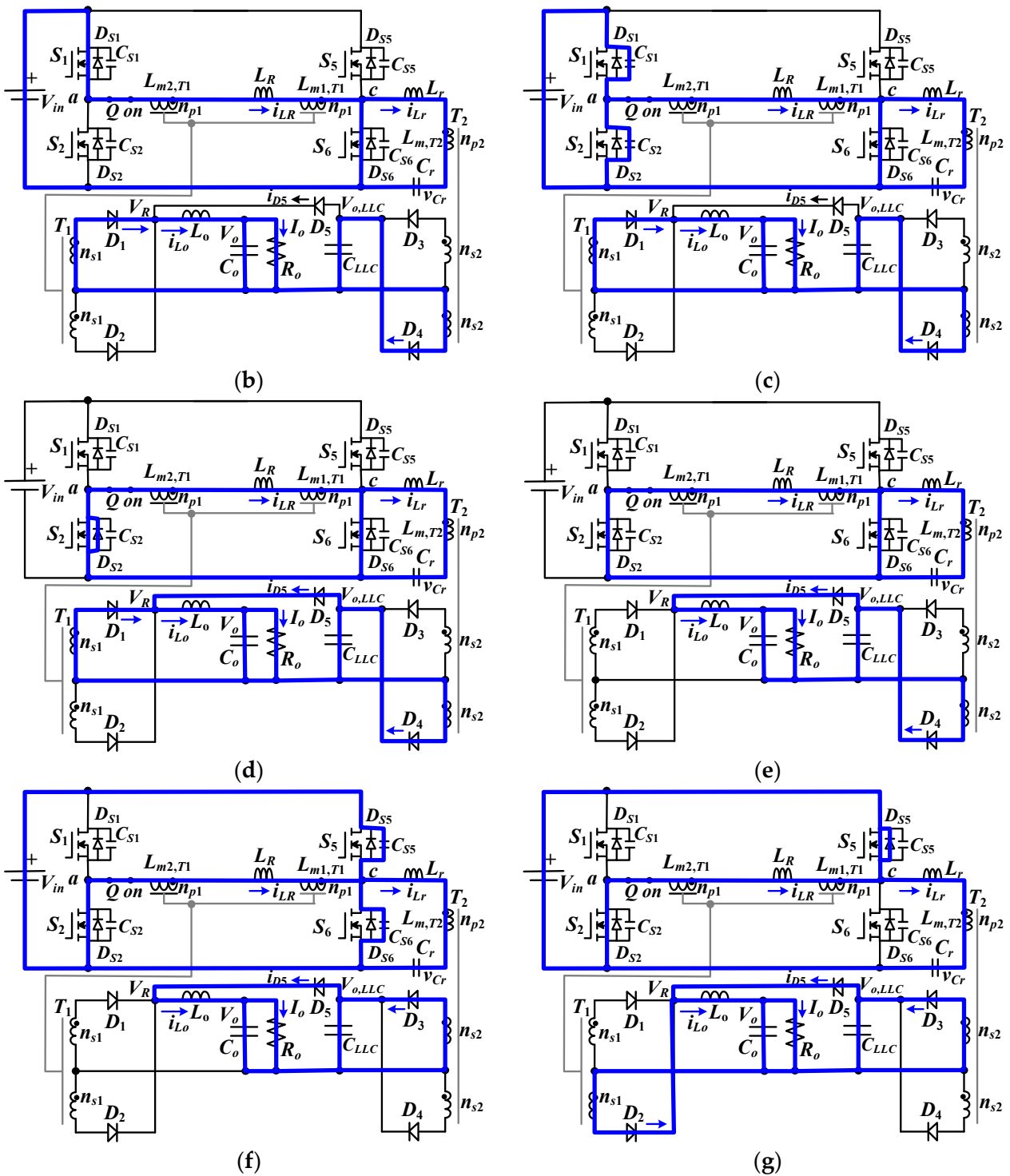


Figure 4. High input-voltage region operation (a) PWM waveforms, (b) state 1, (c) state 2, (d) state 3, (e) state 4, (f) state 5, (g) state 6.

4. Circuit Characteristics

A three-leg full bridge circuit and a LLC resonant circuit are included in the studied converter. Both PWM circuit and LLC circuit will achieve power transfer from V_{in} to V_o . LLC circuit is controlled at constant frequency. Thus, the secondary-side voltage $V_{o,LLC}$ is calculated in (11):

$$V_{o,LLC} = V_{in}n_{s2}/(2n_{p2}) \tag{11}$$

At the freewheeling state, the primary-side leg voltage v_{ac} or v_{bc} is zero and diode D_5 is forward biased. Thus, the rectifier terminal voltage $V_R = V_{o,LLC}$. The primary inductor voltage $v_{LR} = -n_{p1}V_{o,LLC}/n_{s1}$ (low input-voltage region) or $v_{LR} = -2 \times n_{p1}V_{o,LLC}/n_{s1}$ (high input-voltage region) and the primary current i_{LR} will decrease to zero at the freewheeling state. Due to LLC circuit is controlled under the inductive impedance, S_5 and S_6 can turn on at zero voltage. Due to voltage-second balance on L_o , V_o is derived in (2).

$$V_o = \frac{kd_{eff}V_{in}}{n_{p1}/n_{s1}} + \frac{(1 - 2d_{eff})V_{in}}{2n_{p2}/n_{s2}} \tag{12}$$

d_{eff} is the effective duty cycle and $k = 1$ (or 2) under the high (or low) input-voltage region. From Equation (12), the proposed converter has a voltage gain as Equation (13).

$$G_{dc,proposed} = \frac{V_o}{V_{in}} = \frac{kd_{eff}}{n_{p1}/n_{s1}} + \frac{(1 - 2d_{eff})}{2n_{p2}/n_{s2}} \tag{13}$$

If the proposed converter does not use LLC resonant circuit at lagging-leg (S_5 and S_5), then the voltage gain of three-leg converter without LLC converter is derived as:

$$G_{dc,con} = \frac{V_o}{V_{in}} = \frac{kd_{eff}}{n_{p1}/n_{s1}} \tag{14}$$

The voltage gains of the presented circuit and conventional PWM converter are compared and provided as:

$$\frac{G_{dc,proposed}}{G_{dc,con}} = 1 + \frac{n_{p1}(1 - 2d_{eff})/n_{s1}}{2n_{p2}kd_{eff}/n_{s2}} > 1 \tag{15}$$

From Equation (15), the presented circuit has a much larger voltage gain. The power ratings of LLC circuit and full bridge circuit in the presented converter are given as:

$$P_{LLC} = (1 - 2d_{eff})V_{o,LLC}I_o \approx (1 - 2d_{eff})V_{in}I_o / (2n_{p2}/n_{s2}) \tag{16}$$

$$P_{full-bridge} = \frac{2d_{eff}V_{in}I_o}{n_{p1}/n_{s1}} \tag{17}$$

In steady state, the ripple currents Δi_{L_o} of conventional PWM converter and the presented converter are expressed as

$$\Delta i_{L_o,con} > \frac{V_o(0.5 - d_{eff})}{L_o f_{sw}} \tag{18}$$

$$\Delta i_{L_o,proposed} \approx \frac{(V_o - V_{o,LLC})(0.5 - d_{eff})}{L_o f_{sw}} \tag{19}$$

From Equations (18) and (19), the ripple current comparison is given as.

$$\frac{\Delta i_{L_o,proposed}}{\Delta i_{L_o,con}} = 1 - V_{o,LLC}/V_o < 1 \tag{20}$$

That means the presented converter has less ripple current Δi_{L_o} . The voltage ratings of S_1-S_6 and Q are equal to $V_{in,max}$. The voltage rating of D_1 and D_2 is approximately equal to $V_{in,max}/(n_{p1}/n_{s1})$. Similarly, the voltage rating of D_3 and D_4 is approximately equal to $V_{in,max}/(n_{p2}/n_{s2})$. The voltage stress of D_5 is $V_{in,max}/(n_{p1}/n_{s1}) - V_{in,max}/(n_{p2}/n_{s2})$. The DC diode currents of D_1-D_5 are $I_{D1} = I_{D2} \approx d_e I_o$, $I_{D3} = I_{D4} \approx (0.5 - d_e) I_o$ and $I_{D5} \approx (1 - 2d_e) I_o$.

5. Experimental Results

The laboratory prototype with a rated power $P_o = 800$ W is built and tested. The circuit components of the laboratory prototype are provided in Table 1. Figure 5 gives the control block of the studied converter. The general purpose PWM integrated circuit UCC3895 is selected to generate the necessary PWM waveforms to drive the leading and lagging leg switches. A comparator with ± 30 V voltage tolerance is adopted in control block to decide low voltage input or high voltage input range. The reference voltage of Schmitt voltage comparator is designed at 270 V. Thus, the actual low and high voltage input ranges are $V_{in,L} = 120\text{--}300$ V and $V_{in,H} = 240\text{--}600$ V. Figure 6 gives the experimental test bench. The digital oscilloscope Tektronix TDS3014B, the dc electronic load Chroma 63112A, and the dc power source Chroma 62016P-600-8 are used in the laboratory test to measure the experimental results. Figure 7 provides the experimental results at the low voltage region ($V_{in,L} = 120\text{--}300$ V) and full load. Figure 7a,b gives the experimental PWM signals of $S_3\text{--}S_6$ for 120 and 300 V, respectively. The leg voltage v_{bc} , primary currents i_{LR} and i_{Lr} , and resonant voltage v_{Cr} under 120 V input case are provided in Figure 7c. Similarly, the measured waveforms of v_{bc} , i_{LR} , i_{Lr} , and v_{Cr} under 300 V input case are shown in Figure 7d. Comparing Figure 7c,d, the leg voltage v_{bc} at $V_{in} = 300$ V has less duty ratio. Since the secondary-side voltage $V_{o,LLC}$ is connected to the rectified terminal V_R , the inductor voltage v_{LR} at the circulating state is negative and i_{LR} will decrease to zero in this state. Figure 7e,f demonstrates the measured waveforms of i_{D1} , i_{D2} , i_{D5} , and i_{Lo} for $V_{in} = 120$ and 300 V cases. One can observe that the PWM converter has less duty cycle and more ripple current Δi_{Lo} on L_o under $V_{in} = 120$ V input case in Figure 7d,f. Figure 8a provides the PWM signals of S_3 (the leading-leg switch) at $V_{in} = 120$ V input and $P_o = 20\%$ rated load. In the same manner, the measured PWM waveforms of S_3 at $V_{in} = 120$ V input and $P_o = 100\%$ rated load are provided in Figure 8b. Figure 8c,d illustrates the test waveforms of S_3 under $V_{in} = 300$ V input and 20% and 100% rated loads, respectively. The PWM waveforms of S_5 for different input voltages ($V_{in} = 120$ and 300 V) and different loads (20% and 100% loads) are provided in Figure 8e–h. From Figure 8, it is clear that active switches S_3 and S_5 can both turn on at ZVS for 120 and 300 V input cases. Likewise, the test waveforms at high voltage input ($V_{in} = 240\text{--}600$ V) and the rated power are given in Figure 9. Since S_3 and S_4 are off under high voltage input condition, only PWM waveforms of S_1 , S_2 , S_5 , and S_6 are shown in Figure 9a,b for 240 and 600 V, respectively. The measured leg voltage v_{ac} , primary currents i_{LR} and i_{Lr} and resonant voltage v_{Cr} for 240 and 600 V inputs are given in Figure 9c,d, respectively. It can be noted in Figure 9d, i_{LR} will decrease to zero during the circulating interval. The experimental waveforms of i_{Lo} , i_{D5} , i_{D2} , and i_{D1} for $V_{in} = 240$ and 600 V are illustrated in Figure 9e,f. The hysteresis voltage comparator is used in the control block and the reference voltage is designed at 270 V with ± 30 V voltage tolerance. Figure 10a,b shows the PWM signals of S_1 under 240 V input and different load conditions (20% and 100% rated loads). Figure 10c,d provides the test waveforms of S_1 under 600 V input and different loads (20% and 100% loads). The PWM signals of S_5 at different input voltages ($V_{in} = 240$ and 600 V) and different load conditions (20% and 100% loads) are provided in Figure 10e–h. It can be noted that S_1 and S_5 all turn on under zero voltage. Figure 11 gives the test PWM waveforms of Q , S_1 , and S_3 during the input voltage variation between $V_{in} = 120$ and 600 V. When V_{in} increases from 120 to 600 V, Q turns on and S_3 turns off at $V_{in} = 300$ V. At the same time, S_1 is activated at $V_{in} > 300$ V. On the other hand, Q and S_1 turn off and S_3 is activated at $V_{in} = 240$ V when V_{in} decreases from 600 to 120 V. The measured efficiencies of the proposed converter at the rated power are 89.7%, 91.2%, 90.9%, and 93.4% under $V_{in} = 120, 240, 300,$ and 600 V, respectively. Using thermal imaging camera FLIR E85, the measured junction and case temperatures of power MOSFET S_5 at the rated power are 98 °C and 85 °C. The junction and case temperatures of rectifier diode D_1 are 102 °C and 90 °C. The measured core and winding temperatures of filter inductor L_o with MPP core CM343125 are 87 °C and 82 °C, respectively, at the rated power.

Table 1. Circuit parameters in the laboratory prototype.

Items	Parameter	Items	Parameter
V_{in}	120–600 V	L_o	30 μ H
V_o	48 V	$S_1 \sim S_6, Q$	STF15N95K5
P_o	800 W	$D_1 \sim D_4$	MBR40500PT
f_{sw}	70 kHz	D_5	STTH2003CT
C_o	640 μ F/100 V	$n_{p1}:n_{s1}$	16:10
$C_{o,LLC}$	240 μ F/100 V	$n_{p2}:n_{s2}$	22:2
C_r	205 nF	$L_{m1,T1}, L_{m2,T1}$	259 μ H
L_r	27 μ H	$L_{m,T2}$	135 μ H

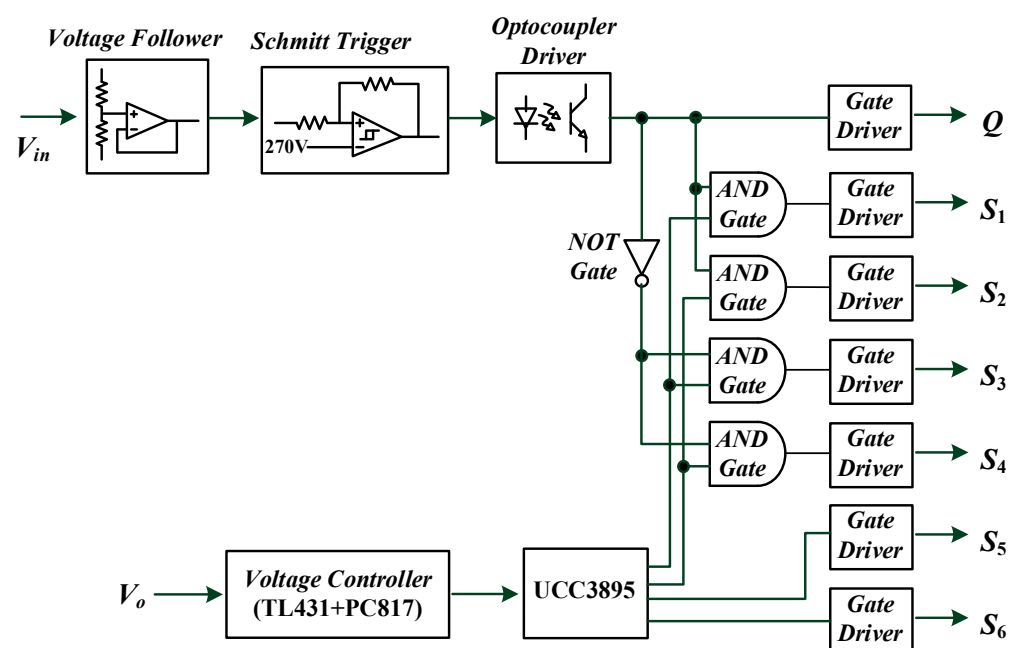
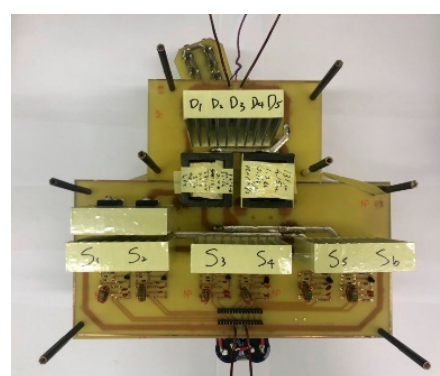


Figure 5. Control block of the laboratory prototype.



(a)



(b)

Figure 6. Pictures of the proposed converter in the laboratory: (a) Prototype circuit, (b) experimental setup.

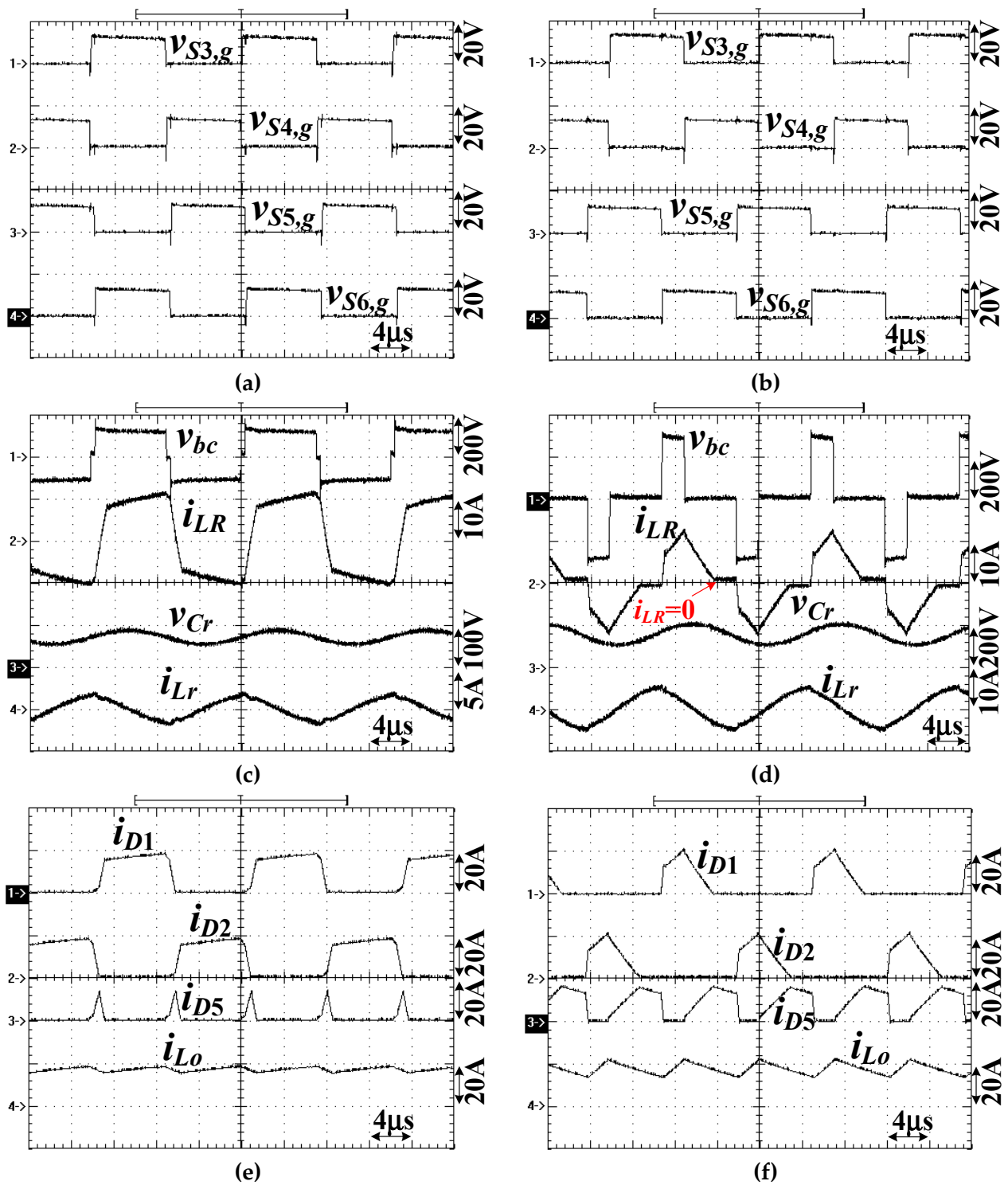


Figure 7. Measured PWM signals at full load and low input-voltage range (a) $S_3 \sim S_6$ at $V_{in} = 120$ V, (b) $S_3 \sim S_6$ at $V_{in} = 300$ V, (c) v_{bc} , i_{LR} , v_{Cr} , i_{Lr} at $V_{in} = 120$ V, (d) v_{bc} , i_{LR} , v_{Cr} , i_{Lr} at $V_{in} = 300$ V, (e) i_{D1} , i_{D2} , i_{D5} , i_{Lo} at $V_{in} = 120$ V, (f) i_{D1} , i_{D2} , i_{D5} , i_{Lo} at $V_{in} = 300$ V.

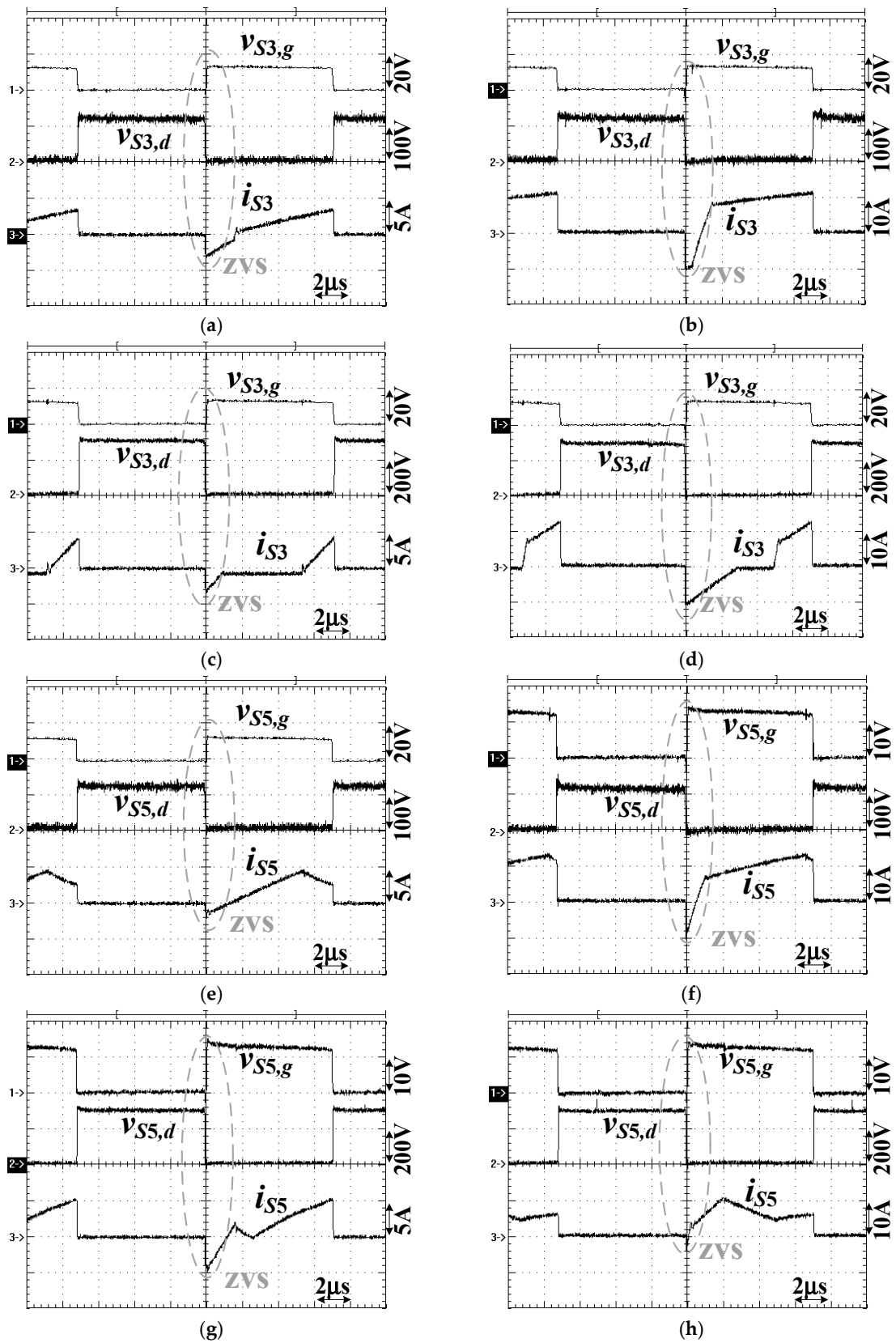


Figure 8. Measured PWM waveforms of S_3 and S_5 at the low input-voltage region (a) S_3 at $V_{in} = 120$ V and $P_o = 20\%$ load, (b) S_3 at $V_{in} = 120$ V and $P_o = 100\%$ load, (c) S_3 at $V_{in} = 300$ V and $P_o = 20\%$ load, (d) S_3 at $V_{in} = 300$ V and $P_o = 100\%$ load, (e) S_5 at $V_{in} = 120$ V and $P_o = 20\%$ load, (f) S_5 at $V_{in} = 120$ V and $P_o = 100\%$ load, (g) S_5 at $V_{in} = 300$ V and $P_o = 20\%$ load, (h) S_5 at $V_{in} = 300$ V and $P_o = 100\%$ load.

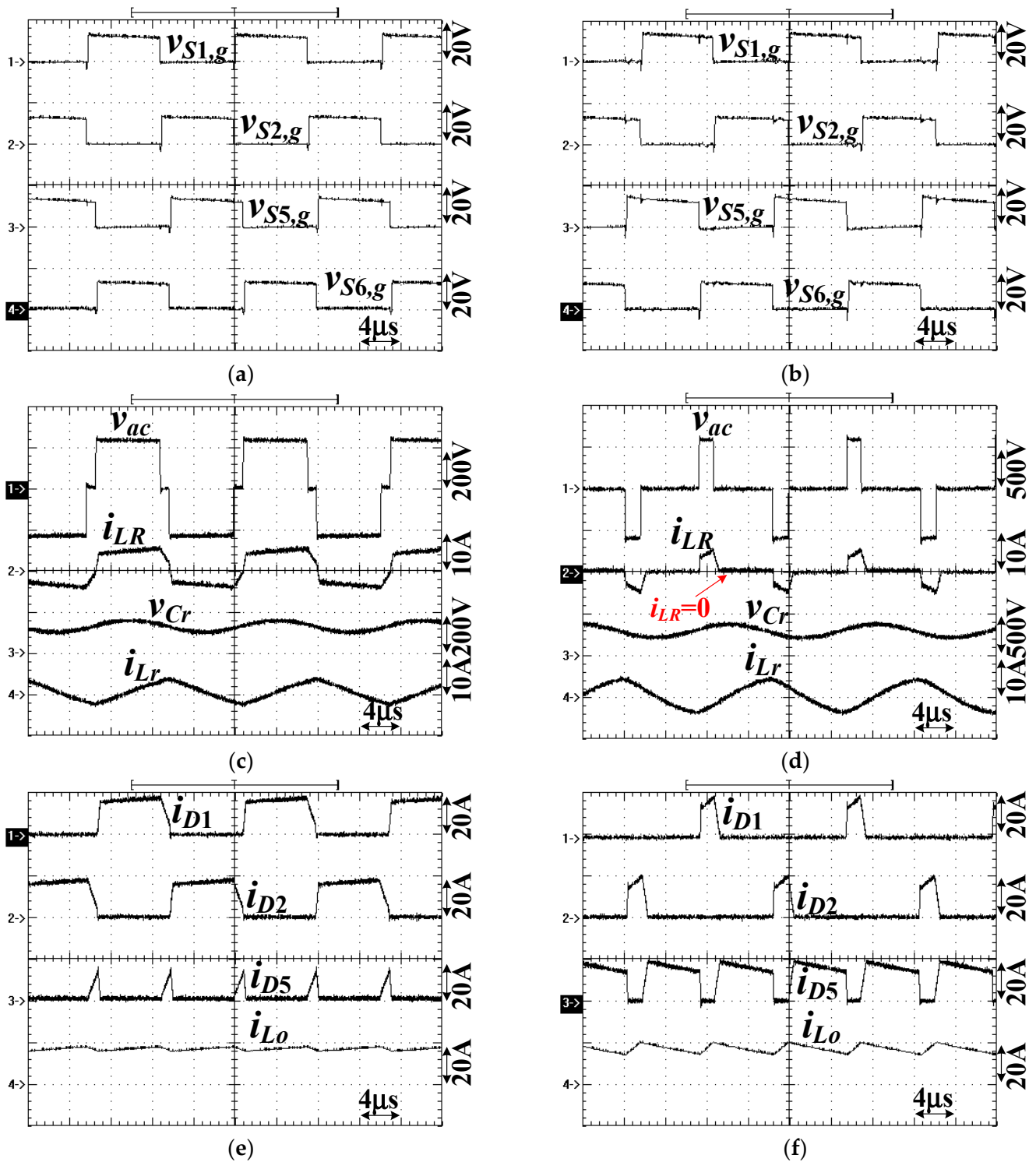


Figure 9. Measured PWM signals at full load and high input-voltage range (a) S_1, S_2, S_5, S_6 at $V_{in} = 240$ V, (b) S_1, S_2, S_5, S_6 at $V_{in} = 600$ V, (c) $v_{ac}, i_{LR}, v_{Cr}, i_{Lr}$ at $V_{in} = 240$ V, (d) $v_{ac}, i_{LR}, v_{Cr}, i_{Lr}$ at $V_{in} = 600$ V, (e) $i_{D1}, i_{D2}, i_{D5}, i_{Lo}$ at $V_{in} = 240$ V, (f) $i_{D1}, i_{D2}, i_{D5}, i_{Lo}$ at $V_{in} = 600$ V.

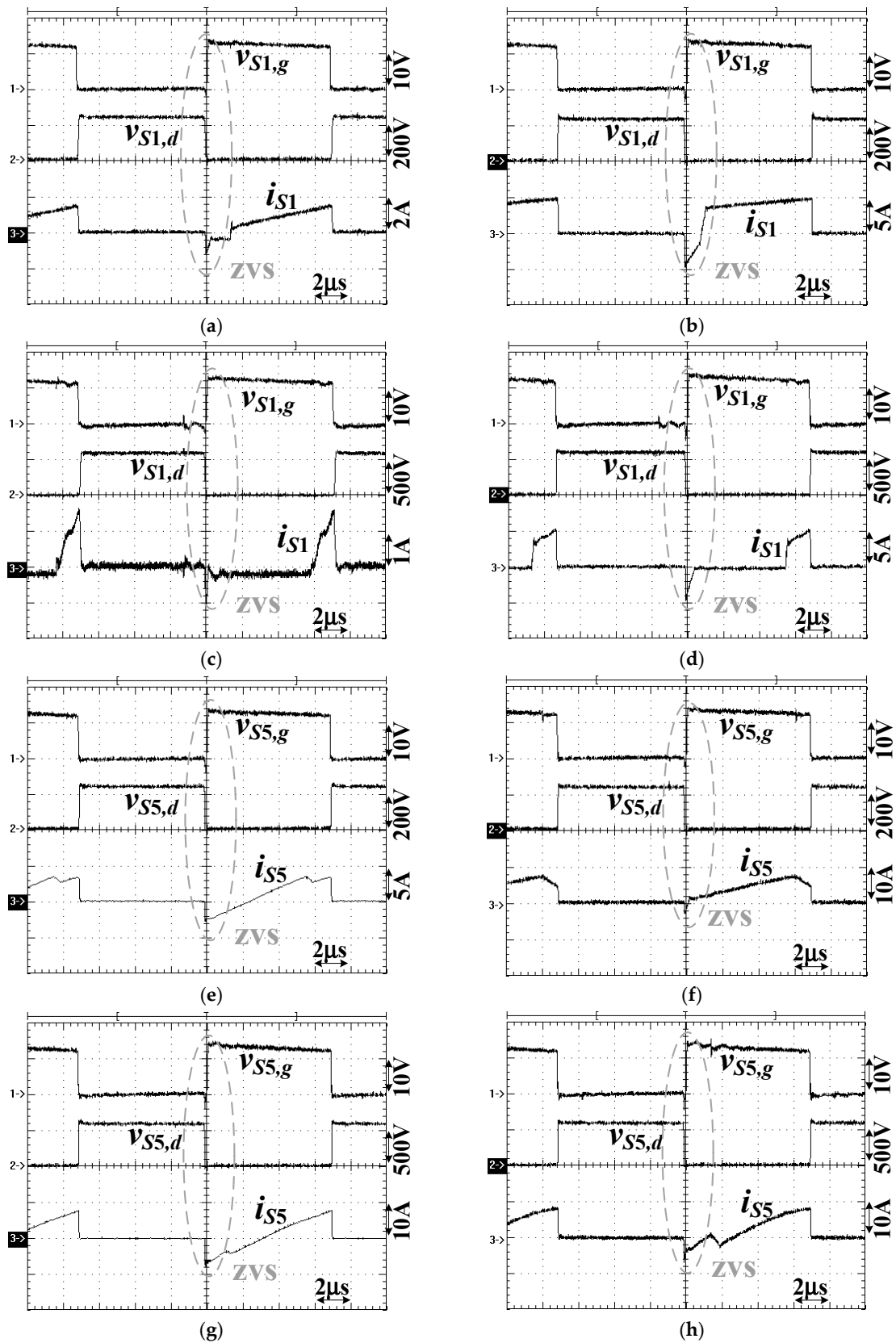


Figure 10. Measured PWM waveforms of S_1 and S_5 at the high input-voltage region (a) S_1 at $V_{in} = 240$ V and $P_o = 20\%$ load, (b) S_1 at $V_{in} = 240$ V and $P_o = 100\%$ load, (c) S_1 at $V_{in} = 600$ V and $P_o = 20\%$ load, (d) S_1 at $V_{in} = 600$ V and $P_o = 100\%$ load, (e) S_5 at $V_{in} = 240$ V and $P_o = 20\%$ load, (f) S_5 at $V_{in} = 240$ V and $P_o = 100\%$ load, (g) S_5 at $V_{in} = 600$ V and $P_o = 20\%$ load, (h) S_5 at $V_{in} = 600$ V and $P_o = 100\%$ load.

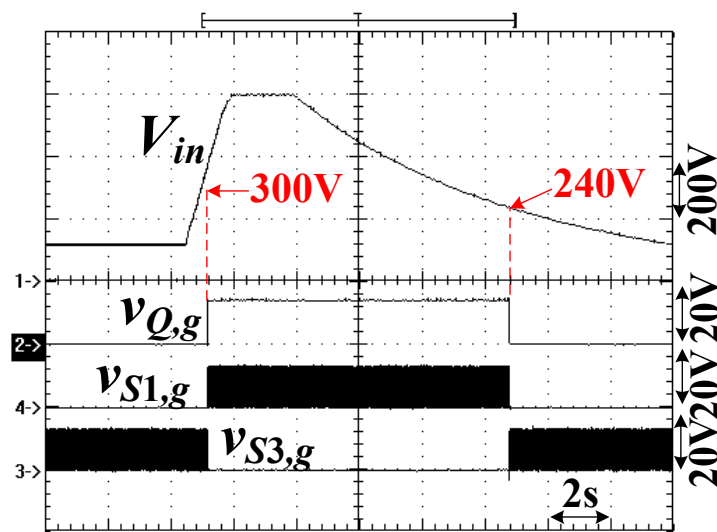


Figure 11. Measured waveforms of V_{in} , Q , S_1 and S_3 between 120 and 600 V input condition.

6. Conclusions

A hybrid PWM converter is presented and investigated to achieve wide voltage operation ($V_{in} = 120\text{--}600\text{ V}$), ZVS operation for all active devices and low primary current loss at the freewheeling state. To solve high circulating current drawback in conventional full bridge converter, a DC voltage comes from a LLC circuit is used at the secondary rectified terminal. Thus, the primary inductor voltage is negative and the circulating current will reduce to zero during freewheeling state. The other drawback of conventional PWM converter is serious switching loss on lagging leg devices. The added LLC circuit shares the same lagging-leg devices as PWM circuit to help the lagging-leg active devices to be turned on at zero voltage. Three-leg PWM circuit structure is used to achieve wide voltage input operation. The circuit performance is provided through the experimental results.

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References

1. Tahir, S.; Wang, J.; Baloch, M.H.; Kaloi, G.S. Digital Control Techniques Based on Voltage Source Inverters in Renewable Energy Applications: A Review. *Electronics* **2018**, *7*, 18. [\[CrossRef\]](#)
2. Almalaq, Y.; Matin, M. Three topologies of a non-isolated high gain switched-capacitor step-up cuk converter for renewable energy applications. *Electronics* **2018**, *7*, 94. [\[CrossRef\]](#)
3. Blaabjerg, F.; Dragicevic, T.; Davari, P. Applications of Power Electronics. *Electronics* **2019**, *8*, 465. [\[CrossRef\]](#)
4. Kim, J.-Y.; Kim, H.-S.; Baek, J.-W.; Jeong, D.-K. Analysis of Effective Three-Level Neutral Point Clamped Converter System for the Bipolar LVDC Distribution. *Electronics* **2019**, *8*, 691. [\[CrossRef\]](#)
5. Steigerwald, R.L. A comparison of half-bridge resonant converter topologies. *IEEE Trans. Power Electron.* **1988**, *3*, 174–182. [\[CrossRef\]](#)
6. Lin, B.-R.; Dai, C.-X. Wide Voltage Resonant Converter Using a Variable Winding Turns Ratio. *Electronics* **2020**, *9*, 370. [\[CrossRef\]](#)
7. Ren, R.; Liu, B.; Jones, E.A.; Wang, F.F.; Zhang, Z.; Costinett, D. Capacitor-clamped, three-level Gan-based dc-dc converter with dual voltage outputs for battery charger applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 841–853. [\[CrossRef\]](#)
8. Safaei, A.; Jain, P.; Bakhshai, A. A ZVS Pulsewidth Modulation Full-Bridge Converter with a Low-RMS-Current Resonant Auxiliary Circuit. *IEEE Trans. Power Electron.* **2015**, *31*, 4031–4047. [\[CrossRef\]](#)

9. Wang, X.; Tian, F.; Batarseh, I. High Efficiency Parallel Post Regulator for Wide Range Input DC–DC Converter. *IEEE Trans. Power Electron.* **2008**, *23*, 852–858. [[CrossRef](#)]
10. Wu, H.; Wan, C.; Sun, K.; Xing, Y. A High Step-Down Multiple Output Converter with Wide Input Voltage Range Based on Quasi Two-Stage Architecture and Dual-Output LLC Resonant Converter. *IEEE Trans. Power Electron.* **2015**, *30*, 1793–1796. [[CrossRef](#)]
11. Lin, B.-R.; Hsieh, F.-Y. Soft-Switching Zeta–Flyback Converter with a Buck–Boost Type of Active Clamp. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2813–2822. [[CrossRef](#)]
12. Jeong, Y.; Park, J.D.; Moon, G.-W. An Interleaved Active-Clamp Forward Converter Modified for Reduced Primary Conduction Loss Without Additional Components. *IEEE Trans. Power Electron.* **2019**, *35*, 121–130. [[CrossRef](#)]
13. Lin, B.-R.; Chao, C.-H. A New ZVS DC/DC Converter with Three APWM Circuits. *IEEE Trans. Ind. Electron.* **2012**, *60*, 4351–4358. [[CrossRef](#)]
14. Pont, N.C.D.; Bandeira, D.; Lazzarin, T.B.; Barbi, I. A ZVS APWM half-bridge parallel resonant DC–DC converter with capacitive output. *IEEE Trans. Ind. Electron.* **2019**, *66*, 5231–5241. [[CrossRef](#)]
15. Lin, B. Resonant converter with wide input voltage range and input current ripple-free. *Electron. Lett.* **2018**, *54*, 1086–1088. [[CrossRef](#)]
16. Wang, P.; Zhou, L.; Zhang, Y.; Li, J.; Sumner, M. Input-Parallel Output-Series DC-DC Boost Converter with a Wide Input Voltage Range, For Fuel Cell Vehicles. *IEEE Trans. Veh. Technol.* **2017**, *66*, 7771–7781. [[CrossRef](#)]
17. Hu, H.; Fang, X.; Chen, F.; Shen, Z.J.; Batarseh, I. A Modified High-Efficiency LLC Converter with Two Transformers for Wide Input-Voltage Range Applications. *IEEE Trans. Power Electron.* **2013**, *28*, 1946–1960. [[CrossRef](#)]