A Triple-Cascode X-Band LNA Design with Modified Post-Distortion Network

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Abstract: This work proposes a novel linearized low noise amplifier (LNA) for X-band applications with flat power gain, low noise performance and enhanced linearity. In this study, a triple-cascode topology with dual-resonant network is utilized and a modified post-distortion network is introduced to improve the linearity. The LNA utilizes a subthreshold auxiliary NMOS transistor to reduce the nonlinearity with low power consumption. In addition, a methodology is proposed to predict the characteristic of the linearity performance of the proposed LNA with modified post-distortion network. With a small increase of 1 mW in power consumption due to the inclusion of the post-distortion network, the input intercept point IIP3 is improved and lies in the range of −3 to +8 dBm over the frequency range from 8 to 12 GHz. Implemented in Global Foundries 130 nm CMOS process, the LNA achieves a peak gain of 18 dB, and a 1.3 dB minimum NF over 8 to 12 GHz. The proposed LNA requires an area of 1.2 mm^2 and a power of 18 mW.

Keywords: CMOS; linearization; low noise amplifier (LNA); dual-resonant network; triple-cascode

1. Introduction

Growing research space applications and radar systems has aroused interest in broadband LNAs. A broadband LNA needs to provide good input matching, high linearity, flat power gain, and low noise figure (NF) over a multi-GHz bandwidth (BW) while consuming low power and die area.

To achieve broadband input matching, band-pass filtering (BPF) network, feedback network, common-gate (CG) stage, and inductive source degeneration techniques have been proposed [1–4]. However, the BPF network requires a large amount of inductance and capacitance leading to an increased area and degraded noise performance. Feedback network increases the noise figure. Although common-gate stage makes the impedance $1/g_m$ for a wider frequency band, its noise figure is greater than the common source stage. On the other hand, a conventional inductive source degradation structure has difficulty achieving wideband input matching.

A non-negligible challenge to broadband LNAs is the stringent linearity requirement over a wide frequency range because of the large numbers of in-band interferences in wideband systems. Cross modulation and inter modulation are caused by blockers and transmitter leakage [5] in a reconfigurable receiver. Higher linearity is also required to suppress interference and maintain a high sensitivity [6]. Therefore, in the CMOS process, many linearization techniques have been proposed to meet the demand of broadband linearization.

Optimizing overdrive voltage $(V_{gs} - V_{th})$ [5,7] leads to a linearity boost region for a fairly narrow range of input amplitude. Using second-order nonlinear parameters to suppress third-order nonlinearity, the feedback technology can improve linearity in a wide frequency band, while the loop gain is limited [8]. A derivative superposition

(DS) method [9] uses an additional transistor's nonlinearity to cancel that of the main device. It utilizes MOS transistors working in a triode or weak inversion region. However, the common problem existing in all the reported DS methods is its difficulty with achieving good input matching and optimized noise performance. Post-distortion usually achieves stable distortion rejection and high linearity with an auxiliary saturated transistor, while the auxiliary transistors consume extra power to operate in saturation mode [10,11]. Several post-distortion (PD) networks have been proposed to enhance the linearity of LNA [10,12,13]. An auxiliary PMOS transistor has been employed to absorb the nonlinear current over a wide frequency range [10]. A folded PMOS intermodulation distortion (IMD) sinker has been proposed to absorb IMD3 current generated by the main transistor [12]. A diode connected transistor has been utilized to linearize the main transistor [13]. A conventional post-distortion technology method will degrade IIP3 performance due to the contribution of the second-order nonlinearity of M_{AUX} [14]. However, few studies have been published to discuss how to improve linearity in a high frequency region.

In this paper, a triple-cascode LNA with a modified post-distortion network is introduced, which has a simple input matching network to expand bandwidth and enhanced linearity compared to prior reported LNAs with conventional post-distortion technique. The proposed post-distortion network is composed of transistor M_{AUX} operating in a weak inversion region consuming low power. An auxiliary L_{sa} is augmented at the source node of M_{AUX} to enhance linearity at high frequency region.

The paper is organized as follows: Section 2 details the design method of the proposed X-band linearized LNA including analysis for the input matching network, power gain, and novel post-distortion technology. Section 3 presents simulated performances of the proposed LNA. Finally, conclusions are given in Section 4.

2. Triple-Cascode LNA with a Modified Post-Distortion Network Analysis

2.1. Input Matching Analysis

The proposed triple-cascode LNA with a modified post-distortion network is shown in Figure 1. The conventional inductive source degeneration common-source CS-LNA is accomplished by making its real part $g_{m1}L_s/C_{gs} = R_S$, where $R_S = 50\ \Omega$ is source impedance. Inductance L_g is connected in series with gate node of M_1 to adjust the imaginary part of input impedance. By taking parasitic capacitance C_{gd} into account or by augmenting an extra capacitance C_{GD}, the input matching bandwidth can be extended. The input impedance of the proposed triple-cascode LNA can be written as

$$Z_{in} = sL_g + \frac{(1 + sL_s(g_{m1} + sC_{GD}))(1 + sC_{GD}Z_L)}{s(C_{gs} + C_{GD} + C_{GD}(g_{m1} + sC_{gs})(sL_s + Z_L))} \tag{1}$$

where Z_L represents load impedance seen from the drain node of transistor of M_1 and can approximately be expressed as

$$Z_L \approx \underbrace{j\omega L_1 + \frac{1}{g_{m2}}}_{Omitting\, C_{gsAUX}} = j\omega L_1 + \underbrace{\frac{1}{j\omega C_{gsAUX}} + \frac{1}{g_{m2}}}_{Considering\, C_{gsAUX}} = R_L + jX_L \tag{2}$$

Based on input impedance analysis and network analysis, the calculation of -10 dB bandwidth for input matching can be derived from the following equations:

$$S_{11} = \frac{Z_{in} - R_S}{Z_{in} + R_S} \tag{3a}$$

$$\frac{Re^2[\text{ Numerator }[S_{11}]] + Im^2[\text{ Numerator }[S_{11}]]}{Re^2[\text{ Denominator }[S_{11}]] + Im^2[\text{ Denominator }[S_{11}]]} = \frac{1}{10} \tag{3b}$$

$$\Delta f_{10\text{dB}} = \omega_{x,H} - \omega_{x,L} \tag{3c}$$
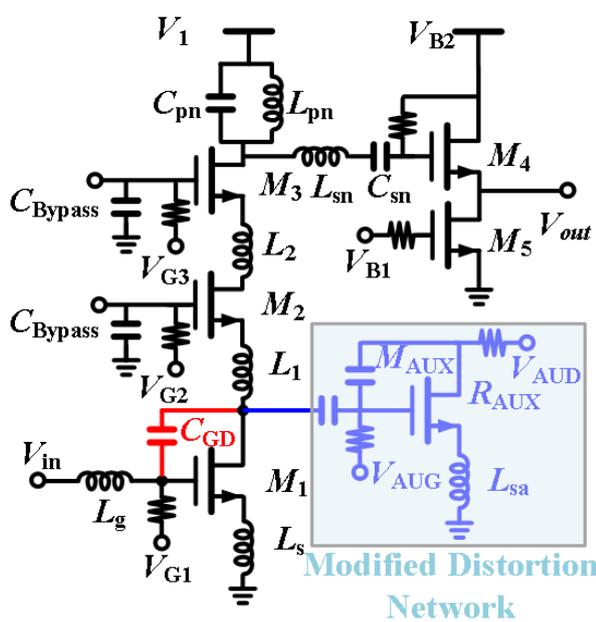
Transistor	L (nm)	Finger Width	Fingers	Unit Cell
$M_{1,2,3}$	130	2 μm	5	16
M_4	130	3 μm	5	2
M_{AUX}	130	2 μm	5	10
Component values				
L_g	1.4 nH	L_s		260 pH
L_1	140 pH	L_2		1 nH
L_{pn}	1.05 nH	L_{sn}		450 pH
C_{pn}	300 fF	C_{sn}		240 fF
L_{sa}	290 pH	R_{AUX}		400 Ω
Bias conditions				
V_{GI}, V_{B1}	600 mV	V_{G2}		1.6 V
V_{G3}, V_1	2.4 V	V_{AUG}		0.5 V
V_{B2}	1.5 V	V_{AUD}		1.2 V

Figure 1. Schematic of the proposed triple-cascode LNA with the modified post-distortion network.

As shown in Equation (1), the parasitic capacitance C_{GD} combined with load impedance Z_L seen from the drain node of transistor M_1 can regulate the input impedance, which in turn can extend input matching bandwidth. The detailed calculus given in Equations (1)–(3) essentially provides a generalized method to calculate the input matching bandwidth with an arbitrary input matching network. Generally, the numerator, denominator in Equation (3b) can be calculated based on input impedance. The numerator and denominator in Equation (3b) are calculated in Appendix A. Numerator and Denominator for Bandwidth Calculation. To verify the generalized method, input matching bandwidth of the proposed LNA is calculated based on Equations (1)–(3). L_g and L_s need to be changed to fix the resonant frequency. The calculated $\omega_{x,H}$, $\omega_{x,L}$, input bandwidth with different C_{GD} are listed in Table 1. The calculated result shows identical simulated value as shown in Figure 2a. Figure 2 plots the S_{11} of input matching network by increasing L_1 from 100 pH to 300 pH to verify the regulating effect with the existence of C_{GD}. Compared with other broadband matching technologies, although the method using C_{GD} has a complicated load calculation, it can effectively extend the input matching bandwidth compared with a conventional inductive source degeneration technique without C_{GD} compensation.

Table 1. Calculated $\omega_{x,H}$, $\omega_{x,L}$, Bandwidth with Different C_{GD}.

C_{GD}	$\omega_{x,H}$	$\omega_{x,L}$	Bandwidth
0 fF	12.2 GHz	8.1 GHz	4.1 GHz
25 fF	12.9 GHz	7.7 GHz	5.2 GHz
50 fF	13.6 GHz	7.4 GHz	6.2 GHz
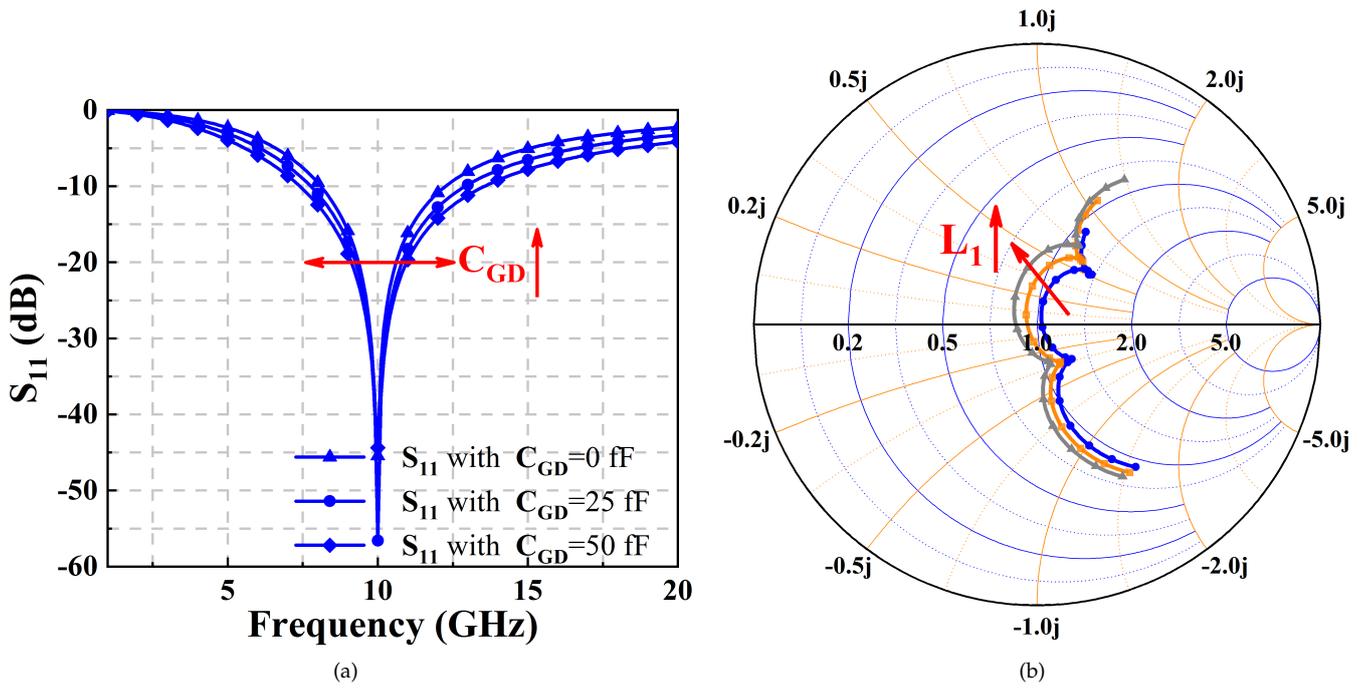
Figure 2. (**a**) Conceptual diagram of bandwidth extension with C_{GD} compensation of S_{11} in dB format; (**b**) simulated S_{11} with L_1 increasing from 100 pH to 300 pH in the Smith chart format.

2.2. Gain Analysis

The proposed triple-cascode LNA incorporates a dual-resonant network. For M_4 in the output buffer, three parallel multifinger transistors with unit transistor size of W = 2 μm, L = 130 nm, and number of fingers N = 5 are used. The input impedance of the output buffer can be modeled as a parallel RC circuit as shown in Figure 3a. The capacitance and resistance can be extracted based on simulated input impedance. The gain analysis can be done by analyzing the characteristics of the dual-resonant network. According to an equivalent model of the dual-resonant network in Figure 3b, the impedance magnitude of the dual-resonant network can be written as

$$mag(Z_{Dual}) \approx \sqrt{\frac{L_{pn}^2 R_p^2 \omega^2 \{1 + C_{gs4}\omega^2 D\}}{\{2C_{gs4}^2 L_{pn}^2 R_p R_s \omega^4 + L_{pn}^2 \omega^2 \{1 + D\} + R_p^2 \{1 + \omega^2[A + B + C]\}\}}} \quad (4a)$$

where

$$A = C_{gs4}\left(-2L_{pn} - 2L_{sn} + C_{gs4}R_s^2 + C_{sn}(L_{pn} + L_{sn})\omega^2\right) \quad (4b)$$

$$B = 2C_{pn}L_{pn}\left[-1 + C_{gs4}\omega^2\left(L_{pn} + 2L_{sn} - C_{gs4}R_s^2 - C_{gs4}L_{sn}(L_{pn} + L_{sn})\omega^2\right)\right] \quad (4c)$$

$$C = C_{pn}^2 L_{pn}^2 \omega^2\left[1 + C_{gs4}\omega^2\left(C_{gs4}R_s^2 + L_{sn}\left(-2 + C_{gs4}L_{sn}\omega^2\right)\right)\right] \quad (4d)$$

$$D = C_{gs4}\omega^2\left[C_{gs4}R_s^2 + L_{sn}\left(-2 + C_{gs4}L_{sn}\omega^2\right)\right] \quad (4e)$$

To derive two peak resonant gain, we firstly neglect resistance in the series and parallel branch. Then, the two peak resonant frequency can be approximately calculated as

$$\omega_{o1} \approx \sqrt{\frac{L_{pn} + L_{sn}}{L_{pn}L_{sn}C_{pn}}} \quad (5a)$$

$$\omega_{o2} \approx \sqrt{\frac{1}{L_{sn}\left(C_{pn} + C_{sn}\|C_{gs4}\right)}} \tag{5b}$$
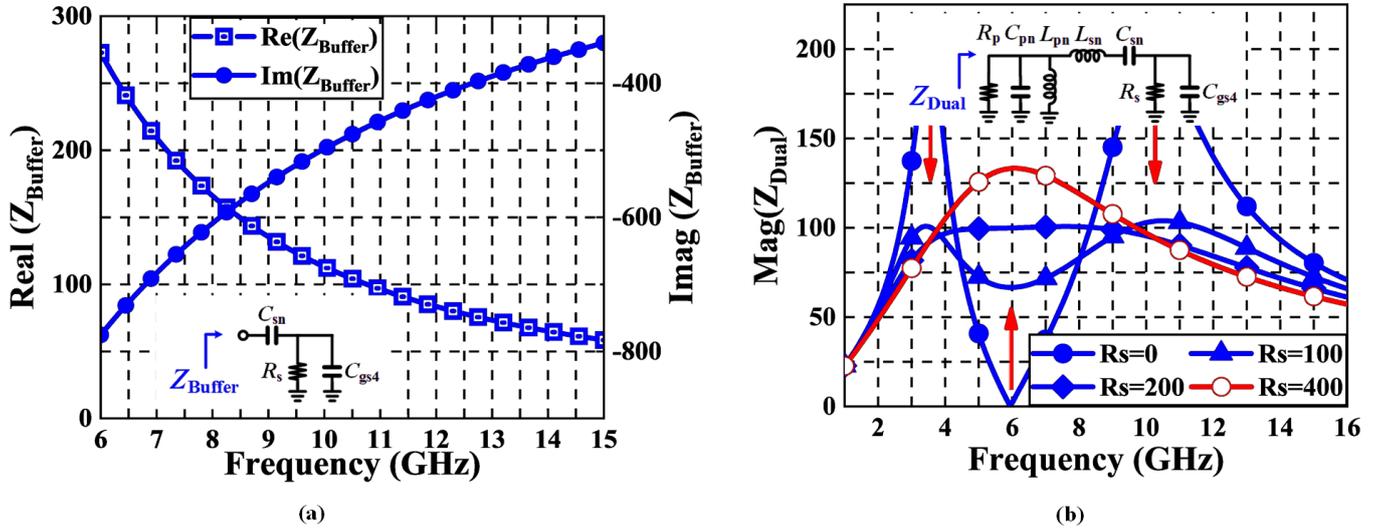
Figure 3. Dual resonant network. (**a**) simulated real and imaginary part and equivalent circuit of the output buffer; (**b**) equivalent circuit of dual resonant network and conceptual flat gain mechanism.

By utilizing parasitic capacitance and resistance seen from gate node of output buffer, the magnitude of the load impedance can be enhanced between two resonant frequency points, which results in flat gain. Therefore, the design of the load network is simplified by choosing proper inductance and designing output buffer stage, which results in double resonant effect and flat power gain.

2.3. Noise Analysis

The noise model for inductively degenerated triple-cascode LNA is shown in Figure 4, the noise factor (F) of CS-LNA can be defined as [15]

$$F = \frac{\overline{i_{o,ns}^2} + \overline{i_{o,nR1}^2} + \overline{i_{o,nRg}^2} + \overline{i_{o,nd1}^2} + \overline{i_{o,nd2}^2} + \overline{i_{o,ndAUX}^2}}{i_{o,ns}^2} \tag{6}$$

$$F = \frac{1}{Dnos}\left(\begin{matrix} Dnos + Dnos1 \\ +4k_BT\gamma g_{d0,1}\left\{g_{m2}R_S\left(\begin{matrix}1\\+jg_{ma}L_{sa}\omega\end{matrix}\right)\left\{\begin{matrix}-1\\+\omega\left[\begin{matrix}-j(C_{GD}+C_{gs})R_S\\+\left[(C_{GD}+C_{gs})L_g+C_{gs}L_s\right]\omega\end{matrix}\right]\end{matrix}\right\}\right\}^2 \\ +4k_BT\gamma g_{d0,AUX}\left\{g_{m2}\left\{\begin{matrix}-1\\+\omega(C_{GD}+C_{gs})(-jR_S+L_g\omega)\\+L_s\omega(g_{m1}+jC_{gs}\omega)\left[-j+C_{GD}\omega(R_S+jL_g\omega)\right]\end{matrix}\right\}\right\}^2 \\ +4k_BT\gamma g_{d0,2}\left\{\omega\left\{\left[\begin{matrix}1+j(g_{m1}L_s+C_{gs}R_S)\omega\\-C_{gs}(L_g+L_s)\omega^2\end{matrix}\right]\left[\begin{matrix}-C_{p1}\\+C_{gs2}(-1+C_{p1}L_1\omega^2)\end{matrix}\right]\right\}\right\}^2 \end{matrix}\right) \tag{7}$$

$$Dnos = 4k_BTR_S\left\{g_{m2}(-j+g_{ma}L_{sa}\omega)\left\{g_{m1}\left[1+C_{GD}L_s\omega^2\right]+jC_{GD}\omega\left(-1+C_{gs}L_s\omega^2\right)\right\}\right\}^2 \tag{8}$$

$$Dnos1 = 4k_BT\left[R_1+R_g\right]\left\{g_{m2}(-j+g_{ma}L_{sa}\omega)\left\{g_{m1}\left[1+C_{GD}L_s\omega^2\right]+jC_{GD}\omega\left(-1+C_{gs}L_s\omega^2\right)\right\}\right\}^2 \tag{9}$$

where k_B is the Boltzmann constant, T is absolute temperature, $g_{d0,1}$, $g_{d0,2}$, $g_{d0,AUX}$ are the conductance of the transistor M_1, M_2, M_{AUX} when the voltage between the drain

and source node equals to zero, respectively. R_1, R_2, R_g represent the series metal loss of inductor L_1, L_2 and gate resistor of M_1, respectively. Parasitic resistance of the inductors can be noise sources to degrade NF performance. To investigate the effective parasitic parameters of the inductors, inductors used in the circuit have been simulated in Figure 5.
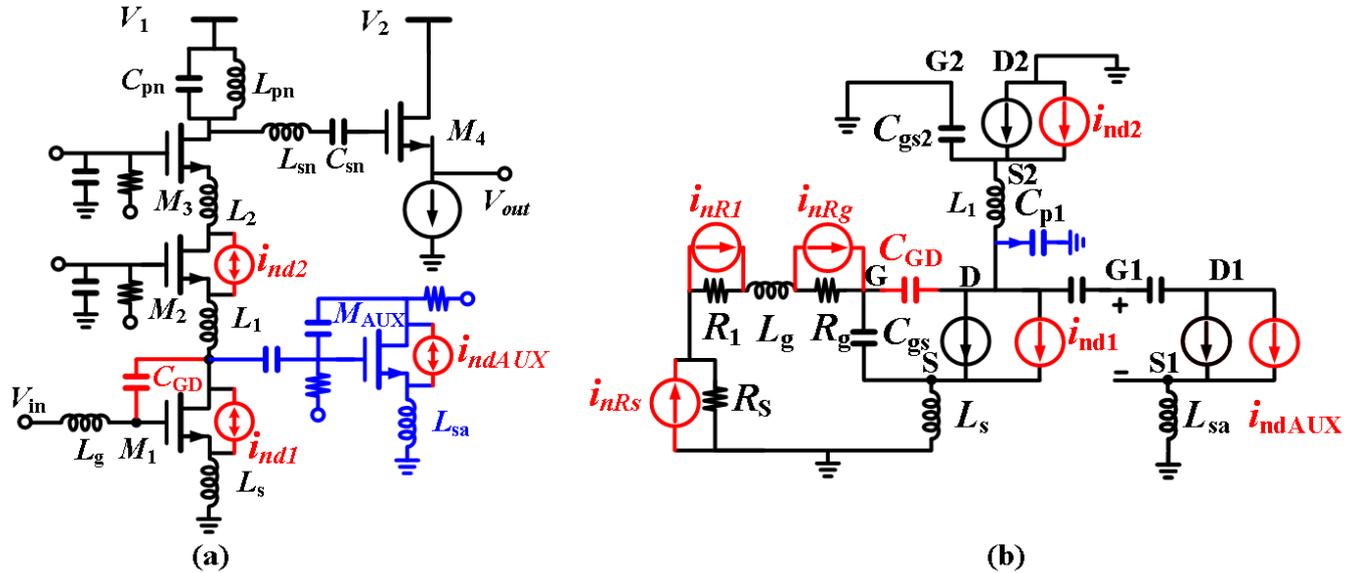
Figure 4. (**a**) Noise model for the inductively degenerated triple-cascode LNA; (**b**) equivalent circuit model for the calculation of noise performance.
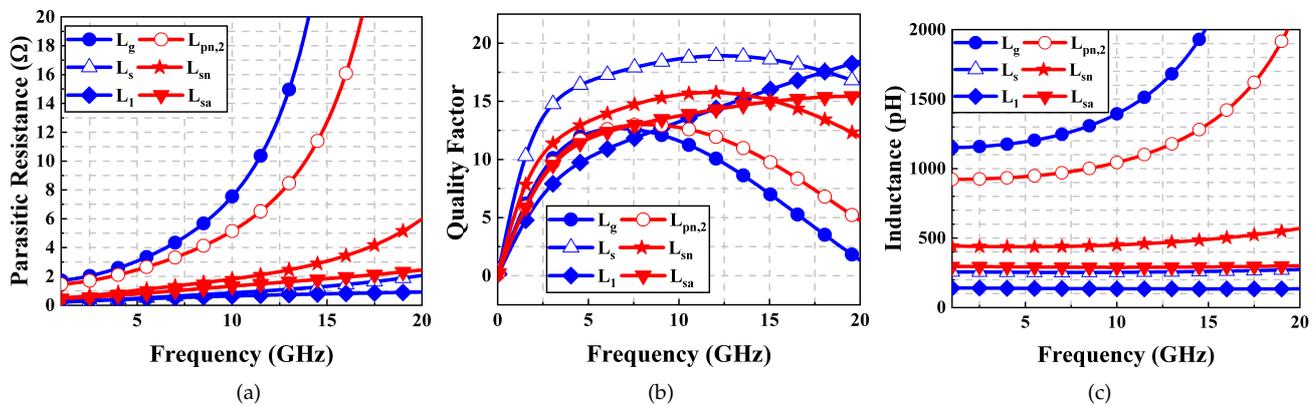
Figure 5. (**a**) Simulated parasitic series resistance of inductors; (**b**) simulated quality factor Q of inductors; (**c**) simulated effective inductance of inductors.

Furthermore, parasitic capacitance of M_2 and M_3 at the source node degrades the noise performance as frequency increases. As shown in Equations (6) and (7), for simplicity, C_{GD} is neglected when calculate $\overline{i_{o,nd2}^2}$. According to Equation (7), ideally, the noise contribution can be cancelled [16] when

$$L_1 = \frac{C_{gs2} + C_{p1}}{\omega^2 C_{gs2} C_{p1}} \tag{10}$$

Hence, we introduce two inductors between M_1, M_2 and M_3 to resonate parasitic capacitance, which results in enhanced noise performance. By utilizing simultaneous noise input matching technology, the triple-cascode LNA can achieve input matching and the minimum noise figure simultaneously. On the other hand, the noise performance can be degraded by gate resistance of transistor M_1 significantly. One can improve the noise

performance by reducing the gate resistance. The gate resistance can be expressed as the following equation:

$$R_g = \frac{R_\square W}{3n^2 L} \tag{11}$$

where $R_\square$ is gate sheet resistance, W is total gate finger width, n is number of fingers, and L is the gate length. According to the above analysis, by optimizing the transistor layout, input matching network, and bias condition, the proposed triple-cascode LNA can achieve low noise performance and enhanced input matching bandwidth. Simulated noise contributions by individual components of proposed LNA are shown in Figure 6.
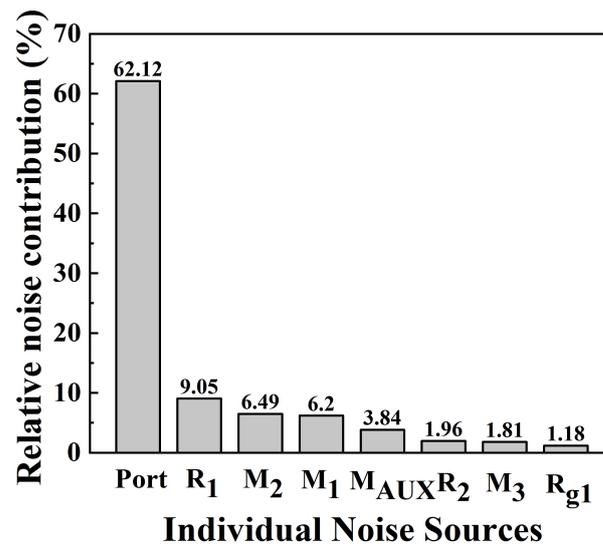
Figure 6. Simulated noise contributions by individual components in proposed LNA.

2.4. Linearity Analysis

The linearization technique based on optimum gate biasing has been proposed to generate zero 3rd-order nonlinearity coefficient [7]. Derivatives of the drain-source dc current I_{DS} of transistor M_1, M_{AUX} with respect to V_{GS} (g_{m1}, g_2, g_3, g_{ma}, g_{2a}, g_{3a}) have been illustrated in Figures 7 and 8. However, the optimum gate biasing technique can only improve the IIP3 in a very narrow V_{GS} range, which is sensitive to process and temperature variations. The modified derivative superposition method has been proposed to eliminate the contribution of the second-order nonlinearity [14]. On the other hand, the modified derivative superposition technique complicates the input matching network to simultaneously achieve good input matching and low noise performance. We propose the triple-cascode configuration LNA combined with a post-distortion network to improve the linearity with a simple input matching network and low noise performance. Although the work in [17] looks similar to a triple-cascode configuration, it is actually a two stage amplifier with the CS and cascode stage in current reuse topology. The reported current-reuse LNA utilized the modified derivative superposition technique to improve the linearity [18]. Essentially, triple-cascode can provide enhancement of linearity [19]. Volterra series has been utilized to analyze linearity of the triple-cascode LNA [13,14,20,21]. The linearity of proposed triple-cascode LNA is dominantly determined by the CS stage. For simplicity, the CG stage is regarded as a linear current buffer as shown in Figure 9, which plays a non-dominated role in linearity analysis [13]. Furthermore, the linearity analysis at the drain node of transistor M_3, according to the simulated result shown in Figure 10, approximately equals the linearity analysis at the drain node of transistor M_1. To calculate linearity of the proposed LNA, the drain current of transistor M_1 and auxiliary transistor M_{AUX} can be modeled up to the third-order and second-order as

$$i_{ds} = g_{m1}V_{gs1} + g_2 V_{gs1}^2 + g_3 V_{gs1}^3 \tag{12a}$$

$$i_{dsa} = g_{ma}V_{gs2} + g_{2a}V_{gs2}^2 \tag{12b}$$
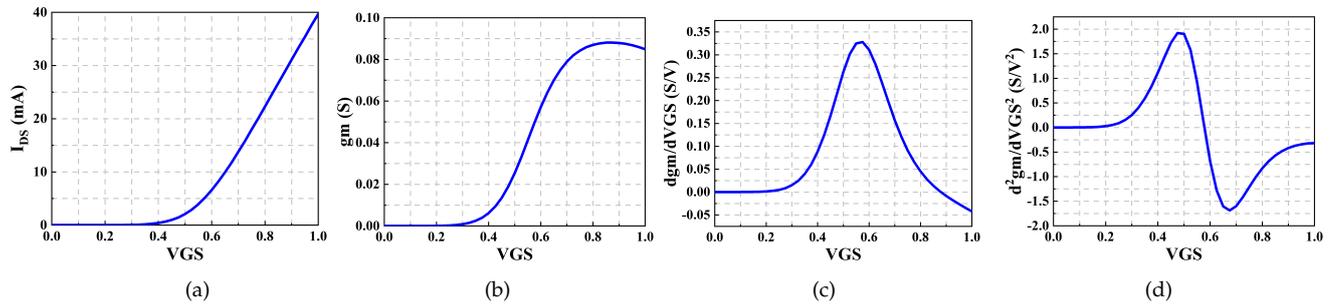
Figure 7. I_{DS} and derivatives versus V_{GS1} of main transistor M_1. (**a**) I_{DS}; (**b**) g_{m1}; (**c**) g_2; (**d**) g_3.
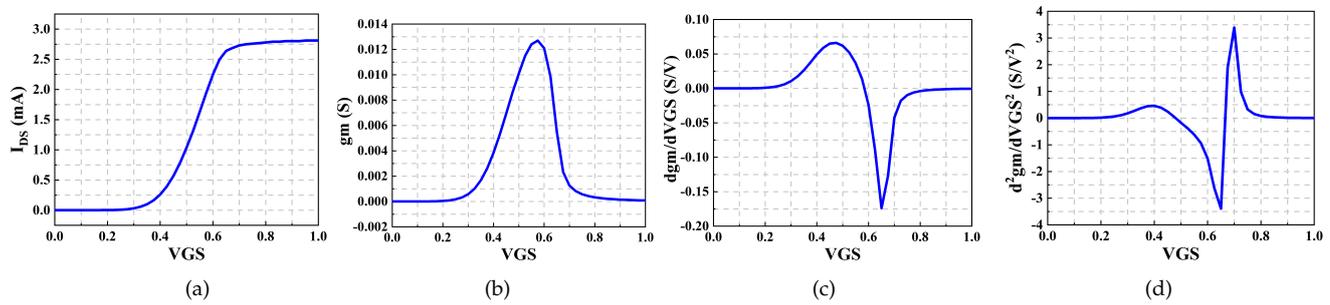
Figure 8. I_{DS} and derivatives versus V_{GSAUX} of auxiliary transistor M_{AUX}. (**a**) I_{DS}; (**b**) g_{ma}; (**c**) g_{2a}; (**d**) g_{3a}.
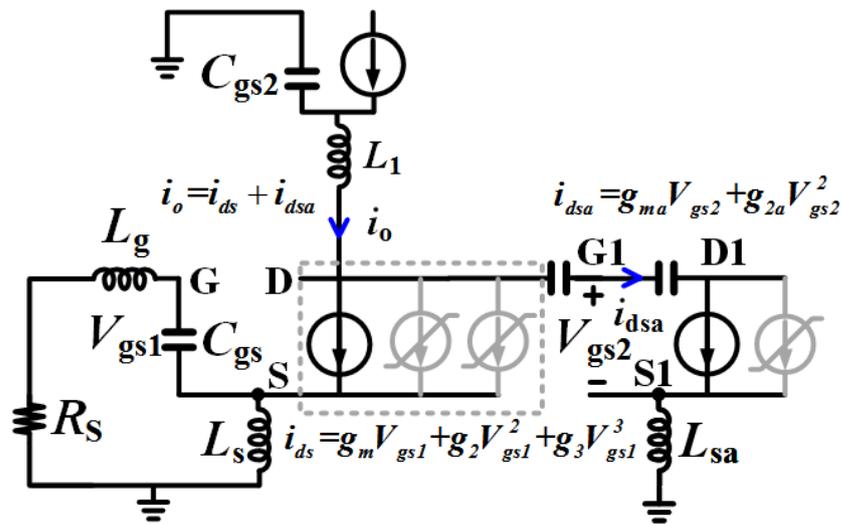
Figure 9. Equivalent circuit model for calculation of linearity.
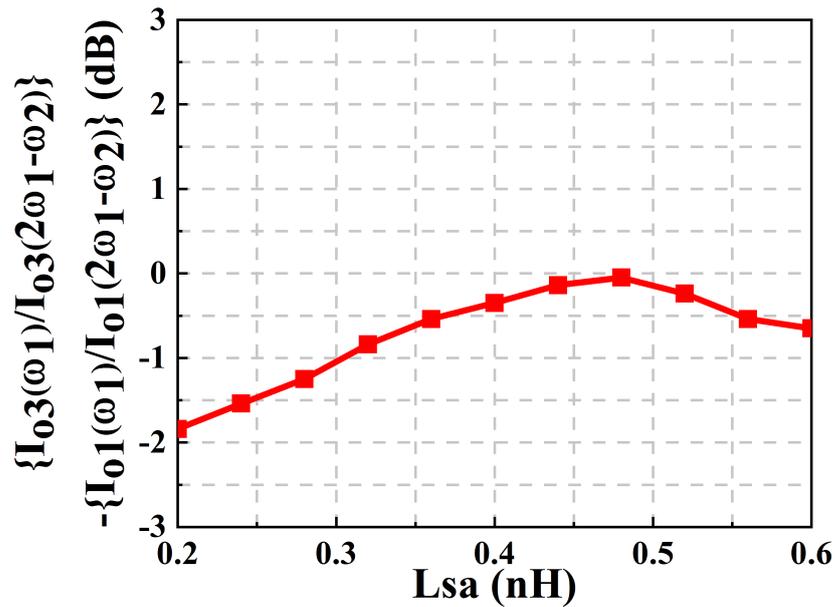
Figure 10. Linearity analysis at the drain node transistor of M_1 and M_3.

The voltage between gate and source node of transistor M_1, M_{AUX} and output current i_o can be considered up to third-order with Volterra theory as the following equations:

$$V_{gs1} = A_1(\omega) \circ V_{\text{in}} + A_2(\omega_1, \omega_2) \circ V_{\text{in}}^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_{\text{in}}^3 \tag{13a}$$

$$V_{gs2} = C_1(\omega) \circ V_{\text{in}} + C_2(\omega_1, \omega_2) \circ V_{\text{in}}^2 + C_3(\omega_1, \omega_2, \omega_3) \circ V_{\text{in}}^3 \tag{13b}$$

$$i_o = E_1(\omega) \circ V_{\text{in}} + E_2(\omega_1, \omega_2) \circ V_{\text{in}}^2 + E_3(\omega_1, \omega_2, \omega_3) \circ V_{\text{in}}^3 \tag{13c}$$

By utilizing the above Volterra series kernels, the output current i_o can be written as

$$
\begin{aligned}
i_o = \\
g_{m1}\left(A_1(\omega) \circ V_{\text{in}} + A_2(\omega_1, \omega_2) \circ V_{\text{in}}^2 + A_3(\omega_1, \omega_2, \omega_3) \circ V_{\text{in}}^3\right) + \\
g_2\left(A_1(\omega)A_1(\omega) \circ V_{\text{in}}^2 + \overline{2A_1(\omega)A_2(\omega_1, \omega_2)} \circ V_{\text{in}}^3\right) + \\
g_3(A_1(\omega)A_1(\omega)A_1(\omega)) \circ V_{\text{in}}^3 + \\
g_{ma}\left(C_1(\omega) \circ V_{\text{in}} + C_2(\omega_1, \omega_2) \circ V_{\text{in}}^2 + C_3(\omega_1, \omega_2, \omega_3) \circ V_{\text{in}}^3\right) + \\
g_{2a}\left(C_1(\omega)C_1(\omega) \circ V_{\text{in}}^2 + \overline{2C_1(\omega)C_2(\omega_1, \omega_2)} \circ V_{\text{in}}^3\right)
\end{aligned}
\tag{14}
$$

The above Volterra series kernels are calculated in Appendix B. Volterra Expansion Analysis. The third-order intercept point IIP3 could be further expressed as [14]

$$A_{IP3}(2\omega_1 - \omega_2) = \sqrt{\frac{4}{3}\left|\frac{E_1(\omega_1)}{E_3(\omega_1, \omega_1, -\omega_2)}\right|} \tag{15a}$$

$$\text{IIP}_3(2\omega_1 - \omega_2) = \frac{1}{6\Re(Z_1(\omega_1))}\left|\frac{E_1(\omega_1)}{E_3(\omega_1, \omega_1, -\omega_2)}\right| \tag{15b}$$

By augmenting an auxiliary L_{sa}, $E_1(\omega)$ can be enhanced at high frequency, which results in improved numerator in Equation (15a). One the other hand, according to above equations, the third-order nonlinearity of the main and auxiliary transistor M_1, M_{AUX} show complicated characteristics as frequency increases. $E_1(\omega_1)$ and $E_3(\omega_1, \omega_1, -\omega_2)$ can be obtained based on above equations and $A_{IP3}(2\omega_1 - \omega_2)$ can be calculated based on Equation (15a). To validate the proposed method, we compare the calculated and simulated normalized third-order intermodulation distortion (linearity improvement) of the combined current versus L_{sa} and frequency with and without modified post-distortion network based on the above equations. It can be shown in Figure 11 that $I_o(\omega_1)/I_o(2\omega_1 - \omega_2)$ can

be boosted by approximately 15 dB by choosing appropriate L_{sa}. The linearity enhancement versus inductor L_{sa} is simulated at 12 GHz as shown in Figure 12. According to simulated results, the IIP3 and OIP3 can be boosted by about 10 dB with proper inductance value. Here, we explain the cancellation mechanism by turning to vector diagram. From Figure 13, ideally, the third order nonlinearity ς_3, $\varsigma_{3,MAUX}$ generated by M_1, M_{AUX} is out of phase, which results in maximum IIP3. However, as frequency increases, ς_3 is non-collinear with $\varsigma_{3,MAUX}$, which degrades the distortion cancellation. To improve the IIP3 at high frequency region, auxiliary inductor L_{sa} is placed at the source node of transistor M_{AUX}. At low frequency, by augmenting the auxiliary inductor L_{sa}, the third-order nonlinearity $\varsigma_{3,MAUX}$ will rotate clockwise, with enhanced amplitude. This will result in degraded IIP3 performance compared with conventional post-distortion network. At the medium frequency range, the third-order nonlinearity $\varsigma_{3,MAUX}$ still rotate clockwise. However, the amplitude will $\varsigma_{3,MAUX}$ decrease with increasing value of L_{sa}. By choosing a proper value, ideally, the vector of ς_3 will be collinear with $\varsigma_{3,MAUX}$ with the out-of-phase state. Then, the IIP3 improvement can be achieved. In the high frequency range, as shown in Figure 13, the sum of the two vector ς_3 and $\varsigma_{3,MAUX}$ will increase by augmenting the L_{sa}. However, on the other hand, L_{sa} will increase the first-order current component. As a result, the IIP3 can be improved effectively compared with the conventional post-distortion method.
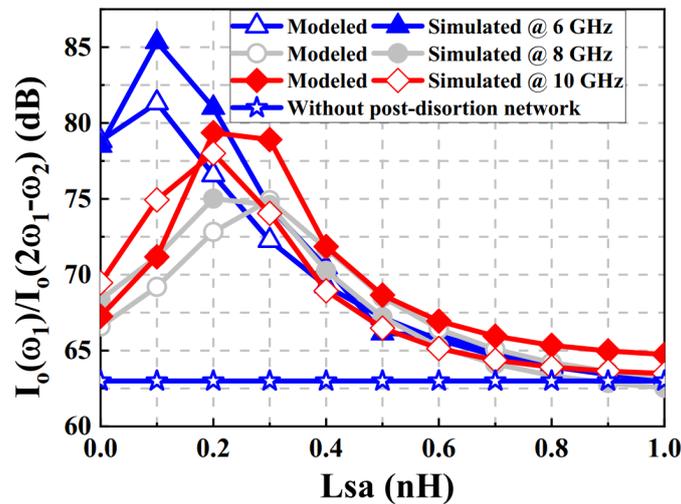
Figure 11. Comparison of calculated and simulated normalized third-order intermodulation distortion (linearity improvement) of the combined current versus L_{sa} and frequency with and without modified post-distortion network based on the above equations.
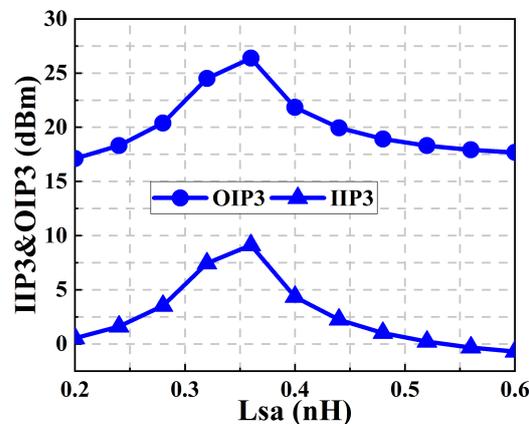
Figure 12. Simulated IIP3 and OIP3 versus L_{sa} of the proposed LNA.
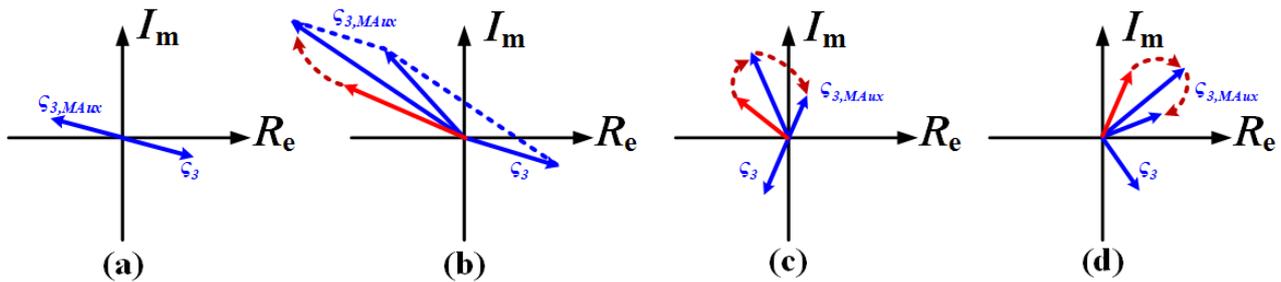
Figure 13. (**a**) Conceptual nonlinear cancellation mechanism; (**b**) ς_3 and $\varsigma_{3,MAux}$ vector diagram as L_{sa} increases in a low frequency range; (**c**) ς_3 and $\varsigma_{3,MAux}$ vector diagram as L_{sa} increase at medium frequency range; (**d**) ς_3 and $\varsigma_{3,MAux}$ vector diagram as L_{sa} increases in the high frequency range.

3. Experimental Results

Figure 14 shows a complete layout of the proposed LNA in a 130 nm CMOS process. To verify the designs, the bias circuit is made separately and not included in the main circuits of the proposed LNAs [5,12,22]. The simulated results of the S-parameters are shown in Figure 15. From Figure 15a, it is observed that the proposed LNA achieves good input matching over the desired band. The simulated S_{21} shows a flat power gain over a frequency of 8–12 GHz due to a dual-resonant network. However, the post layout simulation result shows that S_{21} degrades at a high frequency. The deviation of the power gain is caused by the parasitic capacitance of the layout at the drain node of transistor M_3. The simulated NFs are shown in Figure 15b. The modified post-distortion network contributes its own noise according to the noise analysis and results in increased NF.
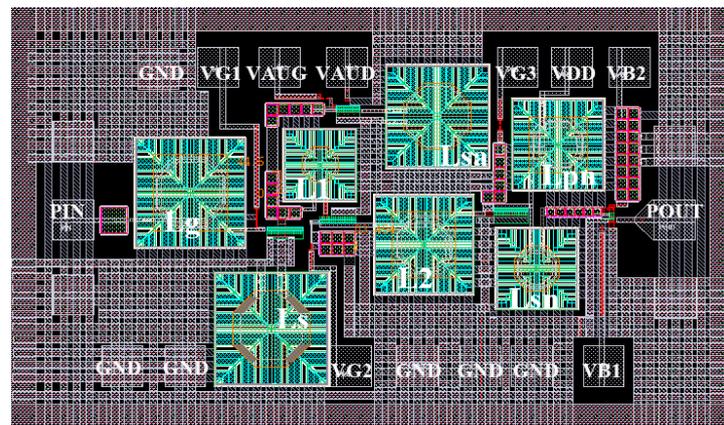
Figure 14. Layout of the proposed LNA.
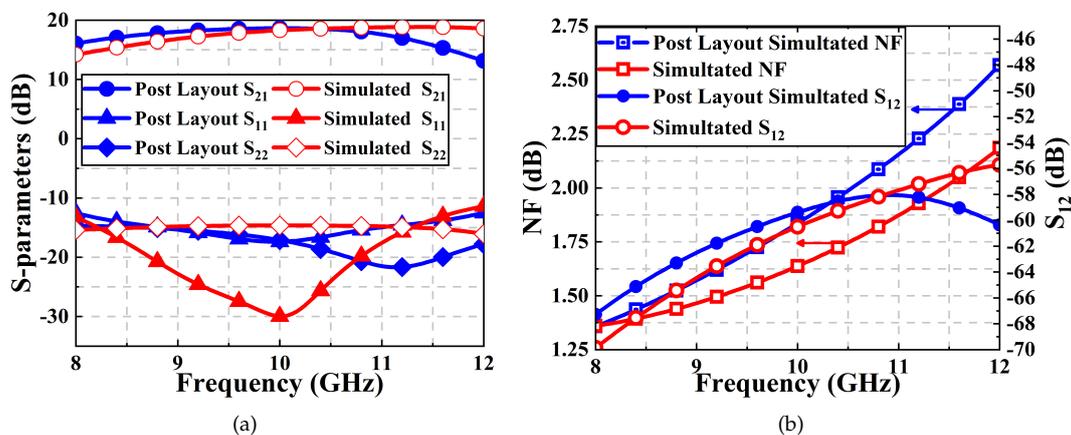
Figure 15. (**a**) Simulated S-parameters of the proposed LNA; (**b**) simulated NF and reverse isolation.

In Figure 16, the IIP3 and OIP3 are simulated by a two-tone test from 8–12 GHz. Compared with the conventional post-distortion network, the proposed technique can improve both IIP3 and OIP3 as frequency increases. According to the simulated result, the IIP3 of the proposed LNA varies from -3 dBm to $+8$ dBm over the X-band frequency range.
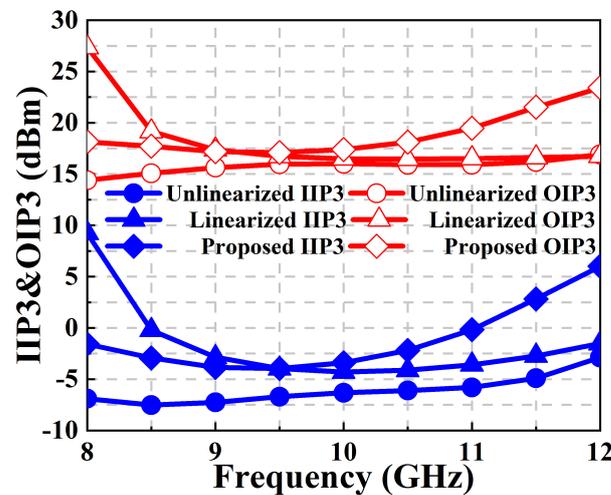
Figure 16. Simulated IIP3 and OIP3 based on the nonlinearized, conventional linearized post-distortion, and proposed post-distortion topology.

The designed LNA has been analyzed for various performance corners and process voltage-temperature (PVT) variations to study the robustness of the design. The process and device mismatch analyses for the proposed LNA are performed using Monte Carlo (MC) simulations for 200 samples of random mismatches. Figure 17 illustrates the temperature and corner changes on S_{11}, S_{21} and NF versus frequency. In general, the corner and temperature variations have little effects on the input matching and gain flatness. As shown in Figure 17, process variations at FF corner result in an increased gain and decreased NF due to the increase in the DC current. In the SS corner, the gain falls and NF rises due to a lower DC current. Figure 18 shows the Monte Carlo simulation distributions for 200 sample values of S_{21}, and NF at 10 GHz and IIP3. The statistical behavior of the gain and NF are plotted in Figure 18a,b, respectively. The LNA has the mean S_{21} of 18.2 dB with standard deviation of 0.32 dB. Similarly, the mean and the standard deviations of the NF at 10 GHz are 1.65 dB and 0.125 dB, respectively. From Figure 18c, the mean value of IIP3 is 2.65 dBm, where the standard deviation is 1.9 dBm. The majority of the results of S_{21}, NF are within one-sigma ($\pm 1\sigma$) and IIP3 of $\pm 3\sigma$ limit in the distribution will correspond to a high yield post-fabrication.
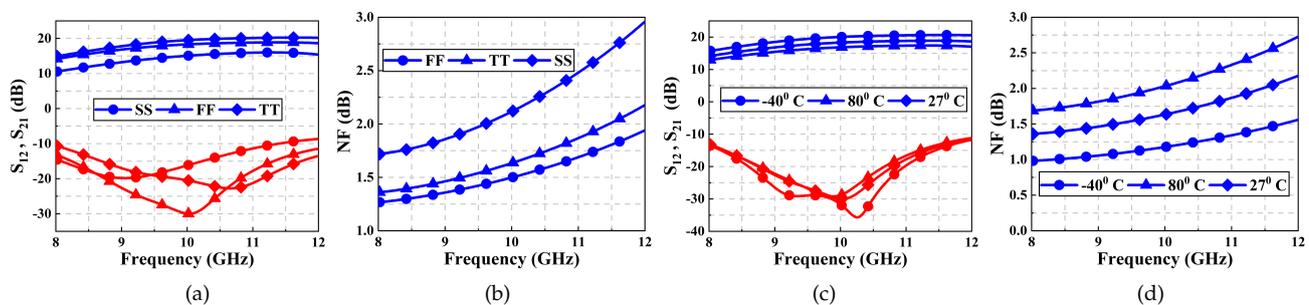
Figure 17. PVT simulation results of S-parameters and NF of the proposed LNA. (**a**) process corner simulations at TT–FF–SS of S-parameters; (**b**) process corner simulations at TT–FF–SS of NF; (**c**) temperature variation simulations of S-parameters; (**d**) temperature variation simulations of NF.
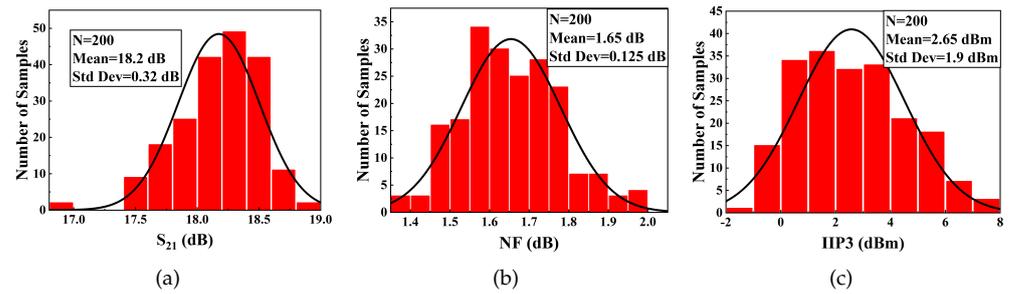
Figure 18. Monte Carlo simulations of the proposed LNA for 200 samples. (**a**) gain; (**b**) noise figure; (**c**) IIP3.

In order to evaluate the overall performance of various LNAs, diverse figure-of-merits (FOM) are employed. FOM1 is the ratio of Gain and BW to P_{DC} and NF. It is more commonly applied for comparing among low power LNAs, which does not include linearity. FOM2 introduces IIP3 in consideration of linearity effects. It is used to compare linearized LNAs [13,23,24]. Table 2 mainly shows a comparison of the cascode, two stage and triple-cascode LNA configuration. The proposed single stage triple-cascode LNA, with moderate power consumption, achieves enhanced bandwidth, flat gain, and excellent noise performance due to the modified input matching and dual-resonant network. On the other hand, the performance of the proposed LNA is competitive to that of noise cancelling LNA. Although the proposed LNA is implemented without the state-of art process, the proposed LNA achieves competitive FOM1 and FOM2:

$$FOM1 = \frac{Gain_{average}[abs]BW[GHz]}{P_{DC}[mW](F_{average}-1)} \tag{16}$$

$$FOM11 = \frac{Gain_{average}[abs]}{P_{DC}[mW](NF_{average}-1)[abs]} \tag{17}$$

$$FOM2 = \frac{IIP3_{average}[mW]Gain[abs]BW[GHz]}{P_{DC}[mW](F_{average}-1)} \tag{18}$$

$$FOM21 = \frac{IIP3_{average}[mW]Gain[abs]f_C[GHz]}{P_{DC}[mW](NF_{average}-1)[abs]} \tag{19}$$

Table 2. Performance comparison with other references.

	This	[19]	[25] [s]	[26]	[27]	[28] [s]	[29]	[30] [s]
BW [GHz]	**7.5~11.5**	6~10.3	2.3~9.3	3~12	1~12.5	3.1~10.6	6.4~7.4	3~5
S11 [dB]	**<−10**	<−10	<−8	<−10	<−10	<−10	<−10	<−10
S21 [dB]	**15~18**	20.5	10.3	14~16	13.7	10.24	18	17.98
NF [dB]	**1.8**	1.3	3.68	4.3	2.3	2.5	2.85	2.9
Power [mW]	**18**	100	9.97	8.5	18	17.92	19	20.73
IIP3 [dBm]	**−3~8**	5.25	−4	−7	−0.2	6.8	−3	−11
FOM1	**19.3**	13.4	5.59	12.04	21.4	5.7	3.58	6.37
FOM2	**24.3**	46	2.23	2.4	20.4	27.4	1.79	0.51
FOM11	**2.1**	1.1	0.6	1.2	0.9	0.4	2.2	1.9
FOM21	**25.9**	28.1	1.4	1.8	6.4	12.1	7.5	0.6
Topology	**TriCas**	TriCas	NC	CG	Two Stage Inverter	Cas	Cas	Two Stage Cas
Technology	**130 nm CMOS**	130 nm SiGe	130 nm CMOS	130 nm CMOS	180 nm CMOS	130 nm CMOS	180 nm CMOS	180 nm CMOS

[s] = Simulated results, Cas = Cascode, TriCas = Triple Cascode, NC = Noise Cancelling, CG = Common Gate.

4. Conclusions

In this paper, the proposed X-band linearized LNA with extra low power consumption is designed. The proposed post-distortion network utilizes the auxiliary transistor M_{AUX} operated in the weak inversion region, which dissipates low power consumption.

The graphical explanation of the post distortion mechanism is discussed explicitly. Compared with the conventional post distortion technique, the proposed auxiliary network can improve the $\varsigma_{1,Combine}$ at a high frequency. Furthermore, due to the dual-resonant network, the bandwidth can be extended. The simulation results show the good performance of the proposed LNA and confirm the reliability of proposed mathematical derivations.

Appendix A. Numerator and Denominator for Bandwidth Calculation

According to the input impedance, the numerator and denominator can be calculated as

$$\text{Re}[Numerator[S_{11}]] = 1 - C_{gs}(L_g + L_s)\omega_x^2 + C_{GD}\omega_x \left\{ \begin{array}{l} -X_L + g_{m1}[R_S X_L + L_s\omega_x(R_S - R_L)] \\ +L_g\omega_x \left[\begin{array}{l} -1 + C_{gs}\omega_x(L_s\omega_x + X_L) \\ -g_{m1}R_L \end{array} \right] \\ +C_{gs}\omega_x(L_s\omega_x X_L + R_S R_L) \end{array} \right\} \tag{A1}$$

$$\text{Im}[Numerator[S_{11}]] = -\omega_x \left\{ \begin{array}{l} R_S[C_{gs} + C_{GD} - C_{gs}C_{GD}\omega_x(L_s\omega_x + X_L)] + \\ C_{GD}[-1 + C_{gs}(L_s + L_g)\omega_x^2]R_L + \\ g_{m1} \left\{ \begin{array}{l} L_s[-1 + C_{GD}\omega_x(L_g\omega_x + X_L)] + \\ +C_{GD}(L_g\omega_x X_L + R_S R_L) \end{array} \right\} \end{array} \right\} \tag{A2}$$

$$\text{Re}[Denominator[S_{11}]] = 1 - C_{gs}(L_g + L_s)\omega_x^2 + C_{GD}\omega_x \left\{ \begin{array}{l} -X_L - g_{m1}[R_S X_L + L_s\omega_x(R_S + R_L)] \\ +L_g\omega_x \left[\begin{array}{l} -1 + C_{gs}\omega_x(L_s\omega_x + X_L) \\ -g_{m1}R_L \end{array} \right] \\ +C_{gs}\omega_x(L_s\omega_x X_L - R_S R_L) \end{array} \right\} \tag{A3}$$

$$\text{Im}[Denominator[S_{11}]] = -\omega_x \left\{ \begin{array}{l} R_S[-(C_{gs} + C_{GD}) + C_{gs}C_{GD}\omega_x(L_s\omega_x + X_L)] + \\ C_{GD}[-1 + C_{gs}(L_s + L_g)\omega_x^2]R_L + \\ g_{m1} \left\{ \begin{array}{l} L_s[-1 + C_{GD}\omega_x(L_g\omega_x + X_L)] + \\ +C_{GD}(L_g\omega_x X_L - R_S R_L) \end{array} \right\} \end{array} \right\} \tag{A4}$$

Appendix B. Volterra Expansion Analysis

To solve the first, second, and third Volterra series kernels in the above equations, we can utilize Kirchhoff's circuit law (KCL) as the following:

$$V_{in} - (R_S + j\omega L_g)V_{gs1}j\omega C_{gs} = V_{gs1} + j\omega L_s(V_{gs1}j\omega C_{gs} + i_{ds}) \tag{A5a}$$

$$-Z_L(i_{ds} + i_{dsa}) = j\omega L_{sa}i_{dsa} + V_{gs2} \tag{A5b}$$

Based on the above equations, the Volterra series kernels can be derived as

$$A_1(\omega) = \frac{1}{H_1(\omega)} \tag{A6a}$$

$$H_1(\omega) = 1 + j\omega L_s g_{m1} + (R_S + j\omega(L_g + L_s))j\omega C_{gs} \tag{A6b}$$

$$A_2(\omega_1, \omega_2) = -\frac{j(\omega_1 + \omega_2)L_s g_2 A_1(\omega_1)A_1(\omega_2)}{H_1(\omega_1 + \omega_2)} \tag{A6c}$$

$$\overline{2A_1(\omega_1)A_2(\omega_1,-\omega_2)} = \frac{2}{3}[-jL_sg_2]\left[\frac{2\Delta\omega}{H_1(\Delta\omega)}+\frac{2\omega}{H_1(2\omega)}\right][A_1(\omega_1)A_1(-\omega_2)A_1(\omega_1)] \tag{A6d}$$

$$A_3(\omega_1,\omega_2,\omega_3) = -\frac{j\omega L_s g_2 2A_1(\omega_1)A_2(\omega_2,\omega_3)+j\omega L_s g_3(A_1(\omega_1)A_1(\omega_2)A_1(\omega_3))}{H_1(\omega_1+\omega_2+\omega_3)} \tag{A6e}$$

$$C_1(\omega) = \frac{-Z_L\times g_{m1}A_1(\omega)}{(1+(j\omega L_{sa}+Z_L)\times g_{ma})} \tag{A6f}$$

$$C_2(\omega_1,\omega_2) = -\frac{(Z_L\times g_{m1}A_2(\omega_1,\omega_2)+Z_L\times g_2 A_1(\omega)A_1(\omega)+(j\omega L_{sa}+Z_L)\times g_{2a}C_1(\omega)C_1(\omega))}{(1+(j\omega L_{sa}+Z_L)\times g_{ma})} \tag{A6g}$$

$$\overline{2C_1(\omega_1)C_2(\omega_1,-\omega_2)} = \frac{2}{3}\left[\begin{array}{l}\frac{2\times Z_L\times g_{m1}A_1(\omega_1)}{[1+(j\omega_1 L_{sa}+Z_L)\times g_{ma}]}\left[\begin{array}{l}Z_L\times g_{m1}A_2(\omega_1,-\omega_2)+Z_L\times g_2 A_1(\omega_1)A_1(-\omega_2)\\+(j\Delta\omega L_{sa}+Z_L)\times g_{2a}C_1(\omega_1)C_1(-\omega_2)\\\overline{\qquad(1+(j\Delta\omega L_{sa}+Z_L)\times g_{ma})\qquad}\end{array}\right]\\\frac{Z_L\times g_{m1}A_1(-\omega_2)}{[1+(j(-\omega_2)L_{sa}+Z_L)\times g_{ma}]}\left[\begin{array}{l}Z_L\times g_{m1}A_2(\omega_1,\omega_1)+Z_L\times g_2 A_1(\omega_1)A_1(\omega_1)\\+(j2\omega L_{sa}+Z_L)\times g_{2a}C_1(\omega_1)C_1(\omega_1)\\\overline{\qquad(1+(j2\omega L_{sa}+Z_L)\times g_{ma})\qquad}\end{array}\right]\end{array}\right] \tag{A6h}$$

$$C_3(\omega_1,\omega_2,\omega_3) = -\frac{\left(\begin{array}{l}Z_L\times g_{m1}A_3(\omega_1,\omega_2,\omega_3)+Z_L\times g_2 2A_1(\omega)A_2(\omega_1,\omega_2)+\\(j(\sum\omega_i)L_{sa}+Z_L)\times g_{2a}2C_1(\omega)C_2(\omega_1,\omega_2)\\+Z_L\times g_3(A_1(\omega_1)A_1(\omega_2)A_1(\omega_3))+(j\omega L_{sa}+Z_L)\times g_{2a}C_1(\omega_1)C_1(\omega_2)C_1(\omega_3)\end{array}\right)}{\left(1+\left(j\left(\sum\limits_{i=1}^{3}\omega_i\right)L_{sa}+Z_L\right)\times g_{ma}\right)} \tag{A6i}$$

$$\begin{aligned}i_o =\ & g_m\big(A_1(\omega)\circ V_{\text{in}}+A_2(\omega_1,\omega_2)\circ V_{\text{in}}^2+A_3(\omega_1,\omega_2,\omega_3)\circ V_{\text{in}}^3\big)+\\&g_2\big(A_1(\omega)A_1(\omega)\circ V_{\text{in}}^2+2A_1(\omega)A_2(\omega_1,\omega_2)\circ V_{\text{in}}^3\big)+\\&g_3(A_1(\omega)A_1(\omega)A_1(\omega))\circ V_{\text{in}}^3+\\&g_{ma}\big(C_1(\omega)\circ V_{\text{in}}+C_2(\omega_1,\omega_2)\circ V_{\text{in}}^2+C_3(\omega_1,\omega_2,\omega_3)\circ V_{\text{in}}^3\big)+\\&g_{2a}\big(C_1(\omega)C_1(\omega)\circ V_{\text{in}}^2+2C_1(\omega)C_2(\omega_1,\omega_2)\circ V_{\text{in}}^3\big)\\=\ &\underbrace{[g_m A_1(\omega)+g_{ma}C_1(\omega)]}_{E_1(\omega)}\circ V_{\text{in}}\\&+\underbrace{[g_m A_2(\omega_1,\omega_2)+g_2 A_1(\omega)A_1(\omega)+g_{ma}C_2(\omega_1,\omega_2)+g_{2a}C_1(\omega)C_1(\omega)]}_{E_2(\omega_1,\omega_2)}\circ V_{\text{in}}^2\\&+\underbrace{\left[\begin{array}{l}g_m A_3(\omega_1,\omega_2,\omega_3)+g_2 2A_1(\omega)A_2(\omega_1,\omega_2)+g_3 A_1(\omega)A_1(\omega)A_1(\omega)\\+g_{ma}C_3(\omega_1,\omega_2,\omega_3)+g_{2a}2C_1(\omega)C_2(\omega_1,\omega_2)\end{array}\right]}_{E_3(\omega_1,\omega_2,\omega_3)}\circ V_{\text{in}}^3\end{aligned} \tag{A7}$$

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