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Analysis of Electrothermal Effects in Devices and Arrays in InGaP/GaAs HBT Technology

Vincenzo d'Alessandro [1,*], Antonio Pio Catalano [1], Ciro Scognamillo [1], Lorenzo Codecasa [2] and Peter J. Zampardi [3]

[1] Department of Electrical Engineering and Information Technology, University Federico II, 80125 Naples, Italy; antoniopio.catalano@unina.it (A.P.C.); ciro.scognamillo@unina.it (C.S.)
[2] Department of Electronics, Information, and Bioengineering, Politecnico di Milano, 20133 Milan, Italy; lorenzo.codecasa@polimi.it
[3] Qorvo, Inc., Newbury Park, CA 91320, USA; Peter.Zampardi@qorvo.com
* Correspondence: vindales@unina.it

Abstract: In this paper, the dc electrothermal behavior of InGaP/GaAs HBT test devices and arrays for power amplifier output stages is extensively analyzed through an efficient simulation approach. The approach relies on a full circuit representation of the domains, which accounts for electrothermal effects through the thermal equivalent of the Ohm's law and can be solved in any commercial circuit simulator. In particular, the power-temperature feedback is described through an equivalent thermal network *automatically* obtained by (i) generating a realistic 3-D geometry/mesh of the domain in the environment of a numerical tool with the aid of an *in-house* routine; (ii) feeding the geometry/mesh to FANTASTIC, which extracts the network without performing simulations. Nonlinear thermal effects adversely affecting the behavior of devices/arrays at high temperatures are included through a calibrated Kirchhoff's transformation. For the test devices, the thermally-induced distortion in *I–V* curves is explained, and the limits of the safe operating regions are identified for a wide range of bias conditions. A deep insight into the electrothermal behavior of the arrays is then provided, with particular emphasis on the detrimental nonuniform operation. Useful guidelines are offered to designers in terms of layout and choice of the ballasting strategy.

Keywords: electrothermal (ET) simulation; finite-element method (FEM); gallium arsenide (GaAs); heterojunction bipolar transistor (HBT); model-order reduction (MOR); thermal resistance

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1. Introduction

Gallium arsenide (GaAs) heterojunction bipolar transistors (HBTs) are the dominant technology for handset power amplifier (PA) design by virtue of their power density, cut-off frequency, and efficiency [1]. However, designing rugged circuits with GaAs HBT devices requires extra care because of strong electrothermal (ET) effects arising from (i) low thermal conductivity of the substrate, (ii) lateral heat confinement by mesa isolation, and (iii) high operating currents. Thermal-aware design methodologies relying on suitable ET simulation tools are highly desired to alleviate or avoid performance and reliability degradation. Unfortunately, the choice of the simulation approach is challenging. Full 3-D ET device simulations based on the finite-element method (FEM), e.g., with Atlas from Silvaco or Sentaurus from Synopsys, are computationally onerous or even unviable when dealing with complex structures like practical transistor arrays and packages.

A more efficient, yet accurate enough, approach is based on the generation and solution of a SPICE-compatible *purely-electrical macrocircuit* that accounts for ET effects by means of the *thermal equivalent of the Ohm's law* (TEOL). In this macrocircuit, the power-temperature feedback is included through an equivalent thermal network (ETN, an electrical circuit relying on the TEOL), the components of which can be optimized in a pre-processing stage

with the aid of 3-D thermal-only FEM simulations. A key part of this strategy is implementing an analytical transistor model as a *subcircuit*, in which the temperature-sensitive parameters are allowed to vary during the simulation run thanks to the TEOL (e.g., [2–4]). We adopted such an approach—based on *in-house* models for individual transistors—to examine the dc and transient ET behavior of devices/circuits for a large variety of technologies and applications, namely, single- and multi-finger silicon-on-glass (SOG) bipolar transistors [5–7]; output arrays of PAs in InGaP/GaAs HBT technology, yet with relevant approximations in describing the geometry of the devices [8]; basic analog blocks, like simple current mirrors [9,10], differential pairs [11,12], and cascode amplifiers [13] in many bipolar technologies (GaAs, SOG, and silicon-germanium); vertical double-diffused silicon-carbide MOS transistors with a multicellular pattern [14].

In our earlier contribution [15], we exploited the aforementioned approach to analyze the dc ET behavior of test devices meant for experimental characterization and arrays for output stages of PAs in InGaP/GaAs HBT technology. In that case, a simple ETN based on the $N \times N$ thermal resistance (R_{TH}) matrix, N being the number of individual HBTs (each associated to one heat source), was adopted in the macrocircuits. The R_{TH}s were determined through pre-processing 3-D linear FEM simulations performed with COMSOL [16] aided by an *in-house* routine [17] for an *exceptionally accurate* and *automated* construction of the geometry/mesh of the structures. Nonlinear thermal effects dictated by high temperatures were taken into account through the Kirchhoff's transformation [18,19]. The ET simulations were performed using the popular PSPICE program [20].

This paper is aimed at extending [15] in a multi-fold way.

- More details of the individual transistor model and its subcircuit implementation are provided.
- Differently from [15], where the arrays were assumed to lie on an unthinned GaAs substrate (as typical for *known-good-die* identification), here they are considered in a realistic phone-board environment, i.e., the substrate is thinned and attached on a laminate, the bottom of which is at T_B = 358 K.
- Similar to [21], in this work the linear power-temperature feedback is described by invoking FANTASTIC [22,23], which is fed with the COMSOL geometry/mesh accompanied with additional information (on position/shape of heat sources, boundary conditions, and thermal conductivities), and rapidly extracts an ETN based on the R_{TH} matrix *without performing simulations*. Contrary to conventional ETNs (like the one used in [15]), the FANTASTIC network allows reconstructing the overall temperature field for selected bias conditions in a post-processing step.
- In [15], the Kirchhoff's transformation was applied by assuming that all materials share the same nonlinear thermal behavior as GaAs. Unfortunately, this was found to lead to a perceptible *overestimation* of ET effects. Here, more realistic results are achieved by carrying out a suitable preliminary calibration procedure, similar to that made in [21].

By virtue of the above points, this work can be reviewed as an improved, and self-consistent, version of [15].

The remainder of the paper is outlined as follows. In Section 2, the technology/layout details of test devices and arrays are given. Section 3 probes into the simulation approach; in particular, the transistor model, its subcircuit representation, the COMSOL geometry/mesh generation, the FANTASTIC extraction of the R_{TH}-based ETN, and the assembling of the final macrocircuit are described. Section 4 reports and discusses the dc ET simulation results carried out by PSPICE. Conclusions are then drawn in Section 5.

2. Devices and Arrays

The structures investigated in this paper are mesa-isolated InGaP/GaAs NPN HBTs manufactured by Qorvo using an HBT-only process (referred to as HBT8) with two metal layers (e.g., [23,24]), the key features of which are reported in Table 1. The individual transistor, hereinafter also denoted as *unit cell* (Figure 1), is composed by four emitter

fingers, each with a 2 × 20.5 μm^2 area (the total emitter area is then equal to 164 μm^2). The emitter is composed by a stack of four layers, namely (from the top):

- an $In_{0.5}Ga_{0.5}As$ cap to reduce the contact resistance with the gold (Au)-based emitter metallization;
- a grading $In_xGa_{1-x}As$ layer (with x spanning from 0.5 to 0) used to ensure a good lattice continuity with the underneath layer;
- a GaAs layer acting as a set-back for an easier manufacturing process;
- an n-doped $In_{0.49}Ga_{0.51}P$ emitter layer, the bottom surface of which corresponds to the metallurgical base-emitter junction.

Table 1. Key features of the investigated HBT technology.

Parameter	Value
Common-emitter current gain at 300 K and medium current levels β_{F0}	135
Open-emitter breakdown voltage BV_{CBO}	27 V
Open-base breakdown voltage BV_{CEO}	17 V
Peak cut-off frequency f_T for V_{CE} = 3 V	40 GHz
Collector current density J_C at peak f_T for V_{CE} = 3 V	0.2 mA/μm^2
Maximum oscillation frequency f_{MAX}	82 GHz

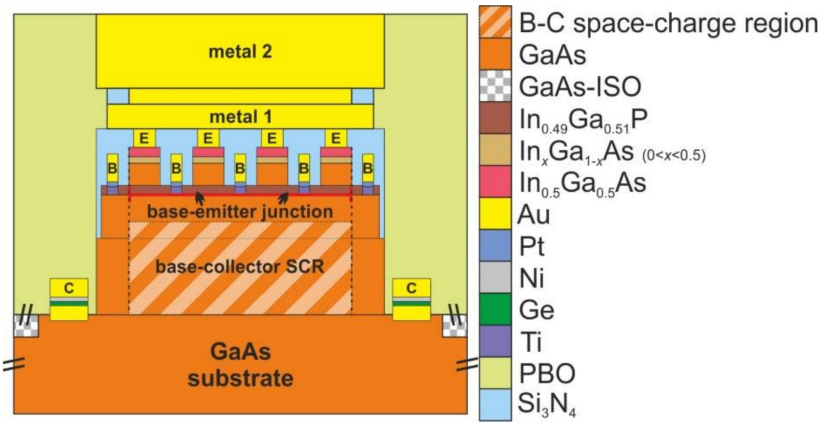

Figure 1. Schematic cross-section of the HBT unit cell highlighting the materials, the base-emitter junction, and the base-collector space-charge region (SCR).

The base is a thin p-doped GaAs layer lying on a thick n-type GaAs mesa.

Both the base and collector contacts are designed with materials compatible with the manufacturing process in order to reduce the parasitic resistances. More specifically, the base contact is composed by the series of titanium (Ti) and platinum (Pt) layers that alloy through the leftover InGaP emitter on the base mesa, while the collector contact is located at the bottom of this mesa on the highly-doped GaAs subcollector layer and consists of a stack of Au-germanium (Ge)-nickel (Ni) layers. A metallization with two Au levels is exploited to electrically connect the unit cells and plays a role in the thermal exchange by favoring heat shunt and spread [24].

The electrical isolation from potential neighboring components is ensured by ion-implant damage (referred to as GaAs-ISO) resulting in an amorphous GaAs layer. Far from the active regions, the metal layers are separated from the GaAs substrate through a thin silicon nitride (Si_3N_4) layer providing some shunt effect. A 10-μm-thick polybenzoxazole (PBO) layer covers the whole structure.

The analysis first focuses on devices fabricated on a 620-μm-thick GaAs substrate (thickness normally used for testing) and provided with 65 × 65 μm^2 pads (in a ground–signal–ground configuration) for bare-die experimental characterization through RF probes. The devices have been designed with a single unit cell, as well as with two and three

paralleled cells, respectively (Figure 2, top). In the analysis reported in Section 4, the temperature T_0 = 300 K (hereinafter also denoted as *reference* temperature) is assumed to be applied to the substrate backside, which can be practically done with a thermochuck.

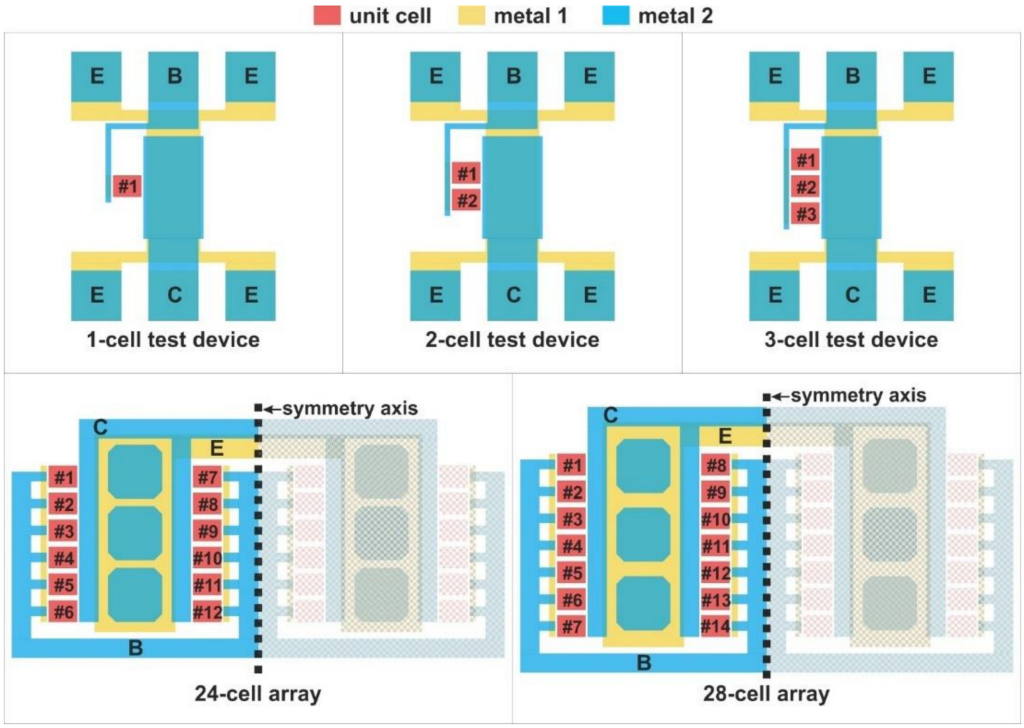

Figure 2. Schematic layouts of all the structures analyzed in this work: (**top**) 1-, 2-, 3-cell test devices; (**bottom**) 24- and 28-cell arrays. As clarified in Section 3.4, only half of the arrays (comprising 12 and 14 unit cells, respectively) was thermally and electrothermally simulated.

Subsequently, the investigation is conducted on transistor arrays for PA output stages, where the unit cells are arranged in columns to (i) ensure an almost uniform distance from them to the through-wafer via providing the ground; (ii) meet the very stringent die size requirements. The arrays are assumed to be operating in a typical phone-board environment. Architectures with even and odd number of unit cells per column are examined to offer helpful guidelines to designers. In particular, arrays comprising 24 and 28 unit cells are considered, which are both arranged in four columns composed by six and seven cells each, respectively (Figure 2, bottom). In contrast to the simplified analysis performed in [15], (i) the arrays lie on a 100 µm-thick die, obtained by thinning the original 620-µm-thick wafer; (ii) the die is attached with epoxy to an 830 × 830 µm^2-wide and 270 µm-thick laminate, which includes eight 600 × 600 µm^2-wide 12 µm-thick Cu plates connected by nine circular Cu vias, all embedded in a dielectric; (iii) as previously mentioned, the laminate bottom is held at T_B = 358 K, which is typical in the phone-board environment.

3. Simulation Approach

3.1. General Description

Similar to our previous papers [5–15,21], we chose to employ a *circuit-based* approach, which provides a good trade-off between computational overhead and accuracy. Such an approach makes use of the TEOL and can be summarized as follows:

- Each four-finger unit cell is represented with one SPICE-compatible *subcircuit* (Section 3.3) implementing a simple analytical transistor model (Section 3.2). This assumption relies on the following considerations: (i) the two metals uniformly distribute the temperature over the base-emitter junction; (ii) the electron currents emerging from

the four closely-spaced individual emitters are expected to spread and give rise to only one heat source. The subcircuit uses (i) a basic/standard bipolar transistor at reference (and unchangeable) temperature T_0 as a *core* component, and (ii) linear and nonlinear controlled sources to account for the variation of the temperature-sensitive parameters during the simulation run, as well as for other specific mechanisms. According to the TEOL, the temperature rise $\Delta T_j = T_j - T_0$ averaged over the base-emitter junction (which mainly influences the ET device behavior) is actually a voltage, while the dissipated power P_D is treated as a current. In addition to the standard transistor terminals (emitter, base, and collector), the unit-cell subcircuit is also equipped with an input node carrying the "voltage" ΔT_j and with an output node offering the "current" P_D.

- The power-temperature feedback is described with a SPICE-compatible *thermal feedback block* (TFB), the construction of which is carried out in a pre-processing stage. The TFB contains an ETN including the matrix of self-heating (SH) R_{TH}s of the unit cells and mutual R_{TH}s among them. The inputs of the ETN are the powers P_D dissipated by the cells (represented with currents), and the outputs are their temperature rises $\Delta T_{jlin} = T_{jlin} - T_0$ for the test devices or $\Delta T_{jlinB} = T_{jlin} - T_B$ for the arrays (all emulated with voltages) under *linear* thermal conditions.
- The ETN is *automatically* determined through the following procedure. First, an accurate 3-D geometry/mesh of the domain is built in the COMSOL environment using an *in-house* routine; then, the geometry/mesh, along with additional information concerning position/shape of heat sources, boundary conditions, and thermal conductivities, is fed to FANTASTIC, which extracts the ETN in a really short time without the need of user's intervention/expertise or onerous FEM simulations (Section 3.5). Generally, the whole process is very fast and error-free. The adoption of FANTASTIC is an improvement over our prior contribution [15], where (i) the R_{TH} matrix was calculated by performing N purely-thermal static COMSOL simulations by activating only one heat source at a time, and (ii) the simple ETN adopted did not allow a post-processing reconstruction of the whole temperature map in the domain.
- As mentioned above, the ETN only accounts for linear thermal conditions. However, *nonlinear* thermal effects can be significant when particularly high temperatures are reached. Such effects are taken into account by making use of the Kirchhoff's transformation, which converts the linear temperature rises ΔT_{jlin} (test devices) or ΔT_{jlinB} (arrays) offered by the ETN into the nonlinear counterparts $\Delta T_j = T_j - T_0$ and $\Delta T_{jB} = T_j - T_B$, respectively. Contrary to [15], here the transformation was properly calibrated (Section 3.4) to improve the ET simulation accuracy.
- Besides the ETN, the TFB also includes N voltage-controlled voltage sources that apply the calibrated Kirchhoff's transformation to the ETN linear outcomes; as a result, the nonlinear temperature rises ΔT_j (test devices) and ΔT_{jB} (arrays) are computed; only for the arrays, the increment $T_B - T_0$ is added to ΔT_{jB} to get the N nonlinear $\Delta T_j = T_j - T_0$ to be provided to the unit-cell subcircuits.
- The subcircuits are then connected to the TFB in the environment of a commercial circuit simulation tool. As a result, the whole domain is transformed into a *purely-electrical macrocircuit*, which inherently accounts for ET effects (Section 3.6): the temperature, and thus the temperature-sensitive parameters, are allowed to vary during the simulation run. The task of solving this macrocircuit is given to the powerful and robust engine of the circuit simulation tool, with very low computational effort and minimized occurrence of convergence issues compared to other numerical methods.

3.2. Bipolar Transistor Model

The analytical model used to describe the dc behavior of the unit cell is simple, accurate enough, and associated to a low-effort parameter extraction process; this provides

high flexibility to the overall approach. The collector current in forward active mode is given by [13]

$$I_C = I_{CnoAV} + I_{AV} = M \cdot I_{CnoAV} = M \cdot \left(1 + \frac{V_{CB}}{V_{AF}}\right) \cdot \frac{1}{B_{HI}} \cdot A_E \cdot J_{S0} \cdot \exp\left(\frac{V_{BEj} + \phi \cdot \Delta T_j}{\eta \cdot V_{T0}}\right) \quad (1)$$

where:

- I_{CnoAV} [A] is the collector current in the absence of impact-ionization (II), or avalanche, effects;
- I_{AV} [A] is the collector current component only induced by avalanche;
- V_{CB} [V] is the collector-base voltage;
- V_{AF} [V] is the forward Early voltage;
- M (≥ 1) is the dimensionless V_{CB}-dependent avalanche multiplication factor;
- A_E [μm^2] is the emitter area;
- J_{S0} [$A/\mu m^2$] is the reverse saturation current density at the reference temperature T_0 = 300 K;
- η is the ideality coefficient at T_0;
- V_{T0} = 0.02586 V is the thermal voltage at T_0;
- V_{BEj} [V] is the internal (junction) base-emitter voltage, that is, $V_{BEj} = V_{BE} - R_B \cdot I_B - R_E \cdot I_E$, where V_{BE} is the externally-accessible base-emitter voltage, I_B, I_E [A] are the base and emitter currents, and R_B, R_E [Ω] are the parasitic base and emitter resistances, respectively;
- the temperature rise ΔT_j [K] is defined as $T_j - T_0$, T_j being the temperature averaged over the base-emitter junction;
- ϕ [V/K] is the temperature coefficient of V_{BEj};
- B_{HI} ($\geq$1) is an I_E-dependent dimensionless term introduced to describe the attenuation dictated by high-injection (HI) effects, i.e., the Kirk-induced gain roll-off.

In this approach, the temperature dependence of I_C is taken into account with a V_{BEj} shift, while J_{S0}, η, and V_{T0} are kept at their T_0 values (e.g., [25]). Coefficient ϕ [V/K] is assumed to vary with emitter current I_E according to the following logarithmic law [11,13,26–29]:

$$\phi = \phi_0 - \eta \cdot \frac{k}{q} \cdot \ln\left(\frac{I_E}{A_E \cdot J_{S0}}\right) \quad (2)$$

where k [eV/K] is the Boltzmann's constant, and q [C] is the (absolute value of the) electron charge; parameter ϕ_0 can be extracted by comparing (1) with I_C–V_{BE} characteristics measured at various backside temperatures at low current levels for V_{CB} = 0 V [29].

As far as factor M is concerned, any model can in principle be adopted. For the GaAs HBTs under analysis, we chose the classic Miller model given by [30]

$$M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^{n_{AV}}} \quad (3)$$

BV_{CBO} [V] and n_{AV} being the open-emitter breakdown voltage and a fitting power factor, respectively.

The HI attenuation term B_{HI} is modeled as [5,13]

$$B_{HI} = 1 + \left(\frac{\alpha_F \cdot I_E}{A_E \cdot J_{HI}}\right)^{n_{HI}} \quad (4)$$

where α_F is the common-base (CB) forward current gain, while J_{HI} [$A/\mu m^2$] and n_{HI} are fitting parameters.

The common-emitter (CE) forward current gain β_F is modeled as

$$\beta_F = \beta_{F0} \cdot \left(1 + \frac{V_{CB}}{V_{AF}}\right) \cdot \frac{1}{B_{HI}} \cdot \exp\left[\frac{\Delta E_G}{k} \cdot \left(\frac{1}{\Delta T_j + T_0} - \frac{1}{T_0}\right)\right] \quad (5)$$

where β_{F0} is the gain at T_0, at medium current levels (i.e., before the Kirk-induced fall-off), and in the absence of Early effect, while ΔE_G [eV] is the positive difference between the bandgaps of emitter and base yielding a negative temperature coefficient (NTC). The CB gain α_F in (4) is related to the CE counterpart by $\alpha_F = \beta_F/(1 + \beta_F)$.

The base current is given by (e.g., [13,31])

$$I_B = I_{BnoAV} - I_{AV} = \frac{I_{CnoAV}}{\beta_F} - (M-1)\cdot I_{CnoAV} = I_{CnoAV}\cdot\left(\frac{1}{\alpha_F} - M\right) = I_C\cdot\left(\frac{1}{\alpha_F M} - 1\right) \quad (6)$$

where use has been made of (1).

We note that replacing the simple M formulation (3) with a more complex one (e.g., [31]), the model can be adopted for bipolar transistors fabricated in *any* technology if a proper parameter calibration procedure is performed (in silicon devices, ΔE_G is *negative*, since the emitter bandgap is narrower than that of the base due to high doping levels).

The parameter extraction procedure is straightforward (details are reported in [29]). The values adopted for the simulations described in Section 4 are reported in Table 2.

Table 2. Model parameter values.

Parameter	Value
A_E	164 μm^2
J_{S0}	3.5×10^{-26} A/μm^2
η	1.01
V_{AF}	1000 V
β_{F0}	135
ϕ_0	5.4 mV/K
$\Delta E_G/k$	200 K^{-1}
J_{HI}	0.35 mA/μm^2
n_{HI}	1
BV_{CBO}	27 V
n_{AV}	9 [32]
R_E	1 Ω
R_B	3.5 Ω

3.3. SPICE Unit-Cell Subcircuit

A sketch of the subcircuit is reported in Figure 3, which evidences the standard bipolar transistor model as a *core* component at temperature T_0, as well as the additional ΔT_j (input) and P_D (output) terminals. Linear/nonlinear controlled voltage/current sources are added to enable the variation of the temperature-sensitive parameters during the simulation run, as well as to account for physical mechanisms not included in the standard transistor (for this reason, the resulting subcircuit is also popularly referred to as *wrapper model*). The II-free collector current I_{CnoAV} accounting for the temperature dependence of V_{BEj}, HI, and Early effects is computed with the nonlinear source denoted with **A**. The II-unaffected base current I_{BnoAV} is calculated by source **B** as I_{CnoAV}/β_F, β_F being evaluated by the nonlinear source **C** from V_{CB}, I_E, and ΔT_j according to (5). The II (avalanche) current I_{AV} is determined as $(M-1) \times I_{CnoAV}$ by source **D**, where factor M described by (3) is provided by the nonlinear source **E**; the collector current I_C is obtained by adding I_{AV} to I_{CnoAV}, while the base current I_B is given by I_{BnoAV}-I_{AV}. The lumped resistances R_B and R_E emulate the parasitic base and emitter resistances, respectively. The subcircuit also includes further nonlinear sources (omitted in Figure 3) to describe the cell behavior in saturation mode. The dissipated power P_D under dc conditions (to be given to the TFB) is determined as

$$P_D = I_B\cdot V_{BE} + I_C\cdot V_{CE} = I_E\cdot V_{BE} + I_C\cdot V_{CB} \quad (7)$$

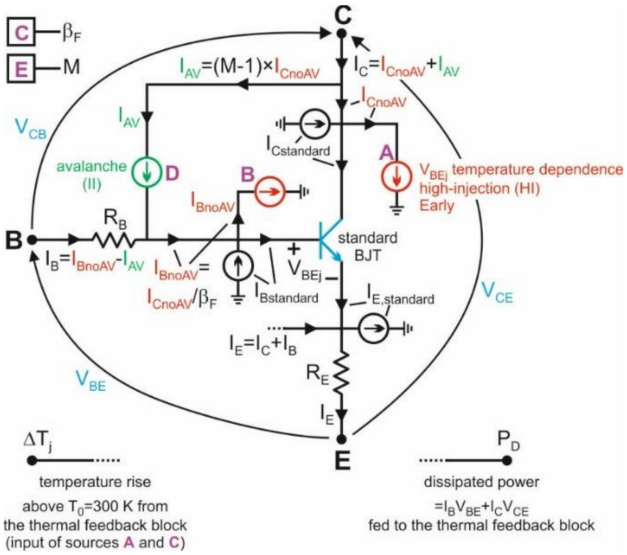

Figure 3. Simplified representation of the SPICE-compatible unit-cell subcircuit implementing the analytical model described in Section 3.2.

3.4. Construction of the Geometry/Mesh in COMSOL and Calibration of the Kirchhoff's Transformation

The 3-D geometry/mesh of each domain was constructed in the environment of the COMSOL software package [16] by making use of an *in-house* routine that relies on the MATLAB-COMSOL Livelink and the Toolbox for files in GDSII format provided by U. Griesmann [17]. The procedure is described as follows: first, the GDS layout file (i.e., the masks used for the technological process) is input to the routine along with the thicknesses of the layers, mask biases, and material parameters; then, the routine *automatically* draws the 3-D geometry, and finally generates and optimizes the mesh in the COMSOL environment. Such a process is error-free and requires a much shorter time compared to a painstakingly-long manual approach.

A single heat source (geometrically coinciding with the base-collector SCR [17]) and a single subcircuit were assigned to each unit cell (Figure 1); as mentioned earlier (Section 3.1), this intrinsically assumes that the fingers within the cell are tightly thermally coupled, and thus not prone to thermal hogging. Figure 4 depicts the geometry of the 1-cell test device, while Figure 5 shows the mesh of the 2-cell one.

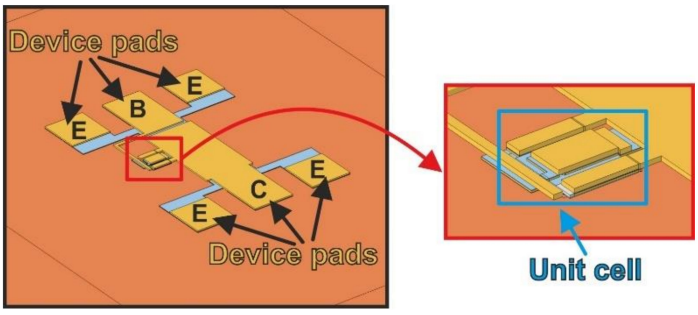

Figure 4. (**Left**) Single-cell test device built in the COMSOL environment (*draw mode*); as can be seen, the pads are arranged in a ground-signal-ground configuration to allow for RF experimental characterization. (**Right**) Magnification of the unit cell.

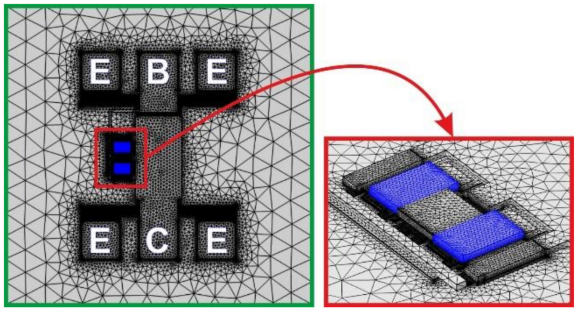

Figure 5. (**Left**) Two-cell test device built in the COMSOL environment (*mesh mode*). The numbers of elements (tetrahedra) and degrees of freedom (DoFs) are 2.4×10^6 and 3.3×10^6, respectively. (**Right**) Magnification of the two unit cells. A horizontally-large substrate (not fully represented in the figure) was considered to safely neglect the effect of the lateral adiabatic sides on the temperature field over the base-emitter junction.

For the arrays, the horizontal symmetry was exploited to construct the geometry/mesh of only half of the domains (Figure 2, bottom), thus alleviating the computational burden; the missing portions were virtually restored by applying an adiabatic boundary condition to the plane of symmetry. Figure 6 illustrates the geometry of (half of) the 24-cell array, while Figure 7 shows the mesh of (half of) the 28-cell array, both in COMSOL.

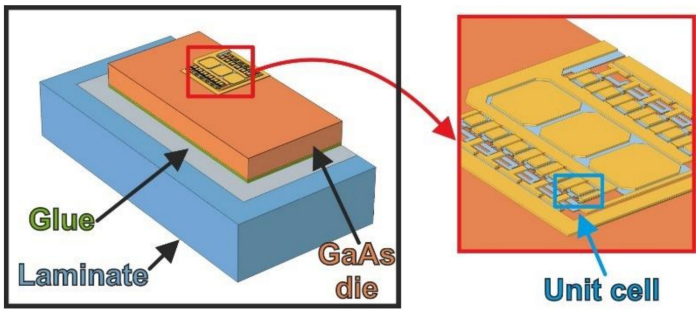

Figure 6. (**Left**) Half of the 24-cell array (with six cells per column) constructed in the COMSOL environment (*draw mode*). (**Right**) Magnification of the die; evidenced is the single unit cell.

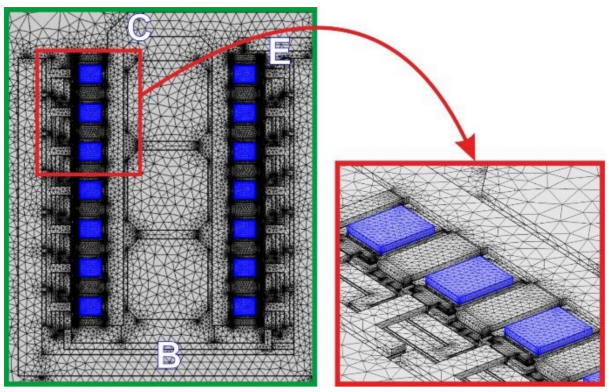

Figure 7. (**Left**) Half of the 28-cell array (with seven cells per column) built in the COMSOL environment (*mesh mode*). The numbers of tetrahedra and DoFs are 3.7×10^6 and 4.9×10^6, respectively. (**Right**) Magnification of some unit cells.

Besides the geometry/mesh of the domains and the position of the heat sources, FANTASTIC [22,23] requires information on the boundary conditions and thermal conductivities to extract the ETN including the R_{TH} matrix (Section 3.5). As mentioned in Section 2, the backside of the GaAs substrate was assumed to be at T_0 for the test devices, while

the laminate bottom was set to T_B for the arrays. All the other surfaces were considered adiabatic (i.e., with zero outgoing heat flux), such an assumption being justified by the particular scratch-protection coating employed in the technology (thick PBO).

The thermal conductivities associated to the materials of the test devices (at T_0) and arrays (at T_B) are listed in Table 3.

Table 3. Thermal conductivities of the materials composing the devices and arrays.

Material	$k(T_0)$ (W/μmK)	$k(T_B)$ (W/μmK)	Temperature Dependence
Si_3N_4	18.5×10^{-6} [33]	19.6×10^{-6}	(8), $\alpha = -0.33$ [33]
$In_{0.5}Ga_{0.5}As$	0.048×10^{-4} [33]	3.9×10^{-6}	(8), $\alpha = 1.175$ [33]
$In_xGa_{1-x}As$ ($0 < x < 0.5$)	0.092×10^{-4} [33] average in the layer	7.4×10^{-6}	(8), $\alpha = 1.212$ [33]
GaAs	4.6×10^{-5} [33]	3.69×10^{-5}	(8), $\alpha = 1.25$ [33]
ion-implanted GaAs	0.046×10^{-5} [33]	0.0369×10^{-5}	(8), $\alpha = 1.25$ [33]
$In_{0.49}Ga_{0.51}P$	0.052×10^{-4} [33]	0.041×10^{-4}	(8), $\alpha = 1.4$ [33]
Au	3.18×10^{-4} [34,35]	3.14×10^{-4}	(9), $\beta = 6.98 \times 10^{-8}$ W/μmK^2 [34,35]
Pt	0.71×10^{-4} [34,35]	0.71×10^{-4}	independent
Ti	0.22×10^{-4} [34,35]	0.22×10^{-4}	independent
Ni	0.91×10^{-4} [35]	0.863×10^{-4}	(9), $\beta = 8.1 \times 10^{-8}$ W/μmK^2 [35]
Ge	0.6×10^{-4} [33]	0.48×10^{-4}	(8), $\alpha = 1.25$ [33]
Cu	3.98×10^{-4} [35]	3.95×10^{-4}	(9), $\beta = 5.83 \times 10^{-8}$ W/μmK^2 [35]
Glue	1×10^{-4}	1×10^{-4}	independent
Polybenzoxazole (PBO)	0.0014×10^{-4}	0.0014×10^{-4}	independent
laminate dielectric	0.0065×10^{-4}	0.0065×10^{-4}	independent

The ETN is generated by FANTASTIC under *linear* thermal conditions (temperature-insensitive thermal conductivities). However, as very high temperatures are reached, *nonlinear* thermal effects can no longer be neglected. More specifically, the thermal conductivities of the materials vary with temperature T according to the following laws:

$$k(T) = k(T_0) \cdot \left(\frac{T}{T_0} \right)^{-\alpha} \tag{8}$$

$$k(T) = k(T_0) - \beta \cdot (T - T_0) \tag{9}$$

where (8) applies to semiconductors and insulators, and (9) to some metals; the accepted values of the α and β coefficients are also reported in Table 3. In order to account for the temperature dependences described by (8) and (9), we resorted to the Kirchhoff's transformation [18,19], which converts the linear junction temperature rises (ΔT_{jlin} and ΔT_{jlinB}) into the nonlinear counterparts (ΔT_j and ΔT_{jB}) through [36]

$$\Delta T_j = T_j - T_0 = T_0 \cdot \left[m_k + (1 - m_k) \cdot \frac{\Delta T_{jlin} + T_0}{T_0} \right]^{\frac{1}{1-m_k}} - T_0 = T_0 \cdot \left[1 + (1 - m_k) \cdot \frac{\Delta T_{jlin}}{T_0} \right]^{\frac{1}{1-m_k}} - T_0 \tag{10}$$

for the test devices, and

$$\Delta T_{jB} = T_j - T_B = T_B \cdot \left[m_k + (1 - m_k) \cdot \frac{\Delta T_{jlinB} + T_B}{T_B} \right]^{\frac{1}{1-m_k}} - T_B = T_B \cdot \left[1 + (1 - m_k) \cdot \frac{\Delta T_{jlinB}}{T_B} \right]^{\frac{1}{1-m_k}} - T_B \tag{11}$$

for the arrays. Contrary to the simplified analysis in [15], where m_k was chosen equal to 1.25 (α value for GaAs) for all the domains under investigation, here a preliminary calibration procedure was performed for this parameter. Let us refer to the 1-cell test device for the sake of simplicity. This HBT was simulated with COMSOL over a wide range of dissipated powers P_D by activating the thermal conductivity dependences upon temperature (8), (9) (nonlinear thermal conditions), and the average temperature rise over T_0 at the base-emitter

junction ΔT_j was computed for each P_D. The linear temperature rise ΔT_{jlin} over the same P_D span was evaluated by multiplying P_D by the R_{TH} obtained by COMSOL under linear conditions. Then the Kirchhoff's transformation was applied to ΔT_{jlin}, and m_k was tuned so as to ensure the best agreement between the nonlinear temperature rise ΔT_j calculated by the transformation and the realistic one evaluated by COMSOL; the optimum m_k value was 0.8333 (Figure 8). The same operation was repeated by activating one cell belonging to an array and considering the average junction temperature rise over T_B; in that case, the optimum m_k value was found to be 0.8932. As a result, m_k = 0.8333 was used in (10) for the ET simulations of the test devices (Section 4.1), whereas m_k = 0.8932 was adopted in (11) for the ET simulations of the arrays (Section 4.2).

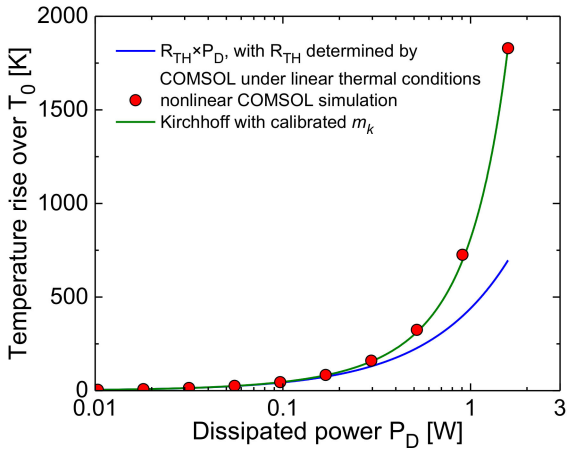

Figure 8. Test device with single unit cell: junction temperature rise over T_0 vs. dissipated power P_D, as evaluated by COMSOL under linear (solid blue line) and nonlinear (red symbols) conditions, along with that computed by applying the Kirchhoff's transformation (10) with calibrated m_k = 0.8333 (solid green line) to the linear COMSOL temperature rise.

3.5. FANTASTIC

The FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits (FANTASTIC), originally presented in [22,23], was conceived and developed to approximate a FEM model of heat conduction in an electronic device, having typically *millions* of DoFs, with a *dynamic* compact thermal model (DCTM), having only *tens* of DoFs, and the corresponding ETN [21]. The extraction of the DCTM and ETN does *not* require to solve the FEM model, as it is performed in short times through a refinement of the truncated balance-based moment matching approach to model-order reduction (MOR) introduced in [37]. Moreover, it also allows the extraction of a *static* compact thermal model (SCTM) and the related ETN relying on the R_{TH} matrix (hereinafter indicated with R_{TH}); for this simplified case, FANTASTIC is even quicker, as briefly discussed below.

The heat conduction problem in the structure, assumed to be *static* and *linear*, is imported from either commercial (e.g., COMSOL) or open-source numerical tools in the form of: mesh discretizing the geometry, position/shape of the heat sources, boundary conditions, and thermal conductivities (also mass densities and specific heats are required for the dynamic case). Both hexahedral and tetrahedral meshes can be used. Arbitrary tensorial thermal conductivity distributions can be defined. Neumann's, Dirichlet's, or Robin's boundary conditions can be applied.

A FEM model of the problem is then assembled by FANTASTIC. In particular, the stiffness matrix **K** is constructed. High-order basis functions can be adopted; the typical choice is to select tetrahedral meshes and 2nd-order basis functions, as a good trade-off between accuracy and efficiency. The M DoFs of the temperature rise distribution, forming the M-row vector $\boldsymbol{\vartheta}$, are solution of the discretized heat conduction problem

$$\mathbf{K}\boldsymbol{\vartheta} = \mathbf{q} \tag{12}$$

in which the power density distribution vector $\mathbf{q}$ takes the form

$$\mathbf{q} = \mathbf{Q}\mathbf{P_D} \tag{13}$$

In (13), $\mathbf{P_D}$ is an N-row vector with the powers dissipated by the N heat sources, and $\mathbf{Q}$ is an $M \times N$ matrix, the n-th column of which is the power density distribution vector of the n-th heat source, with $n = 1, \ldots, N$. The port temperature rises of the N heat sources form the N-row column vector $\Delta\mathbf{T_{jlin}}$ ($\Delta\mathbf{T_{jlinB}}$ for the arrays) defined as [37]

$$\Delta\mathbf{T_{jlin}} = \mathbf{Q}^T\boldsymbol{\vartheta} \tag{14}$$

In order to extract a compact thermal model, an $M \times \hat{M}$ matrix $\mathbf{V}$ with $\hat{M} \ll M$ is defined, which allows expressing $\boldsymbol{\vartheta}$ by means of a reduced number $\hat{M}$ of DoFs, thus forming the $\hat{M}$-vector $\hat{\boldsymbol{\vartheta}}$ so that

$$\boldsymbol{\vartheta} = \mathbf{V}\hat{\boldsymbol{\vartheta}} \tag{15}$$

The $\mathbf{V}$ matrix is used for projecting the discretized heat conduction problem (12)–(14) by the Galerkin's method, deriving an SCTM in the form

$$\hat{\mathbf{K}}\hat{\boldsymbol{\vartheta}} = \hat{\mathbf{q}} \tag{16}$$

where

$$\hat{\mathbf{q}} = \hat{\mathbf{G}}\mathbf{P_D} \tag{17}$$

$$\Delta\mathbf{T_{jlin}} = \hat{\mathbf{G}}^T\boldsymbol{\vartheta} \tag{18}$$

in which

$$\hat{\mathbf{K}} = \mathbf{V}^T\mathbf{K}\mathbf{V} \tag{19}$$

is an $\hat{M}$th-order matrix and

$$\hat{\mathbf{G}} = \mathbf{V}^T\mathbf{Q} \tag{20}$$

is an $\hat{M} \times N$ matrix. The $\mathbf{V}$ matrix is determined by the Algorithm 1 reported below.

Algorithm 1: SCTM extraction

Set $\mathbf{V}$:=**0**
for each heat source n=1, ... , N **do**
1 Solve (21) for $\boldsymbol{\Theta}_n$
2 Update matrix $\mathbf{V}$ by appending $\boldsymbol{\Theta}_n$
3 Generate a SCTM projecting (12)–(14) onto $\mathbf{V}$

At line 1, the temperature response to the n-th heat source is solved for the static heat conduction problem. Thus, equation

$$\mathbf{K}\boldsymbol{\Theta}_n = \mathbf{Q}\mathbf{e}_n \tag{21}$$

is solved for $\boldsymbol{\Theta}_n$, $\mathbf{e}_n$ being the vector selecting the n-th column of $\mathbf{Q}$. Since the coefficient matrices of these linear systems are symmetric positive definite, the most efficient multigrid iterative solvers can be used for their solution.

At line 2, the $\mathbf{V}$ matrix is updated by appending vector $\boldsymbol{\Theta}_n$ to its columns if it is linearly independent with respect to them.

At line 3, the SCTM is determined proceeding as in (16)–(18), and has dimension $\hat{M} \leq N \ll M$. A *much smaller* dimension is thus obtained with respect to the *dynamic* case; moreover, since a much smaller number of discretized heat conduction problems are solved, a large speedup of the algorithm is also achieved.

It is now observed that by solving at limited cost the eigenvalue problem

$$\hat{\mathbf{U}}^T\hat{\mathbf{K}}\hat{\mathbf{U}} = \hat{\boldsymbol{\Lambda}} \tag{22}$$

having as unknown the $\hat{M}$th-order orthogonal matrix $\hat{\mathbf{U}}$, in which $\hat{\mathbf{\Lambda}}$ is an $\hat{M}$th-order diagonal matrix, and introducing the change of variables

$$\hat{\boldsymbol{\vartheta}} = \hat{\mathbf{U}}\hat{\boldsymbol{\xi}} \tag{23}$$

the SCTM Equations (16)–(18) are transformed into the equivalent form

$$\hat{\mathbf{\Lambda}}\dot{\hat{\boldsymbol{\xi}}} = \hat{\mathbf{\Gamma}}\mathbf{P_D} \tag{24}$$

$$\Delta\mathbf{T_{jlin}} = \hat{\mathbf{\Gamma}}^T\hat{\boldsymbol{\xi}} \tag{25}$$

where $\hat{\mathbf{\Gamma}}$ is the $\hat{M} \times N$ matrix $\hat{\mathbf{V}}^T\hat{\mathbf{G}}$. The spatial distribution of the temperature rise is then reconstructed as

$$\boldsymbol{\vartheta} = \Xi\hat{\boldsymbol{\xi}} \tag{26}$$

Being $\Xi = \mathbf{V}\hat{\mathbf{U}}$ an $M \times \hat{M}$ matrix like $\mathbf{V}$. The $\hat{\xi}$ vector encompasses the DoFs of the thermal field. These DoFs are the node temperature rises in the extracted ETN sketched in Figure 9, which is governed by (24) and (25) and represents a simplified version of the dynamic counterpart [21–23], as it benefits from a much lower (by one order of magnitude) number of nodes, resistances, and controlled sources. The ETN transforms the port powers $\mathbf{P_D}$ into the port temperature rises $\mathbf{\Delta T_{jlin}}$ by inherently accounting for the boundary conditions initially applied to the FEM model. The port response of this network defines the N^{th}-order resistance matrix $\hat{\mathbf{R}}_{\text{TH}}$ [K/W] of the SCTM given by $\hat{\mathbf{Q}}^T\hat{\mathbf{K}}^{-1}\hat{\mathbf{Q}}$. Since by construction the $\hat{M}$ columns of the $\mathbf{V}$ matrix span the N columns of matrix $\mathbf{K}^{-1}\mathbf{Q}$, it is straightforward to prove that $\hat{\mathbf{R}}_{\text{TH}} = \mathbf{R}_{\text{TH}}$, where $\mathbf{R_{TH}}$ is the thermal resistance matrix of the discretized heat conduction problem (12)–(14) given by $\mathbf{Q}^T\mathbf{K}^{-1}\mathbf{Q}$. This further strengthens the general result relating the thermal impedance matrices of the compact thermal model and of the discretized heat conduction problem in the dynamic case [38].

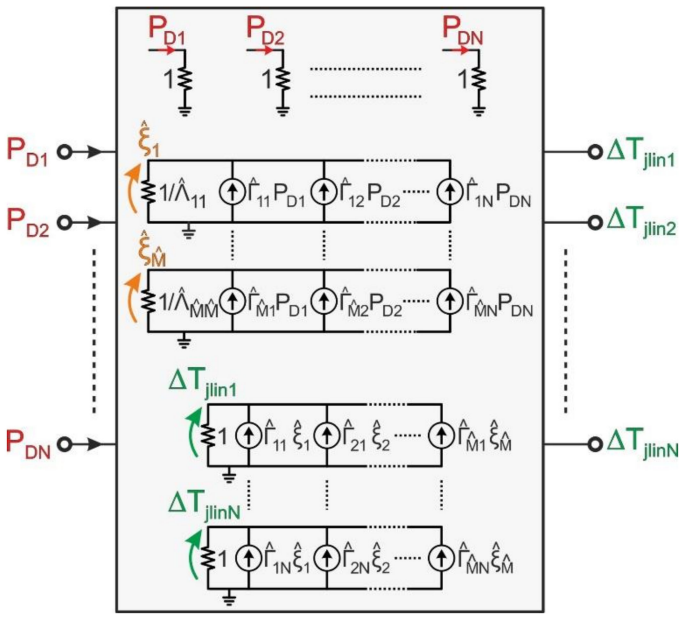

Figure 9. Equivalent thermal network (ETN) determined by FANTASTIC under linear thermal conditions.

The resulting ETN is particularly well-suited to be solved by means of modified nodal analysis in SPICE-like circuit simulators, since all circuit elements are voltage-controlled, and thus the number of variables added by the SCTM is limited to $\hat{M}$. The topology is general and can be implemented into any circuit simulation program.

It is worth noting that, after the circuit simulation, as a post-processing stage, the whole spatial distribution of temperature rise in the examined domain can be reconstructed at negligible computational cost and memory storage using (26), for both thermal-only and ET simulations. The temperature map can be plotted by any proper tool, like e.g., Paraview. This option is *not* allowed using conventional ETNs like in our former paper [15].

3.6. Construction of the Macrocircuit

The ETN derived by FANTASTIC was enriched with N nonlinear voltage-controlled voltage sources to account for the Kirchhoff's transformation, and the TFB was then obtained. The ΔT_j and P_D nodes of the subcircuits (the unit cells) were connected to the TFB, thereby giving rise to the whole TEOL-based SPICE-compatible macrocircuit, a simplified scheme of which is reported in Figure 10. As previously mentioned, the solution of the macrocircuit was delegated to PSPICE [20], although any other commercial circuit simulation software (e.g., LTSPICE, Eldo, Keysight ADS [39], and SIMetrix) could in principle be used.

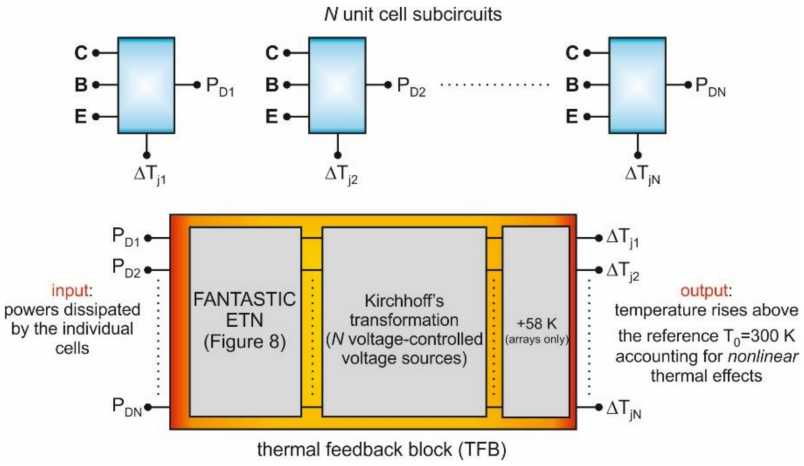

Figure 10. Sketch of the merely-electrical macrocircuit including ET effects through the TEOL. The paralleled (sharing the same base, emitter, collector contacts) subcircuits describing the unit cells are connected to the TFB containing: the ETN preliminarily evaluated by FANTASTIC, the calibrated Kirchhoff's transformation, and a block adding 58 K (for the arrays only).

3.7. Extension to the Dynamic Case

Unlike advanced bipolar transistor models equipped with temperature-dependent parameters and a thermal node (like HiCUM [40], VBIC, AHBT, and Mextram504, all available in ADS), the proposed unit-cell model/subcircuit is only suited to fairly well describe forward active and saturation modes under dc conditions. RF simulations including ET effects can be enabled by resorting to a variant of our approach based on one of the above models in the ADS environment; the strategy can be described as follows.

- The selected transistor model must be provided with a power (output) node, and the internal one- or two-pair thermal network has to be deactivated.
- All parameters of the model must be extracted from experimental data, which is a nontrivial task.
- As mentioned in Section 3.5, if FANTASTIC is also fed with the mass density and specific heat for all materials, it can be enabled to extract a DCTM of the domain and the associated ETN accounting for the dynamic heat propagation [21–23]. Such an ETN, together with the Kirchhoff's transformation sources, will constitute the SPICE- and ADS-compatible TFB.
- Lastly, the macrocircuit has to be built in ADS by connecting the model instances among them and with the TFB.

It is worth noting that the adoption of the one- or two-pair thermal networks embedded in the transistor models instead of our TFB (i) would lead to a significant inaccuracy in terms of SH of the single cell (the typically-used single pair is not enough for the transient SH response [23]), and (ii) would exclude the mutual thermal interactions among unit cells, which however play a relevant role, as demonstrated in Section 4.

As an alternative, one could resort to an ET solver available in recent ADS releases, which couples a quasi−3-D layout-based numerical thermal tool to the circuit simulator (the thermal networks embedded in the model instances being disabled) [41]. However, (i) this strategy is only applicable to device models equipped with a thermal node; (ii) using such a solver for layout optimization is very labor-intensive; (iii) the iterative process leading to convergence is resource-hungry.

4. Results and Discussion

4.1. Test Devices

The analysis of the test devices is two-fold: it is intended (i) to offer an overview of the ET- and II-induced positive-feedback mechanisms limiting the safe operating region, and (ii) to explore the thermally-stabilizing effect ensured by the base ballasting. In the latter case, an integrated resistor R_{Bext} = 400 Ω was used per each cell, as this is the typical ballasting strategy chosen for the arrays investigated in Section 4.2.

Let us first consider the single-cell device, which does not require an ETN, but only a linear SH R_{TH} to which the Kirchhoff's transformation is applied. The R_{TH} was computed to be about 440 K/W, which is in good agreement with the experimental value extracted by means of the classic method proposed in [42]. Figure 11 shows the V_{BE}-constant I_C–V_{CE} and ΔT_j–V_{CE} characteristics. It can be inferred that the curves of the unballasted device are affected by a *flyback* (also denoted as *snapback* or *turnover*) mechanism followed by a negative-differential-resistance (NDR) branch [6,13,31,43–46], which can be simulated/measured by (i) incrementing I_C or (ii) connecting a resistor R_{Cext} to the collector terminal, sweeping V_{Cext} on the available resistor node (Cext), and evaluating V_{CE} as $V_{CextE} - R_{Cext} \cdot I_C$. It is worth noting that increasing V_{CE} beyond the value corresponding to the flyback would have instead led to a *thermal runaway* (shown for V_{BE} = 1.25 V) and sudden device failure. Adding a base-ballasting resistor (as suggested in [31,47,48]) with R_{Bext} = 400 Ω prevents the flyback (and thus the runaway); however, it reduces the internal (junction) V_{BEj} at medium/high current levels, decreasing and limiting the collector current.

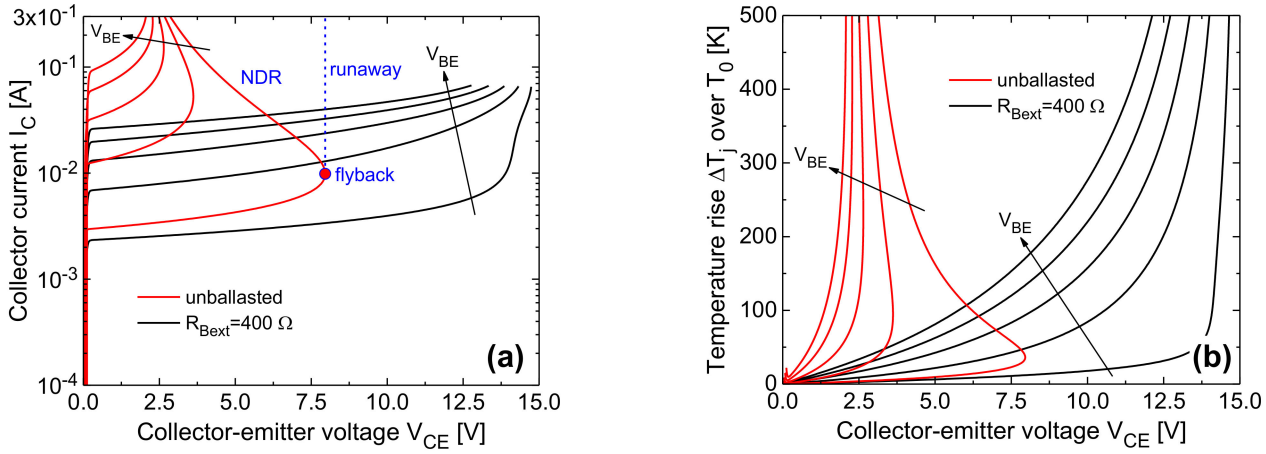

Figure 11. Test device with single unit cell: simulated (**a**) collector current I_C and (**b**) corresponding temperature rise ΔT_j above T_0 against collector-emitter voltage V_{CE} for V_{BE} = 1.25, 1.3, 1.35, 1.4, 1.45 V. The unballasted case (red lines) is compared to the one with R_{Bext} = 400 Ω connected to the base (black).

Figure 12 shows the behavior of the 2-cell test device under I_{BTOT}-constant conditions. As can be seen, a *bifurcation* phenomenon is triggered: beyond a critical V_{CE}, cell #2 tends

to conduct the whole current, while #1 gradually turns off [26,49–51]. For I_{BTOT} = 0.5 mA, the critical V_{CE} is equal to 8 V for the unballasted case, and reduces with increasing I_{BTOT}. It is *not* possible to identify *a priori* which cell will take all the current, since it is determined by *random* (and unavoidable) technology and layout fluctuations. In PSPICE the cells are assumed electrically identical, and the current hogging in cell #2 is favored by a marginally higher SH R_{TH} due to a slight layout asymmetry. As far as the total collector current I_{CTOT} is concerned, a smooth NDR region due to the β_F NTC is observed in the V_{CE} range where I_{CTOT} is equally shared by the two cells. The NDR mechanism is then replaced by a marked I_{CTOT} reduction within the bifurcation region due to the 'faster' temperature growth with V_{CE} in the hotter cell, which implies a significant β_F decrease; such a behavior is also denoted as *collapse of collector current* [49] or *collapse of current gain* [26,50,51]. As V_{CE} exceeds 13 V, the II current I_{AV2} (≈90 μA at V_{CE} = 15 V) can no longer be neglected with respect to I_{BTOT} (=500 μA); as a result, the avalanche-less current I_{BnoAV2}, almost equal to I_{BTOT} + I_{AV2}, perceptibly grows due to the I_{AV2} increase, and in turn raises $I_{CnoAV2} \approx I_{C2} \approx I_{CTOT}$. The inclusion of base ballasting with R_{Bext} = 400 Ω per cell pushes the critical V_{CE} to 16.6 V, restoring a uniform behavior over a large voltage range [47].

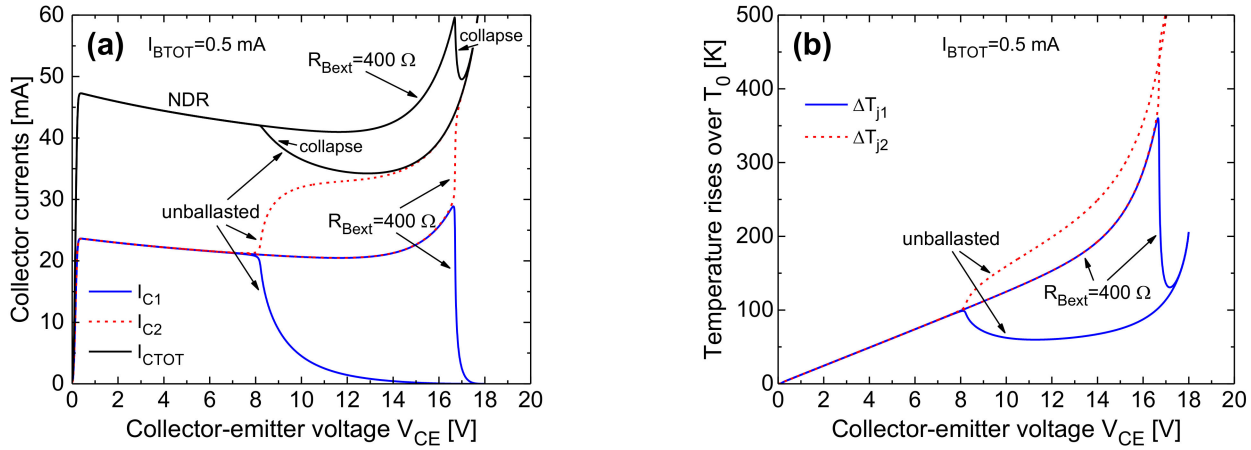

Figure 12. Test device with two unit cells: simulated (**a**) collector currents and (**b**) temperature rises over T_0 vs. collector-emitter voltage V_{CE} for I_{BTOT} = 0.5 mA. Both the unballasted case and that ballasted with R_{Bext} = 400 Ω per cell are reported.

Figure 13 illustrates the behavior of the 2-cell test device under V_{BE}-constant conditions. Let us first examine the unballasted case. If I_{CTOT} is swept, the current is equally divided between the unit cells until a flyback takes place, followed by an NDR branch still showing uniform operation; at low V_{BE} (e.g., 1.2 V), a bifurcation will also occur for relatively low cell temperatures [31]. A similar behavior was observed for more paralleled BJTs in SOG technology [7]; in that case, an uneven current distribution was found to arise beyond the uniform NDR branch under I_{CTOT}-controlled conditions. By increasing V_{CE}, the whole device (or at least one of the two cells) would have blown up beyond the value corresponding to the flyback; this means that our simulations do not confirm the observation of a 'safe' collapse encountered in [50,51].

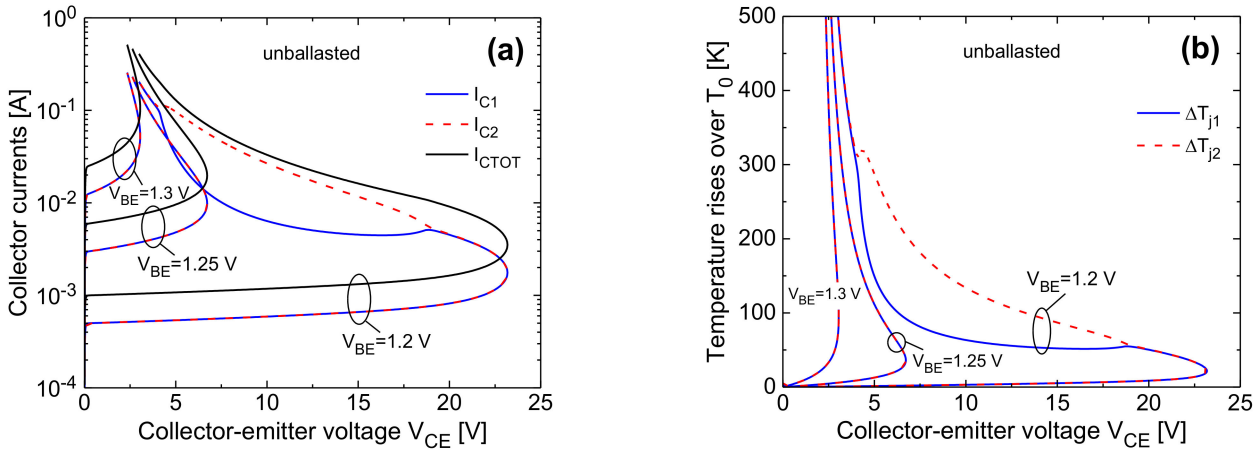

Figure 13. Unballasted test device with two unit cells: simulated (**a**) collector currents and (**b**) temperature rises over T_0 vs. collector-emitter voltage V_{CE} for V_{BE} = 1.2, 1.25, 1.3 V.

Let us next consider the device with base-ballasted cells subject to the same biasing conditions (Figure 14). As far as the V_{BE} = 1.2 V case is concerned, the flyback point moves to the left, thus shrinking the V_{CE}-controlled safe operating region; this can be ascribed to the increased avalanche current flowing in the unit cells, in turn induced by R_{Bext} = 400 Ω, which favors the positive feedback action related to II [31,48]. On the other hand, the thermally-induced bifurcation disappears; it was found than the bifurcation-triggered discrepancy between I_{C1} and I_{C2} reduces with increasing R_{Bext}, and R_{Bext} = 400 Ω is the threshold value for which the uniform behavior is fully restored. For higher V_{BE}s, the ballasting makes the flyback mechanism vanish, thus improving the thermal stability of the device; however, the current capability significantly plummets at high current levels.

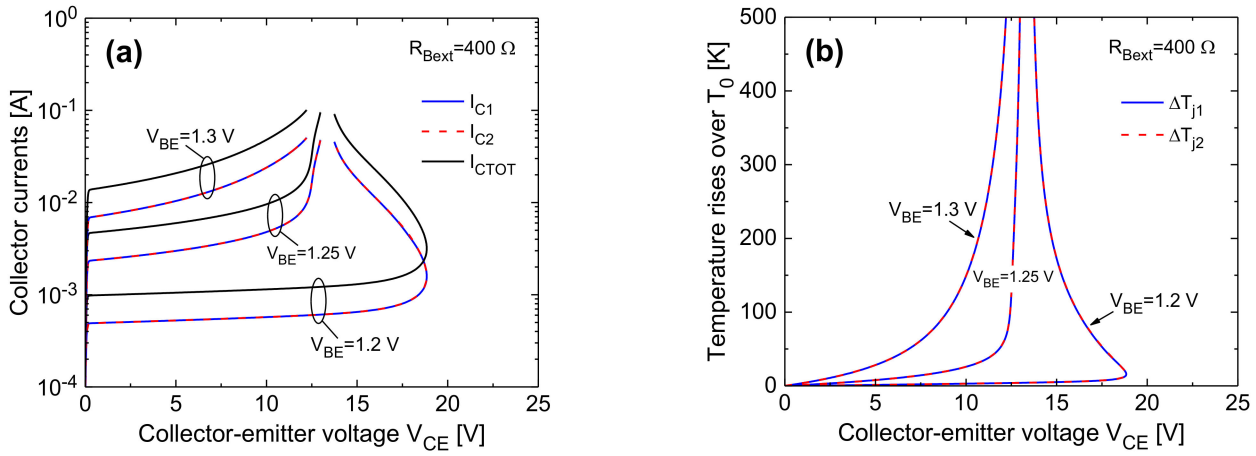

Figure 14. Ballasted (with R_{Bext} = 400 Ω) test device with two unit cells: simulated (**a**) collector currents and (**b**) junction temperature rises over T_0 vs. collector-emitter voltage V_{CE} for V_{BE} = 1.2, 1.25, 1.3 V.

It is also important to analyze the ET behavior of the 2-cell device under I_{ETOT}-controlled conditions, typical for differential pairs and comparators [52,53]. Results obtained by increasing the total emitter current I_{ETOT} for V_{CB} = 8 V are shown in Figure 15 for both the unballasted and ballasted cases. It is shown that without ballasting a bifurcation phenomenon is triggered for a critical I_{ETOT} (33 mA), and the whole I_{CTOT} eventually flows in cell #2, rapidly increasing its temperature; a similar behavior would be obtained by fixing I_{ETOT} and sweeping V_{CB} [6,31]. Applying the resistors R_{Bext} = 400 Ω, thermal effects are weakened and the bifurcation disappears, limiting the maximum temperature reached by the device.

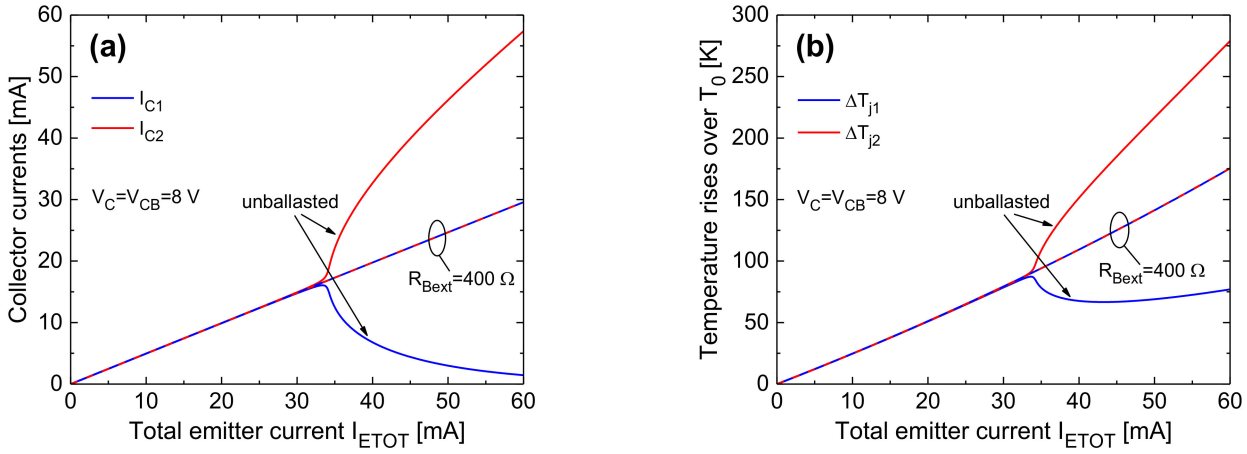

Figure 15. Test device with two unit cells: simulated (**a**) collector currents and (**b**) junction temperature rises over T_0 vs. total collector current I_{ETOT} for V_{CB} = 8 V. Both the unballasted and ballasted (with R_{Bext} = 400 Ω per each unit cell) devices are considered. In (**b**), ΔT_{j1} increases beyond I_{ETOT} = 43 mA due to the thermal coupling with cell #2.

We now consider the ET behavior of the test device composed by three unit cells, assumed ideally identical in PSPICE. The first simulation was performed under CE conditions by increasing V_{CE} with a constant I_{BTOT} = 0.7 mA (Figure 16). Let us focus on the unballasted case. It is found that cell #2 starts conducting more current due to the thermal coupling with both the adjacent (outer) cells #1 and #3. For higher V_{CE} values, a counterintuitive behavior takes place: a bifurcation mechanism involving cells #1 and #3 occurs at V_{CE} = 7 V; in particular, cell #3 eventually bears more current, whereas #1 turns off, as induced by the slightly higher SH R_{TH} of #3 with respect to #1. By further increasing V_{CE}, cell #3 prevails over #2 since the SH R_{TH} of #3 (396.2 K/W under linear thermal conditions) is perceptibly higher than that of cell #2 (361.7 K/W), which experiences a more effective heat flow through metal 2 (top metal). The strongly uneven current distribution for V_{CE} > 7 V turns into a collapse in the I_{CTOT}–V_{CE} curve. For V_{CE} > 13 V, cell #3 conducts the whole current, and therefore $I_{B3} = I_{BnoAV3} - I_{AV3}$ is almost equal to I_{BTOT} = 0.7 mA; the increase in I_{AV3} with V_{CE} due to the enhanced II leads to a growth in I_{BnoAV3}, which dominates over the NTC of β_{F3}, thus driving an $I_{C3} \approx I_{CTOT}$ increase. Adopting R_{Bext} = 400 Ω for all cells pushes the uneven current distribution to V_{CE} > 15.7 V, thus leading to a much wider uniform operating region.

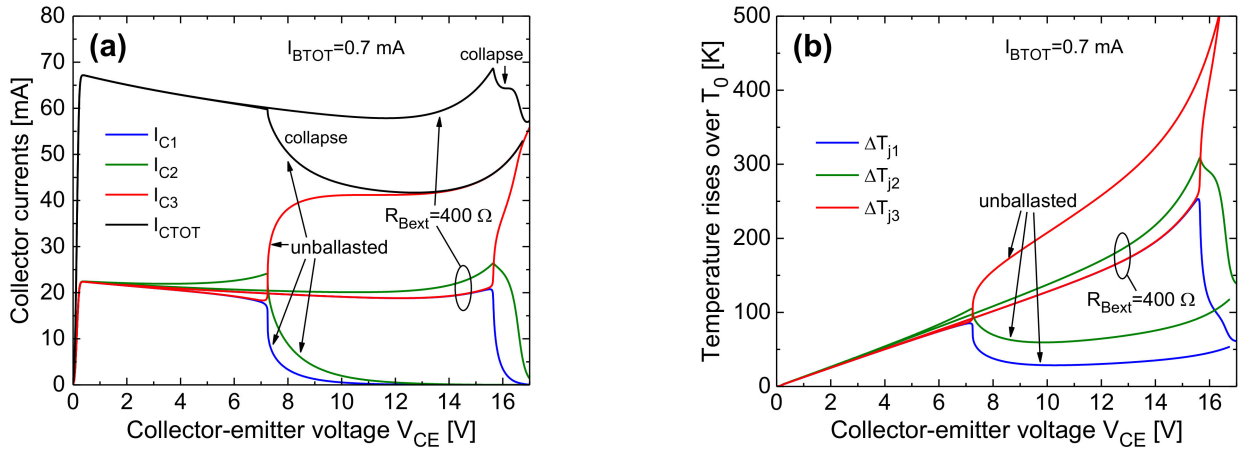

Figure 16. Test device with three unit cells, either unballasted or ballasted with R_{Bext} = 400 Ω per cell: simulated (**a**) collector currents and (**b**) junction temperature rises over T_0 vs. collector-emitter voltage V_{CE}.

It is worth noting that increasing the emitter area of cell #1 by only 1 μm^2, the onset of the bifurcation takes place at the same critical V_{CE}, but the behavior of cells #1 and #3

reverses: cell #1 prevails over #3, and eventually sinks also the current of #2. Nevertheless, the I_{CTOT}–V_{CE} curve would coincide with that obtained for cells sharing ideally identical areas. This means that it is impossible to foresee which of the outer cells will dominate, since it depends on unavoidable technological/layout discrepancies. The practical implication is that the failure analysis should look at planes of symmetry, and not at the specific failed cells.

An overview of the I_{CTOT}–V_{CE} characteristics for various I_{BTOT} values is illustrated in Figure 17 for both the unballasted and base-ballasted cases; it is apparent how the *collapse locus* (which can be reviewed as the boundary of the safe operating area) significantly moves rightward by virtue of the external base resistances [47].

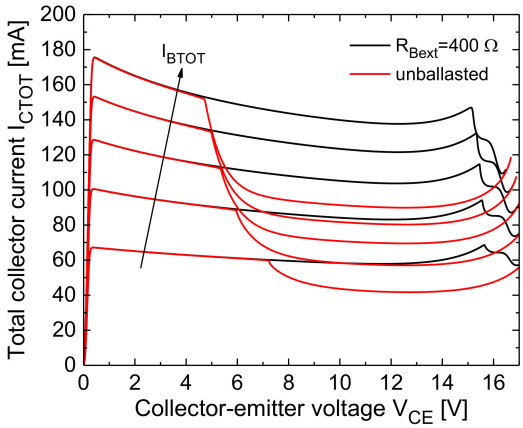

Figure 17. Simulated I_{CTOT}–V_{CE} characteristics for the unballasted (red) and ballasted (black) 3-cell test device for I_{BTOT} = 0.7, 1.2, 1.7, 2.2, 2.7 mA.

In the above analysis, it was stated that the 3-cell test device benefits from a lower SH R_{TH} of the inner cell #2 compared to the outer cells. We decided to quantify the related thermally-stabilizing effect by performing a test simulation where the R_{TH} of cell #2 was considered identical to those of the lateral cells (396 K/W under linear thermal conditions) and the mutual R_{TH}s between adjacent cells were assumed to coincide (115 K/W). Figure 18 shows that the *classic* collapse with #2 conducting the whole current is obtained. Unfortunately, the collapse onset in the I_{CTOT}–V_{CE} characteristic takes place at the same V_{CE} as in the real test device with lower R_{TH} for cell #2; this means that the bifurcation mechanism occurring for the outer cells in the real case is as deleterious as the strong thermal coupling affecting #2 in the ideal device with uniform SH R_{TH}s.

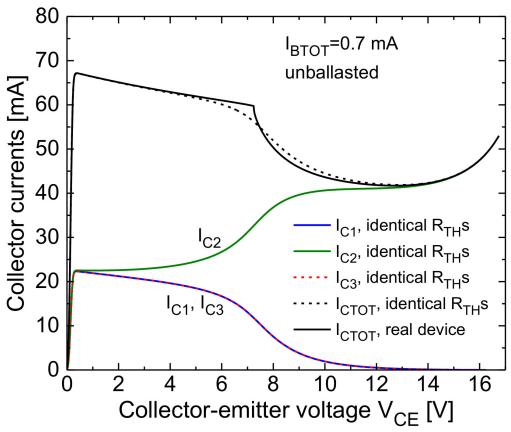

Figure 18. Unballasted 3-cell test device with unit cells sharing ideally identical SH R_{TH}s: simulated collector currents against collector-emitter voltage V_{CE}. Also shown is the I_{CTOT}–V_{CE} characteristic corresponding to the real structure (solid black line).

4.2. Transistor Arrays

As already mentioned in Sections 2 and 3.4, only half of each array for PA output stages was drawn, meshed, and simulated by exploiting the horizontal symmetry. This means that only 12 (14) cells were taken into account for the 24-cell (28-cell) arrays. Our simulation approach allows monitoring the dc ET behavior of the arrays at cell-level, that is, besides the junction temperature, all the key parameters, voltages, and currents are available for each cell; this would have been unviable by performing experiments since the collector layers of the individual cells are all shorted to one another, by being in a single isolation tub.

Hereinafter, I_{CTOT} and I_{BTOT} are the total collector and base currents of the semi-arrays.

The analysis focuses on I_{BTOT}-constant CE conditions, since GSM PAs are more or less biased with a constant I_{BTOT}. A base ballasting with the nominal value R_{Bext} = 400 Ω per unit cell was applied following a strategy denoted as *segmented* or *split*, in which such resistances only appear in the dc path and there is no RF performance penalty. The bottom of the laminate was held at T_B.

Let us first consider the halved 24-cell array. Figure 19 reports the PSPICE results corresponding to I_{BTOT} = 2 mA; the simulation lasted less than 100 s on a normal PC, in spite of the very small V_{CE} step used. A significant current/temperature nonuniformity is observed as V_{CE} exceeds 9 V, leading to an I_{CTOT} collapse; more specifically, the right (internal) column (#7 to #12) conducts the entire current, while the cells belonging to the left (external) one (#1 to #6) tend to turn off. Below V_{CE} = 11 V, the symmetric cell pairs of the right column (namely, #9 and #10, #8 and #11, and #7 and #12) share the same current. For V_{CE} higher than 11 V, a bifurcation mechanism occurs for all these pairs, as dictated by slight layout asymmetries: in particular, the top cells (#7, #8, and #9) prevail over the bottom counterparts (#10, #11, and #12, respectively). The uneven behavior is thus enhanced, and I_{CTOT} decreases more steeply with V_{CE}. Over the V_{CE} span from 11 to 12 V, cell #9 is the hottest cell since it suffers from the stronger thermal coupling with the surrounding cells. As V_{CE} exceeds 12 V, only the adjacent cells #7 to #9 are conducting, whereas cells #10 to #12 run dry; as a consequence, mutual thermal interactions among cells play a minor role, while the behavior is dominated by the SH R_{TH}s of the "active" cells, namely, 541, 533.3, and 531.5 K/W for #7, #8, and #9, respectively, under linear conditions (the closer the cell to the die border, the higher the R_{TH}). For a higher V_{CE}, the total current first focuses over cells #7 and #8 (at V_{CE} = 12.6 V, ΔT_{j7} = 500 K, and ΔT_{j8} = 700 K), and then, if #8 survives, over cell #7 only.

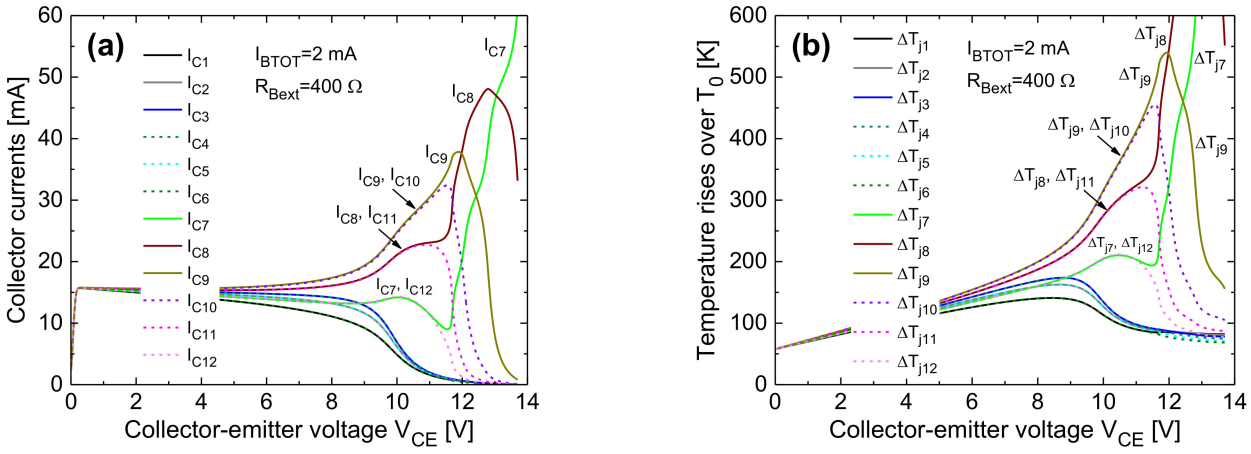

Figure 19. Simulated (**a**) collector currents and (**b**) junction temperature rises above T_0 for the 12 cells of half of the 24-cell array ballasted with R_{Bext} = 400 Ω per cell, and biased with I_{BTOT} = 2 mA.

It must be remarked that introducing an intentional (very small) technological discrepancy between #9 and #10 to favor a slightly higher conduction of #10, for V_{CE} > 11 V the bottom cells of the right column dominate over the top ones; by further increasing V_{CE}, cells #11 and #12 sink the whole current, which eventually focuses in the outer #12 suffering from the highest R_{TH}. The I_{CTOT}–V_{CE} curve, including the collapse region, remains instead unaltered.

If the applied I_{BTOT} is higher, the current nonuniformity (i.e., the collapse onset) and the subsequent bifurcation phenomenon involving symmetric cells occur for slightly lower critical V_{CE}s, as ET effects are exacerbated by the higher currents (and dissipated powers). Clearly, the temperatures reached by the right-column cells at the bifurcation are higher than in the lower-I_{BTOT} case. Figure 20 illustrates the scenario corresponding to I_{BTOT} = 3 mA; here it is shown that, as the bifurcation takes place, the ΔT_j shared by the inner cells #9 and #10 has already exceeded 600 K; this suggests that in a real array the metallization and surrounding interlevel dielectrics of these cells is likely to melt before the bifurcation arises.

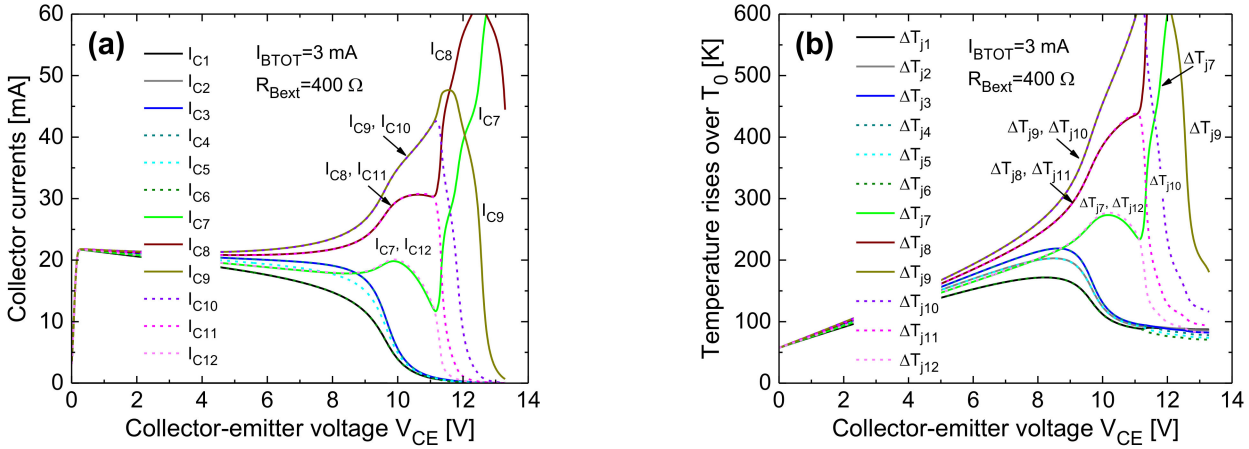

Figure 20. Simulated (**a**) collector currents and (**b**) junction temperature rises above T_0 for the 12 cells of the halved 24-cell array ballasted with R_{Bext} = 400 Ω per cell, with I_{BTOT} = 3 mA applied.

In the total absence of ballasting, the V_{CE} range enjoying uniform current and temperature distribution *dramatically* reduces; beyond a critical (and low) V_{CE}, the pair #9, #10 starts taking more current, which translates in the collapse onset in the I_{CTOT}–V_{CE} characteristic; then, the bifurcation between symmetric cells in the right column arises, and, for a slightly higher V_{CE}, the current flows only in cell #9. An example is reported in Figure 21, which corresponds to I_{BTOT} = 3 mA. It is observed that, as #9 dominates, the cells symmetric with respect to #9 (i.e., #8 and #10, and #7 and #11) tend to exhibit a similar behavior (i.e., they conduct almost the same current and are at the same temperature). Again, by intentionally applying a technological discrepancy leading to a slightly higher current capability for cell #10, the current will focus only on this cell in the deep collapse region, without distorting the I_{CTOT}–V_{CE} characteristic.

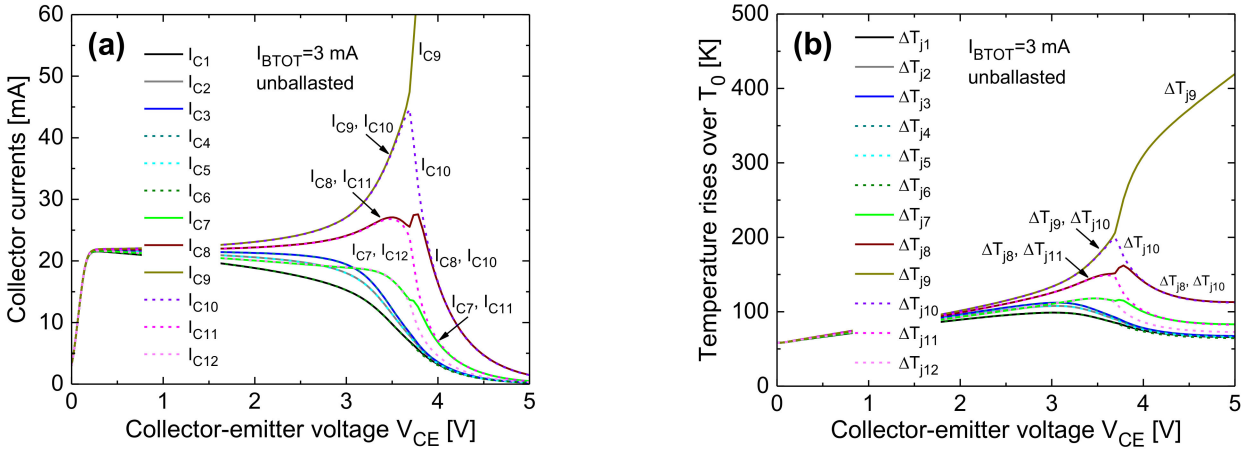

Figure 21. Simulated (**a**) collector currents and (**b**) junction temperature rises over T_0 vs. collector-emitter voltage V_{CE} for half of the unballasted 24-cell array biased with I_{BTOT} = 3 mA.

Finally, the case of emitter ballasting with R_{Eext} = 4 Ω per cell is examined, as it is considered approximately equivalent to R_{Bext} = 400 Ω by circuit designers; however, in this case a significant degradation in terms of f_T and f_{MAX} (both by some GHz), as well as of RF gain, is induced. Figure 22 depicts the individual collector currents of the unit cells and the associated temperature rises above T_0 with I_{BTOT} = 3 mA applied. By virtue of the reduced ET feedback with respect to the unballasted array, (i) the collapse locus is shifted ahead of about 3.5 V and (ii) the bifurcation involving the right-column cells occurs for much higher temperature values; (iii) in the thermally-unstable nonuniform region, the behavior of the individual currents vs. V_{CE} resembles that observed in the unballasted case: beyond the bifurcation onset, a current hogging over cell #9 takes place. Another interesting result is that the stabilizing effect is much less effective than the base ballasting with R_{Bext} = 400 Ω per cell: for this specific I_{BTOT}, the critical V_{CE} triggering the collapse is about 6.5 V, whereas R_{Bext} = 400 Ω allows extending this value to 9 V.

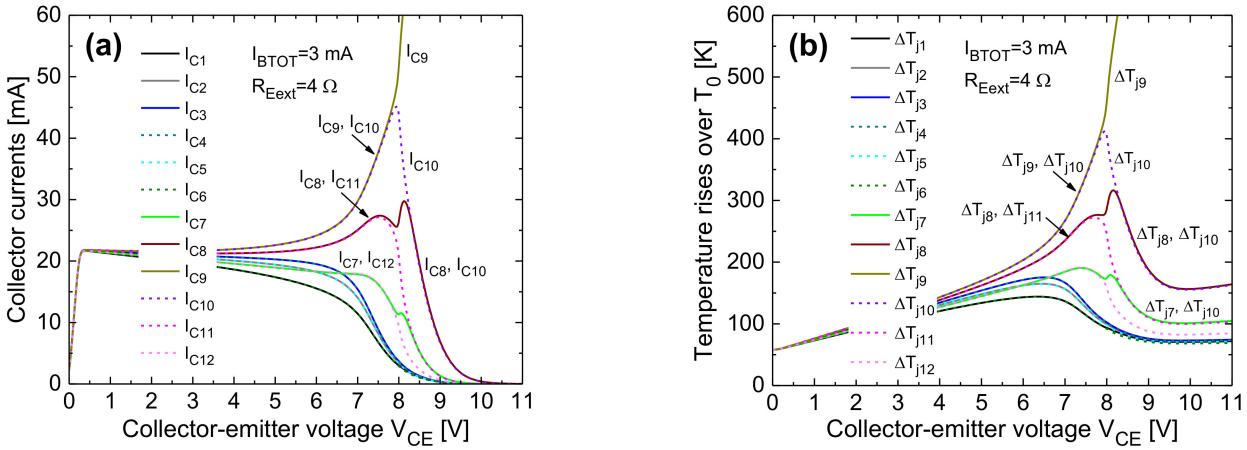

Figure 22. Simulated (**a**) collector currents and (**b**) junction temperature rises above T_0 for the 12 cells of the halved 24-cell array ballasted with R_{Eext} = 4 Ω per cell, and biased with I_{BTOT} = 3 mA.

Figure 23 summarizes the comparison between the ballasting schemes, by showing the I_{CTOT}–V_{CE} curves simulated at various I_{BTOT} values for the case of nominal base ballasting (R_{Bext} = 400 Ω per each cell), emitter ballasting (R_{Eext} = 4 Ω per each cell), and no ballasting, as well as the corresponding temperature rises over T_0 affecting cell #9. A wide I_{BTOT} range was selected so as to cover the typical operating current densities [54]. The considerable reduction in the safe operating region for the unballasted case and the inferior aid ensured by R_{Eext} = 4 Ω with respect to R_{Bext} = 400 Ω are apparent.

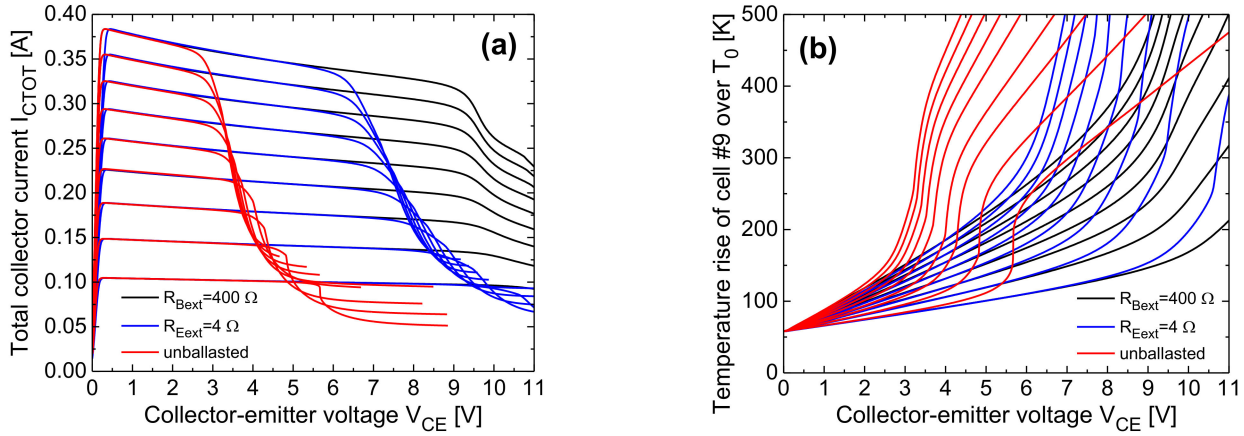

Figure 23. Simulated (**a**) total collector currents and (**b**) junction temperature rises above T_0 of cell #9 against collector-emitter voltage V_{CE} for half of the 24-cell array biased with I_{BTOT} = 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5 mA. Comparison between the case with no ballasting (red lines), and those benefiting from R_{Bext} = 400 Ω (black) and R_{Eext} = 4 Ω (blue) per cell.

From the overall analysis, the following relevant findings emerge:

- The collapse onset in an I_{BTOT}-constant I_{CTOT}–V_{CE} curve is associated to a uneven current/temperature distribution, wherein the right-column cells (in particular, the inner ones) bear almost all the current.
- The steeper I_{CTOT} drop in the collapse region is induced by a bifurcation mechanism involving the symmetric cells belonging to the right column. In the base-ballasted case (with R_{Bext} = 400 Ω) this leads to three adjacent cells conducting all the current (either the top or the bottom ones, depending on small technological/layout discrepancies); a further V_{CE} increase makes the current flow in two cells, and eventually in only one cell (the outer one). In the unballasted and emitter-ballasted case (with R_{Eext} = 4 Ω), for V_{CE} slightly higher than that entailing the bifurcation, the current flows in only one of the inner cells (#9 or #10). This leads to a very sharp and linear temperature increment vs. V_{CE} of this cell (plainly illustrated for cell #9 in Figure 23b).
- Such a linear nature of the ΔT_{j9}–V_{CE} behavior can be straightforwardly explained as follows. Neglecting II effects, which is reasonable in both the unballasted and emitter-ballasted cases, ΔT_{j9} is approximately equal to $R_{TH99}(T_{j9})\cdot\beta_F(T_{j9})\cdot I_{BTOT}\cdot V_{CE}$ + 58 K ($I_{B9} \approx I_{BTOT}$), where R_{TH99} is the SH thermal resistance of cell #9, and 58 K is the difference between T_B and T_0; as V_{CE} increases, there is a compensation between the NTC of β_F and the increase in R_{TH99} with temperature due to nonlinear thermal effects.

We shall now focus on half of the 28-cell array; all cells are base-ballasted with R_{Bext} = 400 Ω. Figure 24 depicts the PSPICE results obtained under CE conditions for I_{BTOT} = 3.5 mA. It is found that beyond V_{CE} = 8.5 V the current distribution becomes uneven, leading to the onset of collapse in the I_{CTOT}–V_{CE} curve. The right-column cells (#8 to #14) carry all the current, while the left-column counterparts (#1 to #7) turn off. In particular, the current is mostly conducted by the inner cells: the highest by the innermost #11, a slightly lower one by each of the symmetric cells #10, #12, an even lower by #9, #13, and so on. At V_{CE} = 10.8 V, a bifurcation occurs for these symmetric pairs, and #10, #9, and #8 prevail over #12, #13, and #14, so that only the top group composed by the adjacent #8 to #11 cells conducts. Further increasing V_{CE}, the current would first focus over the 3-cell group #8 to #10, then over the pair #8, #9, and would eventually flow only in the outermost cell #8, which is affected by the highest R_{TH}. On the other hand, the reduction in the number of conducting top cells is found to occur after the temperature rise of cells #11, #10, and #9 has well exceeded 600 K; consequently, in the practical case, the metallization and dielectrics over such cells are expected to lose their integrity when still the whole group #8 to #11 is conducting.

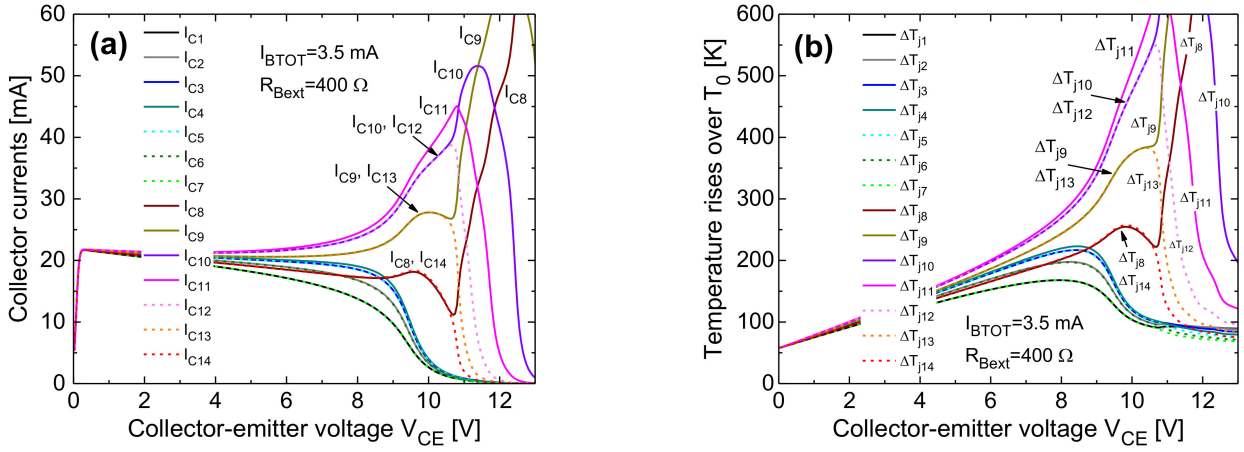

Figure 24. Simulated (**a**) collector currents and (**b**) junction temperature rises above T_0 for half of the ballasted 28-cell array biased with I_{BTOT} = 3.5 mA.

As mentioned in Section 3.5, unlike conventional ETNs, the one derived by FANTASTIC allows the reconstruction of the whole linear temperature rise field $\Delta T_{lin}(x, y, z) = T_{lin}(x, y, z) - T_0$, which can be easily processed through the calibrated Kirchhoff's transformation to get the nonlinear $\Delta T(x, y, z)$, for selected biasing conditions. Figure 25 shows the $\Delta T(x, y, z)$ map for half of the 28-cell array biased with I_{BTOT} = 3.5 mA and V_{CE} equal to 6 V (as representative of the uniform operating region), 10 V (collapse region: all the right-column cells are conducting), and 13.3 V (deep/marked collapse: after the bifurcation mechanism, the current flows only through the group #8 to #11).

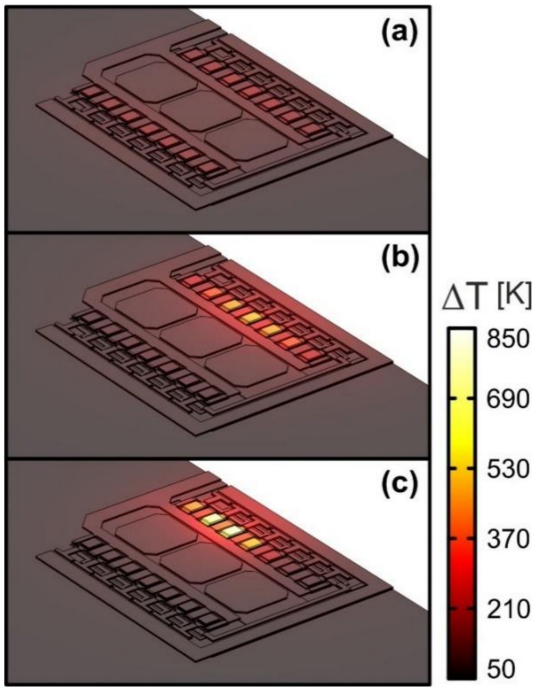

Figure 25. Spatial temperature rise map $\Delta T(x, y, z)$ over half of the 28-cell array, as reconstructed by FANTASTIC equipped with the Kirchhoff's transformation for I_{BTOT} = 3.5 mA and V_{CE} equal to (**a**) 6, (**b**) 10, and (**c**) 13.3 V.

Lastly, an interesting and fair comparison is performed between the halved portions of the base-ballasted 24- and 28-cell arrays by applying various I_{BTOT} values ensuring the same total base current density $J_{BTOT} = I_{BTOT}/A_{ETOT}$ in both cases. Results are reported in Figure 26; more specifically, Figure 26a shows the J_{CTOT}–V_{CE} characteristic

($J_{CTOT} = I_{CTOT}/A_{ETOT}$), and Figure 26b depicts the junction temperature rise of cell #9 for the 24-cell array, and of cell #11 for the 28-cell one. The analysis demonstrates that the 28-cell array featuring an odd number of cells (seven) per column is less thermally robust than the 24-cell counterpart with an even number of cells (six) per column (the collapse locus is shifted leftward). This is attributed to the fact that the nonuniform current/temperature distribution triggering the collapse in the 28-cell structure implies that the innermost cell #11 takes more current than the others, while *two* cells (#9 and #10) concurrently bear this task in the 24-cell array. It is worth noting that, although this seems to be an expected results, there are still many designers using arrays with an odd number of cells per column.

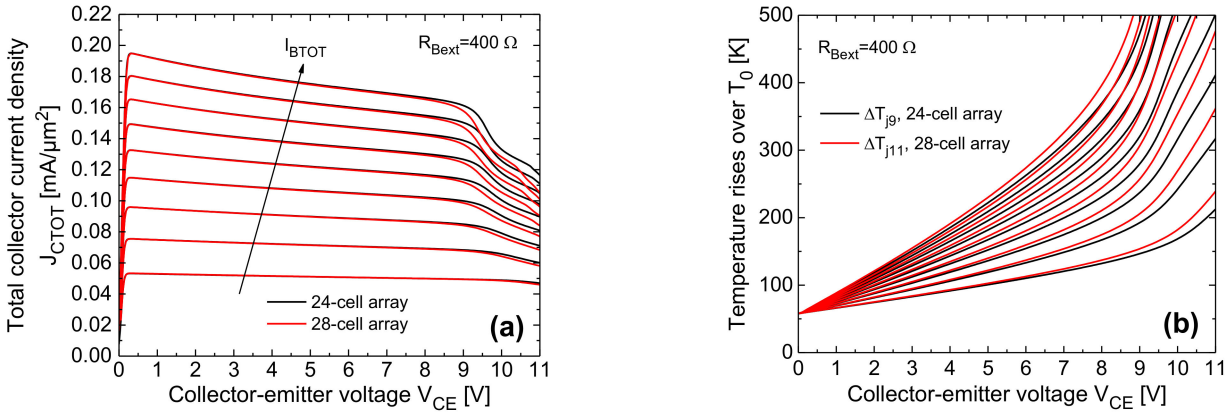

Figure 26. Simulated (**a**) total collector current densities J_{CTOT} and (**b**) junction temperature rises above T_0 of cell #9 (black lines) and #11 (red lines) for the 24- and 28-cell arrays, respectively, vs. collector-emitter voltage V_{CE}. The halved 24-cell array was biased with I_{BTOT} = 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5 mA, while the halved 28-cell one with I_{BTOT} = 1.17, 1.75, 2.33, 2.91, 3.5, 4.08, 4.67, 5.25, 5.83 mA.

5. Conclusions

In this paper, an efficient simulation approach has been used to analyze the dc electrothermal behavior of test devices and arrays for output stages of power amplifiers in InGaP/GaAs HBT technology. The approach relies on a full circuit representation of the structures under investigation (also referred to as macrocircuit), the solution of which can be evaluated by any circuit simulation software and requires tens of seconds at most, despite the complexity of the analysis. The macrocircuit is based on the thermal equivalent of the Ohm's law, and includes subcircuits to describe the unit cells, as well as a thermal feedback block to account for the power-temperature feedback. The thermal feedback block is obtained by combining (i) a FEM thermal tool aided by an *in-house* routine to generate an exceptionally accurate 3-D geometry/mesh of the structure, (ii) the FANTASTIC code to automatically get an equivalent thermal network without the need of simulations or user's experience, (iii) a preliminarily-calibrated Kirchhoff's transformation to include nonlinear thermal effects. The test devices have been analyzed under all the bias conditions of interest. An overview has been given on the thermally- and avalanche-induced distortion in the I–V characteristics, the limits of the safe behavior have been identified, and the beneficial effect of base ballasting has been explored. As far as the HBT arrays are concerned, the approach better shows its potential, as the individual currents, temperatures, and key parameters of all unit cells can be monitored. Some of the most important findings are: the base ballasting has been found to be more effective than emitter ballasting, which is typically suggested for breakdown-limited bipolar transistors; the arrays are more thermally-robust if arranged in columns with an even number of unit cells, where two central cells concurrently bear the heat coming from the outer ones as a nonuniform operating condition occurs. The approach is well suited to support engineers and designers in making choices oriented to develop more thermally-rugged and reliable circuits through, e.g., layout and/or nonuniform ballasting optimization.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

CB	common base
CE	common emitter
DCTM	dynamic compact thermal model
DoF	degree of freedom
ET	electrothermal
ETN	equivalent thermal network
FANTASTIC	FAst Novel Thermal Analysis Simulation Tool for Integrated Circuits
FEM	finite-element method
GaAs	gallium arsenide
HBT	heterojunction bipolar transistor
HI	high injection
II	impact ionization (avalanche)
MOR	model-order reduction
NDR	negative differential resistance
NTC	negative temperature coefficient
PA	power amplifier
PTC	positive temperature coefficient
R_{TH}	thermal resistance [K/W]
SCR	space-charge region
SCTM	static compact thermal model
SH	self-heating
SOG	silicon-on-glass
TEOL	thermal equivalent of the Ohm's law
TFB	thermal feedback block
T_0	reference temperature: 300 K
T_B	temperature of the laminate bottom for the arrays: 358 K
T_j	temperature averaged over the base-emitter junction under nonlinear thermal conditions
$\mathbf{T_{jlin}}$	temperature averaged over the base-emitter junction under linear thermal conditions
ΔT_j	temperature rise T_j-T_0
$\Delta \mathbf{T_{jlin}}$	temperature rise $\mathbf{T_{jlin}}$-T_0
ΔT_{jB}	temperature rise T_j-T_B
$\Delta \mathbf{T_{jlin}}_B$	temperature rise $\mathbf{T_{jlin}}$-T_B

References

1. Fresina, M. Trends in GaAs HBTs for wireless and RF. In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Atlanta, GA, USA, 9–11 October 2011; pp. 150–153.
2. Zarębski, J.; Górecki, K. SPICE-aided modelling of dc characteristics of power bipolar transistors with self-heating taken into account. *Int. J. Numer. Model.* **2009**, *22*, 422–433. [CrossRef]
3. Zarębski, J.; Górecki, K. The electrothermal large-signal model of power MOS transistors for SPICE. *IEEE Trans. Power Electron.* **2010**, *25*, 1265–1274. [CrossRef]
4. Górecki, K.; Górecki, P. Modelling dynamic characteristics of the IGBT with thermal phenomena taken into account. *Microelectron. Int.* **2017**, *34*, 160–164. [CrossRef]
5. Nenadović, N.; d'Alessandro, V.; La Spina, L.; Rinaldi, N.; Nanver, L.K. Restabilizing mechanisms after the onset of thermal instability in bipolar transistors. *IEEE Trans. Electron Devices* **2006**, *53*, 643–653. [CrossRef]

6. La Spina, L.; d'Alessandro, V.; Russo, S.; Rinaldi, N.; Nanver, L.K. Influence of concurrent electrothermal and avalanche effects on the safe operating area of multifinger bipolar transistors. *IEEE Trans. Electron Devices* **2009**, *56*, 483–491. [CrossRef]
7. La Spina, L.; d'Alessandro, V.; Russo, S.; Nanver, L.K. Thermal design of multifinger bipolar transistors. *IEEE Trans. Electron Devices* **2010**, *57*, 1789–1800. [CrossRef]
8. Metzger, A.G.; d'Alessandro, V.; Rinaldi, N.; Zampardi, P.J. Evaluation of thermal balancing techniques in InGaP/GaAs HBT power arrays for wireless handset power amplifiers. *Microelectron. Reliab.* **2013**, *53*, 1471–1475. [CrossRef]
9. Rinaldi, N.; d'Alessandro, V. Analysis of the bipolar current mirror including electrothermal and avalanche effects. *IEEE Trans. Electron Devices* **2009**, *56*, 1309–1321. [CrossRef]
10. D'Alessandro, V.; de Magistris, M.; Magnani, A.; Rinaldi, N.; Grivet-Talocia, S.; Russo, S. Time domain dynamic electrothermal macromodeling for thermally aware integrated system design. In Proceedings of the IEEE workshop on Signal and Power Integrity (SPI), Paris, France, 12–15 May 2013.
11. D'Alessandro, V.; La Spina, L.; Nanver, L.K.; Rinaldi, N. Analysis of electrothermal effects in bipolar differential pairs. *IEEE Trans. Electron Dev.* **2011**, *58*, 966–978. [CrossRef]
12. D'Alessandro, V.; de Magistris, M.; Magnani, A.; Rinaldi, N.; Russo, S. Dynamic electrothermal analysis of bipolar devices and circuits relying on multi-port positive Foster representation. In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Portland, OR, USA, 30 September–3 October 2012.
13. D'Alessandro, V.; D'Esposito, R.; Metzger, A.G.; Kwok, K.H.; Aufinger, K.; Zimmer, T.; Rinaldi, N. Analysis of electrothermal and impact-ionization effects in bipolar cascode amplifiers. *IEEE Trans. Electron Devices* **2018**, *65*, 431–439. [CrossRef]
14. D'Alessandro, V.; Magnani, A.; Riccio, M.; Breglio, G.; Irace, A.; Rinaldi, N.; Castellazzi, A. SPICE modeling and dynamic electrothermal simulation of SiC power MOSFETs. In Proceedings of the IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD), Waikoloa, HI, USA, 15–19 June 2014; pp. 285–288.
15. D'Alessandro, V.; Catalano, A.P.; Codecasa, L.; Moser, B.; Zampardi, P.J. Combined SPICE-FEM analysis of electrothermal effects in InGaP/GaAs HBT devices and arrays for handset applications. In Proceedings of the IEEE International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Toulouse, France, 15–18 April 2018.
16. COMSOL Multiphysics User's Guide, Release 5.2A. 2016. Available online: https://www.comsol.it/ (accessed on 1 October 2020).
17. D'Alessandro, V.; Catalano, A.P.; Codecasa, L.; Zampardi, P.J.; Moser, B. Accurate and efficient analysis of the upward heat flow in InGaP/GaAs HBTs through an automated FEM-based tool and Design of Experiments. *Int. J. Numer. Model. Electron. Netw. Devices Fields* **2019**, *32*, e2530. [CrossRef]
18. Carlslaw, H.S.; Jaeger, J.C. *Conduction of Heat in Solids*, 2nd ed.; Oxford University Press: London, UK, 1959.
19. Joyce, W.B. Thermal resistance of heat sinks with temperature-dependent conductivity. *Solid State Electron.* **1975**, *18*, 321–322. [CrossRef]
20. PSPICE User's Manual, Cadence OrCAD 16.5. 2011. Available online: https://www.orcad.com/ (accessed on 1 October 2020).
21. D'Alessandro, V.; Codecasa, L.; Catalano, A.P.; Scognamillo, C. Circuit-based electrothermal simulation of multicellular SiC power MOSFETs using FANTASTIC. *Energies* **2020**, *13*, 4563. [CrossRef]
22. Codecasa, L.; d'Alessandro, V.; Magnani, A.; Rinaldi, N.; Zampardi, P.J. FAst novel thermal analysis simulation tool for integrated circuits (FANTASTIC). In Proceedings of the International workshop on THERMal INvestigations of ICs and systems (THERMINIC), London, UK, 24–26 September 2014.
23. Magnani, A.; d'Alessandro, V.; Codecasa, L.; Zampardi, P.J.; Moser, B.; Rinaldi, N. Analysis of the influence of layout and technology parameters on the thermal impedance of GaAs HBT/BiFET using a highly-efficient tool. In Proceedings of the IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), La Jolla, CA, USA, 19–22 October 2014.
24. D'Alessandro, V.; Catalano, A.P.; Magnani, A.; Codecasa, L.; Rinaldi, N.; Moser, B.; Zampardi, P.J. Simulation comparison of InGaP/GaAs HBT thermal performance in wire-bonding and flip-chip technologies. *Microelectron. Reliab.* **2017**, *78*, 233–242. [CrossRef]
25. Zhang, Q.M.; Hu, H.; Sitch, J.; Surridge, R.K.; Xu, J.M. A new large signal HBT model. *IEEE Trans. Microw. Theory Tech.* **1996**, *44*, 2001–2009. [CrossRef]
26. Liu, W.; Khatibzadeh, A. The collapse of current gain in multi-finger heterojunction bipolar transistors: Its substrate temperature dependence, instability criteria, and modeling. *IEEE Trans. Electron. Devices* **1994**, *41*, 1698–1707. [CrossRef]
27. Nenadović, N.; d'Alessandro, V.; Nanver, L.K.; Tamigi, F.; Rinaldi, N.; Slotboom, J.W. A back-wafer contacted silicon-on-glass integrated bipolar process–Part II: A novel analysis of thermal breakdown. *IEEE Trans. Electron. Devices* **2004**, *51*, 51–62. [CrossRef]
28. D'Alessandro, V.; Marano, I.; Russo, S.; Céli, D.; Chantre, A.; Chevalier, P.; Pourchon, F.; Rinaldi, N. Impact of layout and technology parameters on the thermal resistance of SiGe:C HBTs. In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Austin, TX, USA, 4–6 October 2010; pp. 137–140.
29. D'Alessandro, V.; Sasso, G.; Rinaldi, N.; Aufinger, K. Influence of scaling and emitter layout on the thermal behavior of toward-THz SiGe:C HBTs. *IEEE Trans. Electron. Devices* **2014**, *61*, 3386–3394. [CrossRef]
30. Miller, S.L. Ionization rates for holes and electrons in silicon. *Phys. Rev.* **1957**, *105*, 1246–1249. [CrossRef]
31. Rinaldi, N.; d'Alessandro, V. Theory of electrothermal behavior of bipolar transistors: Part III–Impact ionization. *IEEE Trans. Electron Devices* **2006**, *53*, 1683–1697. [CrossRef]

32. Zampardi, P.J.; Yang, Y.; Hu, J.; Li, B.; Fredriksson, M.; Kwok, K.H.; Shao, H. Practical statistical simulation for efficient circuit design. In *Nonlinear Transistor Model Parameter Extraction Techniques*; Chapter 9; Rudolph, M., Fager, C., Root, D.E., Eds.; Cambridge University Press: Cambridge, UK, 2011; pp. 287–317.
33. Palankovski, V.; Quay, R. *Analysis and Simulation of Heterostructure Devices*; Springer: New York, NY, USA, 2004.
34. Anholt, R. HBT thermal element design using an electro/thermal simulator. *Solid State Electron.* **1998**, *42*, 857–864. [CrossRef]
35. Lienhard, J.H., IV; Lienhard, J.H., V. *A Heat Transfer Textbook*; Phlogiston Press: Cambridge, MA, USA, 2008.
36. Poulton, K.; Knudsen, K.L.; Corcoran, J.J.; Wang, K.-C.; Pierson, R.L.; Nubling, R.B.; Chang, M.-C.F. Thermal design and simulation of bipolar integrated circuits. *IEEE J. Solid State Circuits* **1992**, *27*, 1379–1387. [CrossRef]
37. Codecasa, L.; D'Amore, D.; Maffezzoni, P. Compact modeling of electrical devices for electrothermal analysis. *IEEE Trans. Circuits Syst. I* **2003**, *50*, 465–476. [CrossRef]
38. Codecasa, L.; Catalano, A.P.; d'Alessandro, V. *A priori* error bound for moment matching approximants of thermal models. *IEEE Trans. Comp. Packag. Manufact. Technol.* **2019**, *9*, 2383–2392. [CrossRef]
39. Keysight Advanced Design System (ADS). 2019. Available online: https://edadocs.software.keysight.com/ads2019 (accessed on 25 January 2021).
40. Schröter, M.; Chakravorty, A. *Compact Hierarchical Bipolar Transistor Modeling with HICUM*; World Scientific Publishing: Singapore, 2010.
41. Keysight ADS Electro-Thermal Simulator (Agilent EEsof EDA). Available online: https://www.keysight.com/upload/cmc_upload/All/ADSElectrothermal.pdf (accessed on 25 January 2021).
42. Dawson, D.E.; Gupta, A.K.; Salib, M.L. CW measurements of HBT thermal resistance. *IEEE Trans. Electron Devices* **1992**, *39*, 2235–2239. [CrossRef]
43. Popescu, C. Selfheating and thermal runaway phenomena in semiconductor devices. *Solid State Electron.* **1970**, *13*, 441–450. [CrossRef]
44. Latif, M.; Bryant, P.R. Multiple equilibrium points and their significance in the second breakdown of bipolar transistors. *IEEE J. Solid State Circuits* **1981**, *16*, 8–15. [CrossRef]
45. Rinaldi, N.; d'Alessandro, V. Theory of electrothermal behavior of bipolar transistors: Part I–Single-finger devices. *IEEE Trans. Electron Devices* **2005**, *52*, 2009–2021. [CrossRef]
46. Jaoul, M.; Céli, D.; Maneux, C.; Zimmer, T. Measurement based accurate definition of the SOA edges for SiGe HBTs. In Proceedings of the IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), Nashville, TN, USA, 3–6 November 2019.
47. Liu, W.; Khatibzadeh, A.; Sweder, J.; Chau, H.-F. The use of base ballasting to prevent the collapse of current gain in AlGaAs/GaAs heterojunction bipolar transistors. *IEEE Trans. Electron Devices* **1996**, *43*, 245–251. [CrossRef]
48. Vanhoucke, T.; Hurkx, G.A.M. Unified electro-thermal stability criterion for bipolar transistors. In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Santa Barbara, CA, USA, 9–11 October 2005; pp. 37–40.
49. Seiler, U.; Koenig, E.; Narozny, P.; Dämbkes, H. Thermally triggered collapse of collector current in power heterojunction bipolar transistors. In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Minneapolis, MN, USA, 4–5 October 1993; pp. 257–260.
50. Liu, W.; Nelson, S.; Hill, D.G.; Khatibzadeh, A. Current gain collapse in microwave multifinger heterojunction bipolar transistors operated at very high power densities. *IEEE Trans. Electron Devices* **1993**, *40*, 1917–1927. [CrossRef]
51. Liu, W. Thermal coupling in 2-finger heterojunction bipolar transistors. *IEEE Trans. Electron Devices* **1995**, *42*, 1033–1038. [CrossRef]
52. Wang, K.-C.; Asbeck, P.M.; Chang, M.-C.F.; Miller, D.L.; Sullivan, G.J.; Corcoran, J.J.; Hornak, T. Heating effects on the accuracy of HBT voltage comparators. *IEEE Trans. Electron Devices* **1987**, *34*, 1729–1735. [CrossRef]
53. Järvinen, E.; Kalajo, S.; Matilainen, M. Bias circuits for GaAs HBT power amplifiers. In Proceedings of the IEEE MTT-S International Microwave Symposium Digest, Phoenix, AZ, USA, 20–24 May 2001; pp. 507–510.
54. Zampardi, P.J. Silicon modelers are from Mars, GaAs modelers are from Venus. In Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Miami, FL, USA, 19–21 October 2017; pp. 257–260.