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Design of a Wideband Doherty Power Amplifier with High Efficiency for 5G Application

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Abstract: This paper discusses the design of a wideband class AB-C Doherty power amplifier suitable for 5G applications. Theoretical analysis of the output matching network is presented, focusing on the impact of the non-ideally infinite output impedance of the auxiliary amplifier in back off, due to the device's parasitic elements. By properly accounting for this effect, the designed output matching network was able to follow the desired impedance trajectories across the 2.8 GHz to 3.6 GHz range (fractional bandwidth = 25%), with a good trade-off between efficiency and bandwidth. The Doherty power amplifier was designed with two 10 W packaged GaN HEMTs. The measurement results showed that it provided 43 dBm to 44.2 dBm saturated output power and 8 dB to 13.5 dB linear power gain over the entire band. The achieved drain efficiency was between 62% and 76.5% at saturation and between 44% and 56% at 6 dB of output power back-off.

Keywords: back-off efficiency; Doherty power amplifier; GaN HEMT; load modulation; wireless communications

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1. Introduction

Recently, with the continuous evolution of wireless systems towards higher data rates and lower power consumption, the need for high-performance transceivers has increased [1–3]. Independent of the specific scenario (base-station, handset, point-to-point radio-links), the power amplifier is one of the most consuming elements of the entire architecture, and it is of paramount importance for it to achieve the highest possible efficiency. This holds true for 5G systems, where PAs are required to provide high efficiency, gain, linearity, and output power in increasingly wider bandwidths [4–7]. The frequency bands for 5G mobile networks are organized into two different ranges, namely FR1 covering the sub-6 GHz bands, some of which were already used by previous standards, and FR2 covering the millimeter wave range, from 24.25 GHz to 52.6 GHz. To achieve high data rates, Orthogonal Frequency Division Modulation (OFDM) schemes are used in modern mobile communications systems, including 5G [8,9]. However, while the wider RF bandwidths achievable in the FR2 range allow relaxing the complexity of the adopted modulation schemes, PAs working in the FR1 range need to operate as efficiently as possible with modulations as complex as 4096-Quadrature Amplitude Modulation (QAM). These kinds of modulations feature a time-varying envelope with a very high peak-to-average power ratio (PAPR); therefore, to cope with such signals, power amplifiers are required to have high efficiency, not only at saturation, but also at lower output power levels [10–13]. This is not the case for conventional power amplifiers, which can have very high efficiency at their maximum output power, but show a sharp efficiency drop with output power back-off [14].

In order to increase back-off efficiency, various techniques have been proposed, both at the PA and at the system level, such as the Doherty power amplifier [13,15] and the Chireix outphasing [16,17] PA, based on the load modulation concept [18], or Envelope Elimination and Restoration (EER) [19,20] and Envelope Tracking (ET) [21,22] techniques, based instead on supply modulation. A combination of both supply and load modulation can be also exploited to maximize the achievable back-off efficiency [23,24]. Among all these techniques, however, the Doherty Power Amplifier (DPA) gained the highest popularity thanks to its architecture simplicity and relatively good linearity [25,26]. However, one of the main open issues of DPAs is related to bandwidth [27,28]. Although various techniques have been reported to increase the bandwidth of Doherty power amplifiers [29–33], they typically have the drawback of increasing the circuit complexity of the DPA. For instance, in [9,12], output compensation stages and post matching networks were added to improve bandwidth, while Reference [3] adopted a non-conventional impedance inverting network. Finally, digital techniques were used in [16,17]. Therefore, a Doherty power amplifier that can achieve a wide bandwidth and high efficiency by keeping its simple original topology is highly desirable [34].

This paper details the development of a wideband 20 W DPA with 6 dB Output power Back-Off (OBO) working in the frequency range from 2.8 GHz to 3.6 GHz, based on the CGH40010F GaN HEMT from Wolfspeed. The target frequency range was selected so as to cover as much as possible the 5G n78 band (3.3 GHz–3.8 GHz) within the limits of the selected device, which are mainly related to the package.

A main limitation to wideband DPA operation is due to the parasitic elements of the transistor. In particular, they make the output impedance of the auxiliary PA in back-off finite and also frequency dependent. This load variation was taken into account in the design of the main matching network, thus achieving wideband performance. The achieved Drain Efficiency (DE) at saturation and at 6 dB OBO was above 62% and 44%, respectively. The measured output power and power gain (at OBO) were, respectively, in excess of 43 dBm and 8 dB.

The paper is organized as follows. In Section 2, the overall structure of the proposed DPA is shown and the design of the output section is discussed. Sections 3 and 4 present the simulated and measured performance, respectively, and compare this work with the literature. Finally, conclusions are drawn in Section 5.

2. Doherty Power Amplifier Design

The schematic of the proposed DPA is illustrated in Figure 1, highlighting its building blocks. The DPA consists of main and auxiliary amplifiers, both based on the same active device biased in class AB and C, respectively. When the input power is low, the main amplifier is ON, and the auxiliary amplifier is OFF. Increasing the input power, the main amplifier reaches its maximum output voltage, and the first peak of efficiency occurs. At that point (break point), the auxiliary amplifier turns on and modulates the load of the main amplifier by injecting current at the common node. In this way, the output voltage and efficiency of the main amplifier remain, in principle, at the maximum value, while the output current and hence output power increase. The theoretical drain efficiency of the DPA is given by:

$$\eta_D = \frac{P_{\text{out}}}{P_{\text{DC}}} = 100\,\frac{0.5\,V_{\text{out}}\,I_{\text{out}}}{V_{\text{DC,M}}\,I_{\text{DC,M}} + V_{\text{DC,A}}\,I_{\text{DC,A}}} \tag{1}$$

where V_{out} and I_{out} are the maximum RF output voltage and current at the fundamental frequency, while $V_{\text{DC,M}}\,I_{\text{DC,M}}$ and $V_{\text{DC,A}}\,I_{\text{DC,A}}$ are the DC power of the main and auxiliary PA, respectively. The output power back-off of the DPA is defined as:

$$OBO = 10\,\log_{10}\left(\frac{P_{\text{out,B}}}{P_{\text{out,S}}}\right) \tag{2}$$

where $P_{out,B}$ and $P_{out,S}$ are the output power levels at the break and saturation points, respectively. Theoretically, the drain efficiency at the break point is equal to the efficiency at saturation and remains high in the entire Doherty region (6 dB in this case). However, because of the parasitic components of the transistors and the knee voltage effect that causes soft auxiliary turn-on, the efficiency profile shows a drop in the Doherty region, and the practically attainable efficiency at the break point is typically lower than the saturated one [35,36].

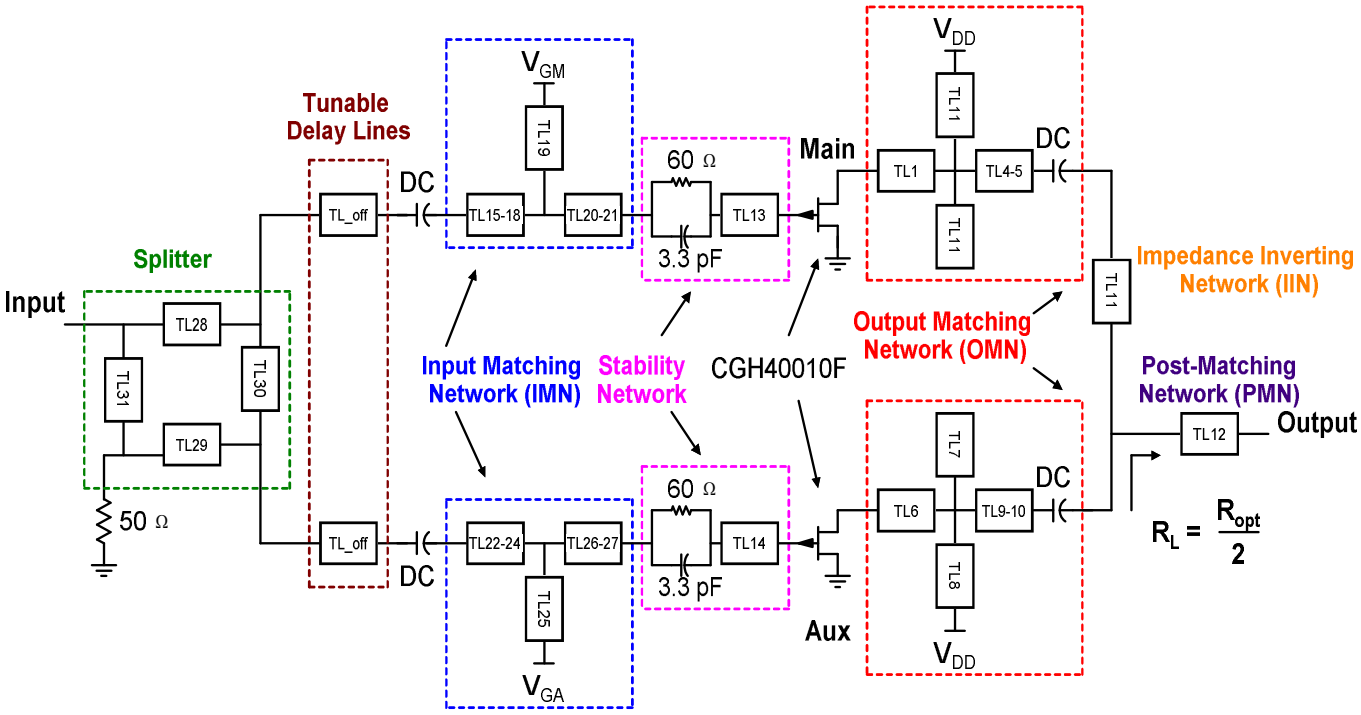


Figure 1. Schematic of the proposed Doherty power amplifier.

2.1. Device Analysis

The CGH40010F GaN HEMT from Wolfspeed (Wolfspeed, Durham, NC, USA) was adopted to design the DPA. The Maximum Available Gain (MAG) of this device for different bias voltages is shown in Figure 2. As shown in Figure 3, the maximum frequency (around 26 GHz) and cut-off frequency (around 11.3 GHz) are only slightly dependent on the bias voltages, V_{GS} and V_{DS}; thus, they do not represent a limit for the bias selection. The drain voltage was set to 28 V, which was compatible with the maximum frequency and voltage swing.

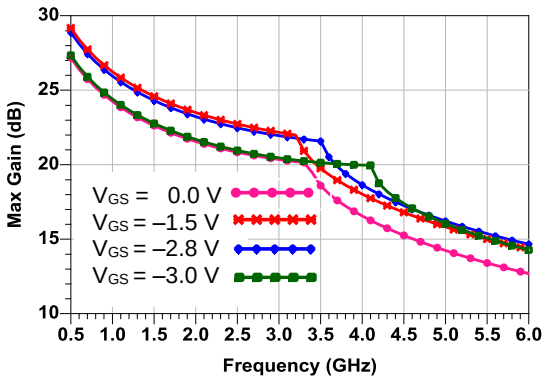


Figure 2. Simulated maximum available gain of the CGH40010F device for different biasing classes.

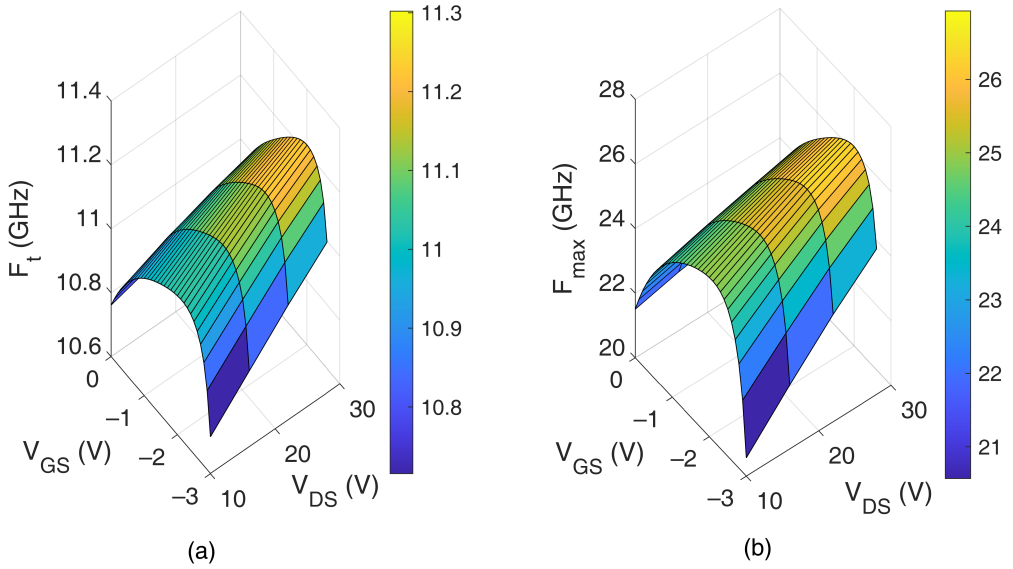


Figure 3. Cut−off (**a**) and maximum (**b**) frequency of the CGH40010F versus V_{GS} and V_{DS}.

The maximum performance of the DPA in terms of output power and efficiency was achieved when the transistor was matched to its optimum intrinsic resistance. Hence, it was necessary to account for the parasitic effects of the transistor. For this reason, load-pull analysis at the extrinsic device reference plane over the whole bandwidth was used to find the actual optimum impedance. As an example, the simulated load-pull contours for the drain efficiency (blue) and the output power (red) at 3.3 GHz are reported in Figure 4a. Through load-pull analysis across the whole bandwidth, the optimum output load trajectories for the main and auxiliary transistors were found from 2.8 GHz to 3.6 GHz, both at saturation and the break point, as reported in Figure 4b. As a first step for designing the output matching networks, the average output impedance was considered, which was estimated in $(17 + j5)\,\Omega$ and $(12 + j14)\,\Omega$ at saturation and the break point, respectively. Then, wideband Computer-Aided Design (CAD) optimization was performed on the designed Output Matching Networks (OMNs) to fine-tune their behavior across the bandwidth.

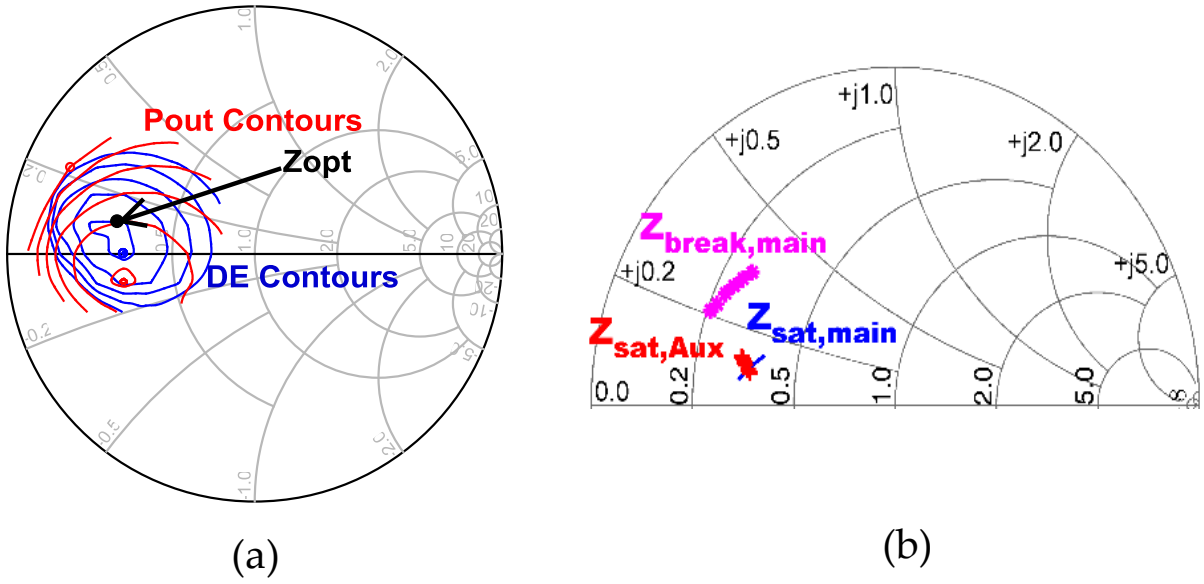


Figure 4. (**a**) Load-pull contours for the drain efficiency (blue) and output power (red) at 3.3 GHz and (**b**) optimum output impedance at saturation and Output power Back-Off (OBO). DE, Drain Efficiency.

2.2. Output Matching Network Design

According to the notation in Figure 5a, the input reflection coefficient (Γ_M) of the main OMN is defined as [35]:

$$\Gamma_M = S_{11} + \frac{S_{12}S_{21}\Gamma_{M1}}{1 - S_{22}\Gamma_{M1}} \tag{3}$$

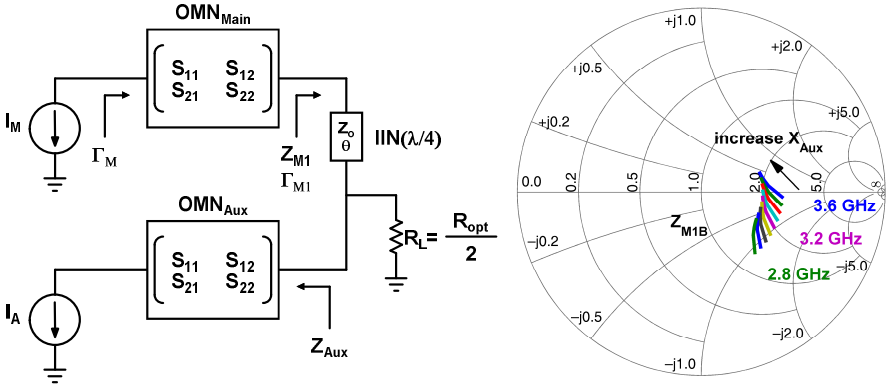
where the scattering parameters are defined with respect to R_{opt}, and the load reflection coefficient of the OMN (Γ_{M1}) is expressed as:

$$\Gamma_{M1} = \frac{Z_{M1} - R_{opt}}{Z_{M1} + R_{opt}} \tag{4}$$

where Z_{M1} is the load impedance of the main OMN. R_{opt} is the intrinsic resistance that simultaneously maximizes drain voltage and current, Z_{M1}, for an ideal DPA is defined as follows:

$$Z_{M1} = R_{opt}(2 - \beta) \tag{5}$$

where β is the ratio between the auxiliary and main current ($\beta = I_A/I_M$). Since in this design, a symmetrical structure was used, the theoretical maximum current for the main and auxiliary was the same. As a result, β was equal to zero and one at the break point and saturation, respectively (Z_{M1} equal to $2R_{opt}$ and R_{opt}).



(a) (b)

Figure 5. (**a**) Block diagram of the output matching networks. (**b**) Variation of the Z_{M1B} versus f (from 2.8 GHz to 3.6 GHz) and X_{Aux} (from 40 Ω to 500 Ω) when the auxiliary power amplifier (PA) is OFF.

The output matching network needs to match the optimum output impedance found from the load-pull analysis with Z_{M1}. The common load R_L was set to $R_{opt}/2$ and transformed into Z_{M1} by the Impedance Inverting Network (IIN), which is typically implemented with a quarter-wave ($\lambda/4$) line. The electrical length of the $\lambda/4$ line changes with the frequency as follows:

$$\theta = \frac{\pi}{2}\frac{f}{f_0} \tag{6}$$

where f is the operating frequency and f_0 is the center frequency at which the line was designed. Moreover, due to the parasitic elements of the transistors, the impedance presented by the auxiliary when in the OFF state was not infinite, but can be expressed as:

$$Z_{Aux} = R_{Aux} + jX_{Aux} \tag{7}$$

To analyze the impact of Z_{Aux} on the DPA behavior, the transformed impedance of the IIN is rewritten as follows [35]:

$$Z_{M1} = Z_0 \frac{(R_L || Z_{Aux}) + jZ_0 \tan(\theta)}{Z_0 + j(R_L || Z_{Aux}) \tan(\theta)} \tag{8}$$

where Z_0 is the characteristic impedance of the IIN:

$$Z_0 = \sqrt{2R_{opt}R_L} \tag{9}$$

By substituting Equations (6), (7) and (9) in (8), Z_{M1} at the break point (Z_{M1_B}) is calculated as:

$$Z_{M1_B} = R_{opt} \frac{-R_{opt}X_{Aux} \tan\left(\frac{\pi}{2}\frac{f}{f_0}\right) + jR_L\left[X_{Aux} + R_{opt} \tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)\right]}{R_L\left[R_{opt} - X_{Aux} \tan\left(\frac{\pi}{2}\frac{f}{f_0}\right)\right] + jR_{opt}X_{Aux}} \tag{10}$$

where only the imaginary part of Z_{Aux} is considered for simplicity. This amounts to assuming that the impedance presented by the auxiliary may not be an ideal open circuit due to partial parasitic compensation, but its resistive component is however negligible. Figure 5b illustrates the Z_{M1B} at the break point for different frequencies when varying X_{Aux} from 40 Ω to 500 Ω. To plot these graphs based on Equation (10), the R_{opt}, R_L, and f_0 were considered to be 50 Ω, 25 Ω, and 3.3 GHz, respectively. As demonstrated, the load impedance of main OMN at the OBO (Z_{M1B}) varied sensibly with both the operating frequency and parasitic reactance of the auxiliary PA (X_{Aux}), thus making the design of wideband DPAs challenging.

After considering the theoretical behavior mentioned above, the next step was the OMN design. The microstrip implementation on a Rogers RO4350B substrate (Rogers Corporation, Chandler, AZ, USA) (ε_r = 3.66; substrate height and metal thickness were 762 µm and 35 µm, respectively) was selected for this design. There are different strategies for designing a wideband matching network [35]. In this case, the stepped impedance technique was preferred. The final layout of the output matching network is presented in Figure 6a and includes the drain biasing network. According to the results obtained in Figure 5b, in the OMN design, the variation of load impedances in the OBO point was considered in order to maximize back-off efficiency. Figure 6b shows the input reflection coefficient (S_{11}) presented by the main output matching network, which was computed with respect to $2R_{opt}$, for different Z_{M1B} values, corresponding to different frequencies and X_{Aux}. This result confirmed that the designed OMN was able to follow the load impedance variations in back-off, achieving wideband matching. The same OMN was also adopted for the auxiliary device, since it was identical to the main one. This choice should also ensure a similar phase variation versus frequency in the two branches, thus easing the enforcement of the appropriate signal phase alignment, which is essential for the Doherty operation.

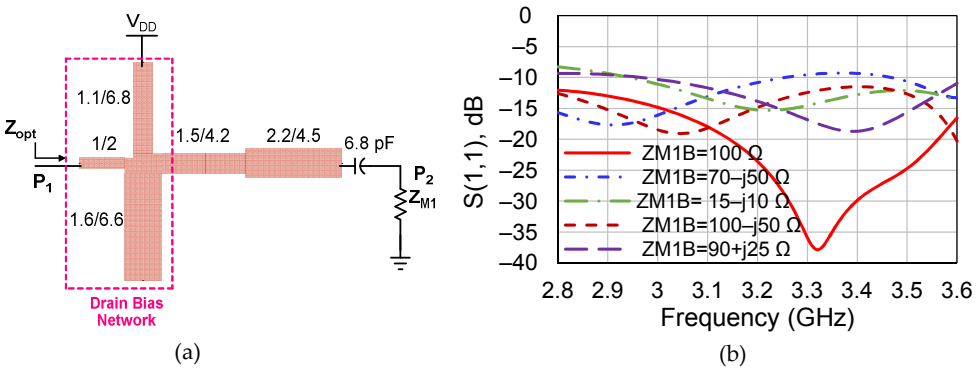


Figure 6. (**a**) Output matching network of the main (dimensions (width/length) are in mm) and (**b**) input reflection coefficient when port 1 is normalized with respect to $2R_{opt}$ for different load impedance at the break point.

2.3. Input Matching Network Design

Once having set the OMN, the Input Matching Network (IMN) can be designed. The proper design of the IMN is crucial to maintain high efficiency and equalize gain over wide bandwidths. Source-pull analysis was therefore performed to find the optimum input impedances for the main and auxiliary, which were (considering again a mean value over the entire bandwidth) $(5 + j30)\,\Omega$ and $(3.2 + j18.5)\,\Omega$, respectively, and were then matched to $50\,\Omega$. The final layout of the input matching network is illustrated in Figure 7. As can be noted, also for the IMN, the stepped impedance approach was followed. The topology for both IMNs was the same; however, the values of the transmission lines were independently optimized to account for the different biasing class. A parallel RC network ($R = 60\,\Omega$ and $C = 3.3$ pF) was inserted in series with the gate to ensure in-band stability with the lowest possible associated losses.

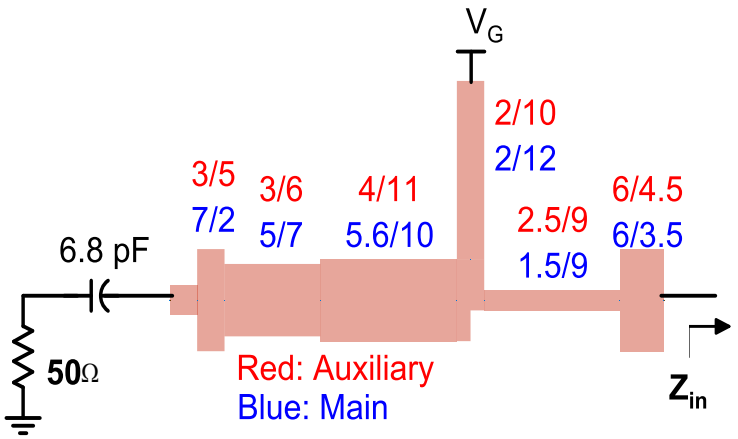


Figure 7. Layout of the input matching network (dimension: width/length (mm)).

Finally, an uneven hybrid 90° (branch line) splitter was designed with a $50\,\Omega$ reference impedance at all ports to provide the necessary splitting of the input signal into the main and auxiliary paths with a 90° phase shift between them. The power splitting ratio was $P_{\mathrm{Aux}}/P_{\mathrm{Main}} = 1.5$. Figure 8 shows the layout and the simulated behavior of the splitter. Return loss was below -10 dB over the entire band. The isolated port was connectorized to allow for the insertion of an external resistor with high power handling capabilities.

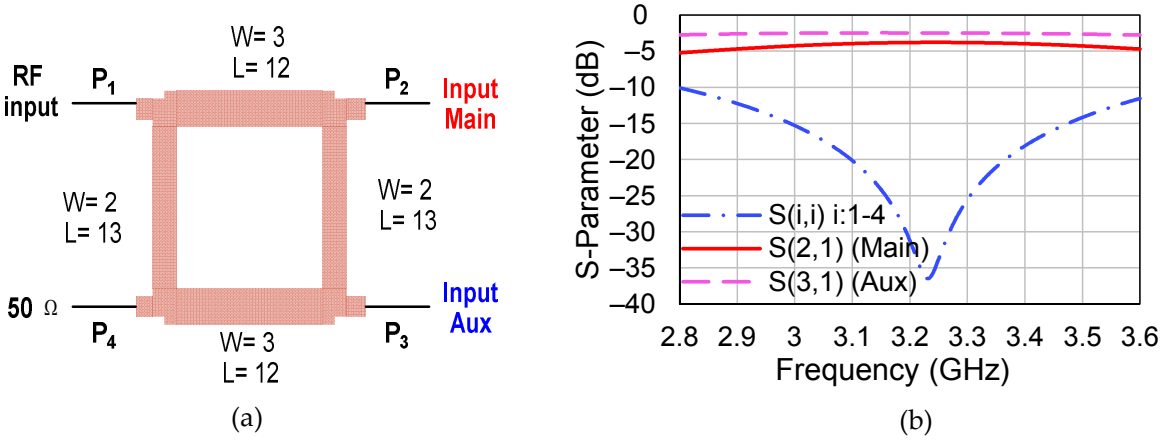


Figure 8. (**a**) Layout of the splitter (dimension: width/length (mm)). (**b**) Performance versus frequency.

2.4. Stability Analysis

The DPA stability must be evaluated for the designed DPA to ensure its unconditional stability at all frequencies. The stability analysis with the Rollett approach is not entirely reliable for Doherty power amplifiers [37]. To investigate the stability of parallel multi-amplifier architectures, the technique proposed by Ohtomo [38] provides more reliable results.

According to the Ohtomo approach, the Nyquist method was applied, considering the number of clockwise rotations around the point 1 + *j*0 of the Nyquist plot of the open loop functions (G_{iM}, G_{oM}, G_{iA}, and G_{oA}), simulated adopting the setup shown in Figure 9, using ideal circulators at the gate and drain nodes. The Nyquist plots are shown in Figure 10 for frequency going from DC to 6 GHz. As shown, none of them enclosed the 1 + *j*0 point; therefore, the proposed DPA was stable.

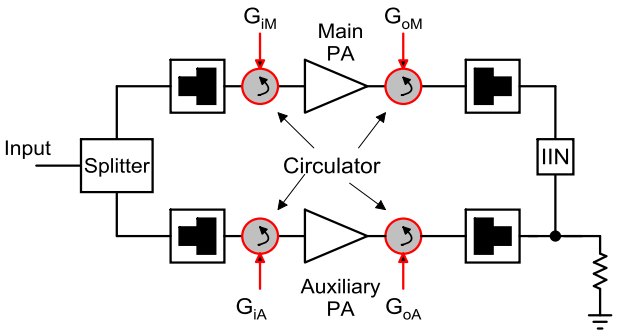


Figure 9. Implementation of the stability test on the Doherty power amplifier. IIN, Impedance Inverting Network.

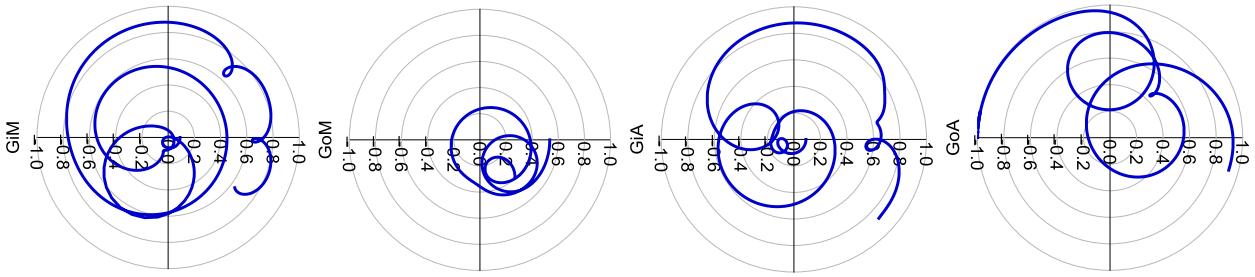


Figure 10. Nyquist plot of the open-loop function for the proposed Doherty power amplifier (DPA) from 100 MHz to 6 GHz.

3. Simulated DPA Performance

The simulated drain efficiency and gain versus output power over the target frequency range are presented in Figure 11. As shown, drain efficiency was above 44% over the 6 dB back-off region, and the maximum output power was approximately 44 dBm.

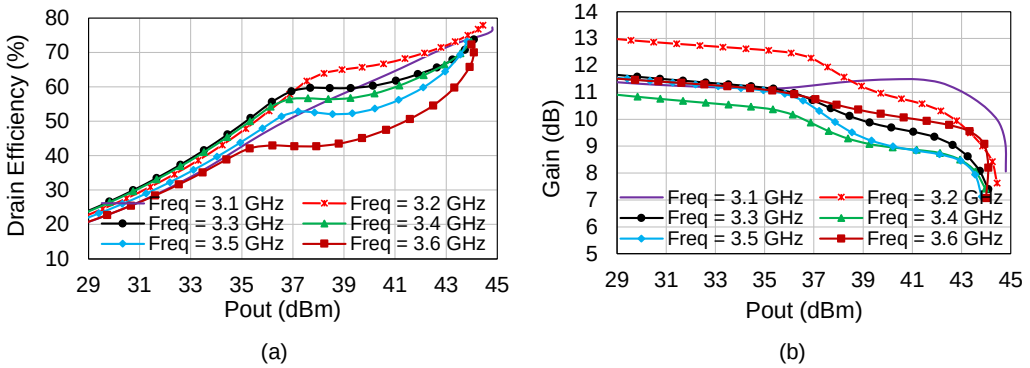


Figure 11. Simulated drain efficiency (**a**) and gain (**b**) of the designed DPA versus output power.

In addition, the linearity of the DPA was assessed in simulation. A two-tone analysis was first performed to evaluate the third and fifth Intermodulation Distortions (IMD3 and IMD5), which are plotted in Figure 12a as a function of input power. As shown, IMD3 and IMD5 were below −18 dBm and −34 dBm, respectively. To test instead the system-level behavior, the designed DPA was simulated under a modulated signal adopting a 16-QAM signal with a 5 MHz bandwidth and 6 dB PAPR. Figure 12b illustrates the simulated input and output power spectra at the center frequency of 3.3 GHz for an average output power of 36 dBm. As shown, the Adjacent Channel Power Ratio (ACPR) was less than −32 dBc. which compares well with the state-of-the-art [9,31], at least in simulation.

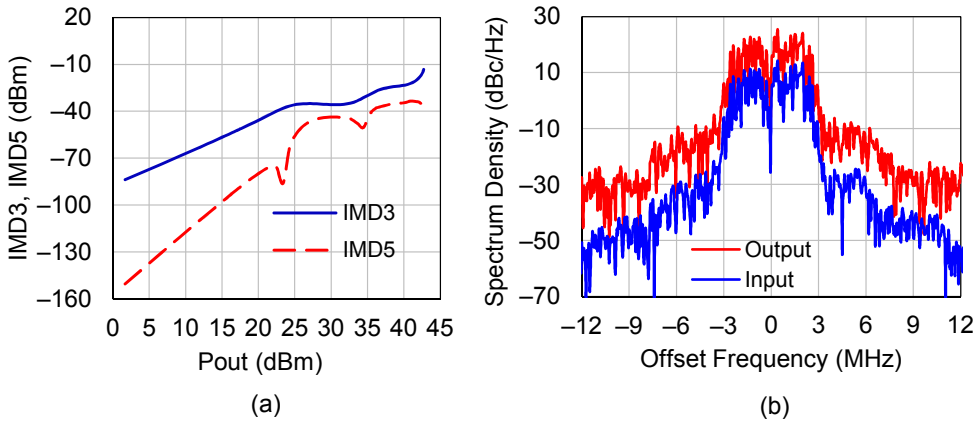


Figure 12. (**a**) Two-tone power sweep simulation at 3.3 GHz. (**b**) Simulated input and output power spectrum at 3.3 GHz for the average output power of 36 dBm. IMD, Intermodulation Distortion.

4. Measurements Results

The photograph of the fabricated DPA is shown in Figure 13. For the DPA characterization, the gate voltages of the main and auxiliary amplifiers were set to −2.8 V and −5.5 V, respectively, while the drain voltage was 28 V. The quiescent drain current was 68 mA.

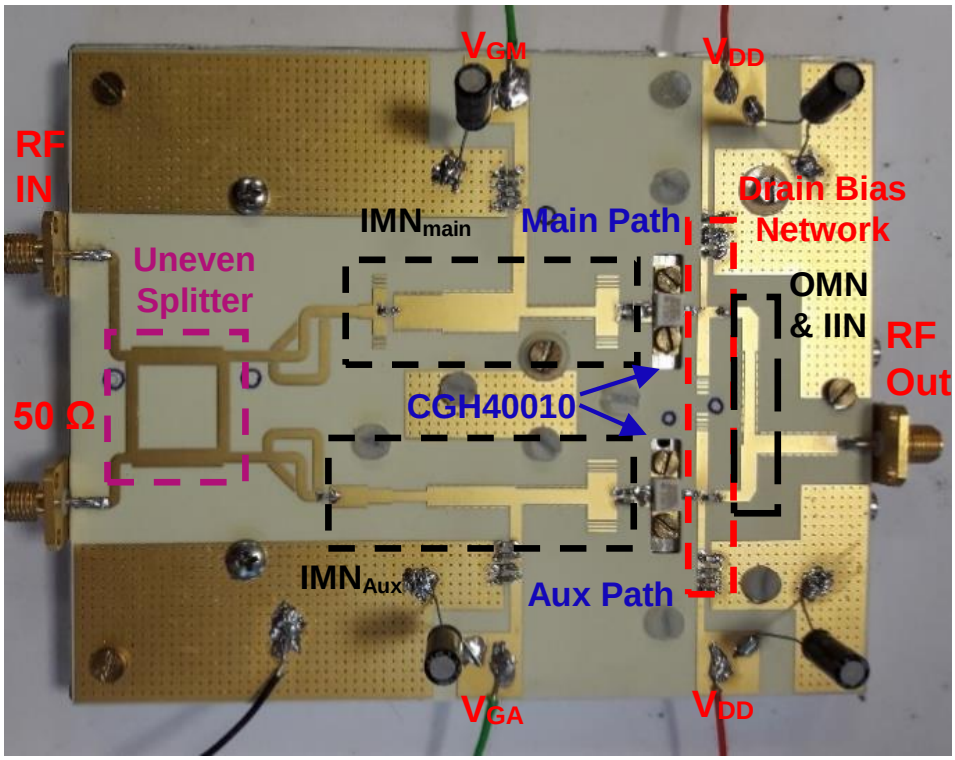


Figure 13. Photograph of the fabricated Doherty power amplifier.

The simulated and measured scattering parameters are reported in Figure 14. Despite a frequency shift towards lower frequencies, a small signal gain around 10 dB was maintained from 2.2 GHz to 3.6 GHz, which allowed fully covering the targeted frequency band. Moreover, input matching around 10 dB was achieved from 2.6 GHz to 3.6 GHz. The output matching results were better than 10 dB in the higher portion of the operating band, namely from 3 GHz to 3.8 GHz, while this slightly degraded at the lower end of the band. To account for the possible inaccuracy of the capacitor and resistor models and mounting/soldering process, we inserted tunable elements in the matching networks. During the measurements, we tuned the networks and the bias to achieve the widest possible bandwidth, thus changing the circuit from the nominal/simulated condition. This led to some mismatches between the simulation and measurements.

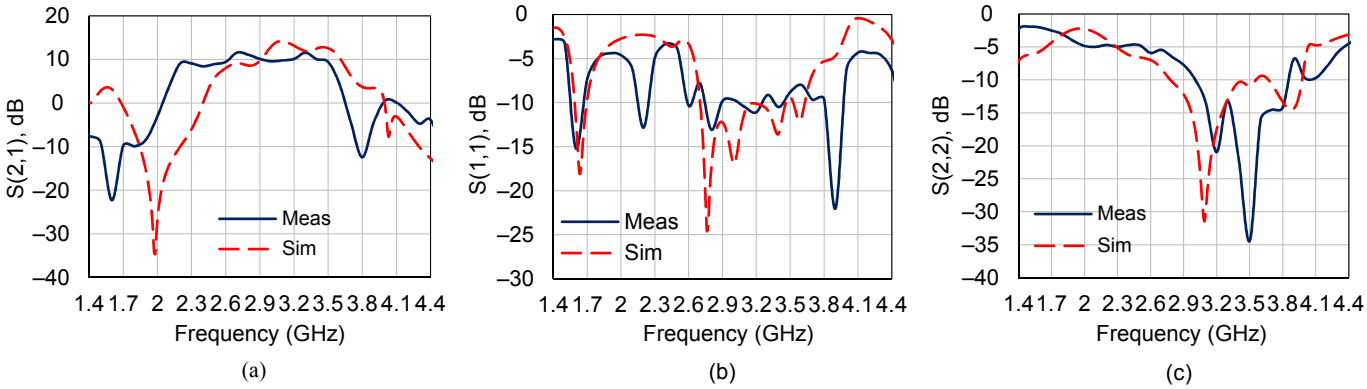


Figure 14. Simulated (dashed) and measured (solid) scattering parameters of the proposed DPA (**a**) $S(2,1)$, (**b**) $S(1,1)$, and (**c**) $S(2,2)$.

Continuous Wave (CW) large signal measurements showed a maximum output power at 3 dB gain compression between 43 dBm and 44.2 dBm. Figure 15 shows the measured gain and drain efficiency with respect to the output power. The large signal performance is summarized and compared to simulations in Figure 16, which shows that the agreement between the measurements and simulations was rather good. The measured drain efficiency ranged from 62% to 76.5% at saturation and from 44% to 56% at 6 dB output power back-off. The obtained gain at 6 dB back-off over the frequency band was between 8 dB and 13.5 dB.

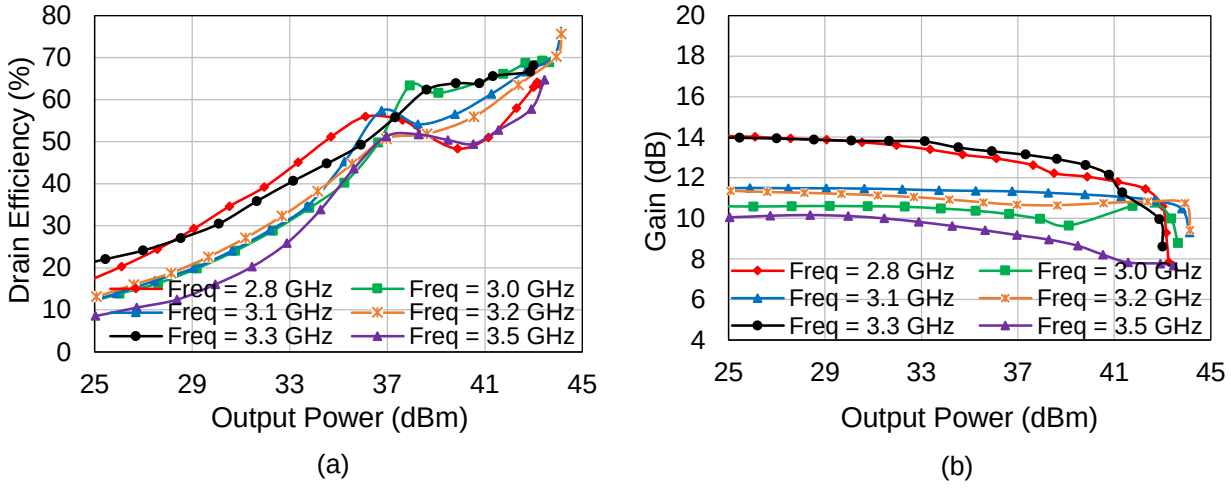


Figure 15. Measured (**a**) drain efficiency and (**b**) gain versus output power.

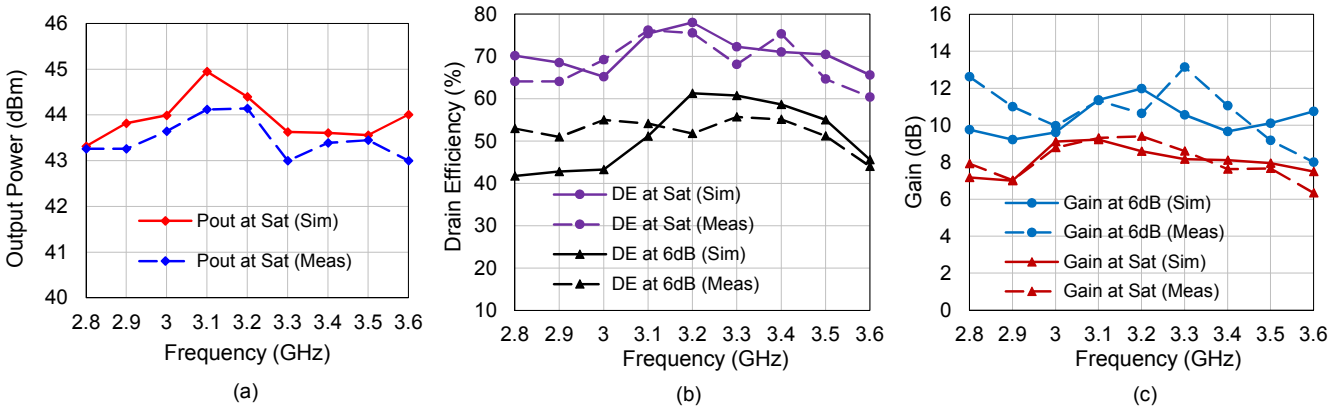


Figure 16. Comparison of simulated (solid) and measured (dashed) large signal performance versus frequency: (**a**) saturated output power and (**b**) drain efficiency and (**c**) gain at saturation and 6 dB back-off.

Table 1 summarizes the performance of the proposed DPA compared to other works where DPAs were designed targeting a similar OBO level on a comparable frequency range and adopting the same device. As discussed, in the proposed DPA, a high drain efficiency together with a high gain were achieved over a fairly wide bandwidth. The performance obtained was well in line with the state-of-the-art in this frequency range, demonstrating that the proposed simple, but effective wideband approach was suitable for 5G applications in the S-band.

Table 1. Comparison of this work with other designs based on the CGH40010F.

Ref.	Freq. (GHz)	Pout (dBm)	DE Sat. (%)	DE OBO (%)	Gain (dB)
[4]	1.7–2.2	42.5	58–72	48–55	8.2–10.2
[9]	2.9–3.3	43.9–44.7	70	40.6–44.2	6–11
[11]	1.4–2.4	41.8–43.5	47.5–64.2	35.5–52	6–13
[12]	2.2–2.6	43–44	60–65	45–53	6–10
[13]	3–3.6	43–44	55–66	38–56	12
[31]	2.2–3	40.2–41.2	52–68	30–53	6–10
[32]	1.5–3.8	42.3–43.4	42–63	33–55	10–13.8
This Work	2.8–3.6	43–44.2	62–76.5	44–56	8–13.5

5. Conclusions

A wideband class AB-C Doherty power amplifier using a 10W GaN HEMT device was presented. By considering the parasitic elements of the transistors and the variations of the transformed impedance at the back-off point, appropriate matching networks were designed to achieve wideband operation from 2.8 GHz to 3.6 GHz. The experimental results showed that an output power above 43 dB was reached together with a drain efficiency in excess of 62% and 44% at saturation and at 6 dB back-off, respectively. The results achieved in this first design were in line with the state-of-the-art. A re-design is on-going pushing toward 4 GHz, in order to better fit the 5G bandwidth. Harmonic tuning strategies are also being considered to further enhance the efficiency-bandwidth trade-off.

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