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TID Circuit Simulation in Nanowire FETs and Nanosheet FETs

Jongwon Lee [1] and Myounggon Kang [1,2,*]

[1] Department of Electronics Engineering, Korea National University of Transportation, Room No.326, Smart ICT Building, 50 Daehak-ro, Chungju-si, Chungbuk 27469, Korea; leejh970@ut.ac.kr
[2] Department of IT·Energy Convergence (BK21 FOUR), Korea National University of Transportation, Room No.326, Smart ICT building, 50 Daehak-ro, Chungju-si, Chungbuk 27469, Korea
* Correspondence: mgkang@ut.ac.kr; Tel.: +82-43-841-5164

Abstract: In this study, the effects of the total ionizing dose (TID) on a nanowire (NW) field-effect transistor (FET) and a nanosheet (NS) FET were analyzed. The devices have Gate-all-around (GAA) structure that are less affected by TID effects because GAA structures have better gate controllability than previously proposed structures, such as planar MOSFETs and FinFETs. However, even for GAA devices with the same channel cross-sectional area and equivalent oxide thickness, structural differences can exist, which can result in different tolerances of TID effects. To observe the device and circuit operation characteristics of these GAA devices with structural differences, n-type and p-type devices were designed and simulated. The circuit simulation according to TID effects was conducted using Berkeley short-channel insulated-gate FET model (BSIM) common multi-gate (CMG) parameters. The NS-FET generated more V_T shift than the NW-FET because the NS-FET had a wider gate oxide area and channel circumference, resulting in more interface hole traps. The abnormal V_T shift leads to causing unstable circuit operation and delays. Therefore, it was confirmed that the ability of the NW-FET to tolerate TID effects was better than that of the NS-FET.

Keywords: total ionizing dose (TID); gate-all-around (GAA); threshold voltage (V_T); circuit simulation; nanowire (NW) FET; nanosheet (NS) FET; inverter

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1. Introduction

Semiconductor devices are widely used in many areas, such as aerospace applications, radiation therapy, and nuclear reactors, where accumulative damage caused by high-energy radiation particles can be a significant threat. High-energy radiation can cause the following phenomena by changing the characteristics of the device, which can interfere with the stable operation of the device: total ionizing dose (TID) effects, displacement damage, and single-event effects [1–4]. In TID effects, when radiation particles pass through the gate dielectric area, electron–hole pairs are generated. Because the mobility of electrons is faster than that of holes, they can exit the area, but some of the holes are trapped at the insulator while moving in the opposite direction to that of the electron by the hopping mechanism. These trapped holes affect the inversion layer charge, generating a threshold voltage (V_T) shift, and the V_T shift decreases the reliability of the operating device [5,6]. For n-type metal-oxide-semiconductor (NMOS) with TID effects, V_T is decreased because of the trapped holes, and this results in more leakage current. For p-type metal-oxide-semiconductor (PMOS), V_T is increased owing to TID effects, and less on current occurs.

To reduce the influence of the short-channel effect (SCE) as the gate length of the device decreases, the structure has been changed so that the gate surrounds the channel to achieve better gate controllability to prevent increasing leakage current or for other reasons, which increases the area of the gate oxide, making it more vulnerable to TID effects [7]. Because the gate oxide becomes thinner, the thickness of the gate oxide can be tunneled by electrons in the channel. To prevent this, a high-k material is used as the gate oxide. This is to maintain the same equivalent oxide thickness and increase the thickness of the

gate oxide [8]. For this reason, the gate oxide area of the gate-all-around (GAA) structure is wider than before, which is necessary to analyze the TID effects.

However, because these radiation-induced phenomena tend to recover slightly within a short time after their occurrence, analysis by measurement has many difficulties [9]. Therefore, the TID effects of the device were analyzed using technology computer-aided design (TCAD) simulation. Because the oxide area of the nanosheet (NS) FET device is wider than that of the nanowire (NW) FET device, there are more hole traps in the NS-FET. However, the oxide area was not the only difference between the devices.

Finally, an inverter SPICE simulation was conducted using device characteristics affected by TID effects owing to the faster operation time of the SPICE simulation. The extraction of TID effects characteristic of irradiated devices was performed using Berkeley short-channel insulated-gate FET model (BSIM) common multi-gate (CMG) parameters.

2. Method of Analyzing TID Effects

In this study, the TID effects between similar GAA structures, the NS-FET, and NW-FET were analyzed. Figure 1 shows the structures designed using TCAD, and Table 1 lists the device design parameters. For an accurate comparison, the channel cross-sectional area was designed in a similar manner. N-type doping of the device was performed using phosphorus, and p-type doping was done with boron. Silicon nitride was used as the spacer between the contacts of the device, and SiO_2 and HfO_2 were used as the gate oxides. Both devices had 0.5-nm-thick SiO_2 and 2-nm-thick HfO_2. The corner of the NS-FET channel was designed in a circular shape with a radius of 1 nm. Owing to the difference in channel shape, the NS-FET had an 8.2-nm-longer channel circumference than the NW-FET.

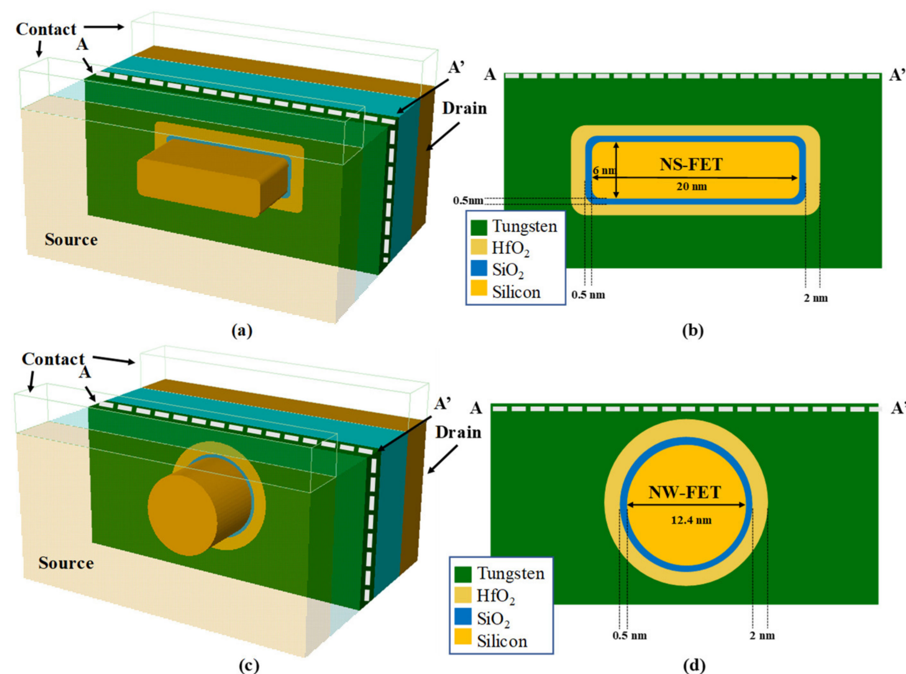

Figure 1. The structures of NS-FET and NW-FET designed by TCAD: (**a**) NS-FET 3D structure; (**b**) the cross section of NS-FET; (**c**) NW-FET 3D structure; (**d**) the cross section of NW-FET.

Table 1. Device design parameters.

Device Parameter	NS-FET	NW-FET
Channel length	5 nm	5 nm
Cross section of oxide area (HfO_2 + SiO_2)	155 nm^2	118 nm^2
Cross section of channel area	119.14 nm^2	120.70 nm^2
Equivalent oxide thickness	0.812 nm	0.812 nm
Circumference of channel	47.14 nm	38.94 nm

For the TID simulation, the Silvaco Victory device was used [10]. In the simulation, radiation stress was applied after the gate and drain voltages were applied to the device. Among the radiation particles, γ-rays of ^{60}Co, which causes large changes in the properties of the device because of its comparatively strong energy between other radiation particles, was used as the radiation source [9]. Various models (trap-detrap, mobility, etc.) were used to improve the accuracy of the simulation [11–14]. After irradiation at 1 rad/s, when the desired amount of radiation stress was applied, the gate voltage was swept to 0 V again. In the study, the TCAD simulation was performed at 100 k, 1 M, 10 M, 100 M rad per each devices, respectively.

3. The Procedure of Parameter Extraction

3.1. Result of TID Effect Simulation

Figure 2 shows the V_T shift for each device as the total radiation dose increased. Both the NMOS and the PMOS graph shifted to the left. This is because V_T decreased in NMOS, but V_T increased in PMOS, resulting in opposite characteristic changes. In the case of NMOS, it was confirmed that V_T decreased, so the on current increased and leakage current increases. In addition, in the case of PMOS, it was confirmed that the on current and leakage current decreased as V_T increased.

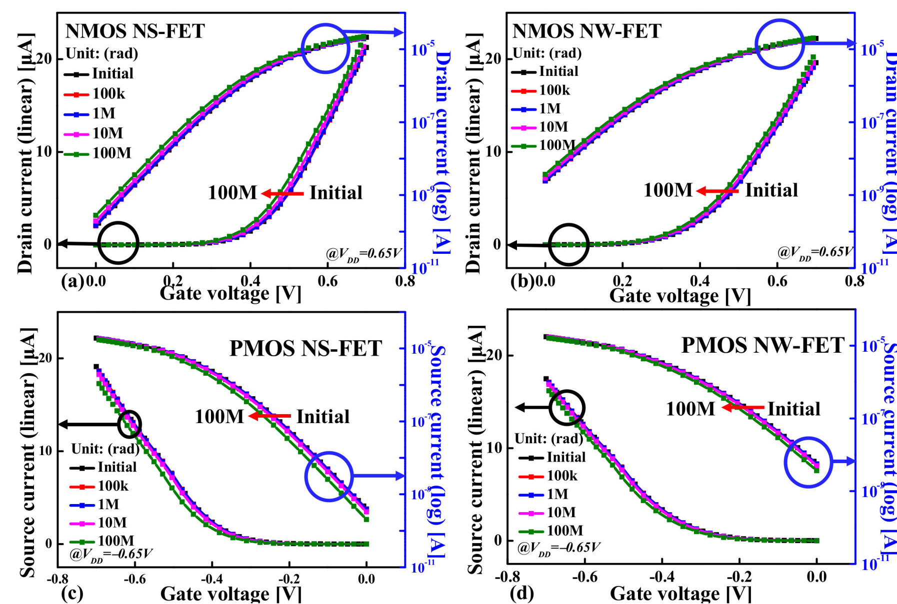

Figure 2. TID simulation I_D–V_G curve of each device: (**a**) NMOS NS-FET; (**b**) NMOS NW-FET; (**c**) PMOS NS-FET; (**d**) PMOS NW-FET.

Figure 3 shows the transconductance for each device as the total radiation dose increased. In the case of NMOS, the transconductance tends to increase as the total dose of radiation increases. On the other hand, a section in which the transfer conductance is seen as a reversal of the tendency is observed at a gate voltage of 0.5 V or more, which is a phenomenon that occurs only in a section in which the transconductance decreases

or the increases are temporarily delayed [15]. It can be seen that the same phenomenon occurred in PMOS as well. In the case of PMOS, as the total radiation dose increased, the transfer conductance tended to decrease, and the period in which the inversion of the trend occurred was also confirmed.

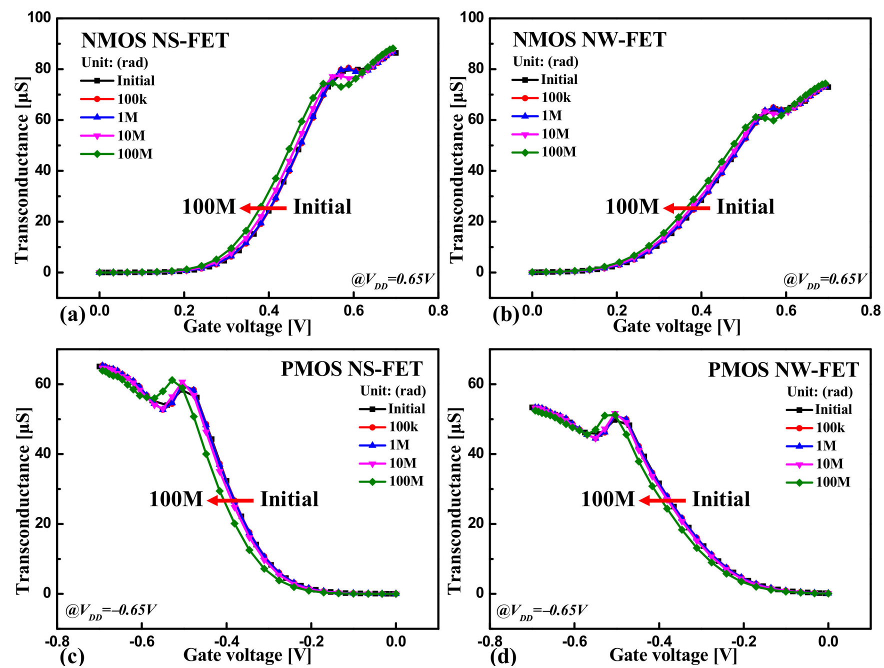

Figure 3. TID simulation transconductance curve of each device: (**a**) NMOS NS-FET; (**b**) NMOS NW-FET; (**c**) PMOS NS-FET; (**d**) PMOS NW-FET.

Table 2 shows the trapped hole densities and hole trap capture rates at the SiO_2 and Si interface. In the NS-FET and NW-FET devices, interface hole traps occurred because of the TID effects. Because of the wider gate oxide of the NS-FET, more hole traps occurred than in the NW-FET. In addition, in the corner region of the NS-FET, on average, more interface hole traps were generated by approximately 30% more than in the flat region. This is because the gate controllability of the corner region of the NS-FET was weaker than that of the flat region owing to the corner effect, making it more vulnerable to TID effects.

Table 2. Hole-trapping characteristics at the SiO_2 and Si interface for the 100 M rad irradiated device: the criterion for measuring the characteristics of NS-FET was at the flat region.

	NMOS NS-FET	NMOS NW-FET
Interface trapped holes	9.02×10^{11} cm^{-2}	8.12×10^{11} cm^{-2}
Trap hole capture rate	6.78×10^{11} cm^{-3}	2.6×10^{11} cm^{-3}

Table 3 shows V_T data of the TID simulation at each total dose rate. Although the numbers of trapped holes per unit area for the two devices are not significantly different, it was confirmed that the more V_T shift at NS-FET. This is not only affected by the total area of the oxide–the circumference of the channel also affected this. The TID effect is a phenomenon that occurs because of the hole trapped in the interface. Even if the trap is the same amount per unit area, the total amount increases in proportion to the channel circumference so that the NS-FET with a wider channel circumference eventually traps more holes.

Table 3. V_T data of TID simulation.

Total Dose Rate	NMOS		PMOS	
	NS-FET	NW-FET	NS-FET	NW-FET
Initial	430 mV	390 mV	400 mV	365 mV
100 k rad	430 mV	390 mV	400 mV	365 mV
1 M rad	429 mV	389 mV	401 mV	365 mV
10 M rad	420 mV	382 mV	407 mV	371 mV
100 M rad	406 mV	370 mV	425 mV	385 mV

Figure 4 shows the shifted VT according to each total dose rate. It has been already known that the VT shifts of PMOS is larger than that of NMOS in planar MOSFET because the gate length is long, and there are many places where trapping can occur in the interface [16,17]. In contrast, the GAA structure has a much shorter channel length and supe-rior gate controllability, with less variation occurring because of TID effects.

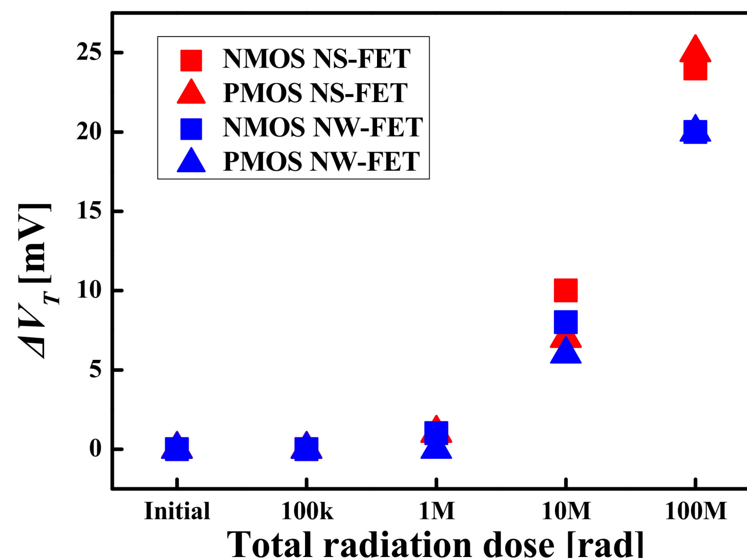

Figure 4. NS-FET and NW-FET V_T shift by TID effects.

3.2. Compact Modeling Using BSIM–CMG Model Parameters

Simulation with TCAD requires an extremely long computation time, so it is difficult to immediately check the simulation results of devices that have changed characteristics (gate length, channel diameter, etc.); however, the SPICE simulation method with the extracted BSIM model parameter can obtain device characteristics faster than TCAD simulation.

The BSIM–CMG model parameters were used instead of various other commercially available BSIM model parameters to extract the device characteristics for TID effects. This is because other models, such as BSIM 4, are based on planar MOSFETs, so it is not easy to adjust a graph between simulation data values and BSIM 4 parameter values in 3D structure devices. Therefore, the BSIM–CMG model parameters were used for consistent fitting.

Figure 5 shows a flow chart of compact modeling considered with TID effects. First, the characteristics of the TID effect simulation data from the TCAD simulation were used for compact modeling. It is similar to an irradiation source, TCAD designs, etc. Next, the BSIM–CMG model parameters with TID effect characteristics were extracted, and the I_D–V_G curve was adjusted between the TCAD simulation data and BSIM–CMG data. The extracted BSIM model parameters include the physical parameters (structure, doping, material, channel length, etc.), linear region fitting parameters (mobility, series resistance, etc.), SCE parameters (drain-induced barrier lowering parameter, gate-induced drain leakage parameter, etc.), temperature, output conductance, etc. With BSIM model

parameters and adjusted data with simulation results, a SPICE circuit simulation can be initiated with a circuit netlist.

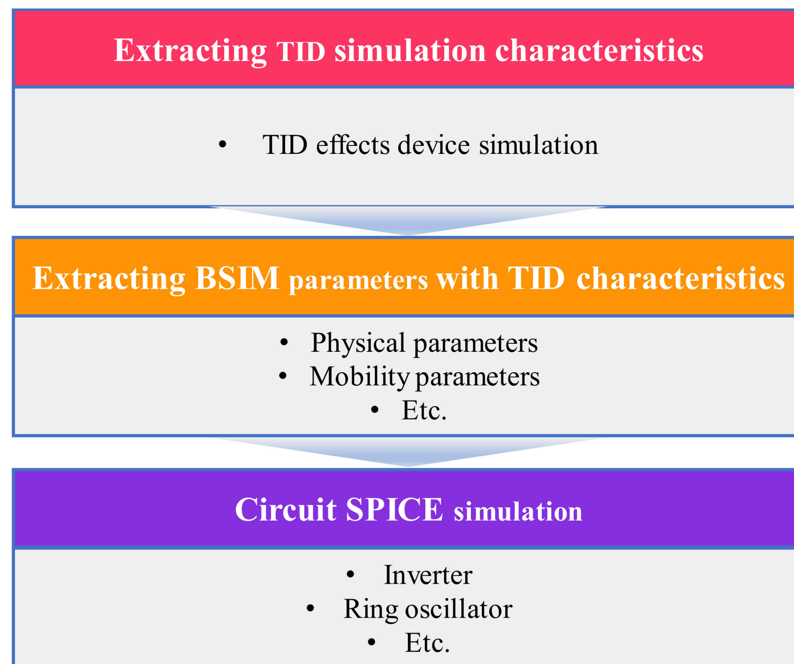

Figure 5. Flowchart of compact modeling according to TID effects.

Figure 6 shows the adjusted I_D–V_G curve between the TCAD simulation data and the BSIM–CMG model parameter data. All TCAD simulation data expressed in Figure 2 were also adjusted using the BSIM–CMG model parameters. This adjustment process must be carried out carefully and consistently because consistency with the simulation data determines the reliability of the circuit simulation.

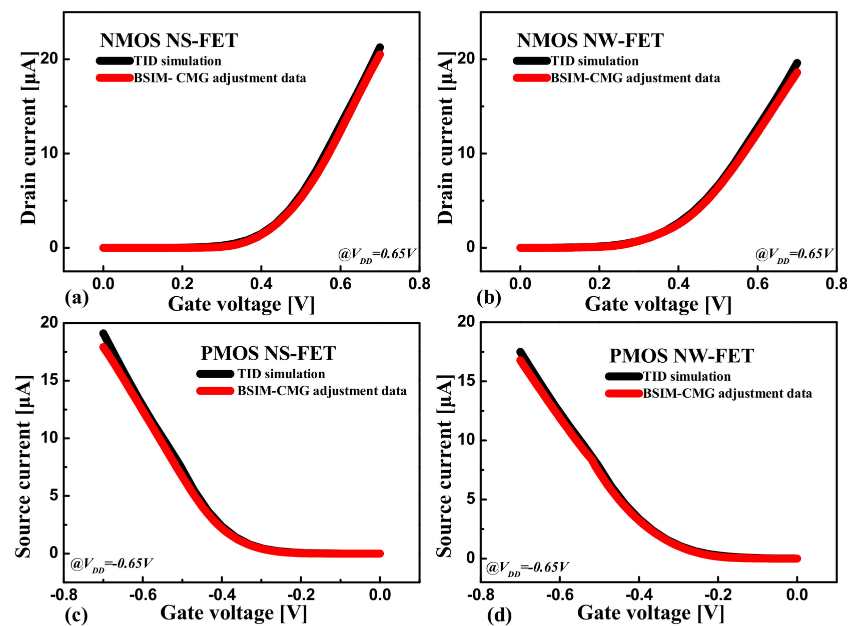

Figure 6. I_D–V_G curve adjustment between TCAD simulation data and BSIM–CMG model parameter data: all curves are nonirradiated device simulation I_D–V_G curves: (**a**) NMOS NS-FET; (**b**) NMOS NW-FET; (**c**) PMOS NS-FET; (**d**) PMOS NW-FET.

4. SPICE Circuit Simulation

Figure 7 shows inverter operation reflecting TID effects. Because the V_T shift occurred, there was a delay in the operation of the inverter circuit [18]. The delay of the rising edge at inverter operation was caused by the V_T shift of the PMOS so that the shifted V_T made the PMOS turn on later in order to start rising later than the nonirradiated device, and the delay of falling edge was caused by the NMOS turning off earlier than the nonirradiated device. Every rising and falling edge delay generated and accumulated after the V_T shift. The more V_T shift that occurred for the NS-FET, the more the delay generated at the NS-FET inverter.

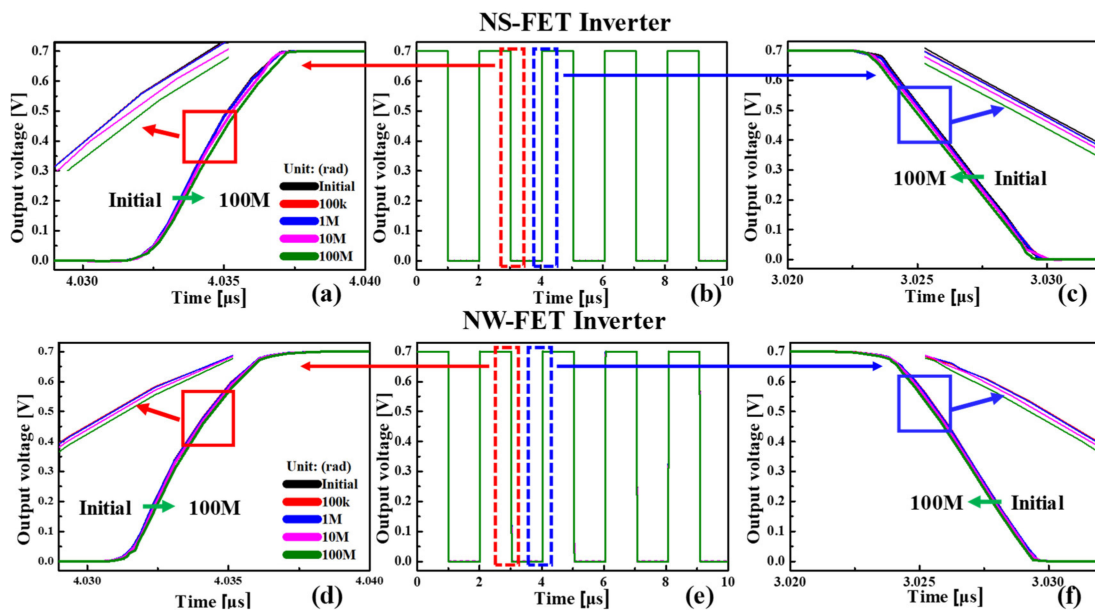

Figure 7. NS-FET and NW-FET inverter operation graph reflecting radiation accumulation: (**a**) NS-FET inverter rising edge; (**b**) inverter output pulse; (**c**) NS-FET inverter falling edge; (**d**) NW-FET inverter rising edge; (**e**) inverter output pulse; (**f**) inverter falling edge; (**a**,**d**) magnified region was at 4.034–4.036 μs; (**c**,**f**) magnified region was at 3.024–3.026 μs.

Figure 8 shows the time delay as a percentage of the inverter operation of NS-FET and NW-FET. The ratio was calculated by extracting the time delay between the device not affected by radiation and the device to be affected at output voltage 0.35 V and dividing it by 10–90% rise time (70 mV–0.63 V) of the device not affected by radiation. Both upsweep and downsweep showed that the delay of the NS-FET was more severe.

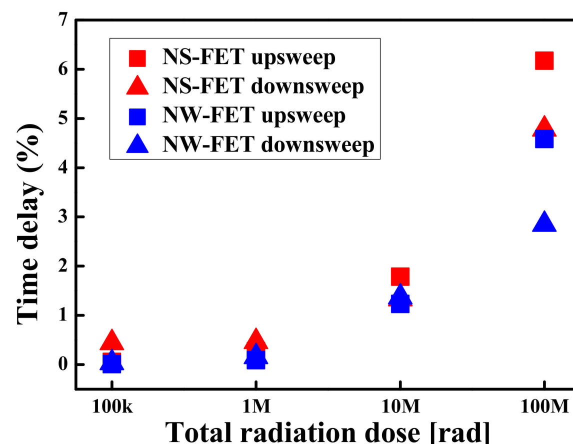

Figure 8. Time delay percentage versus nonirradiated device in upsweep and downsweep during inverter operation of NS-FET and NW-FET.

5. Conclusions

In this study, two different GAA structure devices, NS-FET and NW-FET, were designed and simulated according to the TID effects. The larger number of holes trapped in the NS-FET device was caused by the wider gate oxide area. The channel corners of the NS-FET and channel circumference differences also affected this. Owing to this structural difference, more V_T shift occurred in the NS-FET than in the NW-FET.

The results indicate that it is important to reduce the total oxide area in order to have tolerance of TID effects in the GAA structure, but it is more important to design a device that can reduce the channel circumference or corner effect.

In addition, the BSIM–CMG model parameters were extracted to simulate the inverter circuit with device operation characteristics according to the TID effects. The NS-FET inverter operation had more delay variation than that of the NW-FET inverter because the NW-FET had better tolerance of TID effects, under these assumptions and structural differences, that can reduce V_T shift variation.

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Conflicts of Interest: The authors declare no conflict of interest.

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