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Smooth-Transition Simple Digital PWM Modulator for Four-Switch Buck-Boost Converters

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Abstract: This paper proposes a simple, hardware-efficient digital pulse width modulator for a 4SBB that enables operation in Buck, Boost, and Buck+Boost modes, achieving smooth transitions between the different modes. The proposed modulator is simulated using Simulink and experimentally demonstrated using a 500 W 4SBB converter with 24 V input voltage and 12–36 V output voltage range.

Keywords: four switch non-inverting Buck-Boost; Buck+Boost mode; smooth transition

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1. Introduction

Cascaded Buck-Boost converters are being extensively used in a variety of applications. Two-switch cascaded Buck-Boost converters were first proposed as Power Factor Correction circuits [1]; evolving from this topology, four switch non-inverting Buck-Boost (4SBB) converters have become a preferred choice in non-isolated applications where both voltage step-up and step-down are required. Its applications include space power systems [2], DC microgrids [3], photovoltaic systems [4], and DC power systems [5]. Among other things, this topology features bidirectional power transfer capability, high efficiency, simplicity, and voltage step-up/step-down capabilities. Figure 1 shows a diagram of a conventional 4SBB including a simple digital voltage feedback loop.

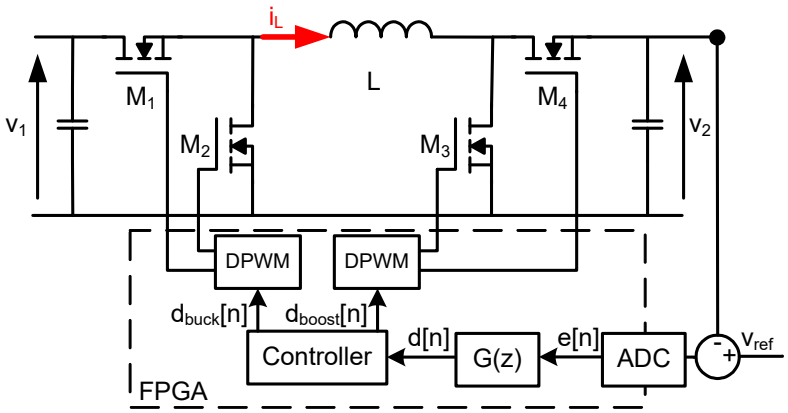


Figure 1. Diagram of a digitally-controlled 4SBB.

Considering v_1 and v_2 as the input and output voltage respectively, it is desirable to operate the 4SBB as a Buck converter when $v_2 < v_1$. This can be simply achieved by turning M_4 on and M_3 off, while switching M_1 and M_2. Conversely, when $v_2 > v_1$, it is desirable to turn on M_1 and turn off M_2, and operate the 4SBB in a Boost-like manner switching

M_3 and M_4. Only one pair of switches operates in each mode, thus minimizing switching losses and enabling high-efficiency operation. Note that this approach requires near-unity conversion ratios when $v_1 \approx v_2$, which are difficult to achieve in practice typically due to pulse-width limitations imposed by driver ICs [6].

Several alternative operating modes have been proposed in the literature to address this issue. In [7] a mixed Buck+Boost mode with all four switches operating at the same time is used to achieve near-unity conversion ratios. In [8] a transition technique is proposed to achieve a full-range, linear conversion ratio using hysteresis methods implemented on a Digital Signal Controller (DSC). However, small discontinuities inherent to this method are perceived in the output voltage. In [9] a DSC is also used to achieve a full-range, continuous conversion ratio using a Buck-Boost operation applying model prediction control. This added complexity limits operation due to long processing times. In [10] a bypass mode is used when $v_1 \approx v_2$, achieving an interesting increase in the efficiency at the cost of losing voltage regulation capabilities. In [11] a different modulation technique, in which the four transistors are switching in the complete operating range, is used to control the converter. A complex transition method based on inductor current sensing is used in [12]. In [13,14] four-mode modulation and duty-locking methods are proposed respectively to operate in the transition region, achieving full-range conversion capabilities. Furthermore, ref. [15] uses a similar four-mode modulation approach, decreasing switching frequency during buck-boost operation to minimize losses.

Although the previously mentioned papers provide different methods for smooth control, little emphasis is placed on the analysis of the transition method and its subsequent implementation on a digital platform, which is the scope of this work.

The operation of the 4SBB converter in Buck+Boost mode used in [7] has proven to be the most adequate approach to achieve simple and efficient near-unity conversion ratios. However, this approach requires generating two distinct duty cycles to control each pair of switches from the control signal d[n]. This paper addresses the issue of adequately generating those signals in the 4SBB converter focusing on the Buck+Boost mode operation and the transitions between modes. In that context, this work proposes a simple Digital Pulse-Width Modulator (DPWM) for a 4SBB converter that automatically enables full-range conversion ratios; the converter operates in the three modes (Buck, Boost, and Buck+Boost) depending on the required conversion ratio, generating the necessary control signals for all switches in each mode and achieving smooth transitions between the different modes. The DPWM is based on a simple state machine that runs on top of two conventional DPWM modulators, each one controlling one pair of switches, M_1/M_2 and M_3/M_4, that can be implemented in an FPGA or ASIC, resulting in a low-resources and easily scalable solution.

The paper is organized as follows: Section 2 describes the operation of the 4SBB converter with near-unity conversion ratios and unveils the problem that arises in such condition; Section 3 describes the operation principles and a simple FPGA-based implementation of the proposed smooth-transition DPWM; Section 4 shows simulation and experimental results; and Section 5 concludes the paper.

2. Operation of the 4SBB Converter

Figure 2a shows an ideal map of the typical operating modes of the 4SBB converter as a function of the control signal d[n] in Figure 1. The conversion ratio M is defined as

$$M = \frac{v_2}{v_1}. \tag{1}$$

When $M < 1$, the 4SBB converter operates as a Buck converter, leaving M_3 off and M_4 on while switching M_1/M_2. In this mode, M_1 is switched on during a fraction of the switching period T_s equal to $T_s \cdot d_{buck}[n]$. When $M > 1$, the 4SBB is operated in Boost mode: M_1 is left on and M_2 is off, while switching M_3/M_4. In this mode M_3 is on during a fraction of the switching period equal to $T_s \cdot d_{boost}[n]$. Figure 3 shows a set of typical operating waveforms in each mode of operation.

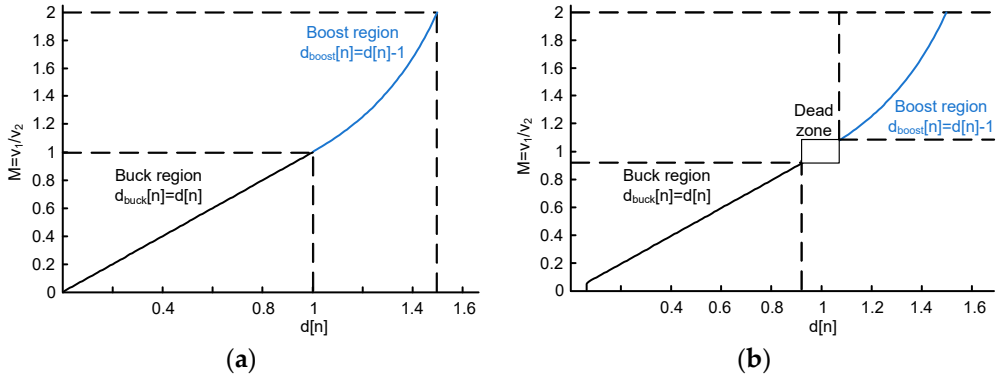


Figure 2. (**a**) Ideal conversion ratio as a function of the duty cycle. (**b**) Dead zones.

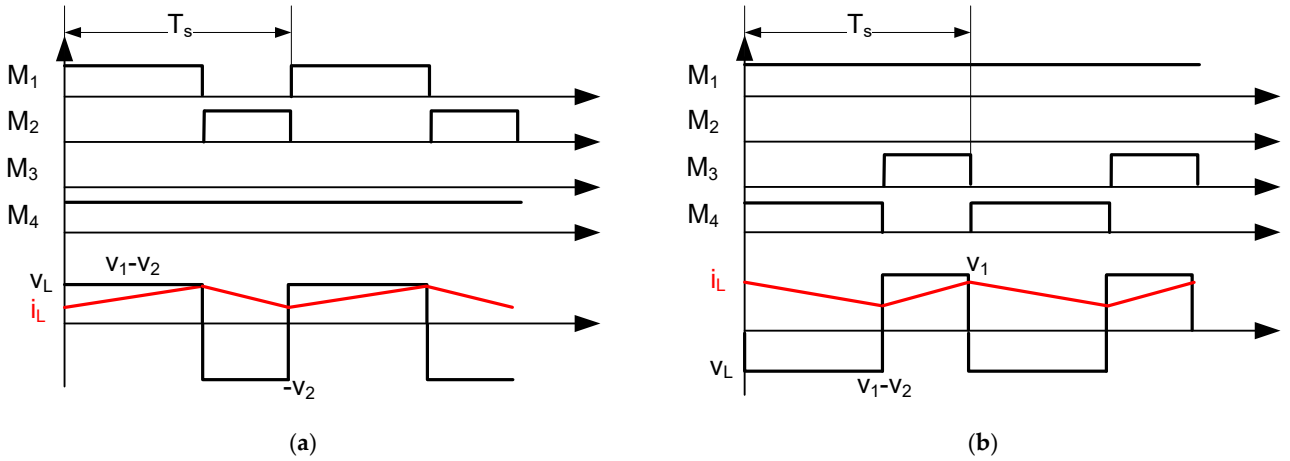


Figure 3. Main operation waveforms of the 4SBB in (**a**) Buck mode; (**b**) Boost mode.

As shown in Figure 1, the control loop produces a unique control signal d[n] from which $d_{buck}[n]$ and $d_{boost}[n]$ need to be obtained. According to previously the described operation, a straightforward mapping to obtain $d_{buck}[n]$ and $d_{boost}[n]$ from d[n] is:

$$\left.\begin{array}{c} d_{buck}[n] = d[n] \\ d_{boost}[n] = 0 \end{array}\right\} \text{ when } d[n] \leq 1 \tag{2}$$

$$\left.\begin{array}{c} d_{buck}[n] = 1 \\ d_{boost}[n] = d[n] - 1 \end{array}\right\} \text{when } d[n] > 1 \tag{3}$$

where $d[n] \in [0,2]$. With this approach $d[n] \leq 1$ indicates Buck operation whereas $d[n] > 1$ indicates Boost operation.

However, this simple mapping is not feasible in practical converters; due to pulse-width limitations imposed by MOSFET driver ICs, an upper limit for $d_{buck}[n]$ ($d_{buck,max}$) as well as a lower limit for $d_{boost}[n]$ ($d_{boost,min}$) exist. Even if very short control pulses could be produced by the drivers, semiconductor devices may not be able to fully switch in such short periods, causing circuit malfunction. Therefore, it is in general desirable to limit the actual operating duty cycles such that $d_{buck}[n] < d_{buck,max}$ and $d_{boost}[n] > d_{boost,min}$. This causes the dead-zone of unachievable conversion ratios shown in Figure 2b, which in turn leads to the modification of (2) and (3) as:

$$\left.\begin{array}{c} d_{buck}[n] = d[n] \\ d_{boost}[n] = 0 \end{array}\right\} \text{ when } d[n] \leq d_{buck,max} \tag{4}$$

$$\left.\begin{array}{c} d_{buck}[n] = f_{buck}(d[n]) \\ d_{boost}[n] = f_{boost}(d[n]) \end{array}\right\} \text{when } d_{buck,max} < d[n] < 1 + d_{boost,min} \text{ (dead zone)} \quad (5)$$

$$\left.\begin{array}{c} d_{buck}[n] = 1 \\ d_{boost}[n] = d[n] - 1 \end{array}\right\} \text{when } d[n] \geq 1 + d_{boost,min} \quad (6)$$

Several representative alternatives proposed in the literature to overcome this problem are briefly described next.

2.1. Bypass and Saturation Modes

A simple solution proposed in [10] is the use of a bypass mode. For the values of d[n] that fall into the dead zone, the input and output voltages are relatively close and, in this mode, the input is directly connected to the output, therefore having $v_2 \approx v_1$. This solution is easily implemented using the following mapping for the dead-zone:

$$\left.\begin{array}{c} d_{buck}[n] = 1 \\ d_{boost}[n] = 0 \end{array}\right\} \text{when } d_{buck,max} < d[n] < 1 + d_{boost,min} \quad (7)$$

A very good efficiency in the dead-zone is obtained using this solution because none of the transistors are switching. The main disadvantage of this technique is the loss of output voltage regulation capabilities.

A similar solution consists in using the saturated values of $d_{buck}[n]$ and $d_{boost}[n]$ when d[n] is in the dead-zone. The corresponding mapping is:

$$\left.\begin{array}{c} d_{buck}[n] = d_{buck,max} \\ d_{boost}[n] = 0 \end{array}\right\} \text{when } d_{buck,max} < d[n] < 1 \quad (8)$$

$$\left.\begin{array}{c} d_{buck}[n] = 1 \\ d_{boost}[n] = d_{boost,min} \end{array}\right\} \text{when } 1 < d[n] < 1 + d_{boost,min} \quad (9)$$

With this technique voltage regulation capabilities are also lost. However, note that in close-loop operation the controller will jump between the nearest allowable duty cycles to, on average, produce the required output voltage. Figure 4 shows the conversion ratio as a function of d[n] with these two alternative solutions.

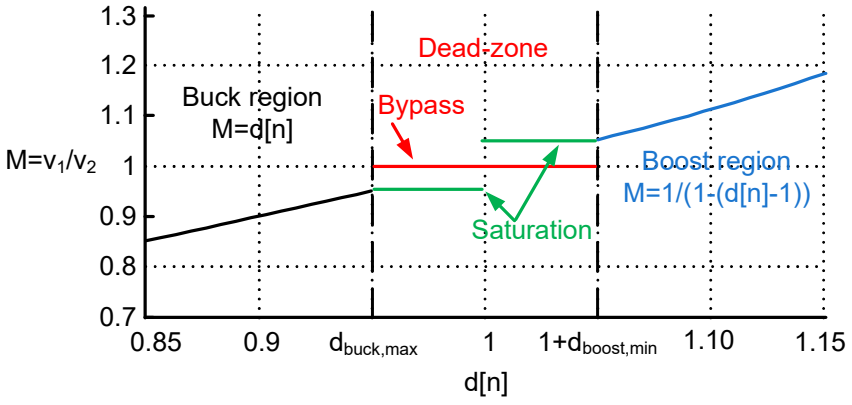


Figure 4. Conversion ratio M as a function of d[n] using the mapping in (7) (bypass) and that is described in (8) and (9) (saturation).

2.2. Buck-Boost Mode

The 4SBB can also be operated as a Buck-Boost converter when $M \approx 1$ [16], which can simply be achieved by setting $d_{buck}[n] = d_{boost}[n]$. Note that in this mode of operation the conversion ratio can be expressed as

$$M = \frac{d_{buck}[n]}{1 - d_{buck}[n]} = \frac{d_{boost}[n]}{1 - d_{boost}[n]}, \quad (10)$$

M = 1 can be achieved by setting $d_{buck} = d_{boost} = 1/2$. Therefore, a simple mapping that fulfills the desired behavior can be defined as:

$$\left.\begin{array}{l} d_{buck}[n] = \frac{d[n]}{2} \\ d_{boost}[n] = \frac{d[n]}{2} \end{array}\right\} \text{ when } d_{buck,max} < d[n] < 1 + d_{boost,min} \tag{11}$$

where the fact that the converter enters Buck-Boost mode when $d[n] \approx 1$ has been used to approximate $d_{buck}[n] = d_{boost}[n] \approx d[n]/2$. With this definition both $d_{buck}[n]$ and $d_{boost}[n]$ can be immediately computed from d[n] at almost no hardware cost. Figure 5 shows the conversion ratio as a function of d[n] with this operating mode.

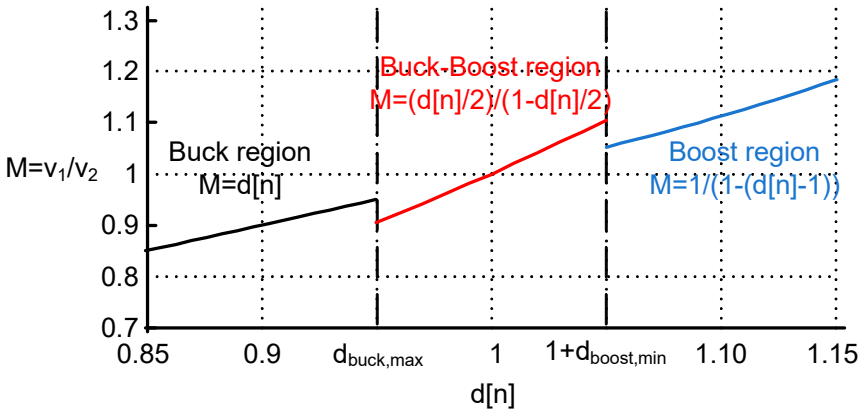


Figure 5. Conversion ratio M as a function of d[n] using the mapping in (11) (Buck-Boost).

However, operation of the 4SBB converter as a true Buck-Boost brings certain drawbacks. First, it may severely increase current stresses in the power stage. Note that the maximum inductor current ripple during Buck operation is

$$\max\{\Delta i_{L,buck}\} = \frac{v_1 d_{buck}[n](1 - d_{buck}[n])T_s}{L} = \frac{V_{in} T_s}{4L} . \tag{12}$$

In the 4SBB operated in true Buck-Boost mode as described above, inductor current ripple is

$$\max\{\Delta i_{L,buck-boost}\} = \frac{v_1 d_{buck-boost}[n] T_s}{L} \approx \frac{V_{in} T_s}{2L} , \tag{13}$$

That is, the inductor current ripple is twice as large as the worst-case Buck mode ripple, and may even exceed rated inductor current ripple for the design, depending on the maximum required step-up ratio. Second, the efficiency of the converter while operating in this mode decreases significantly due to the increased circulating currents.

Also note that when the converter enters Buck-Boost mode the inductor current ripple suffers an abrupt change, from almost zero to a very large value. This sudden change in the converter state variables may pose extra burdens on the control loop and is not desirable. The abrupt state change may also cause stability issues [11].

2.3. Buck+Boost Mode

Figure 6 shows the operating waveforms that correspond to the Buck+Boost operation mode. It consists in operating M_1/M_2 with duty cycle $d_{buck}[n]$, while at the same time M_3/M_4 are operated with duty cycle $d_{boost}[n]$. Using the waveforms of Figure 6, the inductor volt-seconds balance can be found as:

$$v_1 \cdot d_{boost}[n] + (v_1 - v_2) \cdot (d_{buck}[n] - d_{boost}[n]) - v_2 \cdot (1 - d_{buck}[n]) = 0 , \tag{14}$$

resulting in the following conversion ratio:

$$M = \frac{d_{buck}[n]}{1 - d_{boost}[n]}, \tag{15}$$

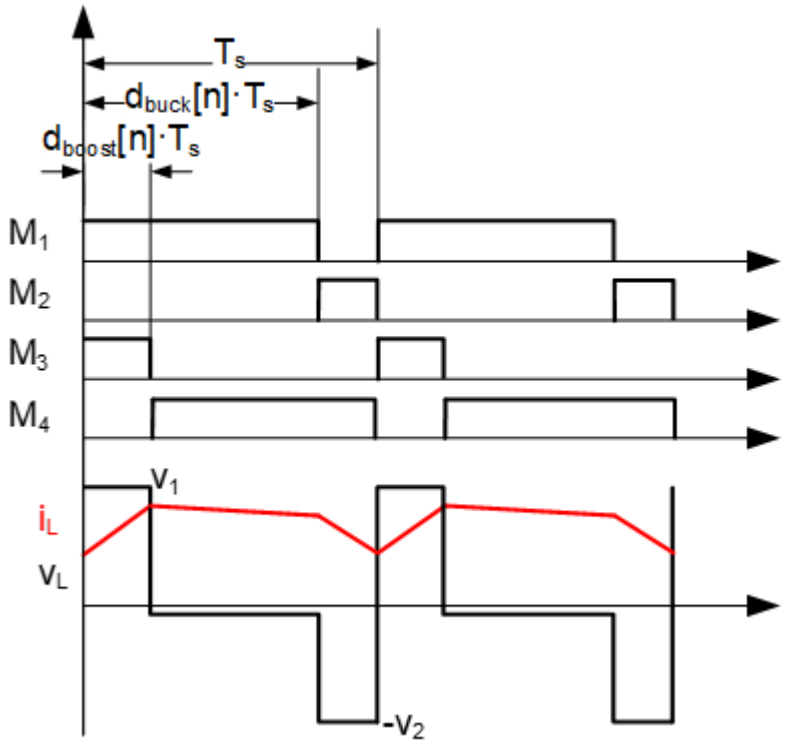


Figure 6. Main operation waveforms of the 4SBB in Buck+Boost mode.

This mode of operation is advantageous as it does not increase inductor current ripple; it also maintains high efficiency operation during the transition and avoids abrupt changes in the inductor current. However, a question arises on how to appropriately obtain $d_{buck}[n]$ and $d_{boost}[n]$ from d[n] given the conditions $d_{buck}[n] < d_{buck,max}$ and $d_{boost}[n] > d_{boost,min}$.

To gain insight into this issue the state of the converter can be plotted in a ($d_{buck}[n]$,$d_{boost}[n]$) plane as shown in Figure 7. Assume that the converter is in Buck mode and d[n] is increasing: the converter then moves along the X axis until it reaches point A at the boundary of the region of unachievable duty cycles. It must then jump to a feasible point B and, after that, move towards D following a certain trajectory (intermediate points C could also be used as it will be shown next). Note that d[n] is being increased throughout the process. Provided that the simple mapping stated in (4) and (6) is maintained, once d[n] reaches $d_{boost,min}$ the converter can safely enter Boost mode where (6) applies and thus move to point E. Note that the selection of points B, C, and D and the trajectory between them determine the evolution of the conversion ratio (M) as a function of d[n]. This issue is addressed in the next section, and it is the main contribution of this work.

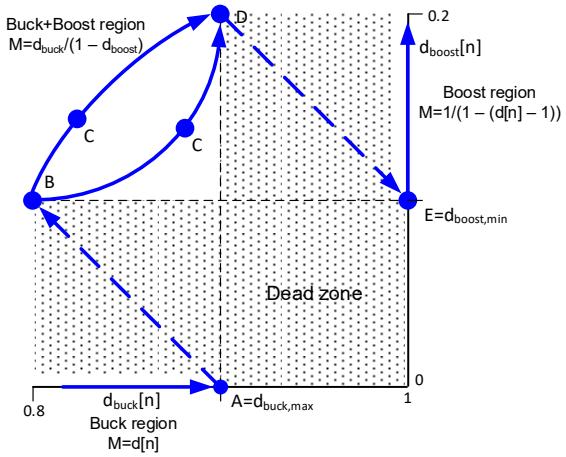
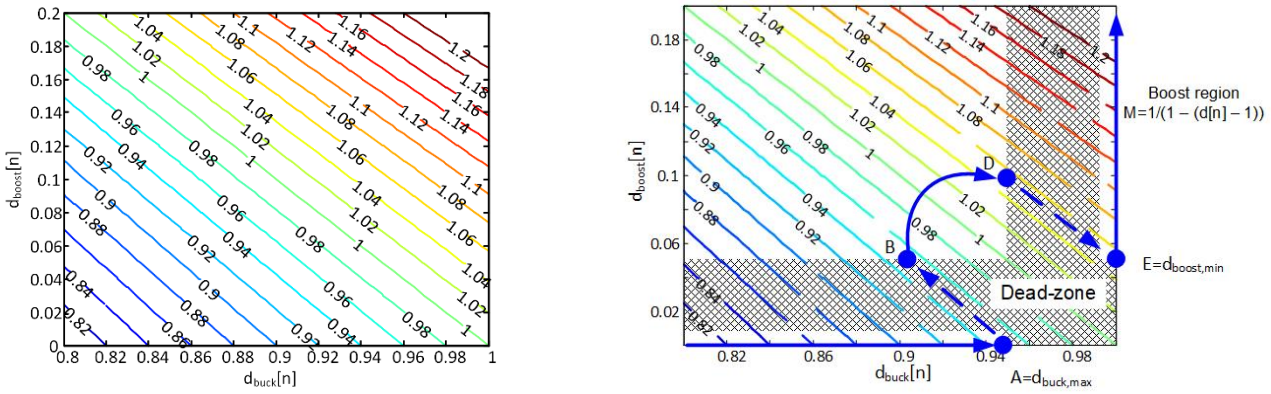


Figure 7. Operation of the 4SBB converter in a (d_{buck}[n],d_{boost}[n]) plain with increasing d[n].

3. Smooth Transition DPWM

In this section a simple method is proposed to achieve a continuous and smooth behavior of the conversion ratio M with respect to d[n]. To find a mapping d[n] → (d_{buck}[n],d_{boost}[n]) that fulfills such requirement, it is useful to examine M in the (d_{buck}[n],d_{boost}[n]) plane. Figure 8a shows contour plots of constant M for different (d_{buck}[n],d_{boost}[n]) pairs. A certain mapping would thus be represented as a trajectory in the (d_{buck}[n],d_{boost}[n]) plane. Assume that the converter is operating in Buck mode, with d_{buck}[n] = d[n] and d_{boost}[n] = 0, and d[n] is increased until it reaches the maximum feasible duty cycle. To ensure continuity in M(d[n]), (d_{buck}[n],d_{boost}[n]) pairs can simply be chosen such that the trajectory moves along a contour of constant M at the transition. Such trajectory is represented in Figure 8b. After moving from B to D, once d[n] reaches $d_{boost,min}$ the converter can move back to Boost mode with d_{boost}[n] = d[n] − 1, d_{buck}[n] = 1. Note that the goal is also to maintain Equations (4) and (6) to mimic the ideal mapping to the largest possible extent.



(**a**) (**b**)

Figure 8. (**a**) Contour plots of constant M for different values of d_{buck}[n] and d_{boost}[n]. (**b**) Possible trajectories to find the appropriate (d_{buck}[n],d_{boost}[n]) pair as a function of d[n] in order to achieve a smooth transition. In this case $d_{buck,max}$ = 0.95, $d_{boost,min}$ = 0.05.

When the converter is in Boost mode, d_{boost}[n] = d[n] − 1 and d_{buck}[n] = 1, and the duty cycle is being decreased, the opposite applies: at the transition point d[n] = $d_{boost,min}$, the converter enters Buck+Boost mode moving along a constant M contour. Such trajectory is the same as the one represented in Figure 2b, but just in the opposite direction. Once d[n] reaches $d_{buck,max}$, the converter can move back to Buck mode with d_{boost}[n] = 0 and d_{buck}[n] = d[n].

3.1. Ideal Smooth Transition DPWM

The conversion ratio as a function of $d_{buck}[n]$ and $d_{boost}[n]$ can be written as:

$$M(d_{buck}[n],\ d_{boost}[n]) = \frac{d_{buck}[n]}{1 - d_{boost}[n]}. \tag{16}$$

Note that (16) is equal to (15) but in this case is used to define the conversion ratio for all modes of operation ($d_{boost}[n] = 0$ in Buck mode, $d_{buck}[n] = 1$ in Boost mode). Moreover, in Buck mode the conversion ratio is:

$$M(d_{buck}[n],\ d_{boost}[n]) = d[n], \tag{17}$$

while in Boost mode the conversion ratio is:

$$M(d_{buck}[n],\ d_{boost}[n]) = \frac{1}{1 - (d[n] - 1)}\ . \tag{18}$$

To mimic the ideal mapping in (2) and (3), the Buck mode conversion ratio (17) is desired when $d[n] < 1$, whereas the Boost mode conversion ratio (18) is desired when $d[n] > 1$. To fulfill these conditions while in Buck+Boost mode (i.e., also fulfilling (16)), ($d_{buck}[n]$,$d_{boost}[n]$) pairs must be appropriately chosen.

To ensure continuity in M(d[n]) during the transition from Buck to Buck+Boost mode, from (16) and (17) the required $d_{buck}[n]$ that guarantees moving along a constant M trajectory in Buck+Boost mode can be found as,

$$d_{buck}[n] = d[n] \cdot (1 - d_{boost}[n]). \tag{19}$$

One possibility to determine ($d_{buck}[n]$,$d_{boost}[n]$) pairs to obtain an ideal transition is to select $d_{boost}[n]$ as $d_{boost,min}$ and calculate $d_{buck}[n]$ using (19) as:

$$d_{buck}[n] = d[n] \cdot (1 - d_{boost,min}). \tag{20}$$

Using this approach, two different but similar trajectories to go from B to D in Figure 7 can be followed. Depending on the values of $d_{buck,max}$ and $d_{boost,min}$ the two possibilities presented in Figure 9 can be considered.

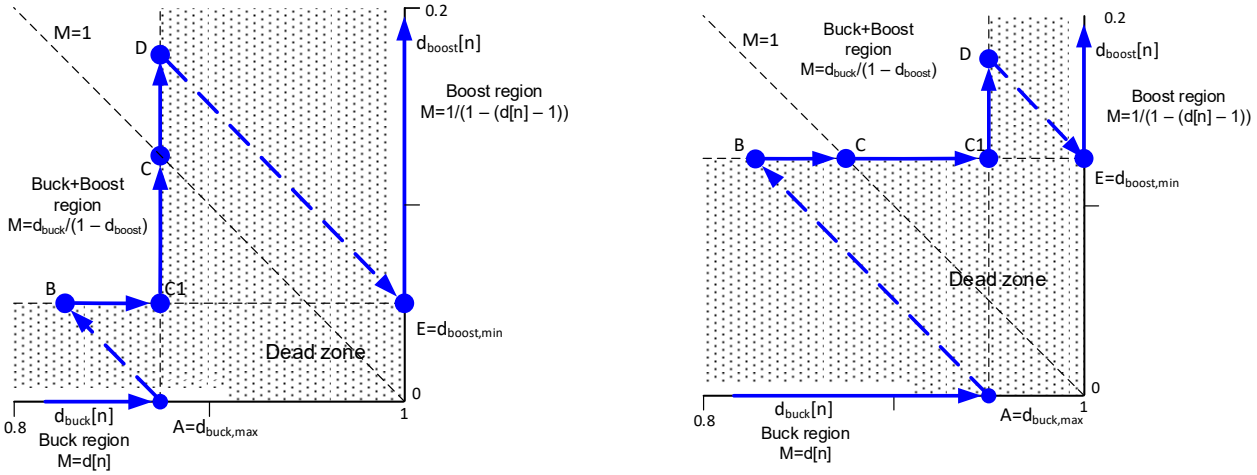


Figure 9. Trajectories defined by ($d_{buck}[n]$,$d_{boost}[n]$) pairs to go from B to D and change from Buck to Boost mode using the Buck+Boost mode. When (**a**) $d_{buck,max} < 1 - d_{boost,min}$ and (**b**) $d_{buck,max} > 1 - d_{boost,min}$.

$d_{buck,max} < 1 - d_{boost,min}$ (Figure 9a): $d_{buck}[n]$ obeys (20) while d[n] is lower than unity (trajectory B-C1). At C1, $d_{buck}[n]$ is fixed as $d_{buck,max}$ and along the trajectory C1-C $d_{boost}[n]$ is calculated using (16) and (17):

$$d_{boost}[n] = 1 - \frac{d_{buck,max}}{d[n]} . \quad (21)$$

When point C is reached (d[n] = 1, M = 1) the trajectory C-D begins. In this case, the conversion ratio of the Boost mode (18) must be followed to ensure continuity in M(d[n]) during the transition between Buck+Boost and Boost mode. Consequently, $d_{boost}[n]$ must be calculated using (16) and (18):

$$d_{boost}[n] = 1 - (1 - (d[n] - 1)) \cdot d_{buck} \quad (22)$$

Again for simplicity, $d_{buck}[n]$ remains fixed as $d_{buck,max}$ and $d_{boost}[n]$ can thus be simplified to:

$$d_{boost}[n] = 1 - (1 - (d[n] - 1)) \cdot d_{buck,max} \quad (23)$$

The previous definitions are summarized in Table 1 and depicted in Figure 3a.

Table 1. Definition of ($d_{buck}[n]$,$d_{boost}[n]$) pairs to go from B to D when $d_{buck,max} < 1 - d_{boost,min}$.

d[n] Ranges	$d_{buck}[n]$	$d_{boost}[n]$	Conversion Ratio (M)	Trajectory
$d[n] < \frac{d_{buck,max}}{1-d_{boost,min}}$	$d[n](1 - d_{boost,min})$	$d_{boost,min}$	d[n]	B-C1
$\frac{d_{buck,max}}{1-d_{boost,min}} < d[n] < 1$	$d_{buck,max}$	$1 - \frac{d_{buck,max}}{d[n]}$	d[n]	C1-C
$d[n] > 1$	$d_{buck,max}$	$1 - (2 - d[n])d_{buck,max}$	$\frac{1}{1-(d[n]-1)}$	C-D

$d_{buck,max} > 1 - d_{boost,min}$ (Figure 9b): from B to C, $d_{boost}[n]$ is fixed as $d_{boost,min}$ and $d_{buck}[n]$ is given by (20) as in the previous case. However, in this case d[n] reaches 1 before $d_{buck}[n]$ (calculated using (20)) reaches $d_{buck,max}$. In this case $d_{buck}[n]$ must be calculated using the conversion ratio of the Boost mode (18) to ensure continuity in M(d[n]) during the transition between Buck+Boost and Boost mode. To follow the trajectory depicted between C and C1 in Figure 9b $d_{boost}[n]$ remains as $d_{boost,min}$ and $d_{buck}[n]$ must be calculated to perform the conversion ratio of the Boost mode (because d[n] > 1) and is given using (16) and (18) as:

$$d_{buck}[n] = \frac{1 - d_{boost,min}}{1 - (d[n] - 1)} . \quad (24)$$

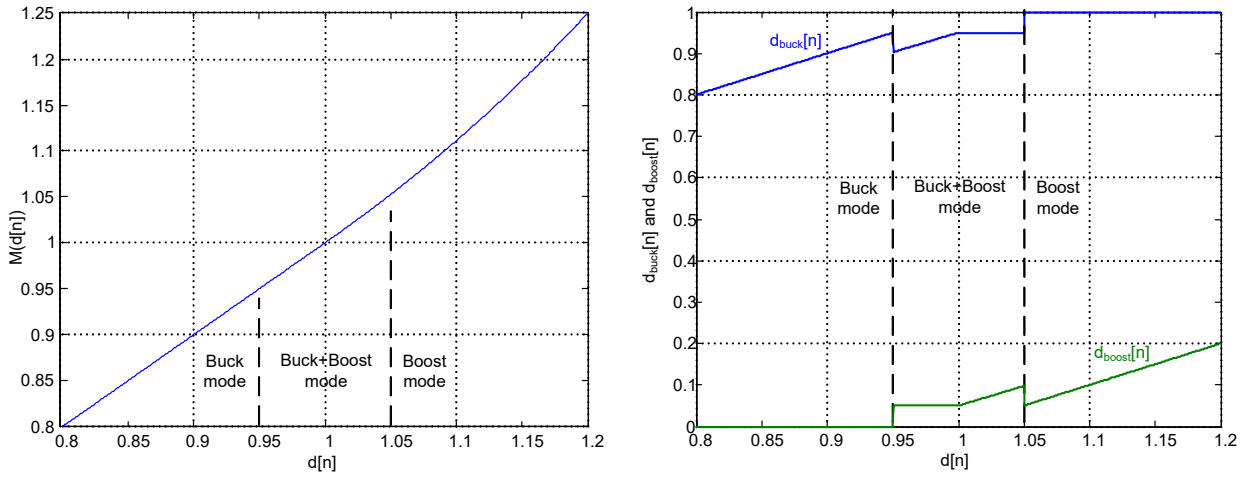
When using (24) $d_{buck}[n]$ reaches $d_{buck,max}$, then $d_{buck}[n]$ is fixed as $d_{buck,max}$ and the trajectory C1-D takes place; $d_{boost}[n]$ is calculated using (23). This possibility is summarized in Table 2 and depicted in Figure 9b.

Table 2. Definition of ($d_{buck}[n]$,$d_{boost}[n]$) pairs to go from B to D when $d_{buck,max} > 1 - d_{boost,min}$.

d[n] Ranges	$d_{buck}[n]$	$d_{boost}[n]$	Conversion Ratio (M)	Trajectory
$d[n] < 1$	$d[n](1 - d_{boost,min})$	$d_{boost,min}$	d[n]	B-C
$1 < d[n] < 2 - \frac{1-d_{boost,min}}{d_{buck,max}}$	$\frac{1-d_{boost,min}}{1-(d[n]-1)}$	$d_{boost,min}$	$\frac{1}{1-(d[n]-1)}$	C-C1
$d[n] > 2 - \frac{1-d_{boost,min}}{d_{buck,max}}$	$d_{buck,max}$	$1 - (2 - d[n])d_{buck,max}$	$\frac{1}{1-(d[n]-1)}$	C1-D

Note that when $d_{buck,max} = 1 - d_{boost,min}$, trajectory C-C1 does not exist and consequently both Figure 9a,b and Tables 1 and 2 are the same.

Figure 10a shows M as d[n] sweeps from 0.8 to 1.2 using the previously defined mapping. Figure 10b shows the values of $d_{buck}[n]$ and $d_{boost}[n]$ selected by the state machine in each operation mode using $d_{buck,max} = 0.95$ and $d_{boost,min} = 0.05$. Note that a perfectly smooth transition is achieved as expected.



(**a**) (**b**)

Figure 10. (**a**) Representation of the conversion ratio M(d[n]). (**b**) (d_{buck}[n],d_{boost}[n]) pairs to obtain a smooth transition between modes.

Note that, although it provides nearly perfect transitions, this ideal mapping requires a significant amount of computational resources. For an FPGA or ASIC implementation, it is desirable to simplify (19), (21), (22), and (24).

3.2. Simplified Smooth Transition DPWM

In order to simplify the computation of d_{buck}[n] and d_{boost}[n], a linearization of the expressions in Tables 1 and 2 is proposed. For simplicity, $d_{buck,max}$ and $1 - d_{boost,min}$ will be assumed to be equal. As has been previously stated, when $d_{buck,max} = 1 - d_{boost,min}$ trajectory C-C1 or C1-C does not exist and the trajectories in Figure 9a,b become the one shown in Figure 11. Considering this simplification only (19) and (22) need to be taken into account.

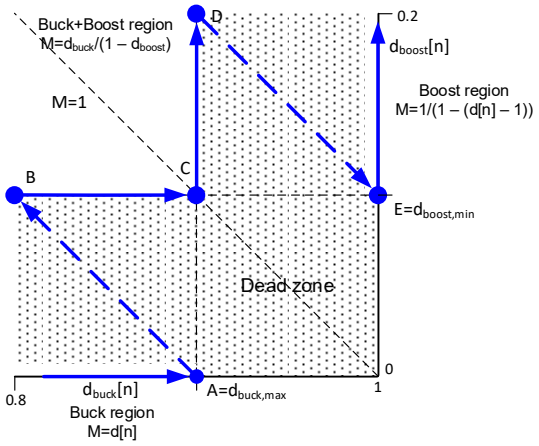


Figure 11. Trajectories defined by (d_{buck}[n],d_{boost}[n]) pairs to go from B to D considering $d_{buck,max}$ = 1–$d_{boost,min}$.

When d[n] = $d_{buck,max}$, the transition from Buck to Buck+Boost mode begins. In this transition, jump from A to B and then trajectory from B to C, d_{boost}[n] is defined as $d_{boost,min}$ and d_{buck}[n] is given by (20); this expression can be approximated by its Taylor series as:

$$d_{buck}[n] = d_{buck}[n]|_B + \frac{\partial d_{buck}[n]}{\partial d[n]}|_B \cdot (d[n] - d[n]|_B), \quad (25)$$

where the values at B are defined as follows:

$$d[n]|_B = d_{buck,max}, \tag{26}$$

$$\begin{aligned} d_{buck}[n]|_B = d_{buck,B} \quad &= d[n]|_B \cdot (1 - d_{boost,min}) \\ &= d_{buck,max} \cdot (1 - d_{boost,min}). \end{aligned} \tag{27}$$

Using (26) and (27) $d_{buck}[n]$ is given by:

$$d_{buck}[n] = d_{buck,B} + (1 - d_{boost,min}) \cdot (d[n] - d_{buck,max}). \tag{28}$$

Finally, to avoid multiplications in (28), $(1 - d_{boost,min})$ is approximated by 1, allowing a simple calculation of the value of $d_{buck}[n]$ as:

$$d_{buck}[n] \approx d_{buck,B} + d[n] - d_{buck,max} = d_{buck,max} \cdot (1 - d_{boost,min}) + d[n] - d_{buck,max}\,. \tag{29}$$

This trajectory ends when $d_{buck}[n]$, calculated using (29), is equal to $d_{buck,max}$ and the point C is reached. To follow the trajectory C–D, $d_{buck}[n]$ is now defined as $d_{buck,max}$ and $d_{boost}[n]$ is given by (22); this expression can be also approximated by its Taylor series as:

$$d_{boost}[n] = d_{boost}[n]|_C + \frac{\partial d_{boost}[n]}{\partial d[n]}|_C \cdot (d[n] - d[n]|_C), \tag{30}$$

where the values at C are defined using (29) as:

$$d[n]|_c = 2d_{buck,max} - d_{buck,max} \cdot (1 - d_{boost,min}), \tag{31}$$

$$d_{boost}[n]|_C = d_{boost,C} = d_{boost,min}. \tag{32}$$

Using (31) and (32) $d_{boost}[n]$ is given by:

$$d_{boost}[n] = d_{boost,C} + d_{buck,max} \cdot (d[n] - 2d_{buck,max} + d_{buck,max} \cdot (1 - d_{boost,min})). \tag{33}$$

Once again, to avoid simplifications in (33), $d_{buck,max}$ is approximated by 1, resulting in:

$$d_{boost}[n] \approx d_{boost,min} + d[n] - 2d_{buck,max} + d_{buck,max} \cdot (1 - d_{boost,min}). \tag{34}$$

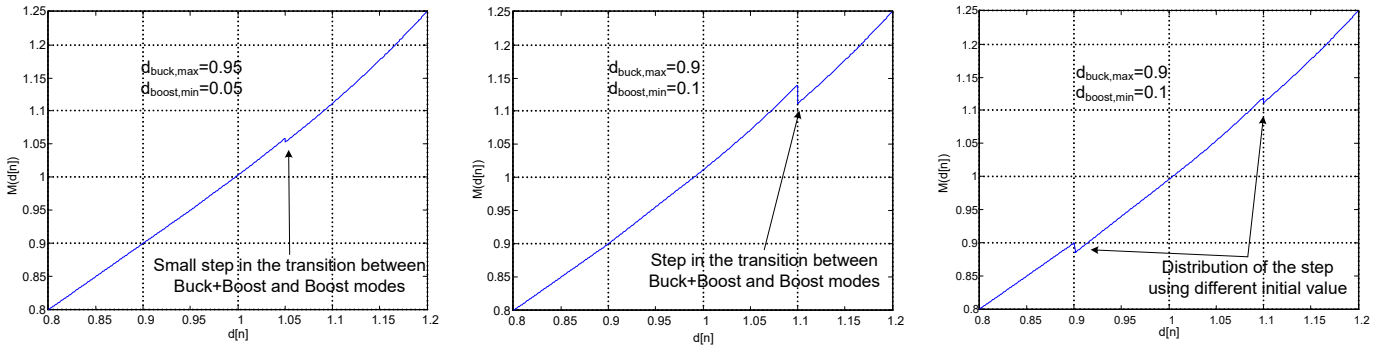
Table 3 summarizes the approximated expressions to calculate ($d_{buck}[n]$,$d_{boost}[n]$) pairs and to obtain the trajectory presented in Figure 11.

Table 3. Definition of ($d_{buck}[n]$,$d_{boost}[n]$) pairs to go from B to D as a function of d[n] using the proposed simplifications. Note that all the expressions are in function of d[n], $d_{buck,max}$, and $d_{boost,min}$ ($d_{buck,B} = d_{buck,max} \cdot (1 - d_{boost,min})$).

d[n]	**$d_{buck}[n]$**	**$d_{boost}[n]$**	**Trajectory**
$d[n] < 2d_{buck,max} - d_{buck,B}$	$d_{buck,B} + d[n] - d_{buck,max}$	$d_{boost,min}$	B–C
$d[n] > 2d_{buck,max} - d_{buck,B}$	$d_{buck,max}$	$d_{boost,\ min} + d[n] - 2d_{buck,max} + d_{buck,B}$	C–D

Using (29) and (34), a simple modulator that chooses adequate ($d_{buck}[n]$,$d_{boost}[n]$) pairs while maintaining quasi-smooth transitions can be implemented. This method reduces the computational requirements and the time required to calculate each duty cycle allowing a very simple and cost-effective FPGA or ASIC implementation.

With the proposed implementation and a proper selection of $d_{buck,B}$, a completely smooth transition can be obtained between Buck and Buck+Boost mode while a small discontinuity appears in the transition between Buck+Boost and Boost mode (see Figure 12a,b). To avoid steps in the transition between Buck and Buck+Boost mode, the point $d_{buck,B}$ has been defined using (27).



(**a**) (**b**) (**c**)

Figure 12. Conversion ratio M(d[n]) using a linear approximation to obtain $d_{buck}[n]$ and $d_{boost}[n]$. (**a**) Small step in one transition using $d_{buck,max}$ = 0.95 and $d_{boost,min}$ = 0.05. (**b**) Higher step using $d_{buck,max}$ = 0.9 and $d_{boost,min}$ = 0.1. (**c**) Distribution of the step in both transitions.

The step in the transition between Buck+Boost and Boost mode is due to the approximations carried out in (29) and (34). Figure 12a shows a representation of M(d[n]) using the proposed implementation in Table 3 and values of $d_{buck,max}$ = 0.95 and $d_{boost,min}$ = 0.05. As can be seen, the step in the transition between Buck+Boost and Boost mode is relatively small. However, for wider ranges of forbidden values of $d_{buck}[n]$ and $d_{boost}[n]$ (wider dead zone) the step can be higher. Figure 12b shows M(d[n]) using the same implementation with values of $d_{buck,max}$ = 0.9 and $d_{boost,min}$ = 0.1. A simple modification is proposed next to reduce the magnitude of the discontinuity.

3.3. Simplified Smooth Transition DPWM with Distributed Conversion Ratio Steps

The discontinuity can be easily distributed between both transitions using a different value for $d_{buck,B}$. The new value that replaces $d_{buck,B}$ is called $d_{buck,B2}$. To determine the value of $d_{buck,B2}$, first the error in the conversion ratio obtained using $d_{buck,B}$, ΔM, is calculated as:

$$\Delta M = M_{buck+boost}|_D - M_{boost}|_E. \tag{35}$$

$$M_{boost}|_E = \frac{1}{1 - d_{boost,\,min}}, \tag{36}$$

$$M_{buck+boost}|_D = \frac{d_{buck,max}}{1 - d_{boost}[n]} = \frac{d_{buck,max}}{-2d_{boost,\,min} + 2d_{buck,max} - d_{buck,B}}, \tag{37}$$

Using (37) the new value ($d_{buck,B2}$) to distribute the step in both transitions can be calculated as:

$$d_{buck,B2} = d_{buck,B} - \Delta M/2. \tag{38}$$

Figure 12c shows the results, where the discontinuity has been evenly distributed between both transitions.

Table 4 shows an estimated error of the different implementations proposed. The Buck-Boost solution presented in Figure 5 and the ideal solution shown in Figure 10 are also shown for reference. This error is calculated using the following expression,

$$\text{error} = \frac{\int \left(M_{ideal}(d[n]) - M_{comp}(d[n])\right)^2}{\int M_{ideal}(d[n])^2} \text{ for } d_{buck,max} < d[n] < 1 + d_{boost,min}, \tag{39}$$

Table 4. Comparison of the conversion ratio obtained with different implementations.

Implementation	Error	Normalized
$d_{buck,max}$ = 0.95, $d_{boost,min}$ = 0.05. One step in the Boost transition	1.04×10^{-5}	4.16
$d_{buck,max}$ = 0.95, $d_{boost,min}$ = 0.05. Two steps distributed	2.50×10^{-6}	1
$d_{buck,max}$ = 0.95, $d_{boost,min}$ = 0.05. Buck-Boost mode.	8.09×10^{-4}	323.6
$d_{buck,max}$ = 0.90, $d_{boost,min}$ = 0.10. One step in the Boost transition	2.13×10^{-4}	4.34
$d_{buck,max}$ = 0.90, $d_{boost,min}$ = 0.10. Two steps distributed	4.90×10^{-5}	1
$d_{buck,max}$ = 0.90, $d_{boost,min}$ =0.10. Buck-Boost mode	3.17×10^{-3}	64.69

$M_{ideal}(d[n])$ being the conversion ratio of the ideal solution and $M_{comp}(d[n])$ the conversion ratio of the implementation under comparison, while d[n] is increased from $d_{buck,max}$ to $1+d_{boost,min}$. Figure 13 shows the different strategies that have been presented in an example with $d_{buck,max}$ = 0.9 and $d_{boost,min}$ = 0.1. From Figure 13 and Table 4, the implementation that distributes the step in both transitions achieves the best results.

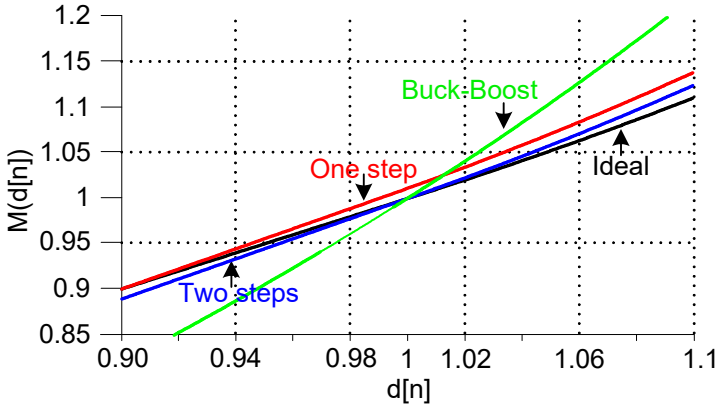


Figure 13. Conversion ratio M(d[n]) in function of d[n] using different implementations in comparison with the ideal.

3.4. Complete Smooth Transition DPWM with Hysteresis and Dead-Times

During practical operation two additional issues arise. First, a hysteresis value (h) needs to be introduced to avoid undesired chattering between modes, in a similar way as in [8]. This value is applied to change from Buck+Boost mode to either Boost or Buck mode.

Second, the use of dead times in each pair of transistors is required. These introduce a slight decrease in the effective duty cycle that in turn causes a decrease in the output voltage and thus in the conversion ratio. In Buck or in Boost mode, only one pair of transistors is switching and thus only its dead time affects the conversion ratio. However, in Buck+Boost mode the four transistors are switching and both dead times contribute to decrease the conversion ratio. This effect can be easily accounted for by adding its value to the calculated duty cycle. Only the effect of the dead time in M_3/M_4 pair of transistors in Buck+Boost mode is corrected. Consequently, the effect of the dead times of only one pair of transistors contributes to decrease the conversion ratio in all the operating modes and thus it does not impact the transition between modes.

Figure 14 and Table 5 show the final DPWM state machine including the hysteresis (h) and the correction of dead time (dt_{boost}) effect in M_3/M_4.

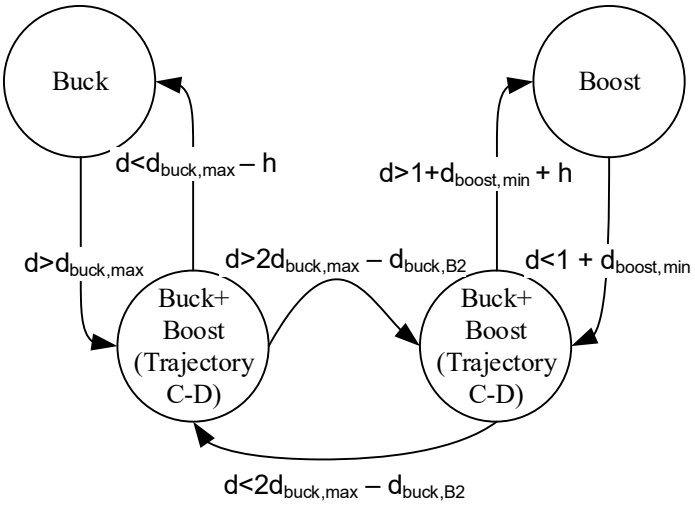


Figure 14. State machine including the hysteresis (h) and the correction of the dead times (dt_{boost} is the dead time used in M3/M4 pair).

Table 5. Definition of ($d_{buck}[n]$,$d_{boost}[n]$) pairs.

Mode	Output
Buck	$d_{buck}[n] = d[n]$ $d_{boost}[n] = 0$
Buck+Boost (Trajectory B-C)	$d_{buck}[n] = d_{buck,B2} + d[n] - d_{buck,max}$ $d_{boost}[n] = d_{boost,min} + dt_{boost}$
Buck+Boost (Trajectory C–D)	$d_{buck}[n] = d_{buck,max}$ $d_{boost}[n] = d_{boost,min} + d[n] - d_{buck,max} + d_{buck,B2} + dt_{boost}$
Boost	$d_{buck}[n] = 1$ $d_{boost}[n] = d[n] - 1$

4. Results and Discussion

The operation of the 4SBB with the proposed modulator has been simulated using Simulink-MATLAB® and the Simpower toolbox. The parameters presented in Table 6 have been used both in simulation and during the experiments.

Table 6. Specifications of 4SBB to obtain simulation and experimental results.

Input voltage:	$v_1 = 24$ V
Output voltage:	$v_2 = 12$–36 V
Maximum power:	$P_{max} = 500$ W
Switching frequency:	$f_{sw} = 100$ kHz
MOSFETs:	IRFB4310Z
Inductance value:	$L = 8$ µH
Output capacitance:	$C_2 = 470$ µF
Maximum duty cycle:	$d_{buck,max} = 0.90$
Minimum duty cycle:	$d_{boost,min} = 0.10$
Dead times:	$dt_{boost} = 0.01$
Hysteresis:	$h = 0.02$

To validate the proposed approach the control variable d[n] is swept from 0.8 to 1.2. The signals $d_{buck}[n]$ and $d_{boost}[n]$ produced by the state machine are fed to two conventional DPWMs that generate the gate signals for M_1/M_2 and M_3/M_4.

Figure 15 shows the simulated output voltage obtained during the sweep for the approaches described in Section 2.1 as a reference. Note that the case where there are no limits for $d_{buck}[n]$ and $d_{boost}[n]$ produces an almost perfectly smooth transition as

expected. The waveform corresponding to the bypass mode using $d_{buck,max} = 0.90$ and $d_{boost,min} = 0.10$, and the waveform corresponding to the mapping $d_{buck}[n] = d_{buck,max}$ when $d_{buck,max} < d[n] < 1$ and $d_{boost}[n] = d_{boost,min}$ when $1 < d[n] < 1 + d_{boost,min}$ are also shown.

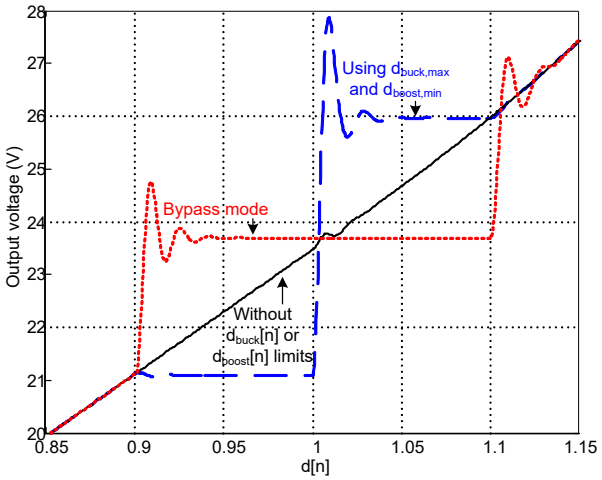


Figure 15. Simulated output voltage considering $d_{buck,max} = 1$ and $d_{boost,min} = 0$ (continuous line). Simulated output voltage for $d_{buck,max} = 0.90$ and $d_{boost,min} = 0.10$, using two simple solutions to determine $d_{buck}[n]$ and $d_{boost}[n]$. Solutions presented in Section 2.1 (dashed and dotted lines).

Figure 16 shows the simulated output voltage for different implementations of the proposed method. The dashed waveform corresponds to the ideal implementation detailed in Tables 1 and 2, without dead-time correction. The continuous waveform shows the ideal implementation with dead-time correction. Finally, the dashed and dotted waveform corresponds to the proposed simple DPWM (Table 3) using $d_{buck,B2}$, whereas the dotted uses $d_{buck,B}$.

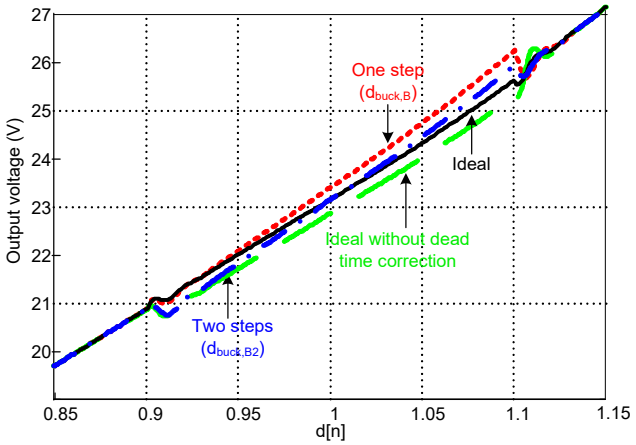


Figure 16. Comparison between the output voltage simulation obtained using the different presented implementations of the state machine to define $d_{buck}[n]$ and $d_{boost}[n]$ depending on the operation mode.

A 4SBB prototype was used to experimentally test the proposed approach. An FPGA Virtex 4 SX35 from Xilinx [17] has been used to implement the control modulator of the prototype. Figure 17 shows a picture of the prototype.

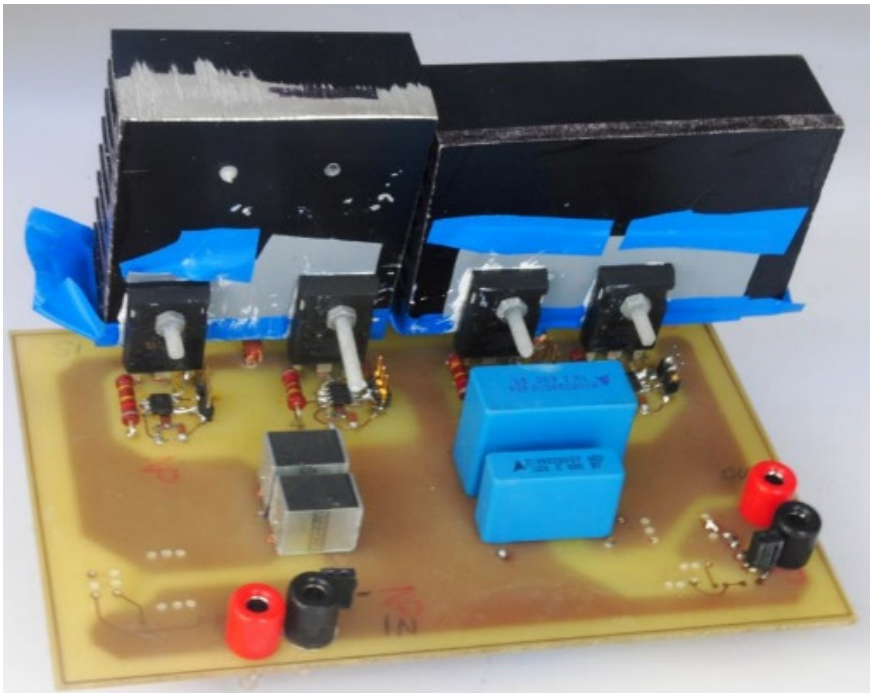


Figure 17. Picture of the 4SBB prototype.

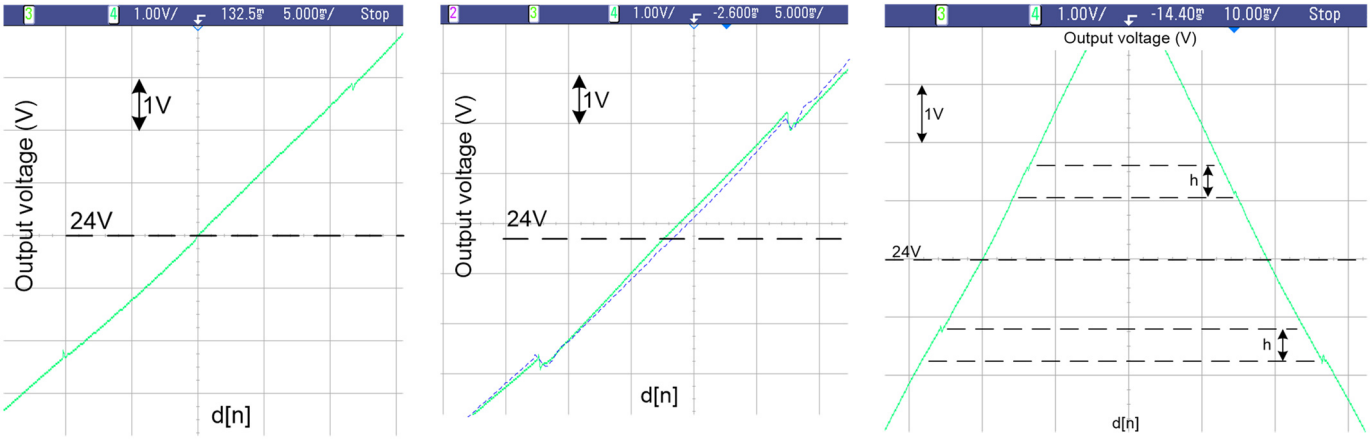
As in the simulation results, a variable duty cycle is generated by the FPGA with the same values (d[n] from 0.8 to 1.2). This signal is used by the proposed modulator to generate the two duty cycles (d_{buck}[n],d_{boost}[n]). Finally, a DPWM modulator generates the complementary control signals of each MOSFET.

The different alternatives mentioned before were synthesized, yielding a resource usage shown in Table 7(prior to synthesizer optimization). As can be seen, the main difference is the required multipliers in the case of the ideal modulator as has been previously detailed.

Table 7. Resources used in the FPGA for the different modulators.

Modulator	Finite State Machine	D-Type Flip-Flop	Adder/Subtractor	Multiplier	Comparator
Ideal	1	73	5	2	5
Simplified	1	73	9	0	5

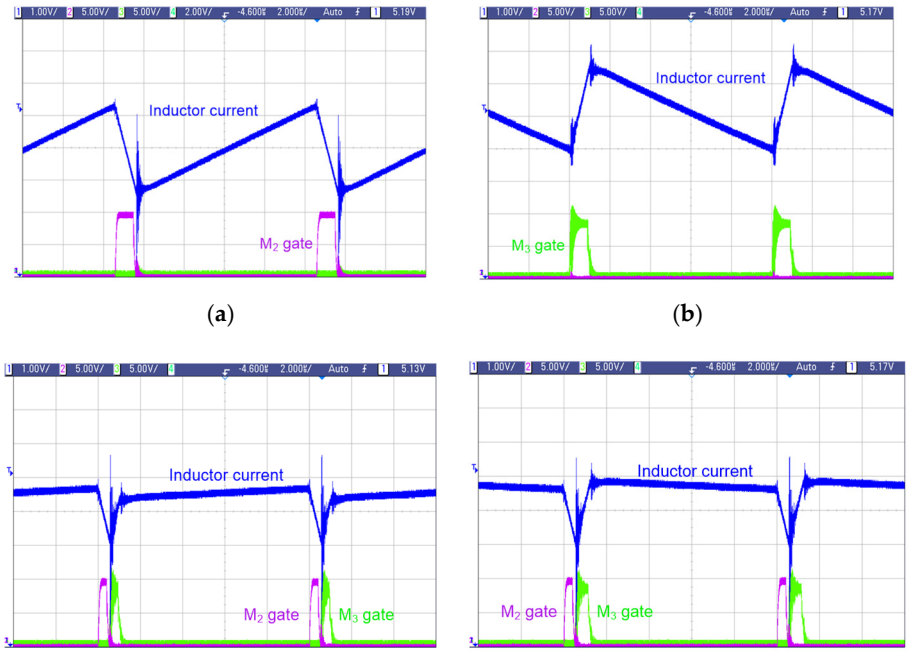
Figure 18 shows the output voltage of the 4SBB using the presented implementations of the proposed control modulator. Figure 18a the ideal implementation presented in Table 2 is used. As can be seen the output voltage shows no discontinuities, achieving an almost perfect transition. Figure 18b shows the output voltage obtained using the proposed simplified method (Table 5); over imposed is the simulation result, showing good agreement. A slight step in the transitions can be appreciated. Figure 18c shows the output voltage using a narrower dead-zone ($d_{buck,max}$ = 0.95 and $d_{boost,min}$ = 0.05), where the discontinuity is almost non-existent, and the effects of the hysteresis are highlighted (also Table 5 is used).



(**a**) (**b**) (**c**)

Figure 18. Experimental results. (**a**) Using the ideal implementation (Table 2). (**b**) Using the proposed simplified method (Table 5) with $d_{buck,max}$ = 0.9 and $d_{boost,min}$ = 0.1. (**c**) Using $d_{buck,max}$ = 0.95 and $d_{boost,min}$ = 0.05 and showing the hysteresis effect.

Finally, the main operation waveforms in each operation mode are shown in Figure 19. As can be seen, the inductor current ripple in Buck+Boost mode is small as expected.



(**a**) (**b**)

(**c**) (**d**)

Figure 19. Main operation waveforms in each operation mode. (**a**) Buck mode (d[n] = 0.90), (**b**) Boost mode (d[n] = 1.10) (**c**) Buck+Boost mode (d[n] = 0.98), and (**d**) Buck+Boost mode (d[n] = 1.02.

A qualitative analysis has been made, testing and comparing this implementation against some of the main referenced methods. The results are listed in Table 8. Apart from overall efficiency and output voltage regulation, other aspects that evaluate their universal applicability have been taken into account. They are computational cost, complexity of the implementation, and scalability.

Table 8. Performance comparison.

Mode	Efficiency	Output Voltage Regulation	Computational Cost	Complexity	Scalability
Pass-through [10]	High	Low	Low	Low	High
One-mode modulation [13]	Low	High	Medium	Low	High
Duty-locking [7]	Medium	Medium	Medium	Medium	Medium
Hysteretic control [8]	Medium	Medium	Medium	Medium	Medium
Model-predictive control [9]	Medium	Medium	High	High	Low
This work	Medium	Medium	Low	Medium	High

From these results, it can be seen that [10] gives the highest efficiency and lowest complexity in general, but the output voltage is not regulated when input and output voltages are similar. Furthermore, [13] sacrifices efficiency for ease of implementation, while [7] and [8] constitute a good compromise between complexity and efficiency. It can be observed that [9] provides a similar result and uses a novel implementation, but its computational cost is way higher than the other options. Our work, on the other hand, while providing similar results, takes computational cost to a minimum and it is more scalable than the other options.

5. Conclusions

Four-switch Buck-Boost converters are widely used in many applications where voltage step up and down capabilities are required; however, near-unity conversion ratios are difficult to achieve due to limitations introduced by driver ICs.

In this work a simple digital pulse-width modulator for 4SBB converters that automatically produces adequate control signals to achieve full-range conversion ratios has been proposed. The modulator enables operation in Buck, Boost and Buck+Boost modes, ensuring high efficiency and guaranteeing relatively smooth transitions between the different modes. A light-resource hardware implementation, FPGA-based, composed of a simple state-machine and two conventional pulse-width modulators is proposed. This way, scalability and adaptability to the different applications is enabled. The proposed solution also addresses non-idealities such as dead-times or hysteresis; its feasibility has been demonstrated through simulations and experiments, achieving full-range conversion ratio and smooth transitions in a 500 W 4SBB converter with 24 V input and 12–36 V output voltage range. However, it should be noted that the proposed DPWM solution still has room for improvement, mainly in the minimization of the step that appears due to the simplification of the duty cycles, but also it would be interesting to study the performance in other aspects, such as increasing switching frequency operation or voltage ripple reduction.

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Abbreviations

The following abbreviations are used in this manuscript

PWM	Pulse Width Modulation
4SBB	4-Switch Buck-Boost
DC	Direct Current
ADC	Analog to Digital Converter
DSC	Digital Signal Controller
DPWM	Digital Pulse Width Modulation
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
ASIC	Application Specific Integrated Circuit

References

1. Ghanem, M.C.; Al-Haddad, K.; Roy, G. A New Single Phase Buck-Boost Converter with Unity Power Factor. In Proceedings of the Conference Record of the 1993 IEEE Industry Applications Conference Twenty-Eighth IAS Annual Meeting, Toronto, ON, Canada, 2–8 October 1993; pp. 785–792.
2. D'Antonio, M.; Shi, C.; Wu, B.; Khaligh, A. Design and Optimization of a Solar Power Conversion System for Space Applications. *IEEE Trans. Ind. Appl.* **2019**, *55*, 2310–2319. [CrossRef]
3. Ramos-Paja, C.A.; Bastidas-Rodríguez, J.D.; González, D.; Acevedo, S.; Peláez-Restrepo, J. Design and Control of a Buck–Boost Charger-Discharger for DC-Bus Regulation in Microgrids. *Energies* **2017**, *10*, 1847. [CrossRef]
4. Chen, C.-W.; Chen, K.-H.; Chen, Y.-M. Modeling and Controller Design for a Four-Switch Buck-Boost Converter in Distributed Maximum Power Point Tracking PV System Applications. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 1663–1668.
5. Thi Kim Nga, T.; Park, S.-M.; Park, Y.-J.; Park, S.-H.; Kim, S.; Van Cong Thuong, T.; Lee, M.; Hwang, K.; Yang, Y.; Lee, K.-Y. A Wide Input Range Buck-Boost DC–DC Converter Using Hysteresis Triple-Mode Control Technique with Peak Efficiency of 94.8% for RF Energy Harvesting Applications. *Energies* **2018**, *11*, 1618. [CrossRef]
6. Ma, J.; Zhu, M.; Zhang, J.; Cai, X. Improved Asynchronous Voltage Regulation Strategy of Non-Inverting Buck-Boost Converter for Renewable Energy Integration. In Proceedings of the 2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC), Taipei, Taiwan, 1–4 November 2015; pp. 1–5.
7. Tsai, Y.-Y.; Tsai, Y.-S.; Tsai, C.-W.; Tsai, C.-H. Digital Noninverting-Buck–Boost Converter With Enhanced Duty-Cycle-Overlap Control. *IEEE Trans. Circuits Syst. II* **2017**, *64*, 41–45. [CrossRef]
8. Restrepo, C.; Konjedic, T.; Calvente, J.; Giral, R. Hysteretic Transition Method for Avoiding the Dead-Zone Effect and Subharmonics in a Noninverting Buck–Boost Converter. *IEEE Trans. Power Electron.* **2015**, *30*, 3418–3430. [CrossRef]
9. Li, X.; Liu, Y.; Xue, Y. Four-Switch Buck–Boost Converter Based on Model Predictive Control With Smooth Mode Transition Capability. *IEEE Trans. Ind. Electron.* **2021**, *68*, 9058–9069. [CrossRef]
10. Callegaro, L.; Ciobotaru, M.; Fletcher, J.E. An Intelligent Pass-Through Algorithm for Non-Inverting Buck-Boost Solar Power Optimizers. In Proceedings of the 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 3–5 September 2019; pp. P.1–P.10.
11. Waffler, S.; Kolar, J.W. A Novel Low-Loss Modulation Strategy for High-Power Bidirectional Buck–Boost Converters. *IEEE Trans. Power Electron.* **2009**, *24*, 1589–1599. [CrossRef]
12. Moon, J.; Lee, J.; Kim, S.; Ryu, G.; Hong, J.-P.; Lee, J.; Jin, H.; Roh, J. 60-V Non-Inverting Four-Mode Buck–Boost Converter With Bootstrap Sharing for Non-Switching Power Transistors. *IEEE Access* **2020**, *8*, 208221–208231. [CrossRef]
13. Zhang, N.; Zhang, G.; See, K.W. Systematic Derivation of Dead-Zone Elimination Strategies for the Noninverting Synchronous Buck–Boost Converter. *IEEE Trans. Power Electron.* **2018**, *33*, 3497–3508. [CrossRef]
14. Tsai, C.-H.; Tsai, Y.-S.; Liu, H.-C. A Stable Mode-Transition Technique for a Digitally Controlled Non-Inverting Buck–Boost DC–DC Converter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 475–483. [CrossRef]
15. Akhilesh, K.; Lakshminarasamma, N. Dead-Zone Free Control Scheme for H-Bridge Buck–Boost Converter. *IEEE Trans. Ind. Appl.* **2020**, *56*, 6619–6629. [CrossRef]
16. Ma, J.; Zhu, M.; Li, X.; Cai, X. Bumpless Transfer of Non-Inverting Buck Boost Converter among Multiple Working Modes. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 1909–1914.
17. Xilinx, Inc. Virtex-4 Family Overview. Available online: https://www.xilinx.com/support/documentation/data_sheets/ds112.pdf (accessed on 20 December 2021).