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Modeling and Fabrication of a Reconfigurable RF Output Stage for Nanosatellite Communication Subsystems

Jose L. Alvarez-Flores [1,2,*], Jorge Flores-Troncoso [1,*], Leonel Soriano-Equigua [2], Jorge Simón [3], Joel A. Castillo [1], Ramón Parra-Michel [4] and Viktor I. Rodriguez-Abdala [1]

[1] Engineering and Applied Technology, Autonomous University of Zacatecas, Zacatecas 98000, Mexico; 26701212@uaz.edu.mx (J.A.C.); abdala@uaz.edu.mx (V.I.R.-A.)
[2] Mechanical and Electrical Engineering Faculty, Universidad de Colima, Colima 28040, Mexico; lsoriano@ucol.mx
[3] Catedras CONACYT, Autonomous University of Zacatecas, Zacatecas 98000, Mexico; jsimonro@conacyt.mx
[4] CINVESTAV-IPN, CINVESTAV Guadalajara, Jalisco 45019, Mexico; ramon.parra@cinvestav.mx
* Correspondence: alvarez_jose@ucol.mx (J.L.A.-F.); jflorest@uaz.edu.mx (J.F.-T.); Tel.: +52-1312-115-2840 (J.L.A.-F.); +52-1492-144-7802 (J.F.-T.)

Abstract: Current small satellite platforms such as CubeSats require robust and versatile communication subsystems that allow the reconfiguration of the critical operating parameters such as carrier frequency, transmission power, bandwidth, or filter roll-off factor. A reconfigurable Analog Back-End for the space segment of a satellite communication subsystem is presented in this work. This prototype is implemented on a 9.5 cm^2 6-layer PCB, and it operates from 0.070 to 6 GHz and complies with CubeSat and IPC-2221 standards. The processing, control, and synchronizing stages are carried out on a Software-Defined Radio approach executed on a baseband processor. Results showed that the signal power at the output of the proposed Analog Back-End is suitable for feeding the following antenna subsystem. Furthermore, the emitted radiation levels by the transmission lines do not generate electromagnetic interference.

Keywords: radiofrequency; analog back-end; FPGA; CubeSat; transceiver

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1. Introduction

Applying the new electronic communication technologies to spatial missions either for remote observation or surface exploration of the earth or other astronomical bodies promises the improvement of sustainability, robustness, and truthfulness of the current missions when sharing spatial resources [1]. This new paradigm requires diverse technologies to achieve a flexible reconfiguration capability between heterogeneous satellites.

The trend in electronic design is governed by Moore's Law, which establishes capacities of the General Purpose Processors (GPPs), Digital Signal Processors (DSPs), and Field Programmable Gate Arrays (FPGAs) [2]. As a result, the processing flow of radio signals—traditionally made with specialized hardware blocks—can be defined and controlled by software known as Software-Defined Radio (SDR). The embedded SDR technique used on a System on a Chip (SoC) turns out to be suitable to implement flexible, adaptable, and reconfigurable satellite communication systems and eliminates the need to implement hardware for each application. Furthermore, this technique allows reducing development time, costs, and system mass.

Several examples of embedded SDR on an SoC for satellite applications are found in the literature. In [3], to integrate a launchable network based on Commercial-Off-The-Shelf (COTS) components and for emulating a network of federated satellites, a system based on a commercial BladeRFx115® is presented. It works with an LMS6002D Integrated Circuit (IC) from 0.30 to 3.8 GHz with a programmable bandwidth from 1.5 to 28 MHz. Moreover, this one is controlled with a Raspberry Pi 2® integrated in an embedded GNU-Radio way.

This challenging implementation interconnects several external subsystems that use an SoC for improving performance, costs, and volume. In [4], an SDR architecture is proposed. In that work, to solve the reconfiguration challenges of the transmitter and the receiver, the SoC device is combined with a programmable radio frequency (RF) transceiver from Analog Devices®. It involves using and implementing COTS such as the FMCOMMS3 (the AD9361 IC for the RF stage) and a ZYNQ 7020 from Xilinx®, among other devices. Tian et al. in [5] designed and implemented an AD9361-based platform for software radio exclusively for the receiver stage and a ZC706 applied to the digital baseband processing module of SoC.

A COST-based SDR architecture applied to the ground segment is presented in [6]. It develops the Digital Down Converter (DDC) stage using the hardware descriptive language VHDL and other baseband processes such as channel coding and data interleaving. The disadvantage of that proposal is that the IP-Cores involved are Xilinx® intellectual property and the transmission rates achieved are relatively low: 1.2 to 19.2 Kbps.

The authors in [7] concluded that hardware reuse is a novel approach in implementing SDR systems to better the performance of communications schemes. In [8], for both the reception and transmission stages, a design of an RF front-end for a nanosatellite is presented, using low-cost commercial components such as the CC2510 IC. However, this IC works in a narrow bandwidth of 2.400 to 2.483 GHz.

In [9], the stage of the baseband processor (BBP) of the communication system was implemented on a Zynq 7020. Nevertheless, the RF stage was just simulated. In [10], for scenarios of next-generation communications satellites, an FPGA application is described to implement an onboard processor and couple it through reconfiguration.

As pointed out in the literature, several satellite communication subsystem proposals are based on digital implementations using SDR systems and others are offered as COTS components. Regardless, the RF Analog Back-End remains partially unexplored and represents a research opportunity. Finally, it should be mentioned that there are companies in the market that offer satellite communications subsystems based on SDR, such as the one commercialized by [11], which can be reconfigured to use different frequency bands such as L, S, or K. Nevertheless, it has the drawbacks of both being expensive and proprietary architecture.

This work describes the modeling, implementation, and testing of a low-cost reconfigurable satellite communications subsystem prototype called the Reconfigurable Analog Back-End (RABE). This development is intended to be placed in the space segment, complying with the CubeSat standard for future applications. The proposed RABE consists of two stages. The first stage performs baseband processing, control, and reconfiguration for the second stage and is implemented in a commercial SoC architecture. The RF stage (second stage), the central goal of this work, includes digital/analog conversion, mixer, and filters based on COTS, operating from 0.070 to 6 GHz.

The rest of the paper is organized as follows: in Section 2, the RABE system architecture, the modeling and development of the PCB for the RF stage, the testbed design, and the software tools used are described; in Section 3, implementation, testing are shown, and the main results obtained are presented and discussed; and in Section 4, the conclusions are exhibited.

2. Materials and Methods

2.1. System Architecture

The RABE design features two interfaces; the first one is a digital I/O data, control, and communication interface between the prototype and the SoC, which is controlled by an FPGA, and which is part of the BBP; the connection interface with the RF stage is achieved through an FMC connector; the second one is an RF analog output with an SMA connector as the interface to the RF filtering stages, power amplifier, and antenna. The main core of the RABE is powered by an AD9354 IC.

Figure 1 shows the communication model that was implemented, the RF stage (of this work) that was designed, implemented, and tested, and tuning for the RABE in yellow, which was the contribution of the paper.

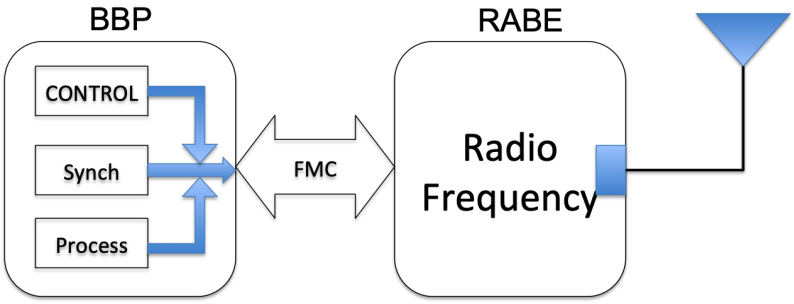


Figure 1. Communication system model. A block sequence about the communication system model and its architecture.

The BBP stage consisted of the development and coupling of the Serial Communication Protocol (SPI), as well as the programming of the registers to control the flow of data, synchronization, and processing of the data from the BBP to the RABE through the FMC connector, which is responsible for carrying all the bits for the operation of both devices, including the voltage and ground lines.

In the RF stage, the SPI was synchronized to program all the necessary registers in the IC, the DACs, the filtering stage, the preamplifiers, and the local oscillator, which were configured to be tuned at the required frequency. It is noteworthy that each of the configured actions corresponds to the programming of register groups in order to obtain the correct result shown in yellow in Figure 2.

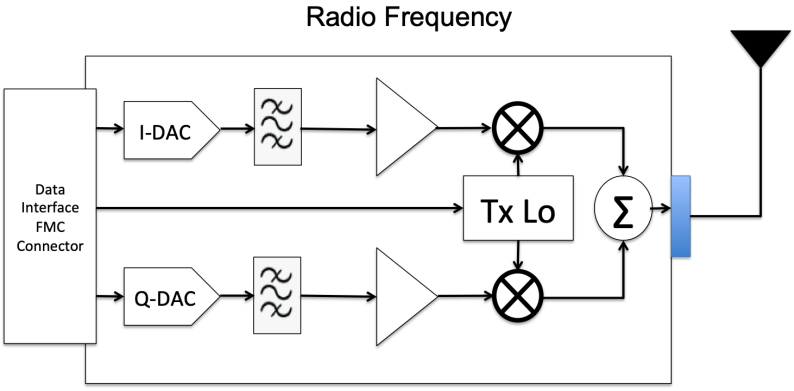


Figure 2. Radio frequency model. RF PCB scheme and AD9364 architecture.

2.2. RF Stage Design

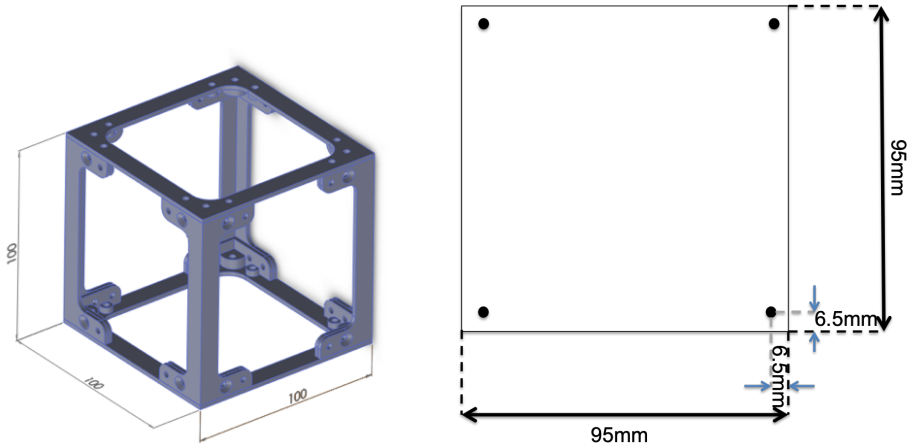
During the design stage of the RABE subsystem prototype, the necessary requirements for the development of the PCB (Printed Circuit Board) were specified to guarantee correct operation, allowing interoperability between the subsystem devices. The requirements are detailed in Table 1.

Table 1. General requirements of the RABE.

Request	Value	Units
Power Suply Vcc	5.000	V
PCB size	9.500 × 9.500	cm
Frequency range	2.200–2.300	GHz
Output Power	−20.000–5.000	dBm
BW	0.200–56.000	MHz
Input connector	FMC ASP-134604-01	
RF connector	female SMA	
Reference CLK	40.000	Mhz
IC	AD9364	
PCB	6 layers	

In general, the design of the RABE features two interfaces; the first one is the digital I/O data, control, and synchronization interfaces between the prototype and the SoC; the second one is the analog RF output with an SMA connector.

The 1U CubeSat standard is restricted to 10 cm^2, as can be seen in Figure 3a. Due to this and considering the physical structure of the CubeSat, it is necessary to implement the PCB inside it, leaving the dimensions shown in Figure 3b.



(**a**) (**b**)

Figure 3. Structure and PCB measurements in mm. (**a**) CubeSat structure. (**b**) PCB size.

The RABE has a read/write register interface carried out via the Serial SPI. Therefore, one of the preliminary tasks was to implement the SPI port in the BBP since it is not a native protocol in the FPGA.

The data lines for the PCB of the RF stage are divided into two sets: the differential and single-ended lines, as shown in Figure 4. The maximum data transfer frequency achieved is 245.76 and 61.44 MHz for the differential bus and single-ended, respectively. However, it depends on the IP-Core processing speed of the SoC and FPGA used by the implementation. The RF output feeds the next stage (it is not the scope of the work) comprised of power amplifiers, filters, and antennas, in order to achieve a high signal-to-noise ratio (SNR) and considering a link range of 2000 km in the free-space Low Earth Orbit (LEO) satellite.

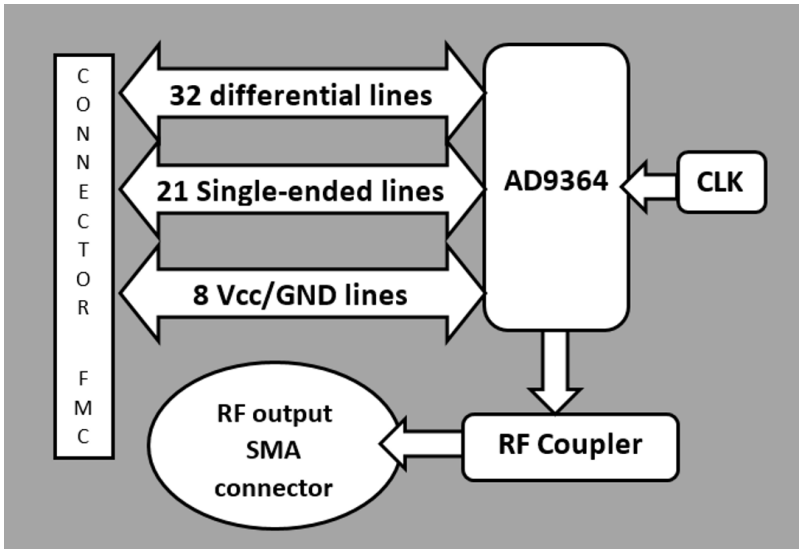


Figure 4. Schematic design of the RABE. This figure shows how AD9364 is connected to the FMC connector, as well as the FPGA and RF Output to the power amplifier stage (not shown at this work).

The RF stage of the RABE prototype uses the AD9364 transceiver, internally composed of ADC converters, DACs, filters, GPOs, PLLs, and an SPI communication control ports [12], as illustrated in Figure 5.

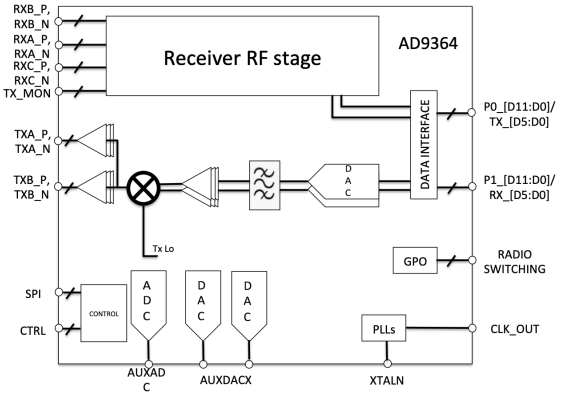


Figure 5. Block diagram of the IC AD9364. In this figure, the AD9364 manufacturer describes how it connects internally.

In this work, the transmission, data entry, DAC, filters, and SPI serial communication stages are used. The radio transmitter is implemented with the ability to operate in various frequency bands, mainly S-band. In addition to this, the configuration to modify in the application of the IC data such as the transmission power, the filtering, and, most importantly, that the prototype design must comply with the size proposed for the CubeSat standard. The IC AD9364 from Analog Devices® [12] is configured as an RF transceiver, operating in the 0.070 to 6.000 GHz frequency range with the ability to tune the bandwidths (BW) from 0.2 to 56.0 MHz and allowing applications proposed by the manufacturer such as point-to-point communication systems, base stations (BS) for femto/pico/microcells and general-purpose radio systems.

Further, the AD9364 IC is set by reading/writing into the registers set described in [13]. According to the manufacturer, the IC has a list of almost 1014 (0x3F6) 8-bit registers with configuration capabilities intended for diverse applications. These IC-specific application steps are initialization, configuration, transmission, reception, and analog records in reception (see Table 2). Record data flow modes can be: read, write, or both. The SPI port of the AD9364 operates at a recommended maximum speed of 50 MHz, according

to the manufacturer's specifications [12]. However, a frequency of 8 MHz was used for testing purposes in this work to ensure a safe transfer of information to registers.

Table 2. Functions of the AD9364 registers.

Modes	Initial		Final
Initialization	0x000	...	0x017
Setting	0x018	...	0x05F
Transmitter Configuration	0x060	...	0x0D7
Receiver Configuration	0x0F0	...	0x1FC
Rx Analog Registers	0x230	...	0x3F6

Regarding the operating and configuration modes of the registers, there is a relatively large number of reserved and/or empty positions; thus, in order not to cause improper operation of the system, it is advisable not to refer to them.

To reduce transients while changing the transmission frequency setting on the device, the power to the matching stage on the transmission lines is directly connected to a 1.3 V voltage source. The capacitors, shown in Figure 6, are intended for removing noise and transients at the transmitter output.

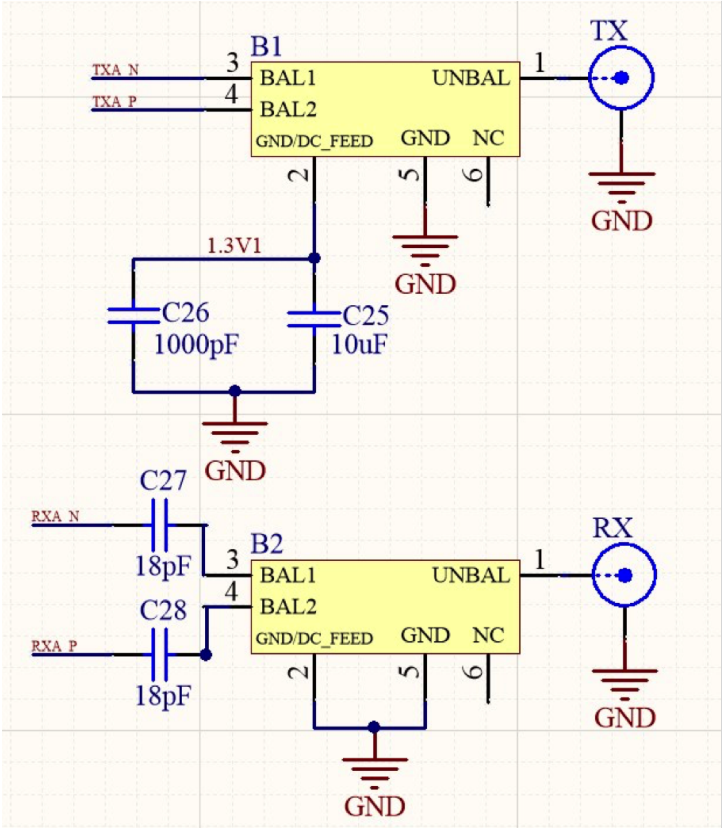
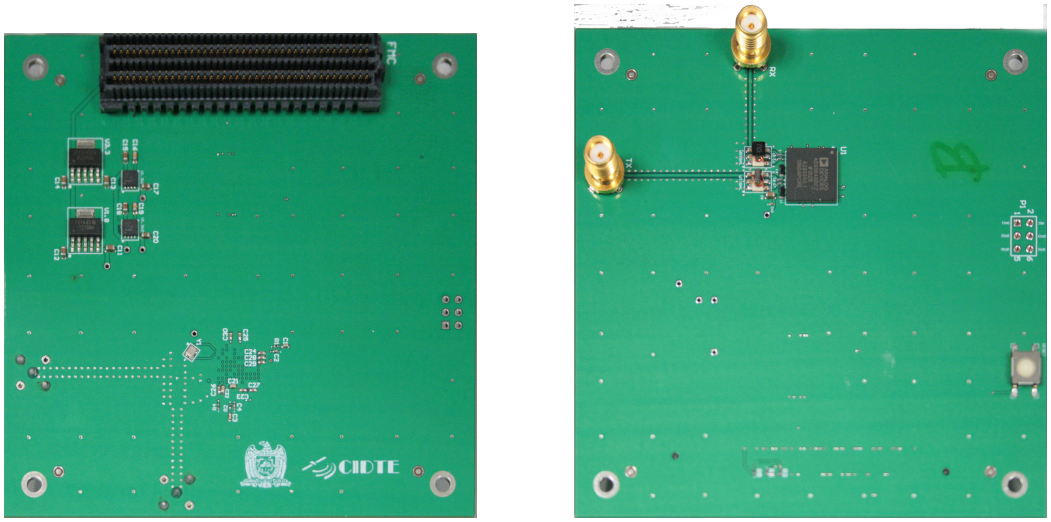


Figure 6. The RF matching stage, designed to avoid interference for 2–3 GHz.

It is worth mentioning that all the designs, measurements, and tests for the resulting devices were carried out in a test laboratory with a controlled environment (temperature, voltage levels, electromagnetic noise, and electric shocks, etc.) in such a way that the results obtained are completely similar to those obtained by simulations tools.

Design rules concerning the CubeSat standard [14] and PCB design [15] were applied to the electronic design process. The final result was a 6-layer PCB of 10 × 10 cm (see

Figure 7); on the other hand, the manufacturer suggests a fixing or soldering area on the PCB with the intention of achieving high performance and achieving adequate operation of the IC [13]. In Table 3, the thickness of the 6 PCB layers is shown.



(**a**) (**b**)

Figure 7. RABE-printed circuit board. A 3D model of the RABE ((**a**) top layer and (**b**) bottom layer).

Within the PCB, it is intended to integrate devices with the ability that they can be selected (RF switch) and digitally tuned [16] to take advantage of the available space in it and to be able to use different devices such as antennas, amplifiers, and filters in frequency bands that are too far apart from the main one.

Table 3. RABE PCB layers.

Layer	Type	Material	Thickness (mm)	Thickness (mil)
	Surface	Air		
Top	Conductor plane	Copper	0.0514	2.025
	Dielectric	FR-4	0.2032	8
L1_PWR	Conductor plane	Copper	0.0342	1.35
	Dielectric	BT-epoxy	0.1524	6
L2_SIG	Conductor plane	Copper	0.0342	1.35
	Dielectric	FR-4	0.2032	8
L3_SIG	Conductor plane	Copper	0.0342	1.35
	Dielectric	BT-epoxy	0.1524	6
L4_PWR	Conductor plane	Copper	0.0342	1.35
	Dielectric	FR-4	0.2032	8
Bottom	Conductor plane	Copper	0.0514	2.025
	Surface	Air		

The PCB for the radio transmitter was designed using Altium®, a high-end PCB design software package. The simulation of signal behavior on the PCB was carried out using Keysigth® EMPro® and Genesys® tools. The purpose of the simulation was both to validate low levels of electromagnetic interference (EMI) between interconnecting tracks and to avoid radiation to other components included in the board before PCB fabrication.

2.3. Testbed Design

The testbed shown in Figure 8 was integrated to measure the transmission power and frequency values and also to check the operation of the RABE prototype. The hardware devices and software used for the testbed implementation are: Keysigth® N9030A Signal

Analyzer, personal desktop computer, Digilent/Xilinx® brand Zedboard test card, RF cables with SMA connector, ethernet cable, RABE prototype, control and programming software for AD9364 IIO Oscilloscope, and IP address monitoring software.

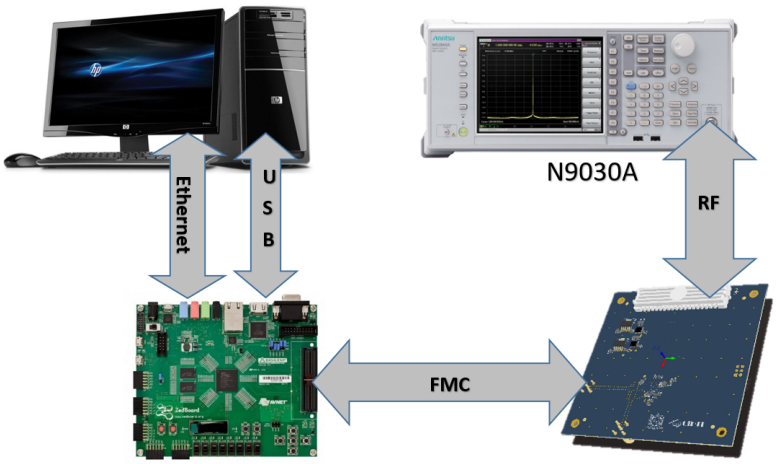


Figure 8. Testbed block diagram. Configuration for the connection of the test bed for the prototype.

The steps for running the testbed are as follows:

1. Download and install the IIO Oscilloscope software on your PC.
2. Insert the RABE to the Zedboard through the FMC connector.
3. Connect the RF cable from the RABE SMA connector to the N9030A.
4. Connect the ethernet and USB cable between the PC and the Zedboard.
5. Run the IIO Oscilloscope software on your PC.
6. Use the IIO Oscilloscope to configure the transmission frequency, bandwidth, attenuation, and other parameters.
7. Configure the N9030A to perform a scan on parameter values close to those set in the previous step.
8. Save the data to the N9030A.

3. Results and Discussion

Using the configuration described in Section 2.3, the testbed was implemented to test the RABE prototype, obtaining similar results to those from the IC manufacturer's test card AD9364 [12].

Two types of experimental measurements were carried out in order to verify the proper operation of the implemented prototype. In both scenarios, the same settings were used for output power, transmission frequency, and bandwidth parameters. As a result, it was noted that RABE output power (Figure 9a) was reduced by 2 dB compared to FMCOMMS4 (Figure 9b), which was 7 dB. It is important to mention that according to the AD9364 datasheet, it is able to transmit with a maximum power of 7.5 dBm when matched to 50 ohms load at 2.4 GHz.

Based on the Nyquist noiseless channel, the theoretical maximum bit rate is defined as equal to twice the bandwidth symbol (BW) per second. If each symbol can carry M different distinguishable levels, then each pulse carries log M bits of information, which is described by

$$\mathbf{C} = 2\mathrm{BW}\ \log_2(M) \quad \text{bits/sec} \tag{1}$$

Since the bandwidth of the AD9364 ranges from 200 KHz to 56 MHz, the data rate capacity for quaternary modulation, $M = 4$, will be between 0.800 and 224 Mbps.

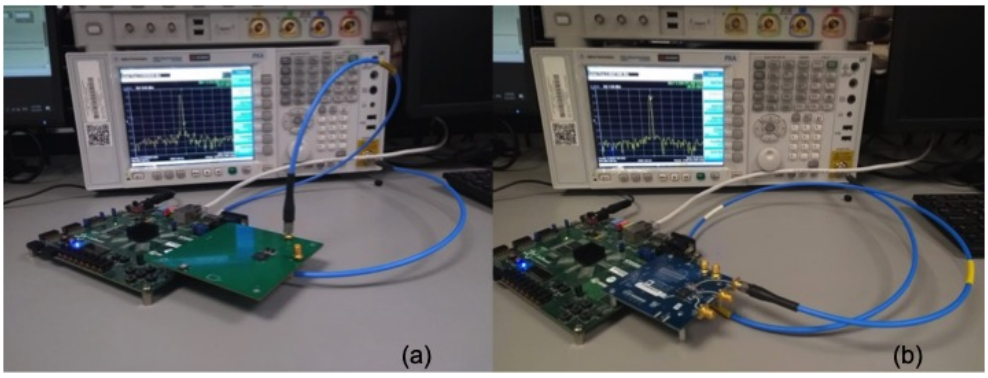


Figure 9. Implementation of the test bed for the RABE prototype. (**a**) tests of the manufactured prototype . (**b**) tests of the FMCOMMS4 card.

In Figure 10, the graph of the data collected in the test bench shows the spectrum transmitted by a signal with a carrier frequency of 2.6095 GHz to verify the correct operation of the design in different frequencies. The spikes shown at 2591 and 2599, are unidentified carriers external to the prototype system. The output power available at the carrier frequency in Figure 10 was −20 dBm, as shown. A Gaussian 3 dB resolution bandwidth (RBW) filter was applied into the signal analyzer followed by a Fast Fourier Transform (FFT) with a BW of 411.9 kHz.

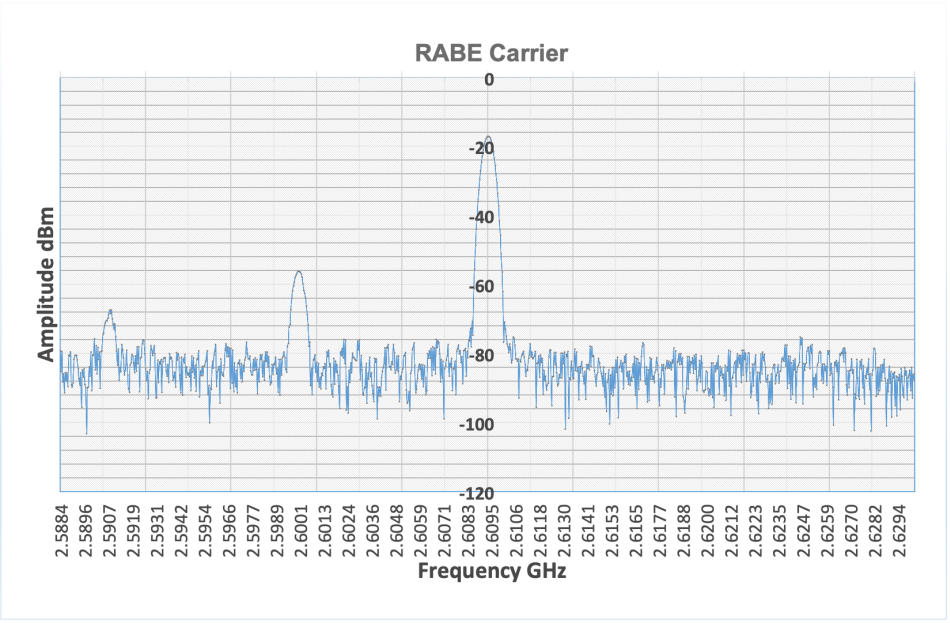


Figure 10. Spectrum of signal transmitted at 2.6095 GHz. Further processing of the data shows the spectrum of the carrier signal transmitted at 2.6095 GHz.

The BBP was set in a QAM modulation scheme at the testbed (as shown in Figure 11). The resulting modulation process was controlled and synchronized by the BBP to the RABE stage via the FMC connector.

The Total Harmonic Distortion (THD) percentage was measured as described in [17] and is given by

$$\mathrm{THD}_n = \sqrt{\frac{\sum_{n=2}^{\infty} Po_n}{Po_1}} \times 100, \tag{2}$$

where Po_n is the output power of the n-th harmonic in watts, and Po_1 is the output power of the fundamental frequency in watts.

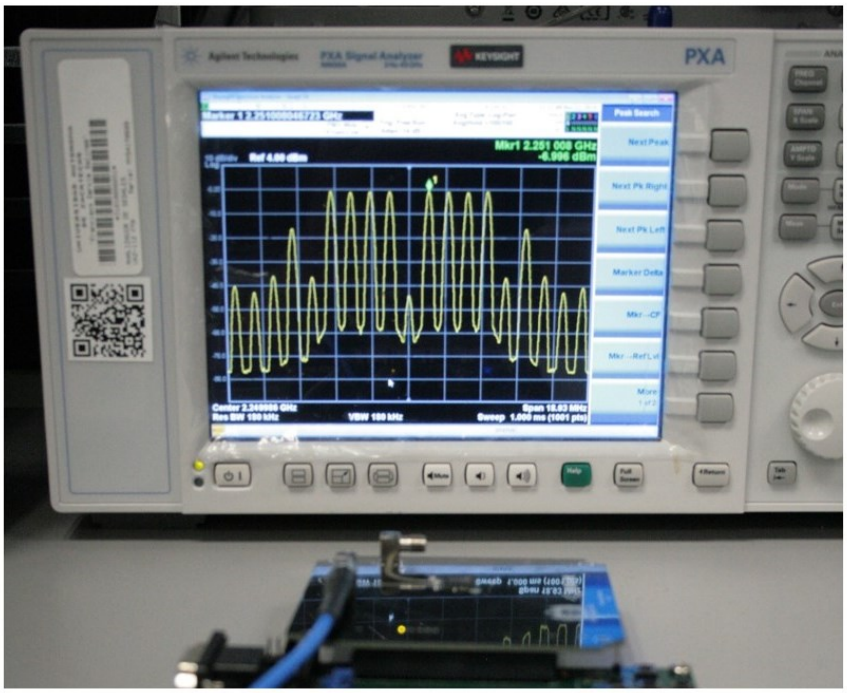


Figure 11. Signal analyzer, RABE and Zedboard on QPSK. The RABE prototype transmitting with 4-tone QPSK modulation, with 1 MHz frequency separations.

According to measurements made in the Lab using the N9030A Signal Analyzer, for $n = 10$ harmonics, as shown in Table 4, it was found that

$$\mathrm{THD}_n = 3.81\%.$$

Table 4. Harmonics generated by the RABE at 2.30 GHz.

Harmonic	Frequency (GHz)	Value (dBm)
1	2.30	−12.01
2	4.60	−40.4
3	6.90	−72.25
4	9.20	−81.3
5	11.50	−80.9
6	13.80	−79.9
7	16.10	−79.7
8	18.40	−76.9
9	20.70	−75.11
10	23.00	−74.32

The distortion values due to the harmonics generated by the transmitter stage could reach values of up to 3.8%, reducing the output power of the RF signal, as shown in Table 4.

Communication systems with a low THD produce less interference between electronic devices connected to or close to the PCB.

In Figure 12, the spectrum generated by the RABE is shown, which was taken directly from the RF output by the N9030A analyzer, all this at a frequency centered at 2.300 GHz, in which it is allowed by the Mexican government for experimental satellite links according to the frequency allocation table [18].

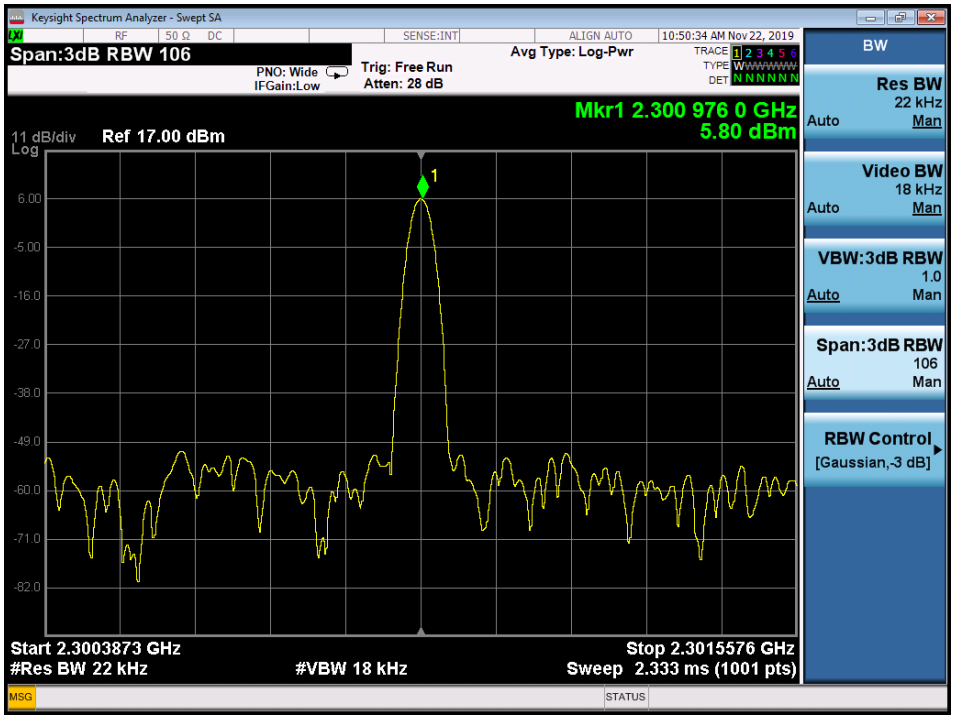


Figure 12. Spectrum radiated by RABE at 2.300 GHz. Image obtained from the signal analyzer with the prototype transmitting a single tone with a frequency of 2.300 GHz.

On the other hand, it is worth mentioning that the development of the PCB was taking into account the CubeSat standard, with the idea of possible inclusion as a payload in a satellite platform and carrying out transmission tests from space. To ensure that the designed device has a correct performance in space, it is necessary to carry out different types of tests so that the prototype can withstand the working conditions (electromagnetic radiation, thermal gradient) in space and being put into orbit (vibration). Among the tests that the prototype will undergo, we can mention those of electromagnetic compatibility and susceptibility, Total Ionizing Dose (TID), vibration and thermo-vacuum.

Some simulations were carried out, and they were obtained according to the PCB of the manufactured prototype, with the aim of comparing and knowing the radiation generated by inducing an electric current in the transmission lines. These simulations were carried out using the Keysigth ®EMPro ®software based on the Finite Difference Time Domain Method (FDTD) because it is one of the numerical analysis techniques best used to simulate electrodynamics, as manifested in [19–35].

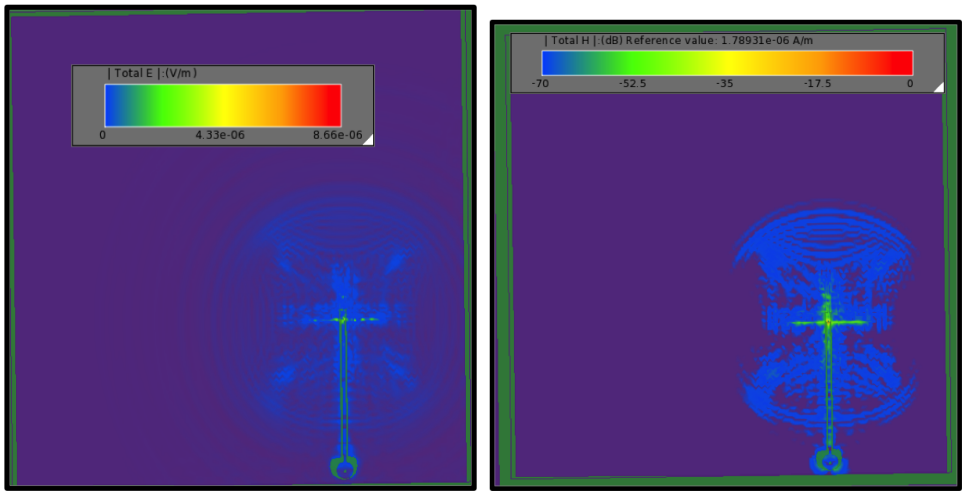
The simulation was carried out taking into account the Transmission Lines (TL) designed on the RABE prototype PCB towards the RF output. The near field for the present prototype is defined as maximum 1λ (wavelength). To perform the simulations, the frequency was defined at 2.3 GHz; therefore, the radiation levels emitted by the TL for the $\vec{E}$ field can be seen in Figure 13a and for the $\vec{H}$ field in Figure 13b.

It can be seen graphically that the radiation levels emitted by the TL of the RABE transmitter do not act as an antenna towards the outside of the PCB with the $\vec{E}$ and $\vec{H}$ fields.

However, when obtaining the Poynting vector with (3), the case is different, because here it can be seen that the radiation pattern exceeds the limits of the PCB.

$$\vec{S} = \vec{E} \times \vec{H} \tag{3}$$

With the simulations of the $\vec{E}$ and $\vec{H}$ fields, the Poynting vector can be obtained, as can be seen in Figure 14, where $\vec{S}$ gives the measure of rate of energy flow per unit surface area at a point in a uniform plane wave.



(**a**) (**b**)

Figure 13. $\vec{E}$ and $\vec{H}$ field simulations on the RABE transmission line. (**a**) Electric ($\vec{E}$) field. (**b**) Magnetic ($\vec{H}$) field.

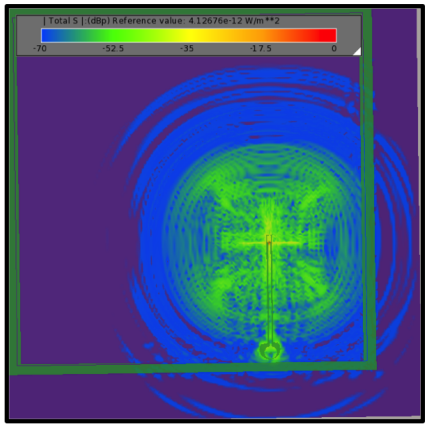


Figure 14. Poynting $\vec{S}$ Vector.

4. Conclusions

In this paper, the design, construction, verification, and test of a prototype for a reconfigurable radio-transmitter called RABE was presented. The proposed prototype can be used as the communication subsystem in a nanosatellite based on the CubeSat standard. Construction and testing were performed under quality standards in a controlled environment. Results show the correct operation of our card similar to that one commercialized by the IC manufacturer.

The resulting implementation of RABE guarantees the reconfiguration of a nanosatellite communication subsystem. Because of this reconfiguration capacity, it is possible to either have a communication with the terrestrial segment or with other devices orbiting in space, as in the BBP stage, different processing stages can be selected (e.g., modulation scheme). Similarly, the RF stage parameters can be modified (e.g., carrier frequency or transmitter power).

In short, this design allows reducing the number of unnecessary components, optimizing the dimensions of the PCB, and having a weight and size adequate to the specifications of the CubeSat standard.

It is necessary to implement reconfigurable devices and systems externally to a satellite communications subsystem, as shown in the present work and in [10,16], in order to obtain and complement what is stated in these proposals.

It should be noted that power values achieved in the RF output stage of the RABE are sufficient for the subsequent stages of the nanosatellite communications subsystem, which include filters, power amplifiers, and antennas, among others.

However, in the future, it will be necessary to carry out measurements of electromagnetic compatibility and susceptibility to the RABE prototype in order to identify anomalies such as interferences with other devices that make up the satellite. In addition to this, it is recommended to carry out Total Ionizing Dose (TID), Single-Event Effects (SEEs), and vibration and thermal vacuum tests to verify the robustness of the design when it comes to being placed in orbit. Furthermore, as future work, it is recommended that both the baseband processing, control, and reconfiguration stage and the RF stage could be integrated on a single PCB trying to minimize the size of the communication system and at the same time optimizing the operating speed.

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Abbreviations

The following abbreviations are used in this manuscript:

CAD	Computer-Aided Design
PCB	Printed Circuit Board
GPP	General Purpose Processor
DSP	Digital Signal Processor
FPGA	Field Programmable Gate Array
SDR	Software-Defined Radio
SoC	System on a Chip
IC	Integrated Circuit
GHz	Gigahertz
MHz	Megahertz
COTS	Commercial-Off-The-Shelf
RF	Radio Frequency
DDC	Digital Down Converter
VHDL	Vhsic Hardware Description Language
BBP	BaseBand Processor
RABE	Reconfigurable Analog Back-End
SMA	SubMiniature version A
FMC	FPGA Mezzanine Card
SPI	Serial Communication Protocol

DAC	Digital–Analog Converter
I/O	Input/Output
SNR	Signal-to-Noise Ratio
LEO	Low Earth Orbit
km	Kilometer
GPO	General-Purpose Output
PLL	Phase-Locked Loop
BS	Base Stations
EMI	ElectroMagnetic Interference
BW	BandWidth
KHz	Kilohertz
RBW	Resolution BandWidth
FFT	Fast Fourier Transform
THD	Total Harmonic Distortion

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