

## Article

# A Low-Voltage, Ultra-Low-Power, High-Gain Operational Amplifier Design for Portable Wearable Devices

Na Bai<sup>1,2</sup>, Xiaolong Li<sup>2</sup>  and Yaohua Xu<sup>1,2,3,\*</sup> 

<sup>1</sup> Key Laboratory of Intelligent Computing & Signal Processing, Ministry of Education, Anhui University, Hefei 230601, China; 11074@ahu.edu.cn

<sup>2</sup> School of Integrated Circuits, Anhui University, Hefei 230601, China; p20301131@stu.ahu.edu.cn

<sup>3</sup> Engineering Technology Research Center of Internet of Things Spectrum Sensing and Testing, Hefei 230601, China

\* Correspondence: xyh@ahu.edu.cn; Tel.: +86-130-330-0855

**Abstract:** Based on the SMIC 0.13 um CMOS technology, this paper uses a 0.8 V supply voltage to design a low-voltage, ultra-low-power, high-gain, two-stage, fully differential operational amplifier. Through the simulation analysis, when the supply voltage is 0.8 V, the design circuit meets the ultra-low power consumption and also has the characteristic of high gain. The five-tube, fully differential, and common-source amplifier circuits provide the operational amplifier with high gain and large swing. Unlike the traditional common-mode feedback, this paper uses the output of the common-mode feedback as the bias voltage of the five-tube operational transconductance amplifier load, which reduces the design cost of the circuit; the structure involves self-cascoding composite MOS, which makes the common-mode feedback loop more sensitive. The frequency compensation circuit adopts Miller compensation technology with zero-pole separation, which increases the stability of the circuit. The input of the circuit uses the current mirror. A small reference current is chosen to reduce power consumption. A detailed performance simulation analysis of this operational amplifier circuit is carried out on the Cadence spectre platform. The open-loop gain of this operational amplifier is 74.1 dB, the phase margin is 61°, the output swing is 0.7 V, the common-mode rejection ratio is 109 dB, and the static power consumption is only 11.2 uW.

**Keywords:** fully differential; common-mode feedback; low voltage; ultra-low power consumption; high gain



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## 1. Introduction

In recent years, portable electronics and smart wearable devices (such as wireless bluetooth headsets, smart watches, digital cameras, and notebook computers) have become widely available. Under the background that it is difficult to increase the battery capacity in such devices, it is necessary to reduce the power consumption of the circuits in order to improve their endurance. Because of the power consumption and supply voltage's positive exponential relationship, reducing the supply voltage has become one of the important initiatives to reduce the power consumption of portable products [1]. For analog circuits, operational amplifiers are the most important basic units and are widely used in various analog integrated circuits, such as digital-to-analog converters, low dropout linear regulators, and phase-locked loops. In addition, in some portable pressure sensor devices, the output signal of the mechanically sensitive element is generally very small, so it must be amplified and transformed by an amplifier processing circuit to meet the requirements of the application. The implementation of low power consumption in analog circuits depends heavily on the power consumption of the operational amplifiers. The op-amp circuit presented in the reference [2] uses a 5.5 V supply voltage with great power consumption. The increase in power consumption can expose the product to the danger of high temperature operation and reduce the stability of the system's operation. In order to

comply with the development goals of low voltage and low power consumption, an op-amp is a better choice for today’s various portable electronic products and smart wearable devices. Based on the 0.13 μm CMOS technology, this paper does not use the typical 1.2 V supply voltage, and adopts with a 0.8 V low supply voltage. A fully differential operational amplifier with low voltage, ultra-low power consumption, and high gain is designed.

### 2. Materials and Methods

The typical unipolar amplifiers have three structures: common source, common drain, and common gate [3]. In addition, based on the basic circuit, the amplifiers also have many commonly used structures, such as the telescopic cascode [4], the folded cascode [5], and the fully differential or two-stage op-amp structures.

The circuit of the sleeve-type cascode amplifier with a fully differential structure is shown in Figure 1a, and the gain expression is:

$$A_v = g_{m1}[(g_{m3}r_{o1}r_{o3})/(g_{m5}r_{o5}r_{o7})] \tag{1}$$

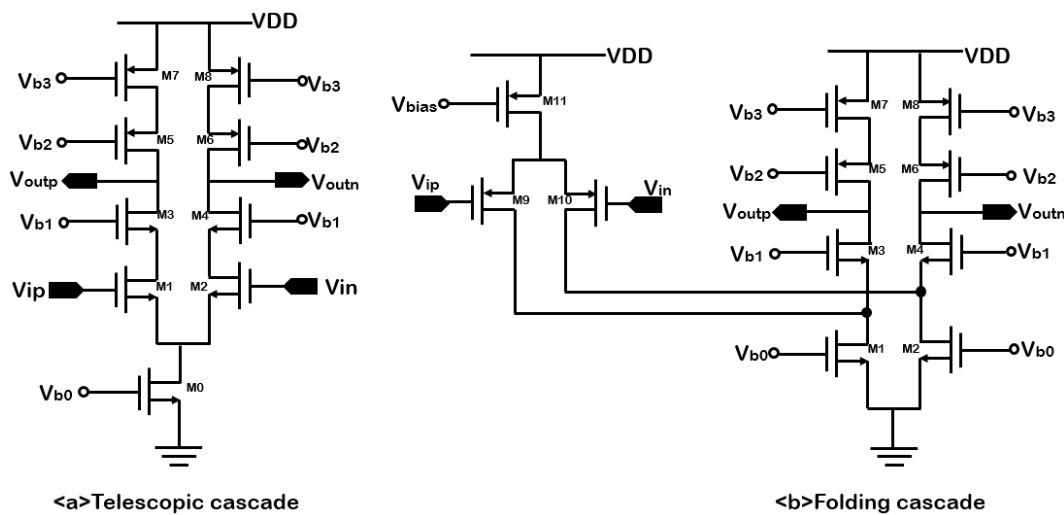


Figure 1. Telescopic cascode and folding cascode.

The advantage of this structure is that it can provide high gain, but due to the large load, the output swing of the operational amplifier is greatly restricted. The output swing expression is:

$$V_{out} = 2[VDD - (V_{OD1} + V_{OD3} + V_{OD0} + |V_{OD5}| + |V_{OD7}|)] \tag{2}$$

In the formula,  $V_{OD}$  represents the overdrive voltage of each MOS tube. Another disadvantage of the telescopic cascode operational amplifier is that it will add extra poles, which will bring additional design costs.

The circuit of the fully differential structure of the folded cascode amplifier is shown in Figure 1b, and the gain expression is:

$$A_v = g_{m9}\{[(g_{m3}(r_{o1}/r_{o3})r_{o9})]/[(g_{m5}r_{o5}r_{o7})]\} \tag{3}$$

The output swing expression of this structure is:

$$V_{out} = 2[VDD - (V_{OD1} + V_{OD3} + |V_{OD5}| + |V_{OD7}|)] \tag{4}$$

Comparing Equations (2) and (4), it can be seen that the output swing of the folded cascode folded structure of the cascode operational amplifier has increased by  $2 V_{OD0}$  compared to the sleeve structure, but due to the equivalent outputs, the impedance of the folded cascode operational amplifier is smaller than that of the sleeve-type structure, so

that the gain is significantly reduced. In addition, the folding structure has disadvantages, such as high power consumption, low pole frequency, and high noise generation.

Based on the analysis of the above theoretical structure, this paper adopts a two-stage operational amplifier circuit structure. The structure combines a fully differential five-tube operational transconductance amplifier (OTA) [6] and a common-source amplifier, which can meet high gain while also providing great swing. In addition, it has the advantages of simple circuit, a strong ability to suppress common-mode noise, and low power consumption.

The operational amplifier this paper designed is composed of an amplifying circuit module, a common mode feedback module, a frequency compensation module, and a current mirror bias circuit, as shown in Figure 2. The first stage of the amplifier circuit is a five-tube OTA circuit, and the second stage is a traditional common source amplifier circuit. The common-mode feedback module includes resistance common-mode detection and error amplification. This article uses a new common-mode feedback method that uses the signal after error amplification as the gate input of the five-tube OTA load, and the self-cascoding composite MOS structure is incorporated into the module. The frequency compensation module includes Miller capacitance compensation and zero resistance compensation. The overall design circuit of the op-amp is shown in Figure 3.

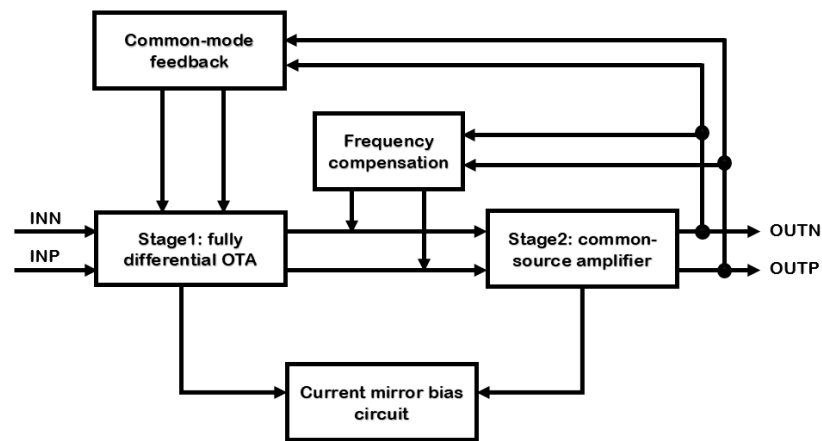


Figure 2. Schematic diagram of the structure of the op-amp in this paper.

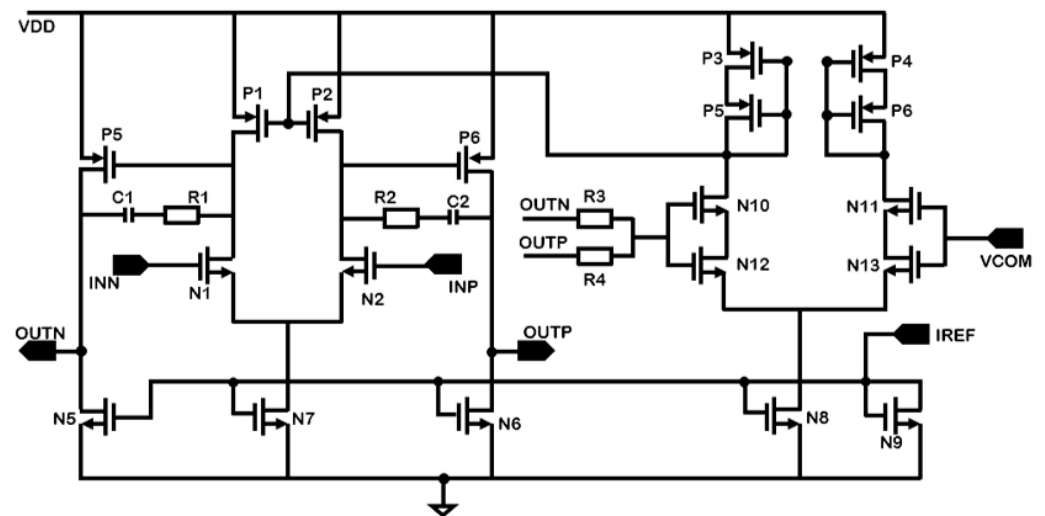


Figure 3. The overall operational amplifier circuit.

### 2.1. Amplifier Circuit Module

With the continuous development of integrated circuits, in some applications, the gain or output swing generated by the traditional unipolar operational amplifier cannot meet the requirements. For example, in [7], the gain of an operational amplifier with a unipolar folded cascode structure is 60.96 dB, and this structure has a low output swing. To solve this problem, this article designed a two-stage op-amp circuit to separate the gain and output swing. The first stage op-amp provides a higher gain for the circuit, and the second stage op-amp provides a great swing.

As shown in Figure 3, the first-stage operational amplifier circuit uses a fully differential five-tube OTA circuit, with N1 and N2 as the pair of input tubes; P1 and P2 as the equivalent current source output loads; and N7 in a saturated state, which acts as a tail current source. Then the first-stage operational amplifier voltage gain expression is:

$$A_{v1} = \frac{\partial V_{out1}}{\partial V_{in1}} = -g_{m1,2}(r_{n1,2} // r_{p1,2}) \quad (5)$$

In the formula,  $g_{m1,2}$  is the transconductance of N1 (or N2),  $r_{n1,2}$  is the on-resistance of N1 (or N2), and  $r_{p1,2}$  is the on-resistance of P1 (or P2).

The second stage operational amplifier circuit uses a typical common source amplifier circuit, with P5 and P6 tubes as the input tubes for the common source; and N5 and N6 tubes as the equivalent current source output load to increase the gain. Then the gain expression of the second stage op-amp is:

$$A_{v2} = \frac{\partial V_{out2}}{\partial V_{in2}} = -g_{m5,6}(r_{n5,6} // r_{p5,6}) \quad (6)$$

In the formula,  $g_{m5,6}$  is the transconductance of P5 (or P6),  $r_{n5,6}$  is the on-resistance of N5 (or N6), and  $r_{p5,6}$  is the on-resistance of P5 (or P6).

### 2.2. Common-Mode Feedback Module

When the op-amp uses a fully differential circuit structure, it is jammy to be unbalanced between the NMOS current source and the PMOS current source, which will cause an offset. The offset current flowing through the output resistance of the amplifier will produce a big voltage mismatch, forcing the side with the larger current enter the linear region. So, it is necessary to design a common-mode feedback (CMFB) circuit to allow each stage to achieve common-mode stability [8].

The common-mode feedback principle commonly used in two-stage op-amps is shown in Figure 4a. The principle is to use the result of the error amplifier to control the fully differential tail current source to achieve the common-mode feedback. The common-mode feedback module in this paper takes a new approach, as shown in Figure 4b. The output of both ends of the fully differential amplifier is passed through the common-mode detection circuit to obtain the common-mode voltage  $V_{CM}$ . The common-mode voltage  $V_{CM}$  is compared with the reference voltage  $V_{COM}$ . The compared error is amplified and output to the gates of P1 and P2 tubes to form a common-mode feedback loop. Ultimately, the output voltages  $V_{outn}$  and  $V_{outp}$  are equal to the reference voltage  $V_{COM}$ . This satisfies the feedback purpose and does not require an additional bias circuit to provide the bias voltage  $V_{b1}$ , reducing the design cost of the circuit. In addition, the error amplifier uses a self-cascoding composite structure to effectively increase the gain. This structure is suitable for low-voltage designs.

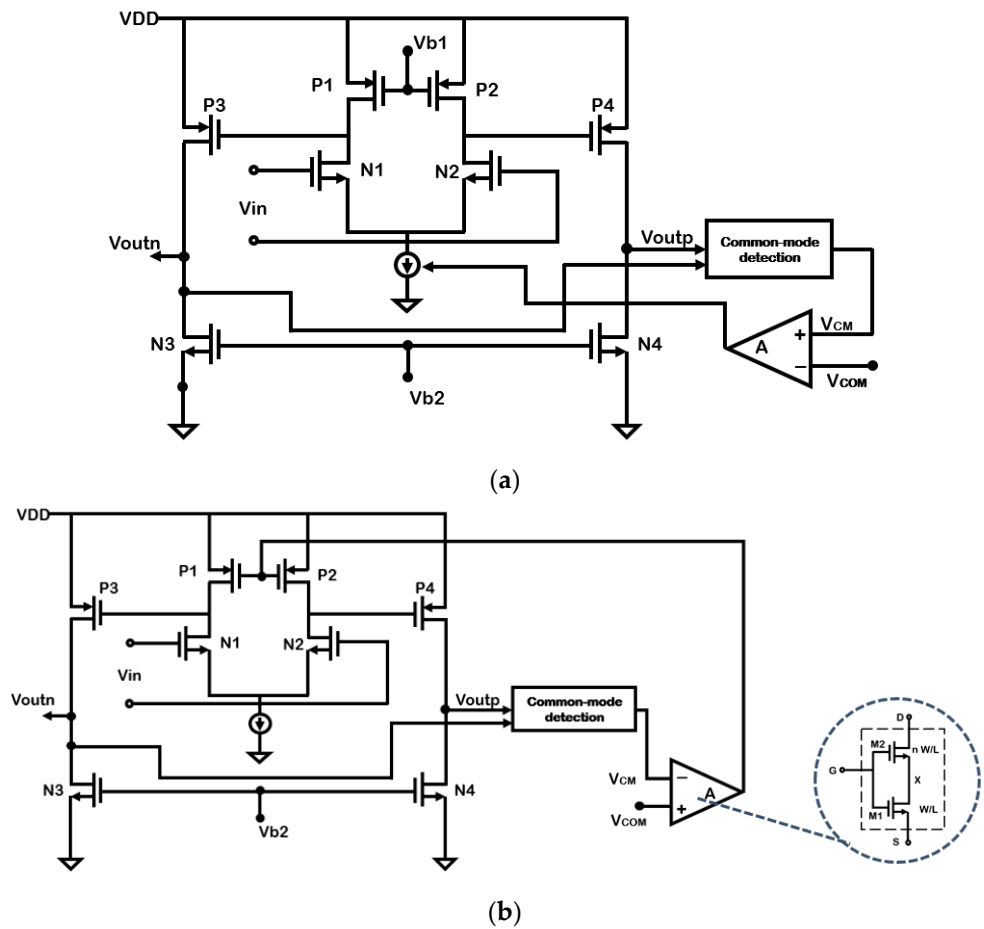


Figure 4. (a) The traditional common-mode feedback circuit. (b) The design of this article.

The self-cascoding composite MOS structure is shown in Figure 5.

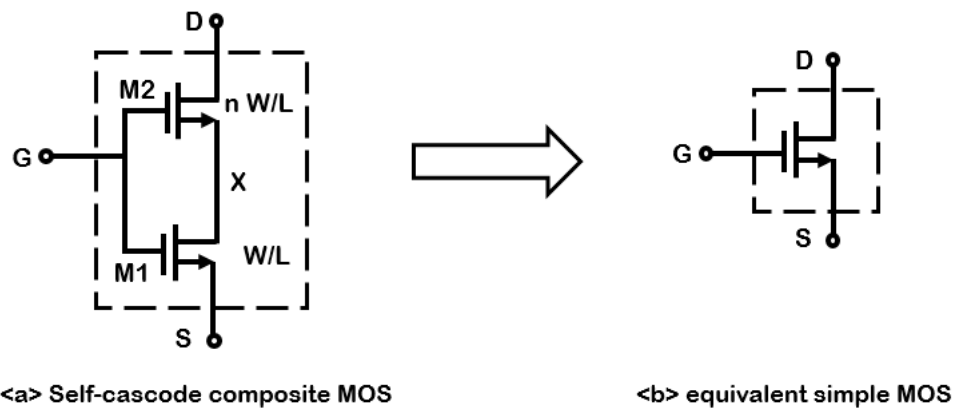


Figure 5. The self-cascoding composite MOS structure and equivalent simple MOS.

In order for the self-cascoding composite structure to work properly, both M1 and M2 must be on, so the following conditions must be met:

$$\begin{aligned} V_G - V_S - V_{TH} &> 0 \\ V_G - V_X - V_{TH} &> 0 \end{aligned} \tag{7}$$

The above formula can be equated as follows:

$$V_X - V_S < V_G - V_S = V_{DSAT} \tag{8}$$

Therefore M1 must be in the linear region with a small source-drain voltage. Thus, the equivalent  $V_{DSAT}$  of a self-cascode MOS tube is close to the  $V_{DSAT}$  of a simple MOS tube. This makes the self-cascode structure suitable for applications in low voltage designs.

For the equivalent output resistance of this structure, the small signal model is shown in Figure 6.

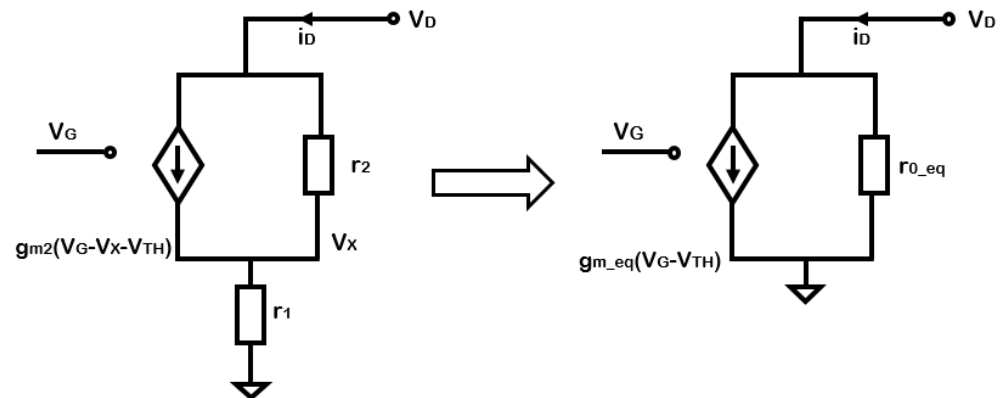


Figure 6. Small signal model of self-cascode composite structure.

The equivalent output resistance of a self-cascode MOS tube is expressed as [9]:

$$r_{o\_eq} = g_{m2}r_2r_1 - r_1 - r_2 \approx (g_{m2}r_1 - 1)r_2 = (n g_{m1}r_1 - 1)r_2 \tag{9}$$

The equivalent transconductance of the self-cascode MOS tube is approximately equal to the transconductance of M1:

$$g_{m\_eq} = g_{m2}/m = g_{m1} \tag{10}$$

From the above analysis, it is clear that the self-cascode MOS tubes effectively increase the output resistance and improve the gain. The increase in gain makes the common-mode feedback loop more sensitive. Even if there is a small potential difference between the output voltage and the reference voltage  $V_{COM}$ , it can be amplified by the error amplifier to make the feedback loop work properly. Eventually, the output voltage is equal to the reference voltage.

### 2.3. Compensation Circuit Module

The output signal with phase shift is superimposed on the input signal, which will cause the op-amp to self-oscillate. The expression of the output function  $H(s)$  is:

$$H(s) = \frac{a_0 + a_1s + a_2s^2 + \dots + a_{m-1}s^{m-1} + a_ms^m}{b_0 + b_1s + b_2s^2 + \dots + b_{n-1}s^{n-1} + b_ns^n} = \frac{H_0 \left(1 + \frac{s}{z_1}\right) \left(1 + \frac{s}{z_2}\right) \dots \left(1 + \frac{s}{z_m}\right)}{\left(1 + \frac{s}{p_1}\right) \left(1 + \frac{s}{p_2}\right) \dots \left(1 + \frac{s}{p_n}\right)} \tag{11}$$

The amplitude-frequency and phase-frequency curves of the multi-pole op-amp system are shown in Figure 7.

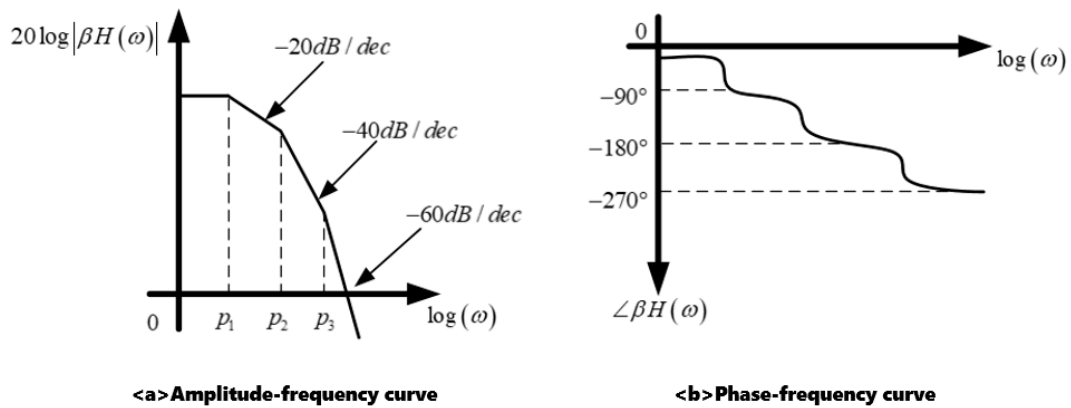


Figure 7. Amplitude-frequency curve and phase-frequency curve of a multi-pole system.

The slope of the amplitude-frequency curve of the op-amp increases by  $-20 \text{ dB/dec}$  with each passing pole, and the phase changes by  $90^\circ$ . Multiple poles cause changes in amplitude and phase frequency characteristics, which may make the system unstable and oscillate, causing its stability to be destroyed. This is where a frequency compensation circuit is needed to improve the stability of the system.

A typical two-stage op-amp with Miller compensation is shown in Figure 8. Node P is the main pole of the circuit. Assuming that the parasitic capacitance of junction P is  $C_P$ , the capacitance at junction P becomes  $C_P + (1 + A_2)C_1$  after the addition of the Miller compensation capacitor. This causes the load capacitance of the main pole to increase; therefore the Miller compensation causes the main pole to move closer to the origin. The two-stage op-amp sub-primary pole analysis is shown in Figure 9.

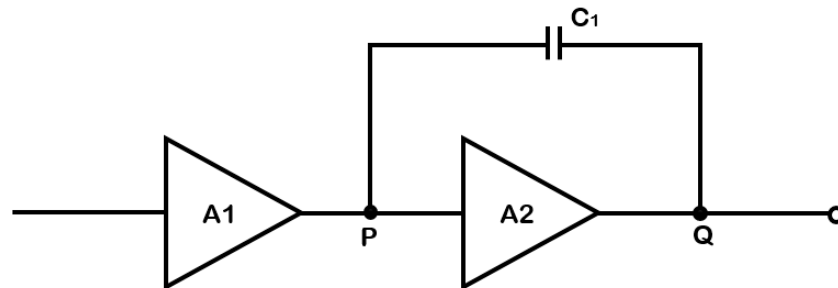


Figure 8. Classic two-stage op-amp Miller compensation.

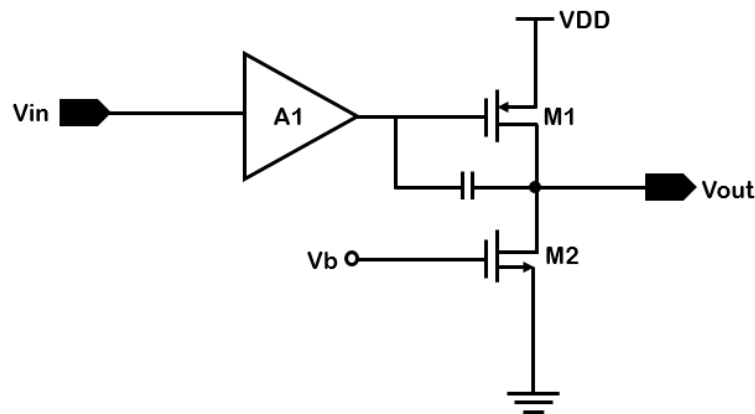


Figure 9. Two-stage op-amp sub-major pole analysis.

When Miller compensation is not added, the frequency of the sub-major pole is:

$$\omega_2 = \frac{1}{R_L C_L} \tag{12}$$

$R_L$  is the load resistance, and  $C_L$  is the load capacitance. After adding Miller compensation, the frequency of the sub-major pole becomes:

$$\omega_{2'} = \frac{1}{\frac{1}{g_{m1}} C_L} = \frac{g_{m1}}{C_L} \tag{13}$$

After adding Miller compensation, the frequency of the sub-major pole becomes larger. The sub-primary pole is shifted away from the origin. Finally, the analysis shows that the main poles of the op-amp are shifted to the left and the sub-major poles are shifted to the right after the Miller compensation. This increases the phase margin of the op-amp and improves the stability. This processing method is also called ‘‘pole splitting’’.

In addition, the miller compensation capacitor will introduce a low frequency zero point [10]. This zero point contributes to a larger phase shift that shifts the phase intersection to the left, greatly reducing the stability of the op-amp. In this case, it is necessary to add a zeroing resistor in series with the Miller compensation capacitor to eliminate the effect of the zero point.

Based on the above theory, in this paper, the Miller capacitor and zeroing resistor are connected in series between the outputs of the first-stage op-amp and the second-stage op-amp to improve the stability of the circuit. Figure 10 shows the results of gain and phase without and with the addition of frequency compensation circuit. When the frequency compensation circuit is not added, the phase margin is  $0.166^\circ$ , as shown in Figure 10a, which is far from the conventional standard of  $60^\circ$  [11]. The circuit is extremely unstable. After adding the frequency compensation circuit, the phase margin is  $61^\circ$ , as shown in Figure 10b, and the circuit has good stability.

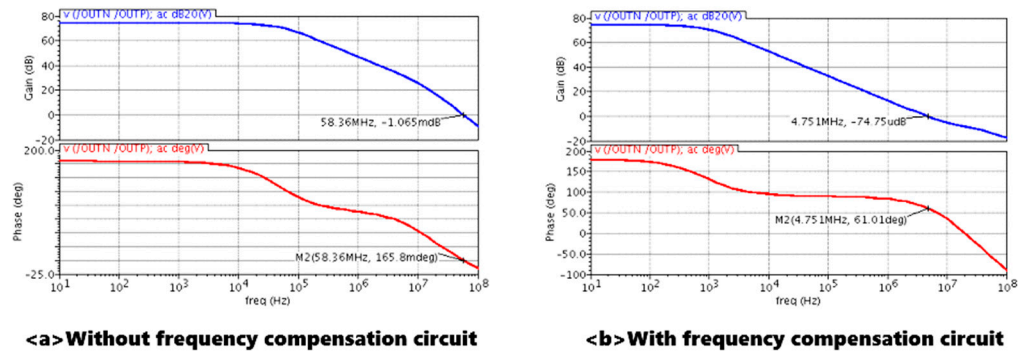


Figure 10. The influence of frequency compensation circuit on the stability.

#### 2.4. Current Mirror Bias Module

Both the fully differential module and the common-mode feedback module that have been determined above need to be set with the correct bias voltage to work normally. In order to achieve ultra-low power consumption of the op-amp and maintain the simplicity of the circuit, the bias circuits in this article are all current mirror bias [12] circuits, as shown in Figure 11.

In order to reduce the power consumption of the circuit as much as possible, the reference current source IREF is set to 2 uA in the circuit, and the total operating current is 14 uA. According to the different currents required, this paper sets the appropriate width-length ratios of the N5, N6, N7, N8, and N9 tubes respectively, so that:

$$(W/L)_5 = (W/L)_7 = (W/L)_6 = 2(W/L)_8 = 2(W/L)_9 \tag{14}$$



$$I_5 = I_7 = I_6 = 2I_2 = 2I_{REF} \quad (15)$$

In the formula,  $(W/L)$  represents the width-to-length ratio of each MOS tube. Here, in order to reduce the influence of the channel length modulation effect on the current mirror, the module uses long-channel MOS tubes.

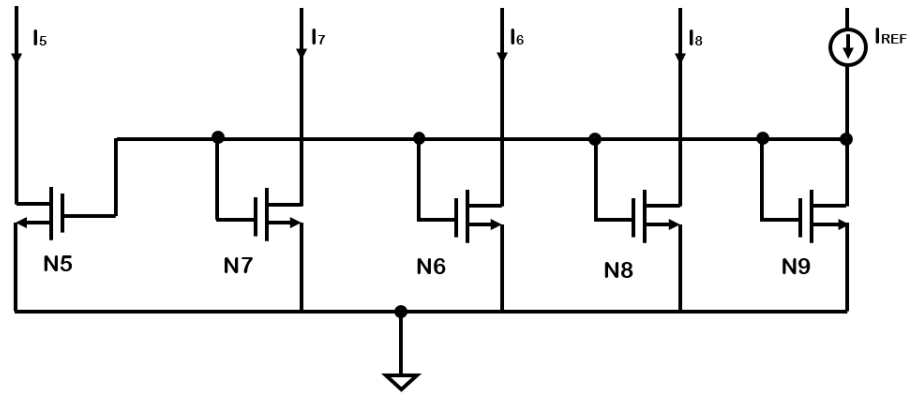


Figure 11. Current mirror bias circuit.

### 3. Results

The following reports the performance simulation of the op-amp circuit. Based on 0.13  $\mu\text{m}$  CMOS technology, the op-amp is simulated in the cadence spectre simulator. The simulation includes voltage gain, phase margin, transient analysis, common-mode rejection ratio (CMRR), noise analysis, and speed characteristic analysis. The simulated temperature is 27  $^{\circ}\text{C}$ , the supply voltage is 0.8 V, the corner is tt, and the static power consumption is only 11.2  $\mu\text{W}$ . The layout of the op-amp is shown in Figure 12. The module design is symmetrical to reduce mismatch and DC offset and make the matching better. In addition, two protection rings are added to the periphery of the circuit to protect the internal circuit from external interference. To avoid the use of long metal interconnecting wires, contact holes are appropriately used as connecting wires.

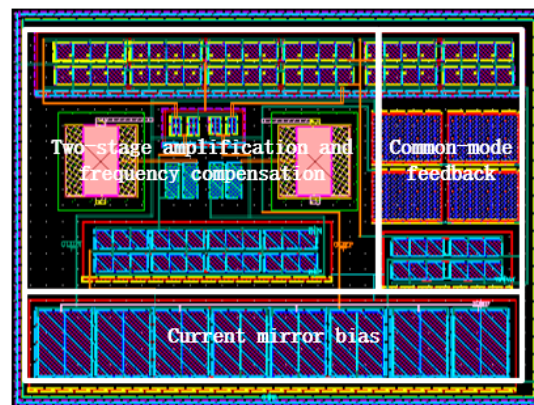


Figure 12. The op-amp layout.

#### 3.1. Voltage Gain

This paper input a pair of ac small signals with opposite phases with a DC bias voltage of 0.6 V at the differential input terminals INN and INP. Then this paper performs a frequency scan on the operational amplifier. The frequency scan range is 10 Hz to 100 MHz. The result is shown in Figure 13. The low-frequency gain of the operational amplifier is 74.07 dB. After the frequency exceeded a certain range, the gain gradually decreased as the frequency increased.

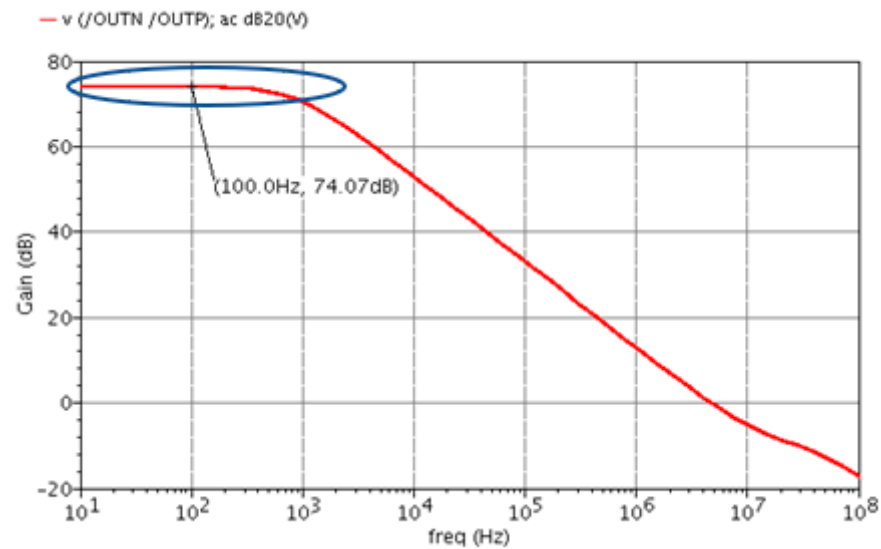


Figure 13. Two-stage op-amp gain simulation.

### 3.2. Phase Margin

The phase margin is mainly used to describe the stability of the negative feedback system of an operational amplifier. Generally speaking, the phase margin of the operational amplifier needs to be no less than  $45^\circ$ . The greater the phase margin, the more stable the operational amplifier, but the speed will slow down. Therefore, considering it comprehensively, it is generally believed that a phase margin of  $60^\circ$  is the most suitable value [11]. If the phase margin is too large, it will slow down the speed characteristics of the op-amp. If the phase margin is too small, it will cause oscillation and stability problems. As shown in Figure 14, it can be seen the bandwidth corresponding to 0 dB in the gain simulation curve. This bandwidth is called the unity-gain bandwidth. It can be seen from the figure that the bandwidth is about 4.751 MHz. Then it can be seen the phase corresponding to the bandwidth in the phase simulation curve, the phase margin, which is about  $61^\circ$ .

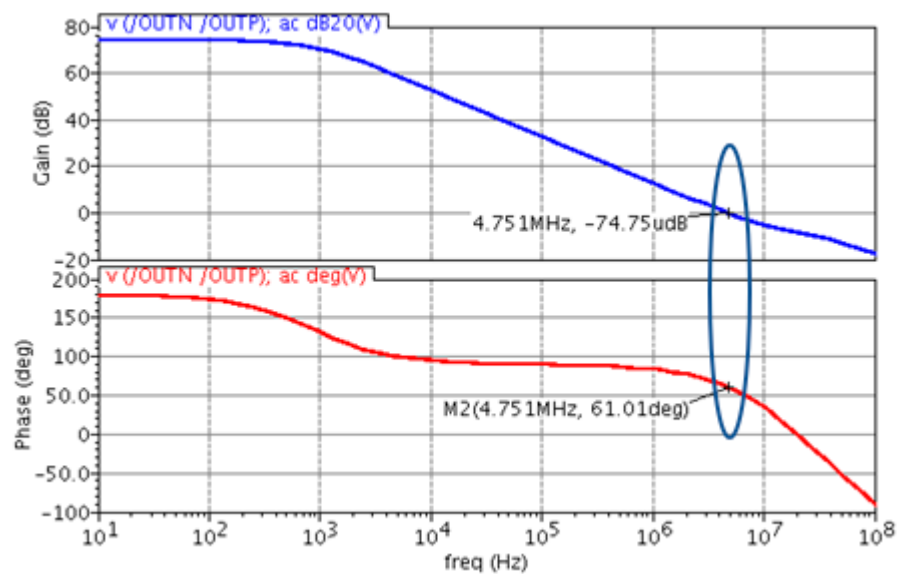
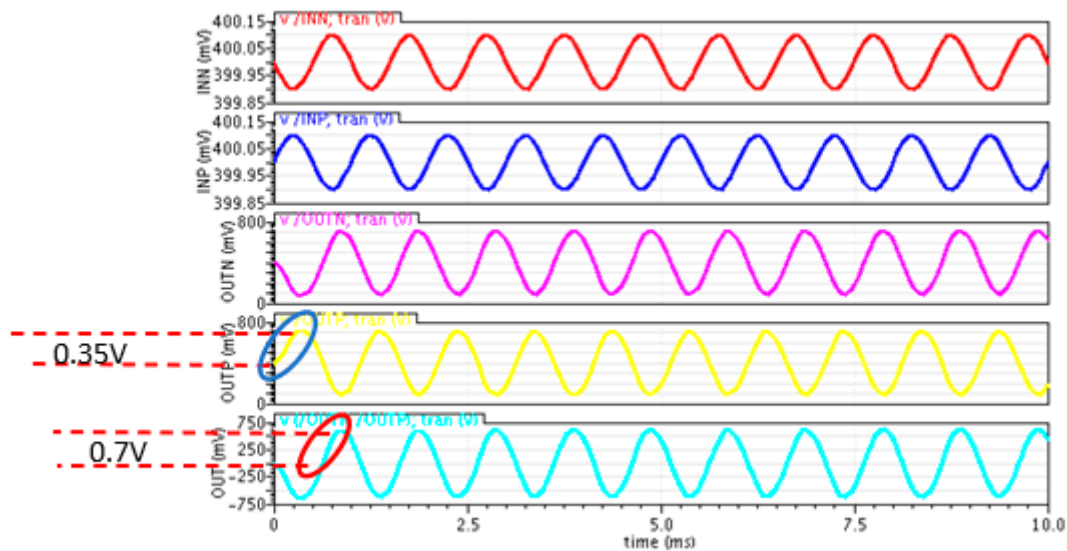


Figure 14. The phase simulation.

### 3.3. Transient Analysis

This paper adds a pair of sinusoidal excitation sources with a DC voltage of 0.6 V, an AC component frequency of 1 KHz, and an amplitude of 200 uV to the differential

input of the op-amp. Moreover, the two sinusoidal excitation sources have opposite phases. The simulation result is shown in Figure 15. The curves in the figure from top to bottom, respectively, represent the input terminals INP and INN; the output terminals OUTP and OUTN; and the final differential output. It can be seen that the unilateral output amplitude of the op-amp is 0.35 V, and the bilateral output amplitude is about 0.7 V. Compared with the supply voltage of 0.8 V, the operational amplifier designed in this article can provide a large output swing.



**Figure 15.** Two-stage op-amp transient simulation.

### 3.4. Common-Mode Rejection Ratio

Call the ratio of the differential-mode gain to the common-mode gain of the operational amplifier the common-mode rejection ratio, abbreviated as *CMRR*, and its expression is:

$$CMRR = \frac{A_D}{A_C} \quad (16)$$

The *CMRR* reflects the ability of the op-amp to suppress common-mode interference [13]. It is generally believed that the higher the *CMRR*, the better the performance of the amplifier circuit. Carry on the differential mode gain simulation and the common-mode gain simulation to the operational amplifier. The results are shown in Figure 16. Know that the common-mode rejection ratio is stable within a certain low-frequency range from Figure 16. At 1 KHz, the common-mode rejection ratio is 109 dB. After the frequency increases to a certain value, its value decreases rapidly.

### 3.5. Noise Analysis

For the simulation of noise performance, the equivalent input noise is generally used to characterize the noise performance of the circuit. The equivalent input noise simulation of the two-stage operational amplifier is shown in Figure 17. The noise is mainly in the low-frequency band, which decreases as the frequency increases, and finally stabilizes. In addition, according to the noise simulation contribution report, the equivalent input noise can be reduced by increasing the length of the PMOS tube in the five-tube OTA circuit. This paper sets the length *L* of the PMOS tube to 4, 5, 6, 7, 8, or 9  $\mu\text{m}$ , and the results are shown in Figure 17. However, the change in the length of the MOS tube inevitably leads to changes in the other performance metrics of the op-amp, and corresponding adjustments should be made according to requirements. Through a careful consideration of input noise and PMOS tube area, this paper chooses the PMOS tube with  $L = 5 \mu\text{m}$ . When the frequency is 100 Hz, the equivalent input noise is  $115\text{nV}/\sqrt{\text{Hz}}$ .

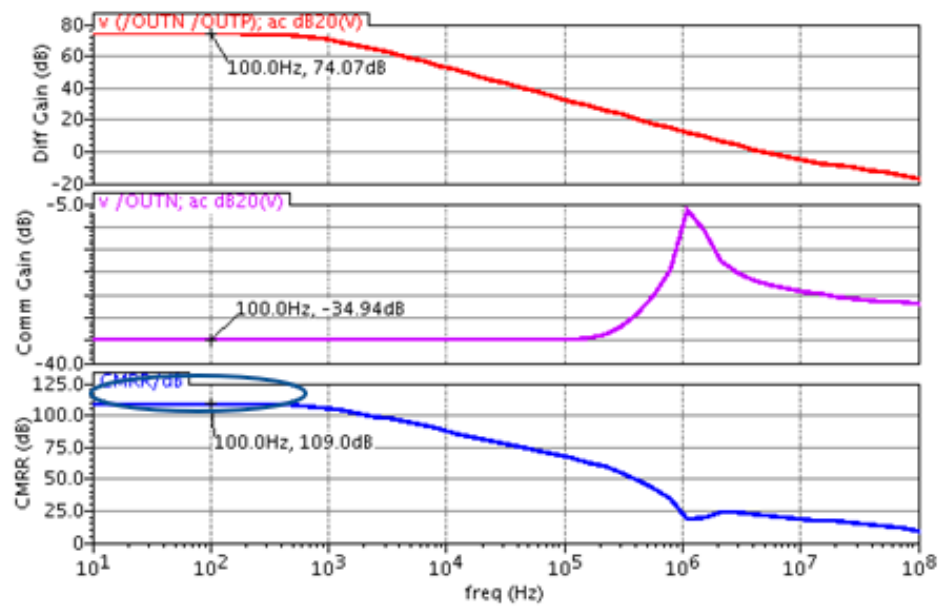


Figure 16. Common-mode rejection ratio simulation.

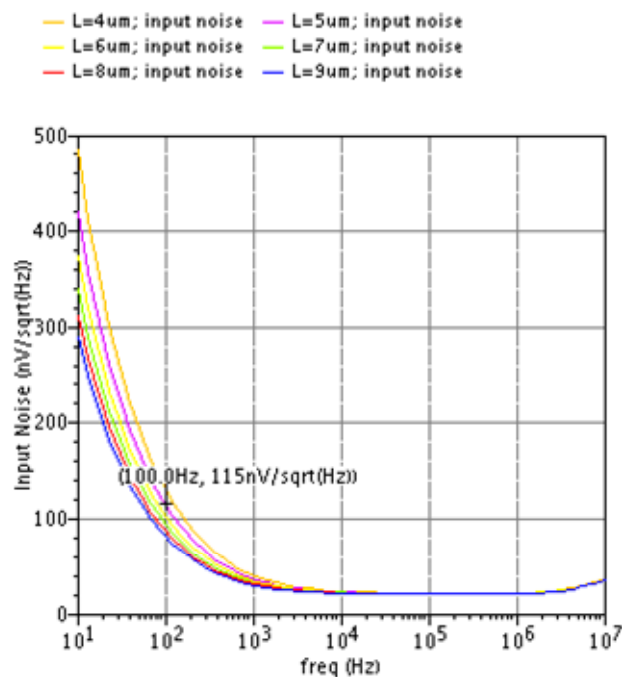


Figure 17. The influence of PMOS length change on input noise.

### 3.6. Response Speed Analysis

The response speed is also one of the crucial indicators used to measure the quality of an op-amp. For the analysis of speed characteristics, two commonly used performance indicators are settling time and slew rate [14]. The setup time reflects how fast the op-amp processes the signal. The shorter the setup time, the faster the op-amp processes the signal. The slew rate reflects the ability of the output to follow the input. This paper inputs a big-step signal at the input end of the op-amp, and observes the voltage at the output end of the op-amp, as shown in Figure 18. The curves in the figure represent the response characteristics of the input terminals INN and INP; and output terminals OUTN and OUTP, respectively. Within the range of 1% stability accuracy, it can be obtained by calculation that the operational amplifier has the following results:

Forward setup time:  $\text{Time}^+ = 640 \text{ ns}$   
 Negative setup time:  $\text{Time}^- = 120 \text{ ns}$   
 Forward slew rate:  $\text{SR}^+ = (1.5450 \text{ V} - 0.7773 \text{ V}) / (0.64 \text{ us}) = 1.19 \text{ V/us}$   
 Negative slew rate:  $\text{SR}^- = (1.5640 \text{ V} - 0.8026 \text{ V}) / (0.12 \text{ us}) = 6.35 \text{ V/us}$

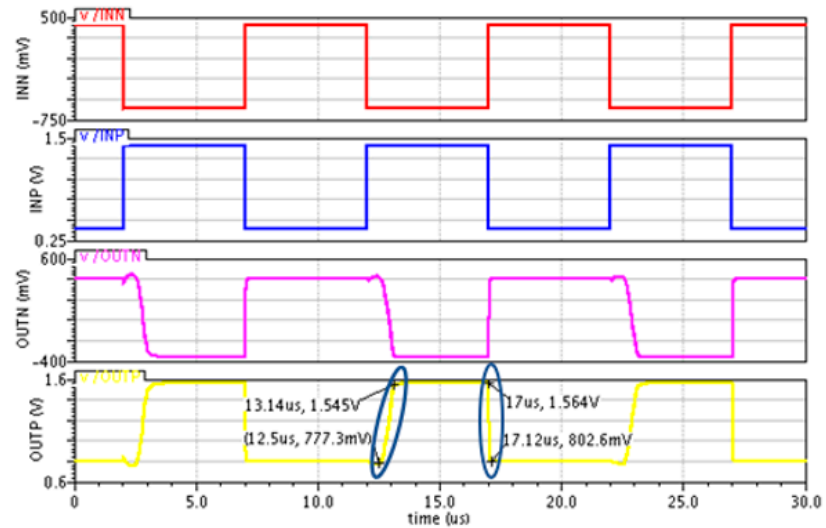


Figure 18. Response speed simulation.

### 3.7. Influence of Temperature and Corner

In order to ensure the robustness of the design, the temperature and corner are simulated. The simulated operational amplifier gain and phase curves are shown in Figures 19 and 20. The temperature range is from  $-100$  to  $100$  °C, with 10 points in the middle. The corners are  $t_t$ ,  $f_f$ ,  $s_s$ ,  $f_s$  and  $s_f$ . In the figure, it can be seen that the temperature and corner have little effect on the gain and phase of the op-amp. The stability is unaffected, indicating that the operational amplifier is robust.

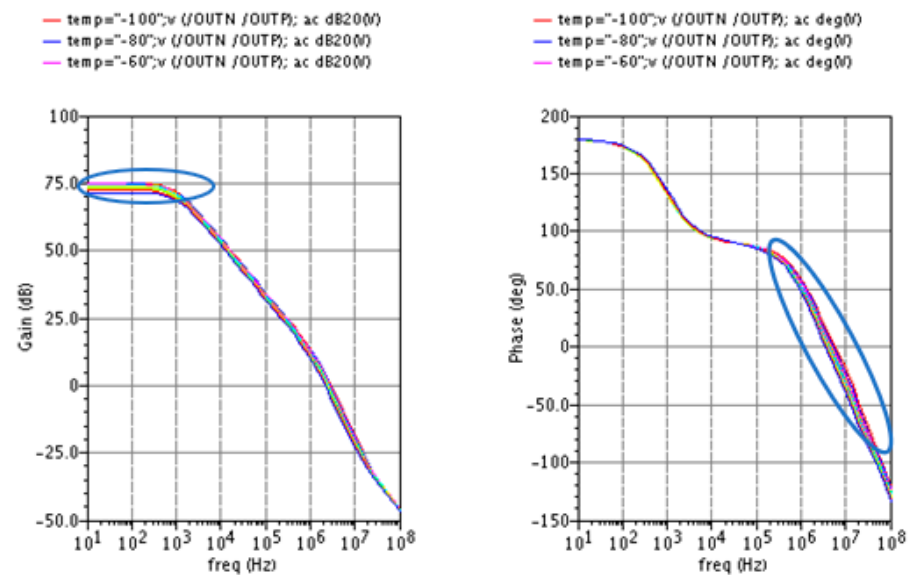


Figure 19. Temperature effect.

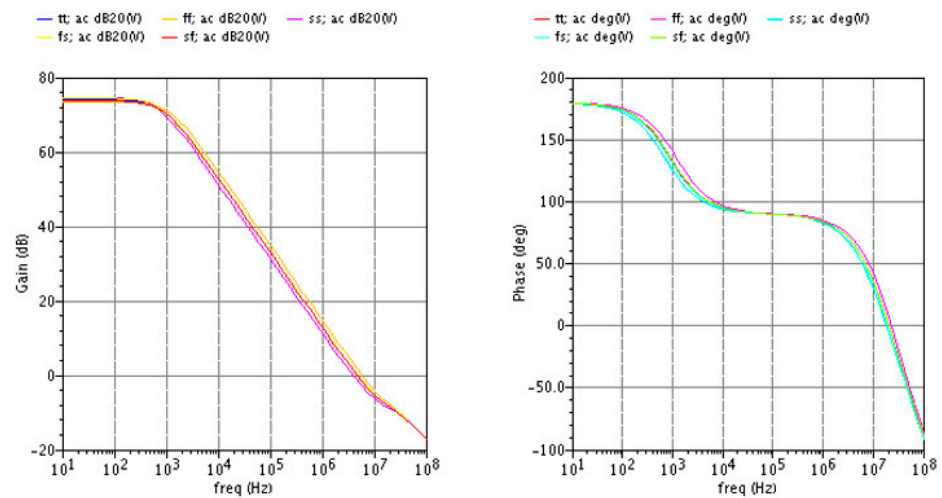


Figure 20. Corner effect.

### 3.8. Power Consumption Analysis

The power consumption of the circuit can be obtained by measuring the current of the op-amp power supply pins. As shown in the Figure 21, a dc scan of the supply voltage is performed to obtain the static current and static power consumption of the op-amp. When  $V_{dd} = 0.8\text{ V}$  and  $I_{vdd} = 13.94\text{ }\mu\text{A}$ , the static power consumption of this op-amp is  $11.2\text{ }\mu\text{W}$ . With the optimization of the circuit structure and the reduction of the supply voltage, the static power consumption of the op-amp is significantly reduced. However, this also sacrifices some other performance, such as gain and bandwidth.

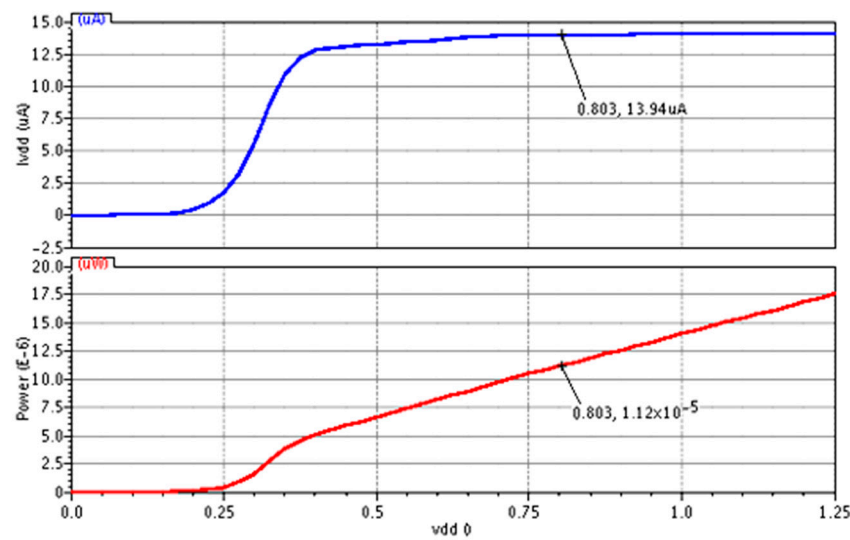


Figure 21. Static current and static power consumption of the op-amp.

## 4. Discussion

Table 1 compares the operational amplifier performance parameters of the design of this article and those of references. Compared with the design in [2], this article’s design has lower power consumption and a higher common-mode rejection ratio, but the gain and stability are weaker. For example, when the frequency is  $1\text{ KHz}$ , the GBW of literature [2] is  $10\text{ MHz}$ , and the GBW of this paper is  $4.75\text{ MHz}$ . Then the gain difference is:  $20\text{ log}(10/4.75) = 6.46\text{ dB}$ . For power consumption, the power consumption of literature [2] is  $230\text{ mW}$ , and the power consumption of this paper is  $0.0112\text{ mW}$ . Then the power consumption difference is:  $10\text{ log}(230/0.0112) = 12.34\text{ dB}$ . It means that this paper only needs to



gain 6.46 dB more and I will obtain 12.34 dB extra in my power consumption. My approach is better than that of literature [2]. Compared with the approaches in the literature [15,16], the paper has lower power consumption and higher gain, but the gain bandwidth and speed performance are weaker. For example, when the frequency is 1 KHz, the difference between the GBW of literature [16] and this paper is:  $20 \log(18.2/4.75) = 11.66$  dB. The difference between the power consumption of literature [16] and that in this paper is:  $10 \log(13.86/0.0112) = 30.92$  dB. It means that we only need to gain 11.66 dB more and I will obtain 30.92 dB extra in power my consumption. Again, the superiority of the method of this paper is proven. When compared to literature [17,18], the low voltage, low power consumption and high gain features of the design in this paper are also highlighted. In conclusion, the circuit designed in this paper has a definite advantage in terms of low power consumption by using a lower supply voltage. The static power consumption is only 3% of the power consumption of the literature [18] and 1‰ of the power consumption of the literature [16]. In addition, the meaning of the trade-off of consumption–response can be understood from the comparison. The “octagonal rule” of the analog design is satisfied.

**Table 1.** The comparison of this op-amp with references.

Operational Amplifier Performance Parameters	Literature [2]	Literature [15]	Literature [16]	Literature [17]	Literature [18]	This Work
Number of stages	2	2	2	3	2	2
Echnology (um)	0.25	0.18	0.18	0.18	0.18	0.13
Vdd (V)	2.2; 5.5	3.3	1.8	1.5	1.8	0.8
Gain (dB)	120	72.21	71.275	70.8	63	74.1
Load Condition (pF)	N/A	N/A	10	30	1.0	3.0
Phase margin (°)	60	50.10	83	60.6	61.8	61
GBW (MHz)	10	10.05	18.2	2.12	0.14	4.75
CMRR (dB)	100	−30	60	N/A	88	109
SR+ (V/us)	6.0	45.45	2.48	1.6	29.7	1.27
SR− (V/us)	5.5	N/A	N/A	N/A	12.6	6.35
Power (mW)	230	0.192	13.86	0.084	0.30	0.0112

## 5. Conclusions

Based on the 0.13 um CMOS technology, this paper designs a low-voltage (0.8 V), high-gain (74.1 dB), ultra-low power operational amplifier. This op-amp has great advantages in terms of low power consumption. The static power consumption is 11.2 uW, which is only 1‰ of the circuit power of the literature [16]. In addition, common-mode feedback and frequency compensation circuits are added to the circuit design to increase the stability of the operational amplifier circuit. Moreover, through the design of the size of the MOS tube, the gain of the circuit is increased. The influence of the channel length effect is reduced. The power consumption is reduced by using a small quiescent current. Through circuit simulation, the phase margin is  $61^\circ$ , the output swing is 0.7 V, the CMRR is 109 dB, the equivalent output noise is  $115\text{nV}/\sqrt{\text{Hz}}$ , and the slew rate is 6.35 V/us. By comparing this paper with the references, it is shown that the op-amp has good performance and excellent robustness. The low voltage and ultra-low power consumption make this op-amp have a broad application prospect in portable wearable devices.

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