


Article

Evaluation of GaN HEMTs in H³TRB Reliability Testing

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Abstract: Gallium Nitride (GaN) power devices can offer better switching performance and higher efficiency than Silicon Carbide (SiC) and Silicon (Si) devices in power electronics applications. GaN has extensively been incorporated in electric vehicle charging stations and power supplies, subjected to harsh environmental conditions. Many reliability studies evaluate GaN power devices through thermal stresses during current conduction or pulsing, with a few focusing on high blocking voltage and high humidity. This paper compares GaN-on-Si High-Electron-Mobility Transistors (HEMT) device characteristics under a High Humidity, High Temperature, Reverse Bias (H³TRB) Test. Twenty-one devices from three manufacturers were subjected to 85 °C and 85% relative humidity while blocking 80% of their voltage rating. Devices from two manufacturers utilize a cascade configuration with a silicon metal-oxide-semiconductor field-effect transistor (MOSFET), while the devices from the third manufacturer are lateral p-GaN HEMTs. Through characterization, three sample devices have exhibited degraded blocking voltage capability. The results of the H³TRB test and potential causes of the failure mode are discussed.

Keywords: power electronics; reliability; wide-bandgap



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1. Introduction

Gallium Nitride (GaN) High-Electron-Mobility Transistors (HEMT) have become favorable devices for power electronics applications due to their high bandgap, mobility, and critical field [1]. GaN devices have lower thermal conductivity than silicon (Si) devices but offer lower overall power dissipation and improved efficiency [2]. Compared to Silicon Carbide (SiC) power devices, commercially available GaN HEMTs have lower blocking voltage capability due to their lateral design. However, they have lower parasitic capacitance, making them suitable for high-frequency operation [3]. The lower blocking voltage for GaN HEMTs can be overcome using modular power converter designs by stacking several low voltage devices for high voltage operation with high efficiency [2]. These characteristics have allowed the development of high-power density and high-efficiency power electronics systems, resulting in GaN HEMTs being heavily integrated into power supplies and fast chargers for EV applications [4]. These applications require high-power density systems that limit the available cooling capacity and thus operate the GaN HEMT at high operating temperatures. Implementing GaN HEMTs in EV charging stations means operating in potentially humid environments. Thus there is great interest in evaluating the reliability of GaN power HEMTs under thermal stresses.

Reliability testing of GaN HEMTs has primarily focused on thermal stresses. A known reliability issue with GaN HEMTs is its dynamic on-state resistance due to hot-carrier injection and trap buffers [5], resulting in higher conduction losses and reduced current conduction. This effect is temperature-dependent and can be suppressed by using a substrate with high thermal conductivity, such as a SiC substrate [6]. However, most GaN HEMTs for power electronics applications are grown on a Si substrate due to cost [4], so reliability tests have focused on thermal stresses induced by a current bias. Several

works in reliability testing of GaN HEMTs evaluated its current capabilities in single or repetitive pulsing [7,8], where the change in its current conduction determines the degradation. Q. Song et al. have evaluated GaN cascode HEMTs under surge current events and transient overvoltage conditions [9]. There have also been works focused on accelerated aging due to thermal stresses from thermal power cycling between 25 and 125 °C [10]. S. Song et al. observed electrical cracks in the degraded devices, corresponding to increased leakage current, while the threshold voltage and on-state resistance have been unaffected [11]. These works have not included a combination of humidity, high temperature, and blocking voltage in their testing, as they can accelerate power devices' failure mechanisms [12].

The High Humidity, High Temperature, Reverse Bias (H^3TRB) accelerated lifetime test evaluates the robustness of the semiconductor device. Humidity can penetrate the device's packaging, causing accelerated cracking and corrosion [12]. The presence of high ambient temperature can further accelerate corrosion once moisture is present in the package [13]. Several works have evaluated Si IGBT modules and discrete devices using the H^3TRB test [14–16] to identify characteristics that help estimate the remaining lifetime. Electrochemical corrosion and electrochemical migration were the primary failure mechanisms of these Si IGBTs [16]. These works have implemented current sensing to monitor the leakage current of the devices during testing. Changes in leakage current are potential signs of accelerated aging of the device or device degradation [17]. An end-of-life H^3TRB reliability study was conducted for 600/650 V enhancement-mode GaN HEMTs [18]. These devices were tested at 85 °C with relative humidity (RH) of 85% and blocking voltage of 480 V, with pauses for device characterization every 500 h. A. Brunko et al. found no device failure unit after 2300 h of testing. The PCB housing for their devices had degraded after 1200 h of testing, highlighting the challenge of conducting reliability testing under humidity. Although different enhancement-mode GaN HEMTs were tested, the discussion about the observed failure modes was limited. The proposed work establishes a testbed to subject commercial GaN HEMTs to an H^3TRB test to evaluate their reliability and to investigate any failure mechanism that arises due to humidity.

This paper presents a comparative study of GaN HEMTs evaluated under the H^3TRB test, following the JEDEC standard JESD22-A101. GaN power devices from three manufacturers were utilized based on blocking voltage and current rating. Seven devices from each manufacturer were selected for a total of twenty-one devices. These devices were placed in an environmental chamber with an ambient temperature of 85 °C and 85% RH while blocking 80% of their voltage rating as part of the JEDEC standard. Their leakage current was monitored for each device under test (DUT) during testing to detect when device failure has occurred. Testing was conducted for one thousand hours. After testing, the characteristics of the devices were measured to identify degradation. The result of the test and potential failure mechanisms are discussed.

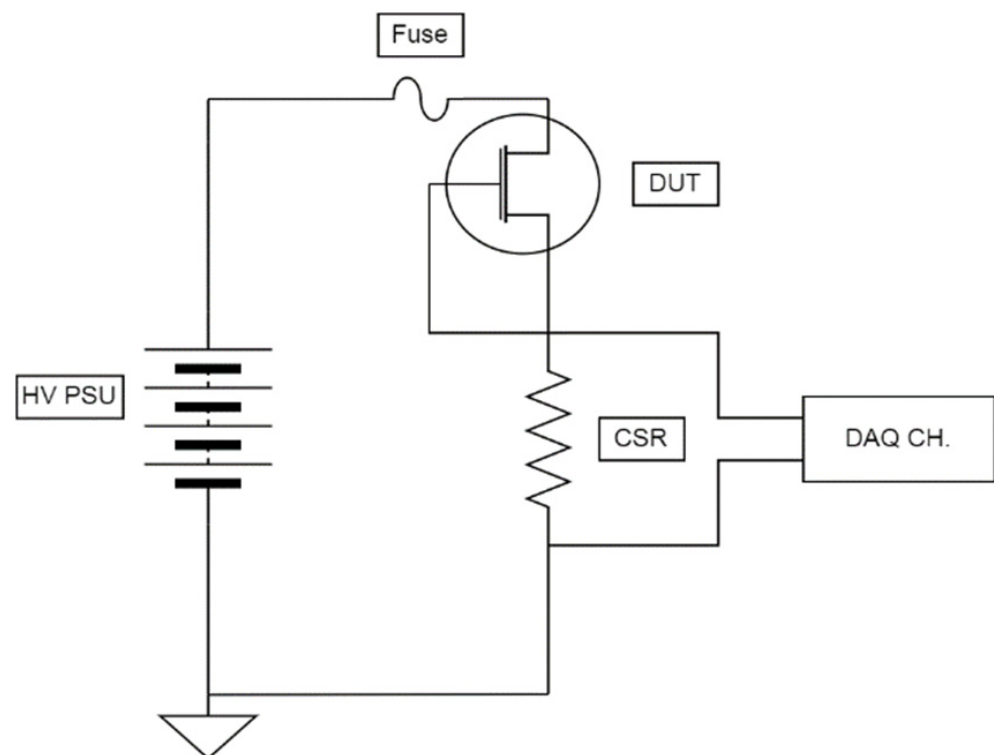
2. Methodology

This section presents the methodology for performing the H^3TRB test on the GaN HEMTs. A sample of twenty-one devices was used for testing, sharing a blocking voltage rating of 650 V and a forward current rating between 30 A and 42 A. Device group D1 consists of TP65H035G4WS from Transphorm, device group D2 consists of GAN063-65WSAQ from Nexperia, and device group D3 consists of GS-065-030 from GaN Systems. Devices from groups "D1" and "D2" utilize a HEMT cascode configuration, where a GaN depletion-mode HEMT is in series with an internal low voltage Si metal–oxide–semiconductor field-effect transistor (MOSFET) to achieve a normally-off transistor device. This topology is the most common among GaN HEMTs for power electronics applications [4]. Devices from group "D3" are p-GaN HEMTs that use a p-type gate to achieve a normally-off device. The main advantage of p-GaN HEMTs over the cascode configuration is direct control of the GaN device and a less complex device structure. However, it has a lower threshold voltage that is prone to instability [19]. Table 1 lists the electrical parameters of the DUTs [20–22].

Table 1. Characteristics of devices under test.

Device Parameter	Group "D1"	Group "D2"	Group "D3"	Unit
Part #	TP65H035WS	GAN063-650WSA	GS-065-030-2-L	
Blocking Voltage	650	650	650	V
Forward Current	46.5	34.5	30	A
On-state Resistance	35	50	50	m Ω
Threshold Voltage	4	3.9	1.7	V
Forward Current @ V_{th}	1	1	10	mA

Each DUT has its biasing circuit consisting of a fuse and a current sense resistor (CSR) for low-side sensing. Figure 1 shows the biasing circuit for a single DUT. A Sorensen XHR 600-1.7 high voltage power supply provides the high voltage bias of 520 V across the drain and source of the DUT, following JEDEC standards. The 200 mA fuse allows the H³TRB test to run uninterrupted from device catastrophic failures. A 100 Ω CSR is utilized to measure the leakage current of each device during testing. The DUTs are mounted onto a daughterboard which allows several devices to be tested simultaneously. An acrylic coating is applied to the daughterboard to withstand operation inside the environmental chamber. High voltage putty was also applied around unused and exposed terminals to minimize the likelihood of voltage breakdown not caused by device degradation. The DUTs are subjected to 85 °C and 85% RH inside a T2RC-A-F4T Environmental Chamber for a thousand hours. Figure 2 shows the overall H³TRB testbed.

**Figure 1.** Schematic of H³TRB testbed.

An NI data acquisition system (USB-6255 myDAQ) measured the voltage drop across the CSR with a sampling rate of 1 sample every 10 s. Fast sampling rates are unnecessary as the devices are DC-biased, and the leakage current is expected to increase gradually. The average leakage current per hour was calculated, and the averaged data are presented in Figure 3.

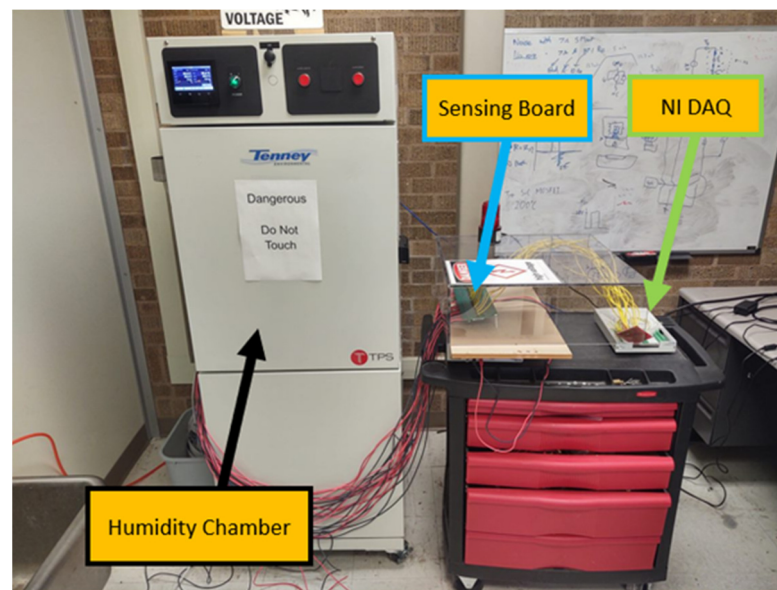


Figure 2. H³TRB testbed.

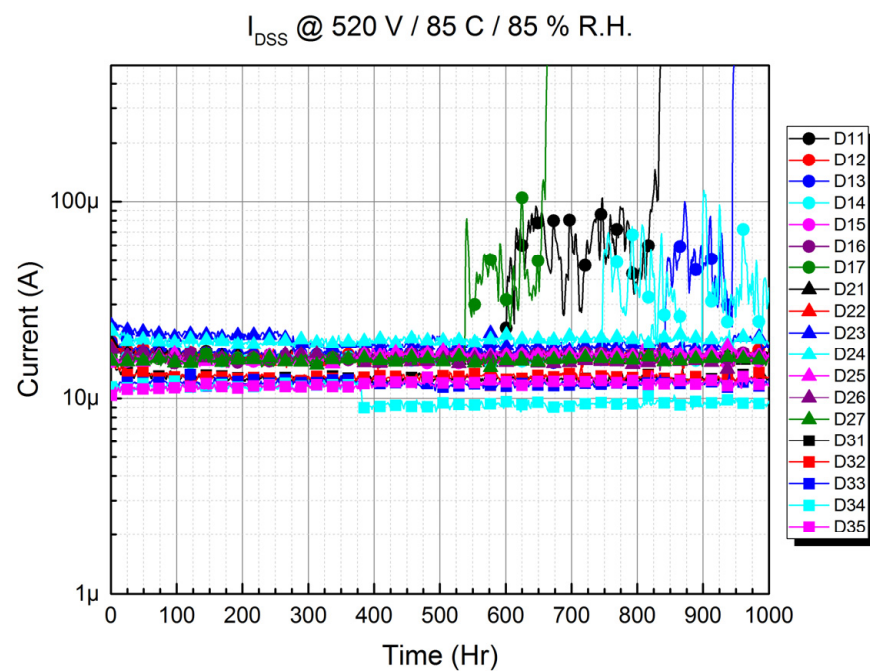


Figure 3. Leakage current of DUT during testing.

The average leakage current for all devices was between 10 μA and 20 μA . Devices “D11”, “D13”, and “D17” exhibit an increase in leakage current before sharply increasing above the leakage current threshold of 200 μA . Table 2 shows a summary of the results from the H³TRB test. The fuses for these three DUTs were blown, suggesting that the devices had shorted during testing. From Figure 3, device “D11” is expected to have shorted 825 h into the test, device “D13” has shorted after 950 h, and device “D17” has shorted after 650 h. Device “D14” has also shown increased leakage current but has not sharply risen above the threshold like the other three devices. Leakage current data are missing for devices “D36” and “D37” due to a software error but were otherwise tested under the same test conditions as the other devices. Out of the sample of devices tested, devices “D11”, “D13”, and “D17” are considered degraded.

Table 2. Summary of H³TRB test.

Device Group	Failure Present	Affected Devices	Issue
D1	Yes	D11, D13, D17	Opened fuse
D2	No	None	None
D3	No	None	None

3. Results

The characterization results of the DUTs are presented. The DUTs were characterized using a B1505A curve tracer before and after the test to identify degraded electrical characteristics. The blocking voltage curve, transfer characteristic curve, gate-source leakage curve, and output characteristic curve was measured for all DUTs.

Figure 4 shows the blocking voltage curve for device group “D1”. For all DUTs except devices “D11”, “D13”, and “D17”, the leakage current is consistent between testing. The breakdown voltage curve for devices “D11”, “D13”, and “D17” quickly increases to the leakage current threshold of 100 μ A, confirming that the devices are unable to hold off voltage in the off state. Device group “D1” utilizes the GaN cascode topology, where the Si MOSFET initially holds off the voltage in the off state. As the blocking voltage increases, the gate-source of the internal GaN HEMT is biased negatively, pinching off its channel and thus allowing the internal GaN HEMT to block voltage. The degraded DUTs’ inability to hold off voltage suggests that either a short is present between the drain and source of the DUT or the DUT’s internal Si MOSFET is damaged. Figure 5 shows the gate-source leakage current for device group “D1”. The gate current is below 40 pA for all devices and between testing. The internal Si MOSFET oxide layer of the degraded devices is intact.

Figure 6 shows the transfer characteristics for device group “D1”. The threshold voltage was measured with a compliance limit of 10 mA on the SMU of the B1505A. The threshold voltage curve for the non-degraded devices is consistent between testing. However, the curve tracer cannot measure the threshold voltage curve for the degraded devices due to its drain current limit.

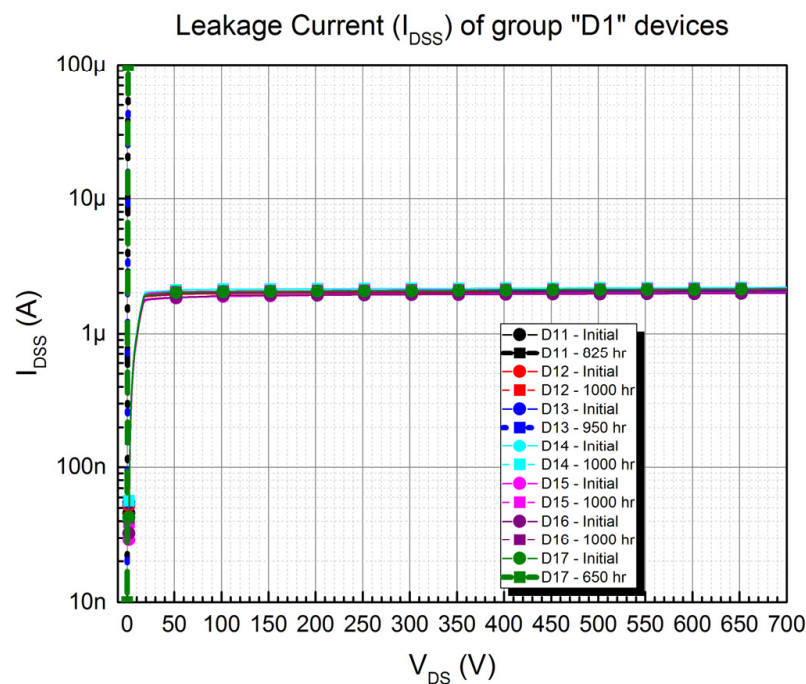


Figure 4. Blocking voltage curve for device group “D1”.

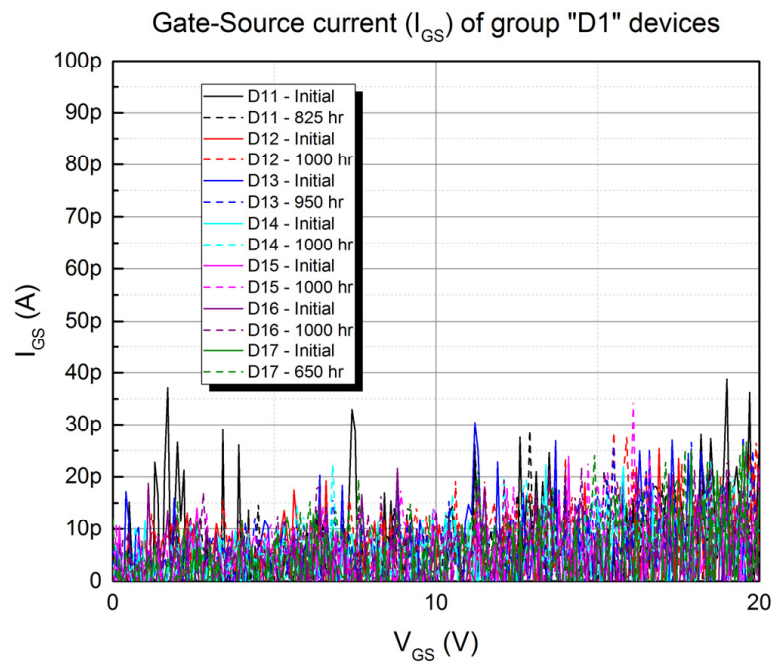


Figure 5. Gate leakage current curve for device group “D1”.

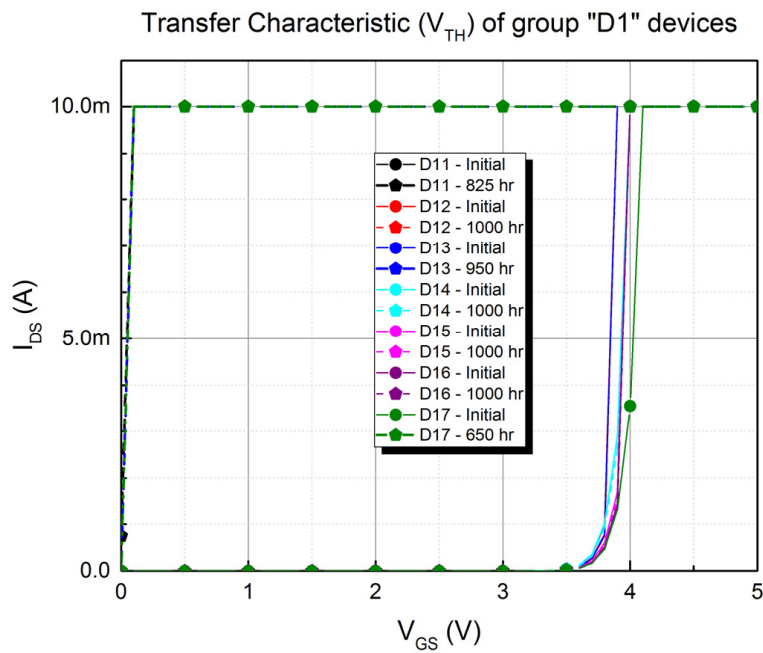


Figure 6. Transfer characteristic curve for device group “D1”.

Figures 7–9 show the output characteristics between testing of the degraded devices “D11”, “D13”, and “D17”, respectively. For all three devices, significant current flow is measured at 0 VGS and 4 VGS, where it was in the off state in the initial characteristics. The forward current reached 6 A, 1 A, and 2 A with a 3 VDS bias at 0 VGS for devices “D11”, “D13”, and “D17”, respectively. However, the forward current of the degraded devices increases approximately to the same level as their initial characteristics at 8 VGS and above. Table 1 and Figure 6 show that the degraded devices’ initial threshold voltage is 4 V. The output characteristic curves show that the internal Si MOSFET channel resistance can be controlled with the gate–source voltage.

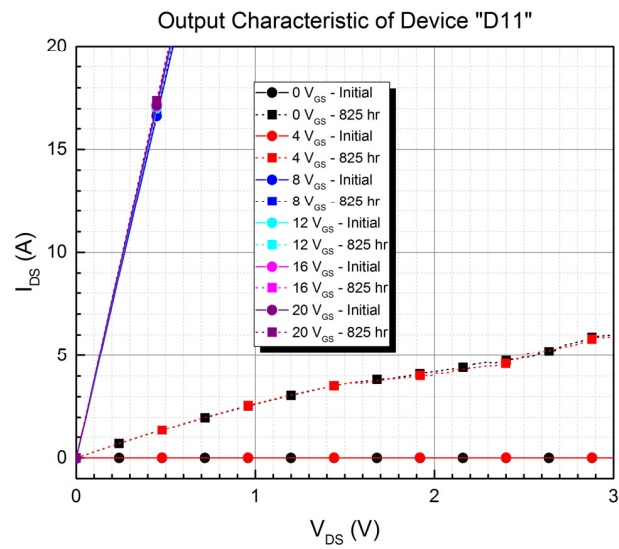


Figure 7. Output characteristic curve of device "D11".

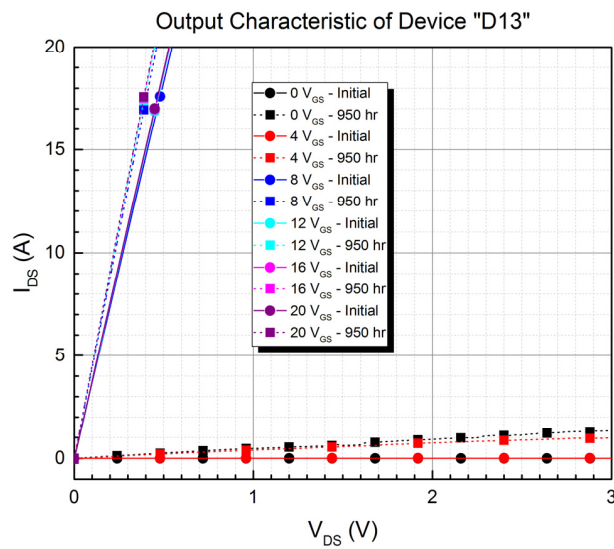


Figure 8. Output characteristic curve of device "D13".

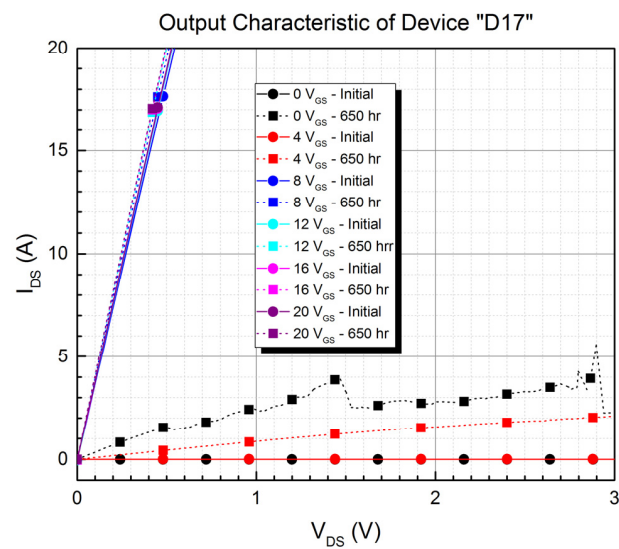


Figure 9. Output characteristic curve of device "D17".

The drain–source resistance was calculated using the same data from the previous output characteristic figures. Figures 10–12 show the drain–source resistance of the degraded devices “D11”, “D13”, and “D17”, respectively. The gate–source voltage was swept from 0 to 20 VGS. The measured drain–source resistance varies between 0.4 and 2.0 Ω from 0 to 4 VGS, whereas at 5 VGS and above, the drain–source resistance drops towards its initial on-state resistance value. The resistance difference between the initial and final on-state resistance was 0.3 mΩ for device “D11”. However, devices “D13” and “D17” have a much more significant drop of 4.0 mΩ and 2.0 mΩ. The overall current-conducting capabilities of the degraded devices were not affected, but their ability to block voltage was.

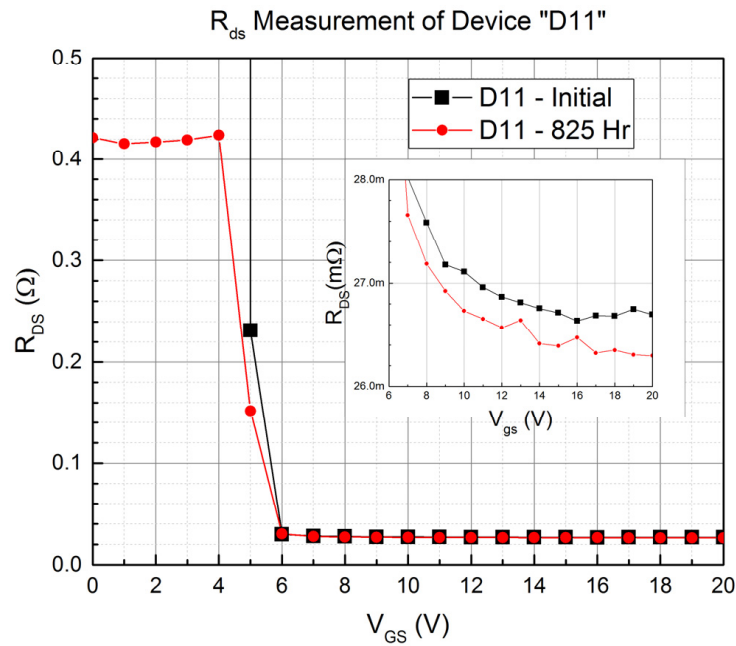


Figure 10. Drain–source resistance curve of device “D11”.

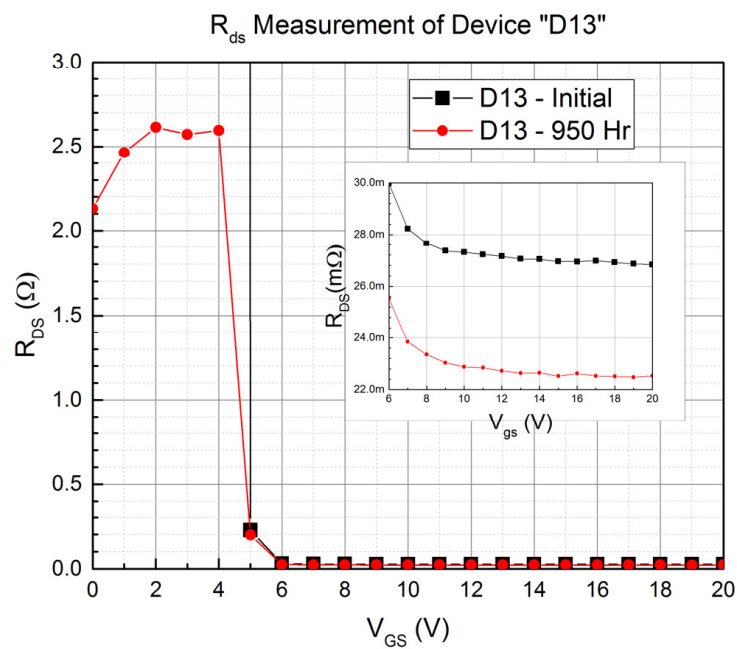


Figure 11. Drain–source resistance curve of device “D13”.

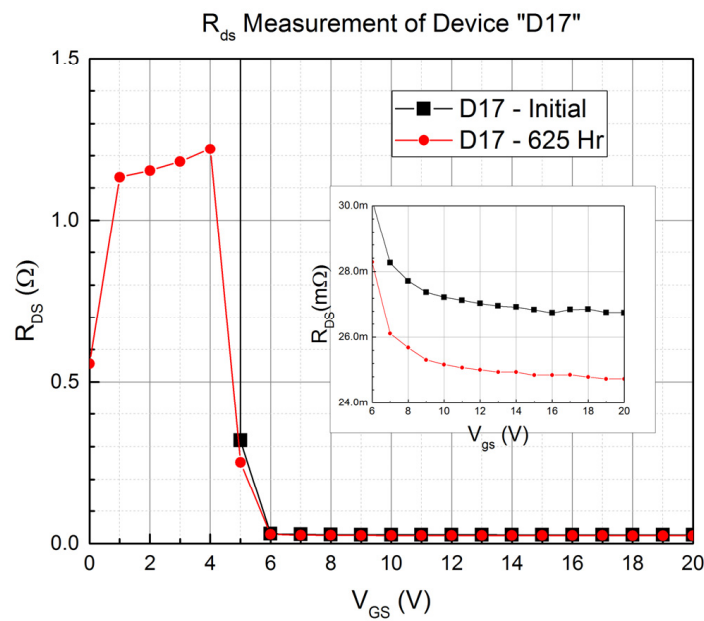


Figure 12. Drain–source resistance curve of device “D17”.

The remaining devices from groups “D2” and “D3” were characterized. Figures 13 and 14 show the blocking voltage curve for device groups “D2” and “D3”, respectively. The leakage current in the figures is consistent between testing. As shown in Figure 3, the leakage current from device groups “D2” and “D3” were constant throughout testing.

Figures 15 and 16 show the transfer characteristic curve for device groups “D2” and “D3”, respectively. The threshold voltage was measured with a compliance limit of 100 mA for device group “D3”. The high compliance limit was set to the threshold voltage at 10 mA following the datasheet specifications of device group D3, while the other two groups specified threshold voltage at 1 mA. While the threshold voltage curve for device group “D2” is consistent between testing, there was an increase in the rate of drain current for devices “D31”, “D32”, “D36”, and “D37”. This increase in the current drain rate suggests that the transconductance has shifted. All devices from device group “D3” have minor threshold voltage shifts up to 0.2 V, and both positive and negative shifts are observed.

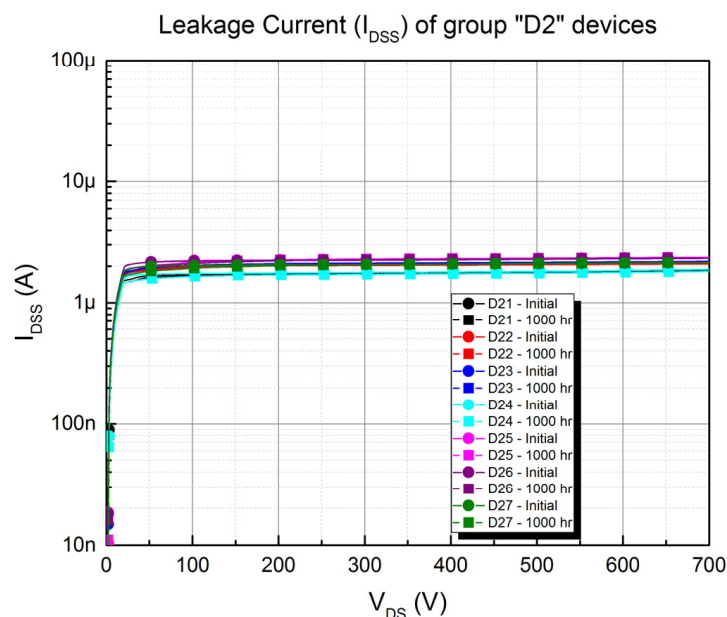


Figure 13. Blocking voltage curve for device group “D2”.

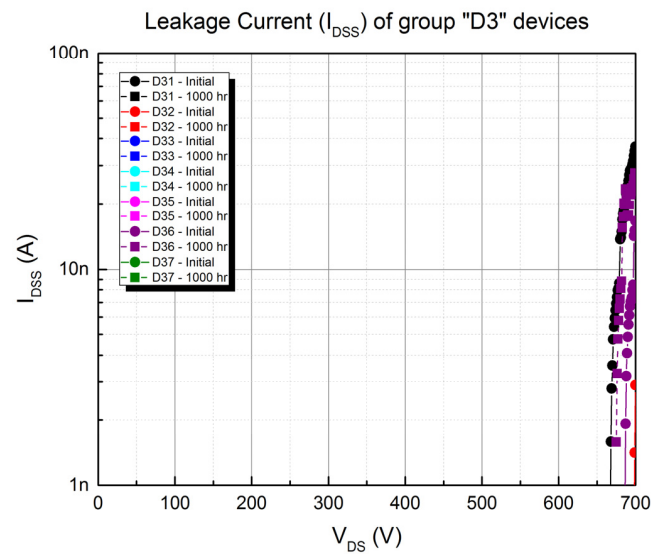


Figure 14. Blocking voltage curve for device group "D3".

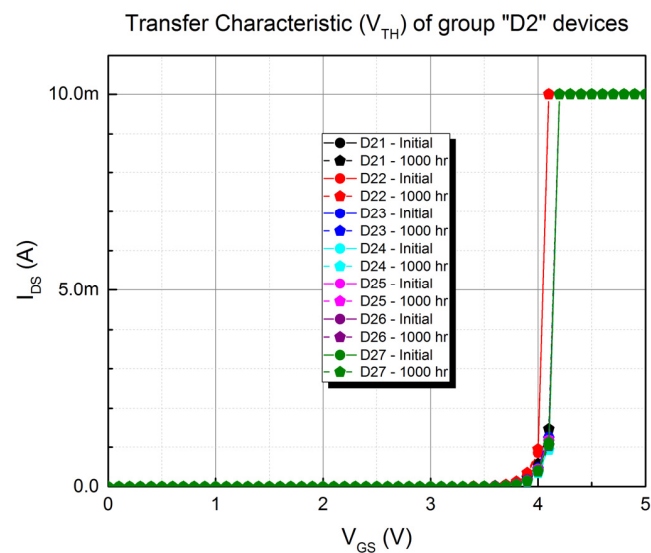


Figure 15. Transfer characteristic curve for device group "D2".

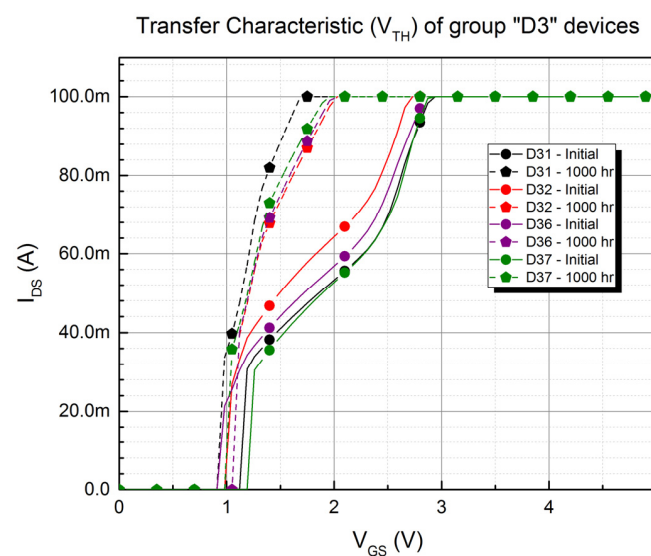


Figure 16. Transfer characteristic curve for device group "D3".

Figures 17 and 18 shows the output characteristic curve of device “D27” and “D37”. Since the previous characterization curves for device group “D2” have not shown any changes, it is expected that all the devices in that group have a similar forward current profile, as shown in Figure 17. An increased current flow is observed for device group “D3” once the gate–source voltage is above the threshold. However, the forward current reaches the same level as the initial characteristics at 3 VGS and above. This behavior is observed for all devices in device group “D3”. The devices’ forward current and blocking voltage capability from device groups “D2” and “D3” have not been affected by the H³TRB test.

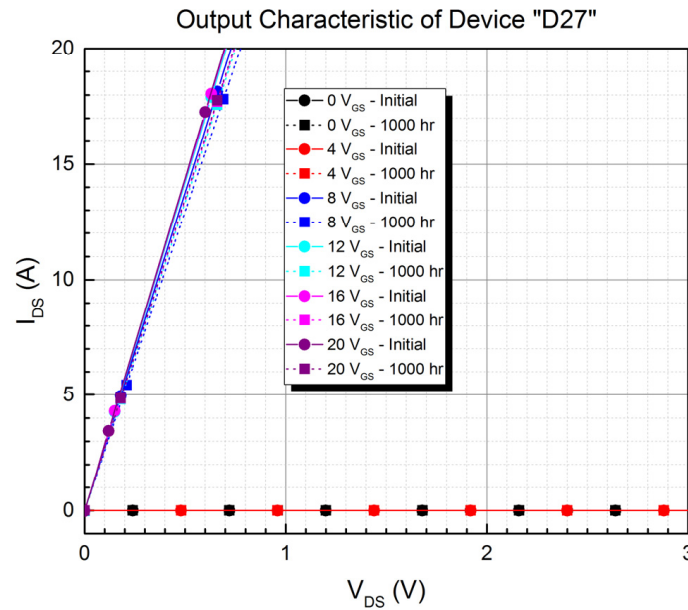


Figure 17. Output characteristic curve of device “D27”.

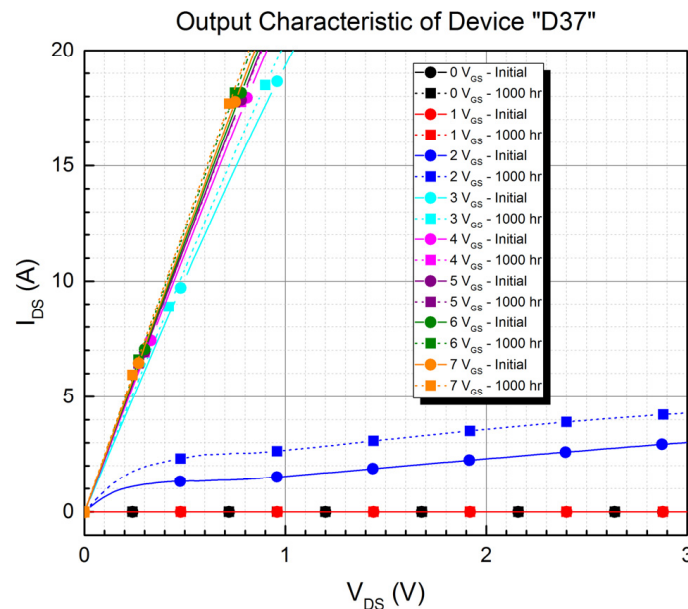


Figure 18. Output characteristic curve of device “D37”.

4. Discussion

Utilizing the output characteristics and drain–source resistance curves of the degraded devices “D11”, “D13”, and “D17”, some inferences can be made about the likely cause of degradation. For each degraded device, the drain–source resistance is between 0.41 Ω and 2.6 Ω when the gate bias is below the initially tested threshold voltage value. However, the

degraded drain–source resistance falls below the initial values once the gate bias surpasses the threshold voltage. This change in drain–source resistance indicates that the internal Si MOSFET is intact and that there is a secondary path between the gate and drain of the internal GaN HEMT that allows current flow when the device is in the off state. Transphorm and Q. Song et al. [9,23] observed and documented this short in their reliability testing and caused dielectric failure in the device when subject to a high electric field. The test conditions of the previous works are different from the presented work. However, all three cases subject the DUT to heat, either localized or from the environment, and a high electric field due to a transient or static voltage bias. Based on the characteristic curves of the degraded devices, it is believed that the failure mode observed in the degraded devices are like the failure modes seen in [9,23].

Although the underlying cause for this failure is known, the results from the presented work still provide novel information on the long-term reliability of GaN HEMTs operating in high humidity, high temperature environments. Similar failure modes have been observed in three different testing environments. The test conditions and time to failure reported by Transphorm are of interest for comparison due to using the same devices. Transphorm provides reliability data under High Temperature Reverse Bias (HTRB) testing following the JEDEC standard JESD22-A108. The devices were biased at 520 V between drain and source with an operating temperature of 150 °C. Transphorm tested 231 devices for qualification, with all devices passing after one thousand hours of testing [24]. When comparing the HTRB results presented by Transphorm to the presented work results, there is a clear distinction between the number of device failures seen. The lower operating temperature of the H³TRB test should result in a significantly longer lifetime. However, more devices failed well before the one thousand hour mark indicating a different factor is a dominant cause for failure. With both tests being held to their respective JEDEC standard, the additional humidity component is the only substantial environmental factor. Thus, it is evident that the presence of high humidity drastically reduces the time to failure of the devices in group “D1”. The high humidity in the environment likely exacerbated this failure mode, as it increases the presence of mobile charges, such as Na⁺ and K⁺, for charge trapping [25,26]. As humidity penetrates the packaging, positive mobile charges attach to the passivation layer on the edge termination, enhancing the local electric field above the critical field of the insulator to create a short [9,27].

Through analyzing the electrical characteristics of the DUTs, some inferences can be made as to possible reasons why the high humidity did not cause any failures in device group “D2”. The difference between the processing techniques of each manufacturer is speculated to create a passivation layer that is less susceptible to defects caused by charge trapping in high humidity environments. As the passivation layer degrades due to charge trapping, these processing techniques influence the enhancements on localized electric fields and whether dielectric breakdown occurs. Such differences include passivation material and implementation of field rings. Simulation work was conducted by R. Natarajan et al. on different passivation materials for GaN HEMT devices and found differences in the electric field distribution, thus influencing the breakdown voltage [28]. From a design perspective, increasing the number of field rings between the gate and drain of the GaN HEMT would better shield the passivation from a high localized electric field [29]. Further investigation into the device structure for device groups “D1” and “D2” is required.

Humidity is also expected to have changed the transfer characteristic curve for some devices in device group “D3”. Unlike GaN cascode HEMTs, p-GaN are more prone to threshold voltage instability issues [19,30–32] due to their Magnesium acceptors [19,31]. Much of the reliability assessment for threshold voltage for wide-bandgap has been under a high temperature, gate bias (HTGB) test [33,34], or gate bias stress under characterization [30,32] for p-GaN HEMTs. Ultimately, performance degradation was not observed in the device group “D3”.

5. Conclusions

This paper evaluates commercial GaN devices under high humidity, high temperature, and high voltage accelerated tests. Twenty-one GaN HEMTs from three manufacturers were tested at 85 °C, 85%, while blocking voltage at 520 V for one thousand hours. Degradation was observed in three devices. Although two manufacturers used similar device topology, all degraded devices were from one manufacturer. The degraded devices could not block voltage, but their forward current capabilities were unaffected. It is suspected that the humidity has accelerated charge trapping in the degraded devices, resulting in higher localized electric fields. It is speculated that the differences seen between device groups “D1” to “D2” are due to either a processing difference in the passivation layer or a design difference in the number of field rings. Future work includes failure analysis of the degraded devices through decapsulation to verify the failure mechanism and an investigation into the device structure of the devices.

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