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Design for Ultrahigh-Density Vertical Phase Change Memory: Proposal and Numerical Investigation

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Abstract: The integration level is a significant index that can be used to characterize the performance of non-volatile memory devices. This paper proposes innovative design schemes for high-density integrated phase change memory (PCM). In these schemes, diploid and four-fold memory units, which are composed of nano-strip film GST-based memory cells, are employed to replace the memory unit of a conventional vertical PCM array. As the phase transformation process of the phase change material involves the coupling of electrical and thermal processes, an in-house electrothermal coupling simulator is developed to analyze the performance of the proposed memory cells and arrays. In the simulator, a proven mathematical model is used to describe the phase change mechanism, with a finite element approach implemented for numerical calculations. The characteristics of the GST-strip-based memory cell are simulated first and compared with a conventional vertical cell, with a decrease of 32% in the reset current amplitude achieved. Next, the influences of geometric parameters on the characteristics of memory cell are investigated systematically. After this, the electrothermal characteristics of the proposed vertical PCM arrays are simulated and the results indicate that they possess both excellent performance and scalability. At last, the integration densities of the proposed design schemes are compared with the reference array, with a maximum time of 5.94 achieved.

Keywords: vertical array architecture; phase change memory; high-density integration; selective circuit; electrothermal simulation

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1. Introduction

Phase change memory (PCM), a promising non-volatile storage technology, along with resistive random access memory (RAM) [1], ferroelectric RAM [2], and magneto-resistive RAM [3], has drawn a lot of attention. Its outstanding embeddability, endurance, stability, and compatibility with the CMOS process make it promising for meeting storage capacity requirements in the big data era [4–6].

The storage component in a PCM cell is composed of a chalcogenide compound, e.g., $Ge_2Sb_2Te_5$ (GST), and the origin of information storage is the electrical contrast between the high resistive amorphous and conductive crystalline states of these phase change materials. The thermally switching phase state of the phase change component makes it possible to write and erase the stored information dynamically. In writing and erasing operations, self-heating and thermoelectric effects occurring in the phase change structure work as heating sources to motivate the temperature increase, i.e., the switching process [7,8]; that is, the PCM performances are intimately linked to the microscopic properties of the phase change materials, and a fully coupled electrothermal mathematical model should be utilized to evaluate the phase transition process [9]. In [10–13], models based on a current continuity equation and thermal conduction equation were developed and validated by comparing the simulated results with measured ones.

To analyze the characteristics of PCM cells, numerical approaches such as finite element time-domain (FETD) and finite difference time-domain methods were employed to numerically discrete the electrothermal coupling mathematical models [10,12]. However, all reported studies focused on the simulation of the performance of PCM cells based on 2-D or 3-D geometric models. In this paper, a coupled FETD method and domain decomposition method (DDM)-based parallel numerical approach is specially implemented to investigate the PCM cells and arrays [12].

The integration density and power dissipation are two key indexes of a PCM device [14,15]. As the phase transition of the PCM mainly depends on the Joule heat generated inside the chalcogenide itself, reducing the size of the phase change region is an effective means to reduce power dissipation. Based on this rule, lots of impressive memory cell designs have been reported in previous studies, such as the mushroom [16], pillar [17], and wall structures [18]. Further, to achieve highly integrated storage devices, 3-D array architectures were proposed by reasonably designing the selective and peripheral circuits [6,19]. The crosspoint (X-point) array is one of the mostly studied and fabricated PCMs, whereby the memory component is connected to a selector device that is located at the crosspoint of the paired electrodes [20]. As reported in [21], an ideal $4F^2$ architecture was possible when a two-terminal selector was implemented. However, the silicon-based selector devices should be made using single-crystal silicon, and it is usually hard to grow single-crystal silicon over a large area on an amorphous oxide. Another promising array architecture is the 3-D vertical chain-cell-type PCM (VCCPCM) [22,23]. Compared with the X-point version, the vertical architecture features the formation of a memory chain in stacked multi-layer gates by using a single mask, and a vertical MOS-like thin film channel was designed to allow the selection of a single memory cell, replacing the selection transistor. These features ensure the excellent scalability of the VCCPCM. In this paper, improved design schemes for high-density integrated PCM based on the conventional architecture are proposed and a performance analysis is carried out utilizing an in-house simulator.

The rest of this article is organized as follows. The geometric architectures of the proposed PCM arrays are presented first in Section 2. Then, the operation sequences, physical model, and numerical computation scheme are outlined. The numerical scheme is implemented to develop an in-house simulator. In Section 3, the electrothermal characteristics of nano-strip PCM cells are systematically investigated using the in-house simulator. In Section 4, the electrothermal characteristics of the proposed arrays are studied and the integration densities of the conventional VCCPCM are presented. Some conclusions are finally drawn in Section 5.

2. Modeling and Numerical Scheme

2.1. Array Architecture

Figure 1 presents the schematics of the conventional PCM array and the separated unit [22]. In this structure, vertical memory chains are uniformly arranged on the bottom electrode array. At the bottom of a vertical memory chain, a chain switch such as a silicon MOSFET and p-n diode is firstly fabricated to ensure flexible activation of a certain vertical chain. The stacked storage units are fabricated on the electrode of the chain switch. Here, the p-n diode is chosen as the chain switch. To further locate the operated memory unit, a poly-Si layer with a thin film insulator layer is fabricated adjacent to the GST layer to form a MOS-like switch. When the switch is in "on" state, the conductivity of the poly-Si channel is much larger than that of the GST film, and almost all of the current flows through the poly-Si channel. In the opposite state, the conductivity of the poly-Si channel is much smaller that the GST film. The current that flows through the GST film can induce a phase change, i.e., a writing or erasing operation. Consequently, by applying the bias voltage to the adjacent gate electrode plane, the chosen memory cell can be operated.

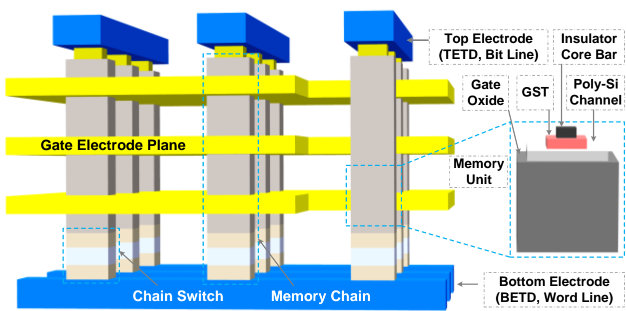

Figure 1. Schematic of a conventional 3-D vertical PCM array.

To improve the integration density of the PCM array, two innovative design schemes are proposed. The architectures of the improved PCM arrays are shown in Figure 2a,b, where diploid and four-fold memory units are designed to replace the unit in the conventional array. The diploid unit and four-fold unit are composed of two and four nano-strip GST film memory cells, respectively. The lateral and cross-sectional views of the nano-strip GST film memory cell are illustrated in Figure 3. A poly-Si thin-film-based MOS-like switch is also designed to work as the unit switch.

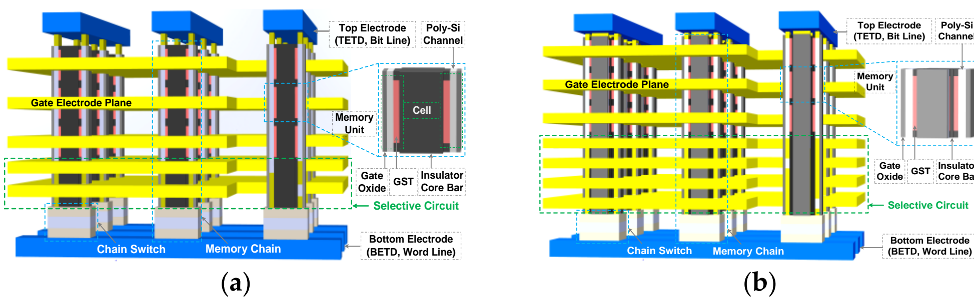

Figure 2. Schematics of the proposed vertical PCM arrays with a (**a**) diploid unit and (**b**) four-fold unit.

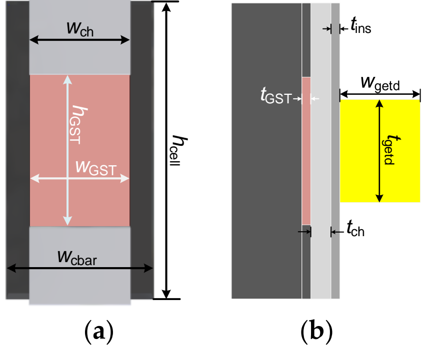

Figure 3. Schematics of the proposed PCM cell: (**a**) top view; (**b**) side view.

However, these polycell units would bring a challenge to the selection operation process, as the switch framework in the conventional array structure cannot select a specified cell in a single memory unit. To overcome this issue, an additional selective circuit is designed and integrated into the array architecture, as shown in Figure 2. In the array with the diploid unit, a dual-layer selective circuit is added. One of the two current channels in the same layer is designed to be a poly-Si-based MOS-like switch and another is filled with a thin metal film. The opposite configuration is assigned to the other layer. In this way, the switch between the two current channels can be separately controlled, and the designated memory cell can be located. In other words, the improved switch framework, which is composed of a memory chain switch, unit switch, and additional selective circuit, can locate to any designated memory cell in the array through a specific switch configuration. Similarly, in the array composed of four-fold units, an additional four-layer selective circuit

is integrated to realize the operation of the designated memory cell, as shown in Figure 2b. The definitions and values of the geometric parameters are given in Table 1.

Table 1. Geometric parameters of the PCM cells and arrays.

Parameter	Definition	Value
w_{cbar}	Width of core insulator bar	28 nm
h_{cell}	Height of memory unit	54 nm
t_{ch}	Thickness of poly-Si channel	7.5 nm
w_{ch}	Width of poly-Si channel	24 nm
t_{ins}	Thickness of gate insulator layer	4 nm
t_{getd}	Height of crossgate electrode	25 nm
w_{getd}	Space between two memory chain	20 nm
h_{GST}	Height of storage film	25 nm
w_{GST}	Width of a storage film	24 nm
t_{GST}	Thickness of storage film	2 nm

The operation sequences of the proposed PCM arrays are illustrated in Figure 4. To achieve information writing and erasing of the designated memory cell, the selection framework should be configured appropriately. A nominal bias voltage and reference voltage are applied to the top and bottom electrode line pair of the selected memory chain to turn on the chain switch. At the same time, a bias voltage V_{off} is applied to both the gate electrode planes of the unit switch and the related selective circuit layer. As shown in Figure 4a, the bias voltage V_{off} applied to the second electrode of the selective circuit turns the left poly-Si channel off, and the current flows through the right channel. Meanwhile, the bias voltage V_{off} applied to the second gate electrode plane turns the unit switch off (high-impedance state) and the current route is changed. The resulting current path is indicated by the blue line. The operation sequence for the array with the four-fold unit is illustrated in Figure 4b, and a similar biasing configuration is utilized to achieve the required current path.

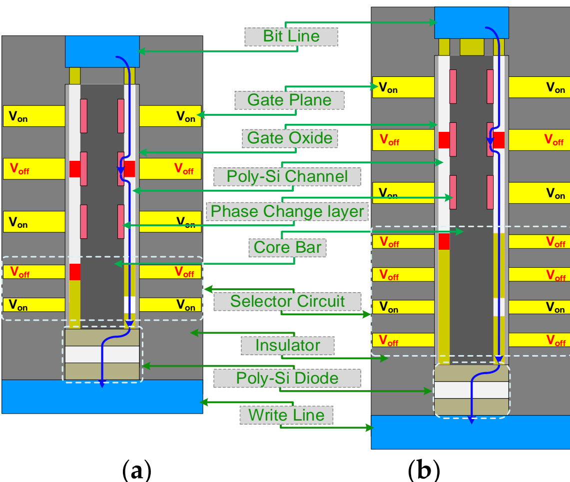

Figure 4. Operation sequences of the proposed PCM arrays: (**a**) diploid unit array; (**b**) four-fold unit array.

2.2. Model and Solution

To describe the physical mechanism of the phase state transformation in the PCM, an electrothermal mathematic model in which the current continuity equation is coupled with the Fourier heat equation is utilized. In this paper, an in-house simulator is developed to conduct the simulation of the proposed PCM cells and arrays. The architecture of the in-house simulator is presented in Figure 5, where the finite element method is employed to numerically solve the electrothermal mathematic model. To solve the current continuity

equation, the Dirichlet boundary condition (i.e., $V = V_o$) and the impedance boundary condition (i.e., $\vec{n} \cdot \sigma \nabla V = V/(RA)$) are used, where R and A are the surface resistance and cross-sectional area, respectively. In these simulations, the selectors are modeled as a cube with equivalent high and low conductivity for on and off states, respectively. In the solution of the Fourier heat equation, the thermoelectric effect is included by adding the Peltier heating $Q_P = T\vec{J} \cdot \nabla S(T)$ to the left-hand side of the equation [12]. Meanwhile, the equivalent thermal resistance boundary models are assigned to the contact boundary between the different materials [24]. In addition, a non-linear material model library is included in the in-house simulator to characterize the influence of the physical fields on the material properties and to serve as coupling paths between electric and thermal fields [25–27]. The influences of geometry-induced quantum effects presented in [28] are not included in this work.

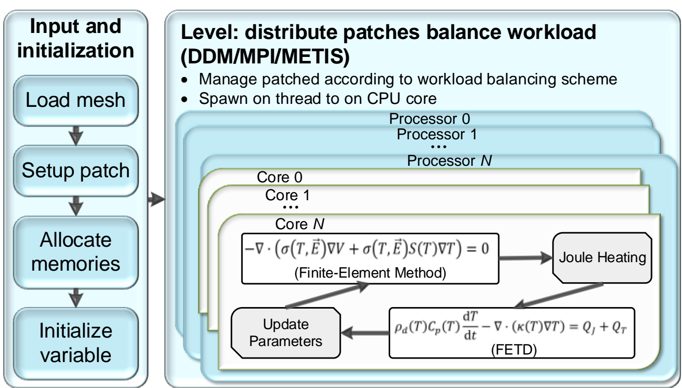

Figure 5. Hierarchical structure of the developed parallel simulator.

On the other hand, parallel computation is a powerful way to solve large-scale problems. In this paper, the J parallel adaptive unstructured mesh applications infrastructure (JAUMIN) is employed to implement the parallel computing [29]. With the help of the METIS software package, the whole computational domain is divided into a number of small subdomains and the electrothermal coupling problem is solved separately on each subdomain [30]. Meanwhile, the massage passing interface (MPI) parallel programming scheme is implemented to minimize the number of successive subdomains and improve the efficiency of the information interaction. The reliability and performance of the in-house-developed parallel simulator was evaluated in our previous paper [12].

3. Electrothermal Simulation of PCM Cells

To implement the information writing and erasing phases in a PCM cell, the reset and set operations should be performed. During the reset operation, the GST in the crystalline state is amorphized via melting using high-power pulse injection (~873 K), followed by rapid solidification to prevent state reversion. To reset the PCM cell, the GST is crystallized via heating above the glass transition temperature (~428 K). The maximum temperature of the reset operation is much higher than that of the set operation; therefore, only the reset operation is investigated here. In this section, the reset operation of the nano-strip film PCM cells is simulated using the in-house simulator. A short trapezoidal current pulse with a 2 ns duration and 0.2 ns rising–falling time is injected into the GST film to melt it via self-heating. The performance of the nano-strip film PCM cell is first compared with that of a conventional vertical PCM cell, and then the influences of geometric parameters h_{GST} and w_{GST} on the PCM cells' characteristics are studied. In the simulations, the channel width w_{ch} is in step with w_{GST}. The characteristics of nano-strip film PCM cells with different h_{GST} and w_{GST} are finally concluded.

3.1. Characteristics of PCM Cells

The electrothermal characteristics of nano-strip film PCM cells with the dimensions given in Table 1 are simulated and compared with those of the reference vertical PCM cell shown in Figure 1. The width of the core bar and GST film and the thicknesses of the GST film, poly-Si channel and insulator layer are set to be 28 nm, 24 nm, 2 nm, 7.5 nm, and 4 nm, respectively, which ensures that the cross-sectional areas of the GST film in the proposed and reference PCM cells are calculated to be 48 nm^2.

The simulated results of two types of PCM cells are presented in Figure 6, where I_{reset} indicates the reset current pulse amplitude, T_{max} is the maximum temperature, and R_{set} and R_{reset} are the cell resistances of the set and reset states, respectively. Here, the resistance ratio of a PCM cell is R_{reset}/R_{set}, and the reset current is the amplitude of the current pulse, which can achieve a resistance ratio of 700 ± 5. The maximum temperature and reset resistance versus the current pulse amplitude are shown in Figure 6a,b, respectively. It is evident that the I_{reset} of the nano-strip film cell is 32% smaller than that of the conventional cell. This is mainly because the effective GST thickness in the four corners of the square loop is about 2.8 nm, which is 1.4 times thicker than the thickness of the nano-strip. The larger reset current would also result in a higher maximum temperature in the conventional cell than that in the nano-strip cell, thereby increasing the potential for thermal crosstalk.

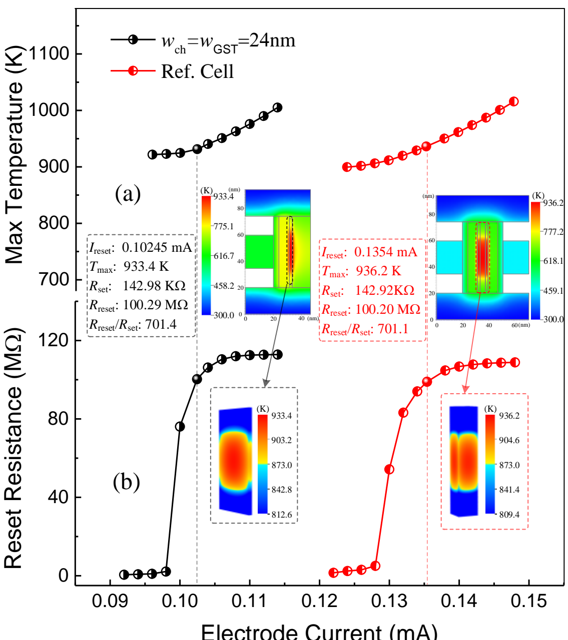

Figure 6. (**a**) Maximum temperature and (**b**) reset resistance of norm and stripe cells versus the reset current pulse amplitude. The inserts show the temperature distributions on symmetrical cross-sections and 3-D GST strips of cells at t = 1.8 ns.

Moreover, with the increase in current amplitude, an inflection point appears in the reset resistance curve. This is because the temperature is at a maximum at the center point of the GST component and decreases with the distance from the center, i.e., the region around the center of the GST component will be amorphized first, then the amorphized region extends outward with the increasing input power. Before the middle part of the GST film is totally amorphized, the total resistance can be treated as a parallel of R_{reset} and R_{set} and is dominated by R_{set}, while at the time that the amorphized region reaches the side boundary of the film, R_{reset} becomes dominant, as shown in Figure 7.

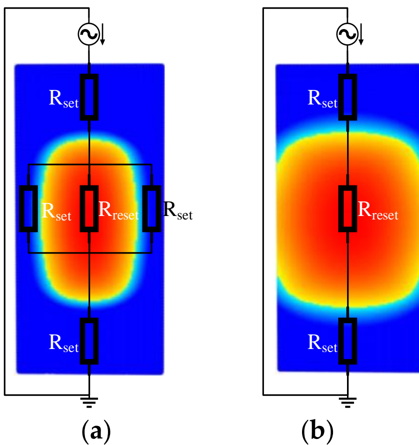

Figure 7. Amorphized regions and equivalent circuit models of GST film with different input current pulses: (**a**) I_{reset} = 0.96 mA; (**b**) I_{reset} = 0.1095 mA.

3.2. Scaling Effect of Cells

Here, the influences of geometric parameters h_{GST} and w_{GST} on the cell characteristics are studied. In Figure 8, the reset resistance and the resistance ratio curves of nano-strip cells with different h_{GST} values (15 nm, 20 nm, and 25 nm) versus the current pulse amplitude are presented. It is evident that the set and reset resistances are in proportion to h_{GST}, which is mainly because the resistance of a conducting wire is proportional to its length. In Figure 8b, the resistance ratio curves versus the current amplitudes for all three cases obey a similar regular pattern. However, the reset current pulse amplitude is increased from 0.1095 mA to 0.1199 mA with h_{GST} decreasing from 25 nm to 15 nm, as given in Figure 8c–e.

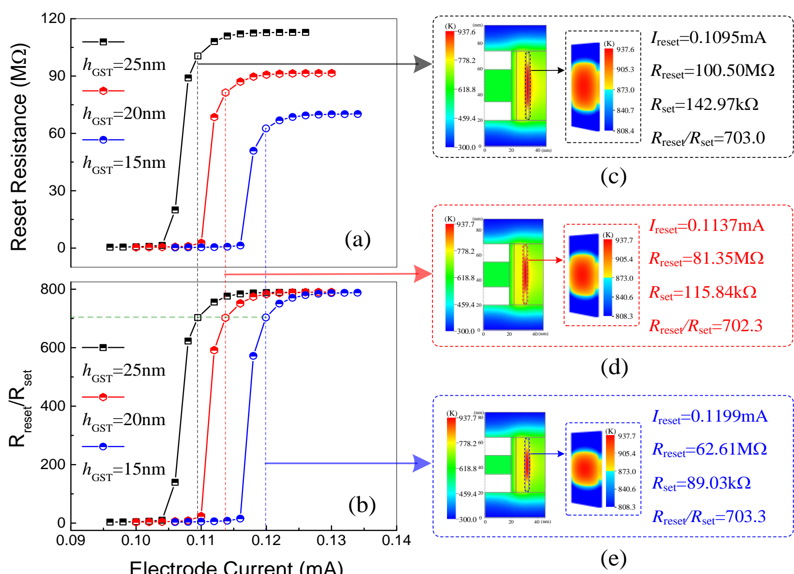

Figure 8. (**a**) Reset resistance and (**b**) resistance ratio of cells with different h_{GST} values. (**c**–**e**) The temperature distributions on symmetrical cross-sections and 3-D GST strips at t = 1.8 ns.

The reset resistance, resistance ratio, amorphized volume, and maximum temperature curves of the cells with different values of w_{GST} (24 nm, 18 nm, and 12 nm) versus the current amplitude are presented in Figure 9a–d. It is shown that with the decreasing w_{GST}, a dramatic decrease in the reset current amplitude from 0.1095 mA to 0.0606 mA is achieved, and the maximum temperature drops from ~938K to ~922K. This is mainly because the smaller the w_{GST}, the faster the amorphized region reaching the side boundary of GST film. At the same time, the decrease in the amorphized volume and the inverse increase in reset resistance result from the decrease in the cross-sectional area of the GST film.

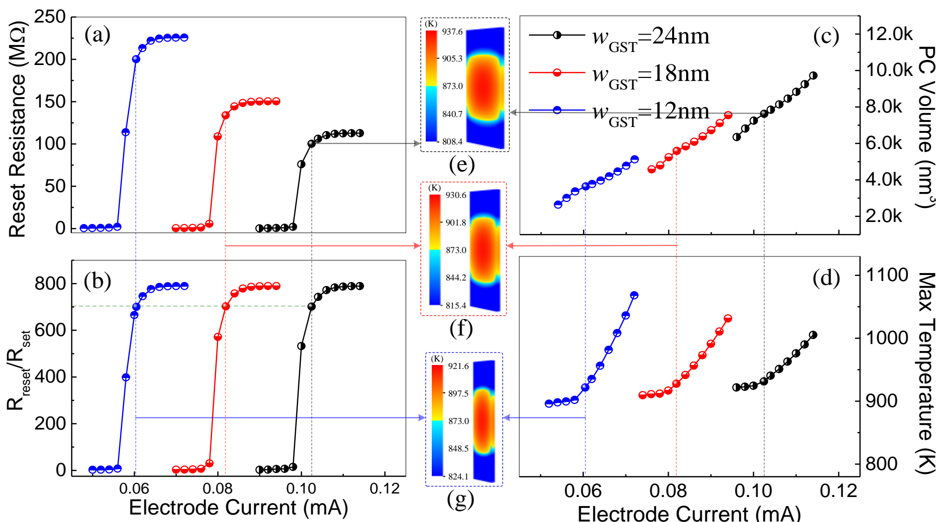

Figure 9. (**a**) Reset resistance, (**b**) resistance ratio, (**c**) phase change volume, and (**d**) maximum temperature values of cells with different w_{ch}. (**e**–**g**) The temperature distributions of 3-D GST strips at $t = 1.8$ ns.

The characteristics of PCM cells with different h_{GST} and w_{GST} values are summarized in Table 2, with the following information concluded:

(a) I_{reset}, T_{max}, the reset power W_{reset}, and the amorphized volume V_a are in proportion to w_{GST}, while R_{set} and R_{reset} are in inversely proportional for specific h_{GST} values;
(b) R_{set}, R_{reset}, W_{reset}, and V_a are proportional to h_{GST} and an inverse trend can be observed in I_{reset} for specific w_{GST} values;
(c) T_{max} for cells with the same w_{GST} remains stable.

Table 2. Simulated results of the PCM cells with different w_{GST} and h_{GST} values.

w_{GST} (nm)	w_{ch} (nm)	h_{GST} (nm)	I_{reset} (mA)	R_{reset} (MΩ)	R_{set} (kΩ)	R_{reset}/R_{set}	T_{max} (K)	W_{reset} (J)	V_{pc} (nm³)
12	12	15	0.0660	124.97	178.13	701.6	922.4	5.735×10^{-14}	2.307×10^{-24}
		20	0.0629	162.43	231.64	701.2	922.2	6.537×10^{-14}	2.974×10^{-24}
		25	0.0606	200.40	285.23	702.6	921.9	7.314×10^{-14}	3.645×10^{-24}
18	18	15	0.0926	83.37	118.74	702.3	930.6	7.622×10^{-14}	5.609×10^{-24}
		20	0.0881	108.78	154.82	702.6	930.6	8.650×10^{-14}	4.591×10^{-24}
		25	0.0849	134.12	190.65	703.5	930.6	9.675×10^{-14}	5.593×10^{-24}
24	24	15	0.1199	62.61	89.03	703.3	937.7	9.598×10^{-14}	4.956×10^{-24}
		20	0.1137	81.35	115.84	702.3	937.7	1.084×10^{-13}	6.248×10^{-24}
		25	0.1095	100.50	142.97	703.0	937.6	1.212×10^{-13}	7.610×10^{-24}

4. Electrothermal Simulation of PCM Arrays

This section presents an electrothermal simulation of the PCM arrays. The influences of geometric parameters w_{GST} and w_{getd} on the performance are analyzed. The integration densities of the proposed arrays referring to the vertical array reported in [22] are estimated.

4.1. Array with Diploid Unit

The electrothermal properties of the 3 × 3 × 3 array composed of diploid units are simulated. In the simulation, one of the memory cells of the diploid unit located in the second layer of the middle memory chain is activated. The obtained temperature distributions on the *yz*-plane cross-section, 3-D structure, and *zx*-plane cross-section of the array with $w_{GST} = 12$ nm are presented in Figure 10a–c. It is evident that thermal crosstalk occurs in adjacent cells. To further illustrate the influence of thermal crosstalk,

the temperature distributions on lines through the weight point of the activated cell's GST component along the coordinate axis are extracted and shown in Figure 11. The simulated results show that the thermal-crosstalk-induced temperature increases in adjacent cells are much lower than the crystalized temperature of the amorphous GST, i.e., 423 K.

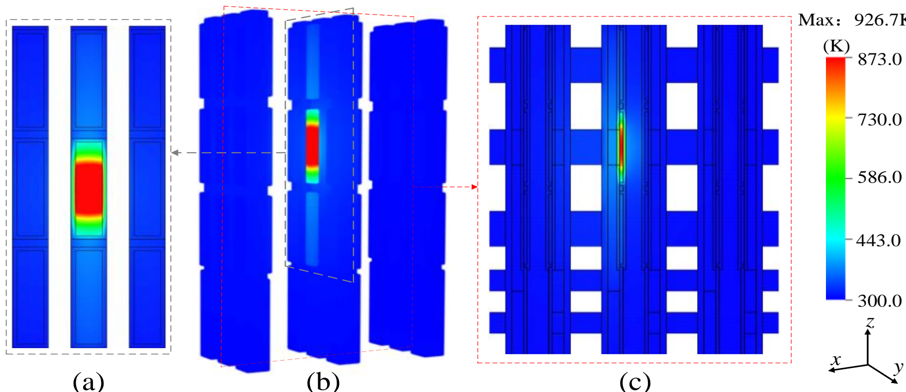

Figure 10. Temperature distributions of a PCM array composed of a diploid unit with $w_{GST} = 12$ nm: (**a**) cross-section in *yz*-plane; (**b**) 3-D structure; (**c**) cross-section in *zx*-plane.

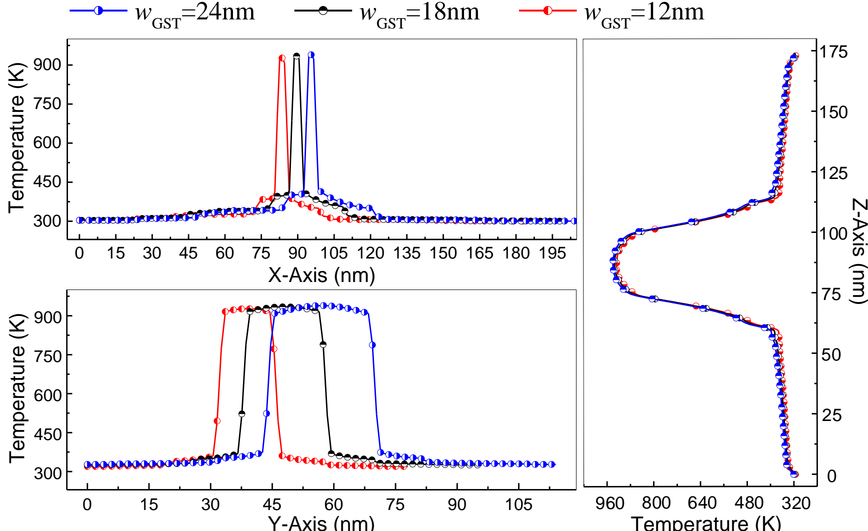

Figure 11. Temperature distributions on lines through the center point of the GST structure of the activated cell along the axis with changing w_{GST} values.

Further, the influence of w_{getd} on the electrothermal properties of the arrays is studied here, and w_{GST} is set as 12 nm. Figure 12 shows the temperature distributions on lines along the *x*-axis and *y*-axis. The inserts in Figure 12a,b show the temperature distributions of adjacent cells in *x*- and *y*-directions. It can be observed that the temperatures in adjacent cells increase slightly with the decreasing w_{getd}. For example, the maximum temperature in the cell to the right of the activated cell along *x*-direction increases from 320.4 K to 325.9 K as w_{getd} decreases from 20 nm to 10 nm. However, the temperature increases are small and the maximum temperatures in victim cells for all cases are much lower than the crystalized temperature of GST, indicating that the integration density can be improved by decreasing w_{getd}.

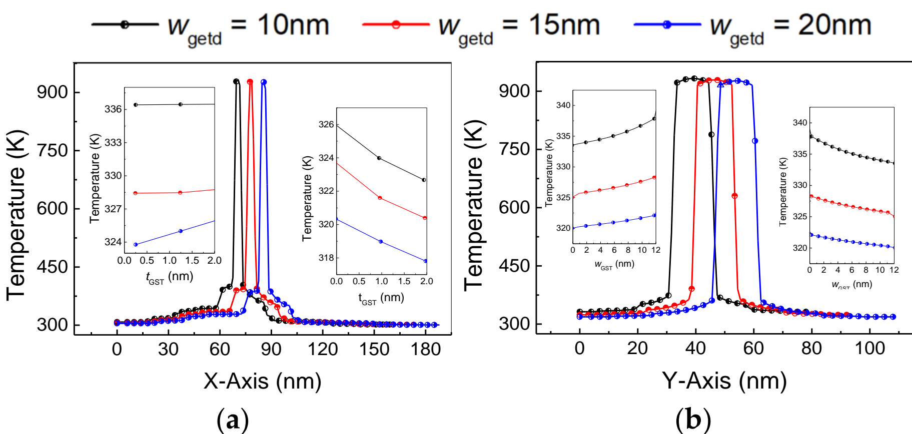

Figure 12. Temperature distributions on lines through the center point of the GST structure of the activated cell along the axis with changing h_{GST} values: (**a**) temperature distributions along x-axis; (**b**) temperature distributions along y-axis.

4.2. Array with Folder Unit

In this subsection, the influences of w_{GST} and w_{getd} on the electrothermal characteristics of the $3 \times 3 \times 3$ array composed of four-fold units are investigated. Similarly, one of the memory cells located in the second layer of the middle memory chain is activated. Figure 13 shows the temperature distributions in the array with $w_{GST} = 12$ nm, and thermal crosstalk can be observed in adjacent cells. In Figure 14, the temperature distributions on lines through the weight point of the activated cell's GST component are presented to further illustrate the influence of thermal crosstalk on the victim cells. Similar to the previous results, the simulated results indicate that the thermal-crosstalk-induced temperature increases in victim cells are much lower than the crystalized temperature of the GST.

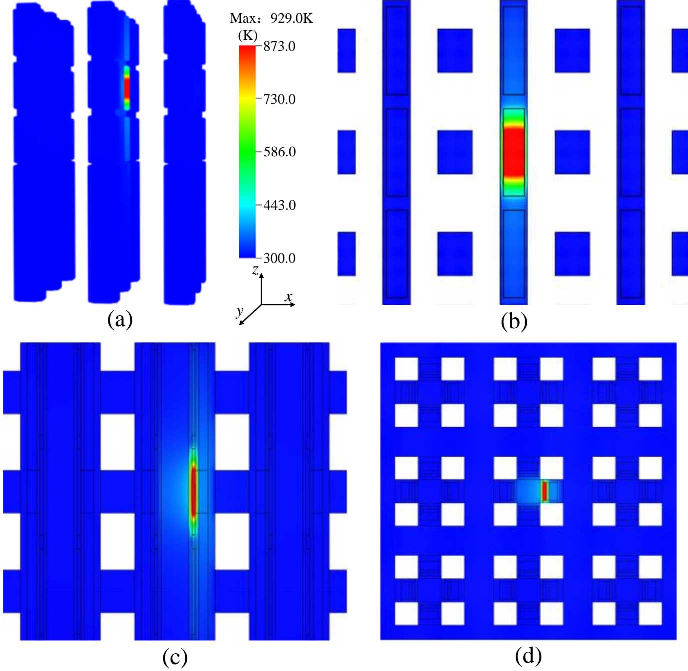

Figure 13. Temperature distributions of the PCM array composed of a four-fold unit with w_{GST} = 12 nm: (**a**) 3-D structure; (**b**) cross-section in the *xz*-plane; (**c**) cross-section in the *yz*-plane; (**d**) cross-section in the *xy*-plane.

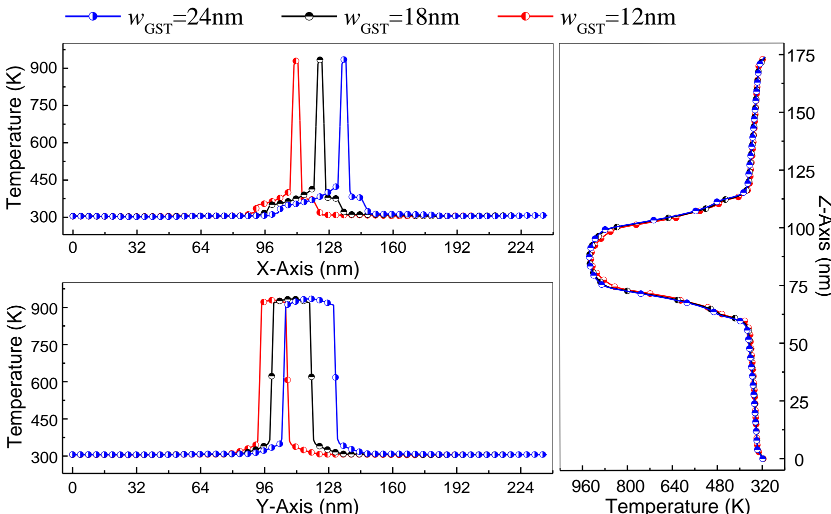

Figure 14. Temperature distributions on lines through the center point of the GST structure of the activated cell along axis with changing w_{GST} values.

In addition, the electrothermal characterizations of arrays with different w_{getd} values are investigated here. Figure 15a,b show the extracted temperature distributions on lines along x- and y-axes. The inserts in Figure 15a,b show the temperature distributions of adjacent cells in x- and y-directions, respectively. It can be observed that the maximum temperature rise in victim cells is kept smaller than 5 K as w_{getd} decreases from 20 nm to 10 nm, indicating that scaling w_{getd} can effectively improve the integration density of the proposed PCM array.

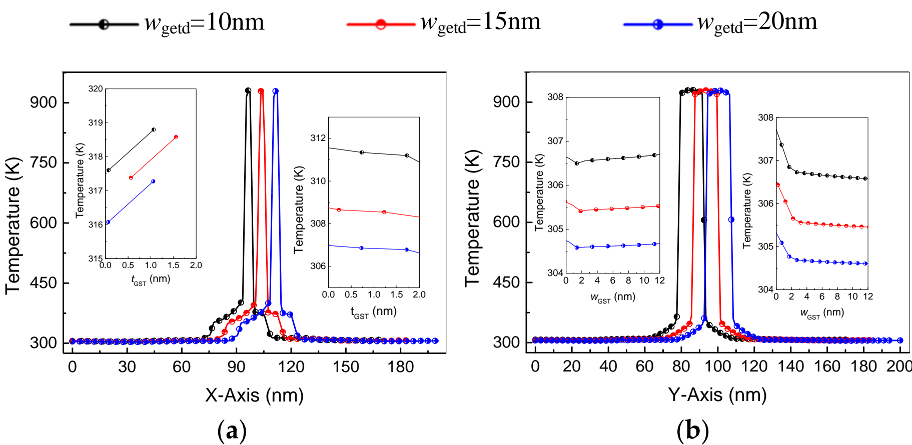

Figure 15. Temperature distributions on lines through the center point of the GST structure of the activated cell along axis with changing h_{GST} values: (**a**) temperature distributions along x-axis; (**b**) temperature distributions along y-axis.

4.3. Integration Density

Referencing the cross-sectional area of the referred conventional vertical PCM cell, the integration densities of the proposed array schemes are calculated and presented in Figures 16 and 17. Taking the conventional PCM array presented in Figure 1 as a reference, the relative integration density of the proposed PCM array is defined as:

$$D_{\mathrm{int}} = \frac{s_{c*}}{s_{\mathrm{ref}}} n_{cell}$$

where the n_{cell} values equal 2 and 4 for the diploid and four-fold unit, respectively; s_{ref} is the cross-sectional area of the referenced memory unit; s_{c*} is the cross-sectional area of the array with diploid units or four-fold units.

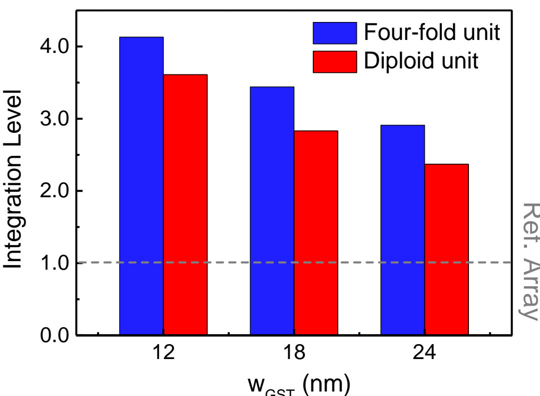

Figure 16. Integration density of vertical PCM arrays with diploid and four-fold units referred to the conventional vertical PCM array in [22] as functions of w_{GST}.

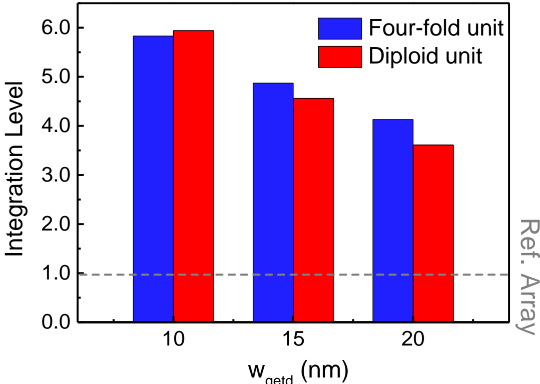

Figure 17. Integration density rates of vertical PCM arrays with diploid and four-fold units compared to the conventional vertical PCM array in [22] as functions of w_{getd}.

As shown in Figure 16, when the cross-sectional area of the nano-strip GST film is the same as that of the reference unit, the integration densities of PCM arrays with a diploid unit and four-fold unit are 2.5 and 3 times larger than that of the reference array, respectively. As w_{GST} scales from 24 nm to 12 nm, the integration densities of the arrays composed of the diploid unit and four-fold unit increase from 2.5 to 3.5 and from 3.0 to 4.1. In Figure 17, the integration densities of the proposed arrays versus w_{getd} are presented. As w_{getd} scales from 20 nm to 10 nm, the integration density increases from 3.5 to 6.0 and from 4.1 to 5.8 for arrays with a diploid unit and four-fold unit, respectively. During the scaling down of w_{getd}, the integration variation of the array composed of the diploid unit is much larger than that of the four-fold-unit-based array. This can be interpreted as the change rate in the cross-sectional area of the four-fold unit being much smaller than that of the diploid unit as w_{getd} scales down. At last, the performances of the proposed PCM cells and arrays are compared with those of the cells and arrays shown in [22]. It can be observed that the proposed PCM cells and arrays perform better in terms of power consumption and integration, as shown in Table 3.

Table 3. Comparison between proposed PCM cells and the cell discussed in [22].

PCM Cell/Array	I_{reset} (mA)	T_{max} (K)	W_{reset} (J)	Integration Level
$w_{GST} = 24$ nm $h_{GST} = 25$ nm	0.1095	937.6	1.21×10^{-13}	3.0
$w_{GST} = 12$ nm $h_{GST} = 15$ nm	0.0660	922.4	5.7×10^{-14}	6.0
Ref. [22]	0.1354	936.2	1.6×10^{-13}	1.0

5. Conclusions

In this work, two design schemes for high-density phase change memory arrays were proposed and numerically investigated. In these schemes, significant improvements in power consumption and integration density were achieved by replacing the memory cell in the conventional vertical array with a diploid unit and four-fold unit. Moreover, additional selective circuits were specially designed to implement the operation on the designated memory cell. The characteristics of the PCM cells and arrays were investigated by utilizing an in-house-developed simulator. The results indicated that the power consumption of the stripe film PCM cell was 32% lower than that of the cell in the conventional vertical array, and with w_{GST} scaling from 24 nm to 12 nm, a 40% drop in power consumption was achieved. Further, the electrothermal characteristics of PCM arrays composed of a diploid unit and four-fold unit were simulated and analyzed. Although thermal crosstalk could be observed in cells adjacent to the activated cell, the induced maximum temperatures in victims were much lower than the crystalized threshold of the amorphous GST. Next, the influences of w_{GST} and w_{getd} on the thermal crosstalk in arrays were also studied and the results indicated that the scaling of both parameters just slightly influenced the arrays' performance. At last, the integration densities of the proposed arrays were compared with a reference design, with 1.5-fold and 2.0-fold increases achieved for the arrays with diploid unit and four-fold unit, respectively, with w_{GST} = 24 nm. Moreover, with w_{GST} = 12 nm and w_{getd} = 10 nm, the integration densities of the proposed PCM arrays were 6.0 times and 5.8 times the values of the conventional array, respectively. Above all, the simulated results showed that the proposed arrays possess both excellent performance and a high integration density. In addition, the influences of the quantum effects on the performance of the PCM cells and arrays were not studied in detail in this work, and more in-depth studies will be carried out in following studies.

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