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Pre-Emphasis Pulse Design for Reducing Bit-Line Access Time in NAND Flash Memory

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Abstract: This paper describes pre-emphasis (PE) pulses to reduce bit-line (BL) access time in NAND flash memory. Optimum PE pulse widths and resultant minimum BL delay times are investigated, where the BL delay is determined by the sense current at the input terminal of a sensing circuit in contrast with the word-line (WL) delay that is determined by the WL voltage at the gate of a selected memory cell. Two BL models are used, namely, a single-line model (SLM) for the shielded BL read operation and a three-line model (TLM) for the all-BL read operation. Under the condition that the sense current delay is defined by the time when the sense current becomes stable between 110% and 90% of the cell current and the BL voltage delay is defined by the time when the BL voltage at the selected cell reaches a window between 110% and 90%, SPICE simulation results show that the sensed current delay and the BL voltage delay are reduced by 43% and 36% in the case of SLM and by 16% and 28% in the case of TLM, respectively. Thus, the key results are the following: (1) PE pulses are effective to reduce the sense current delay time for BL access, as well as the BL voltage delay time for both SLM and TLM; (2) the sensitivity of the PE pulse on the delay time is much larger for the sensed current delay than the BL voltage delay due to the absence of filtering with the RC delay element in BL delay; and (3) address-dependent PE pulse control can reduce the sense current delay significantly, especially for access to cells closely located to the sensing circuit.

Keywords: pre-emphasis pulse; bit-line delay; NAND flash; address-dependent pulse

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1. Introduction

The access time for memory is a critical element in computing. Memory access is composed of address decoding, word-line (WL), and bit-line (BL) delays, in addition to data output. Among these, WL and BL delays are limiting factors, especially for devices with large memory arrays, such as NAND flash and storage class memories. Pre-emphasis (PE) pulses are design techniques to reduce the access line delay of 3D NAND devices [1] and large flat panel displays [2]. By driving large RC delay lines with a pulse whose initial period is made with a voltage higher than the target voltage, the entire WL delay time can be reduced significantly, where the delay time is defined by the farthest point of WL. Circuit analyses have been discussed to design PE pulses for minimizing the WL delay time in [3–5]. PE pulses are also effective for memory devices used for storage or 3D cross-point memory [6–10], where the WL delay is determined by the point at the selected cell. The delay time strongly depends on the column address. Thus, an address-dependent optimum pulse width of the PE pulse can significantly reduce the delay time according to the position of the selected memory cell across a selected WL [11]. All the aforementioned studies have focused on PE pulse design for reducing WL access delay. Another interesting factor is whether PE pulses can be also effective for BL access, which is the motivation of this paper. Unlike WL, with no direct current path, BL has two current states depending on the cell states. Two sensing operations are known, namely, shielded BL [12] and all BL [13] operations.

Figure 1 illustrates a simplified BL path of NAND flash. The value of parameter x represents the position of a selected cell along the BL. The nearest and farthest cells have

x percentages of 0% and 100%, respectively. After one WL is selected with 1 V in this example, keeping all the remaining WLs grounded, the BLs are pre-charged with PASS high. Conventional BL path operations are performed with a step pulse for PASS in both shielded BL [12] and all BL [13] operations. This paper investigates BL delay with a PE pulse for PASS, as shown by the waveform in blue. An overdrive voltage during the PE pulse that is 20–30% higher than the target voltage is effective to reduce the voltage delay [3,4]. Therefore, the BL voltage at the input terminal of the sensing circuit is assumed to be 600 mV during the PE pulse and 500 mV after the PE pulse in this paper. BL voltages go up to lower and higher levels via source follower PASS transistors depending on the cell states. In this paper, data "1" and "0" correspond to higher and lower cell currents, respectively. Please note that BL voltages do not always rise monotonically depending on the PE pulse width and the position that the BL voltage is observed. These details are discussed in Section 2. After the sense current (I_{SENSE}) is stabilized to be as high as the cell current, pre-charging transistors turn off with PREB high. The charges stored in the capacitors at sense nodes (C_{SN}) are discharged with I_{SENSE} to BLs. Because BL "1", which is the BL connected with the selected cell whose data is "1", has a higher current than BL "0", the sense node voltage for BL "1" reduces much faster than that for BL "0". After the voltage window at the sense nodes between "1" and "0" becomes sufficiently large, the sense signal SNS becomes high to output the data to a NAND controller. If the PE pulse can reduce the BL delay, one can start a sensing operation, which contributes to reduction in latency. Accordingly, the BL delay time decreases as the BL voltage during the PE pulse increases, whereas the energy associated with BL charging increases. Thus, there is trade-off to design the PE pulse. Energy increases by about 4% when an overdrive voltage of 20% is used for the PE pulse [4]. This paper does not pay attention to energy thereafter.

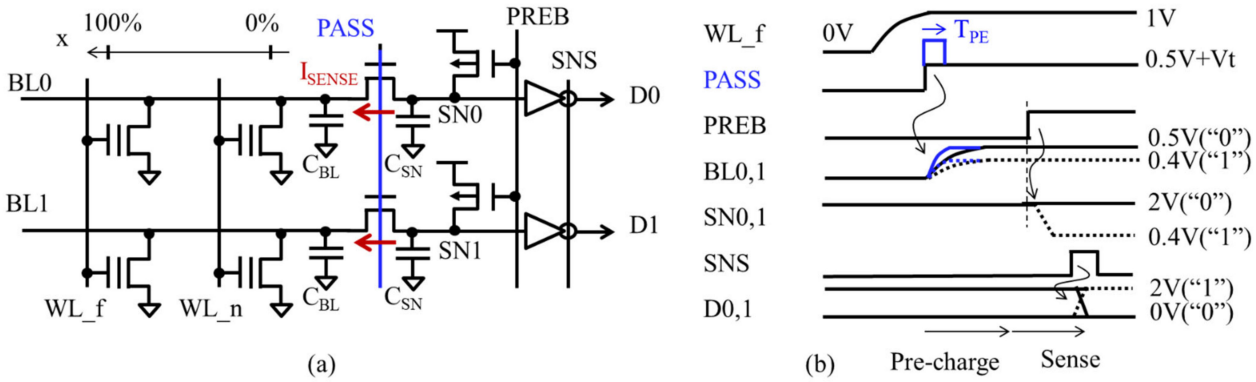

Figure 1. (**a**) BL path of NAND flash. (**b**) Signal waveform for data sensing.

In this paper, PE pulse design is discussed using the three different BL models as shown in Figure 2. Single-BL read (SBL) operation can be analyzed with a single line model (SLM). Three-line model (TLM) is suitable for All-BL read (ABL) operation. Figure 2c shows actual BL control with PASS transistors. The cell current model given by a liner resistor RC is omitted in (b) and (c), but each RC is connected with each BL in actual netlists for simulation. This paper is organized as follows. In Section 2, a single-line model is used for a shielded BL read operation. The characteristics of the sensing current delay as a function of PE pulse width are compared with those of the BL voltage delay. The differences that arise afterwards are investigated in detail. Section 3 discusses a three-line model to see how adjacent BLs affect the delay of the target BL in all-BL read operation. It is shown that the optimum PE pulse width for the sensing current delay is longer by a factor of two than that for the BL voltage delay. The effectiveness of the address-dependent PE pulse width on the average BL delay is shown in Section 4.

2. Single Line Model (SLM)

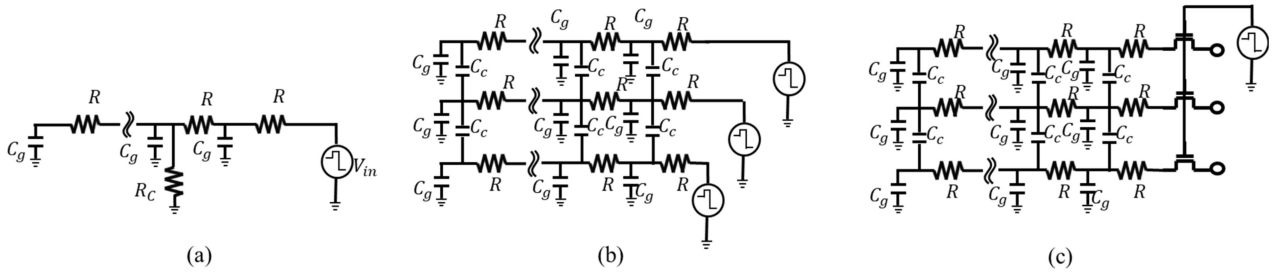

Figure 2. BL path models studied in this paper. (**a**) Single line model (SLM). (**b**) Three-line model (TLM) and (**c**) TLM with PASS transistors. The cell current model given by a liner resistor R_C is omitted in (**b**,**c**), but each R_C is connected with each BL in actual netlists for simulation.

Table 1 summarizes the device and design parameters used in this study. The memory cells are modeled by linear resistors for simplicity. Distributed RC elements are used for BL operations. The selected memory cells are located at x percentages of 25%, 33%, 50%, 66%, 75%, and 100%.

Table 1. Device and design parameters used in this study.

Device/Design Parameters		Values
R		1.0 MΩ
C (= Cg + 2Cc)		3.0 pF
$I_{CELL\_1\ (0)}$		100 nA (10 nA)
$R_{CELL\_1\ (0)}$		5.0 MΩ (50 MΩ)
V_{BL_PRE}		600 mV
V_{BL}		500 mV
	Cg	**Cc**
SLM	3 pF	0 pF
TLM	1 pF	1 pF

Figure 3a shows the BL voltage waveform with different PE pulse widths when the "0" cell at 25% of the BL is selected. At the transition in PASS from the PE voltage to the target one, the BL voltage reduces due to charge distribution in BL capacitance. After a certain amount of time, the BL voltage increases again. When the acceptable voltage window is as large as 10% of the target BL voltage, with Tpre = 1.0 μs, the BL voltage delay is about 1.6 μs (shown by "Tdly2"). With Tpre = 1.2–2.2 μs, the delay is about 0.7 us (shown by "Tdly1"). With Tpre = 2.4 μs, the delay is about 2.4 μs (shown by "Tdly3"). A BL voltage with too short of a Tpre time has a large drop after Tpre, which results in a long Tdly value. A BL voltage with too long of a Tpre values becomes higher than the target voltage, which also results in long Tdly value. Thus, a voltage window of 10% translates into a wide time window for Tpre. Thus, the BL voltage delay (Tdly) has a good shape with respect to Tpre, even though Tdly is longer when a farther cell is selected. The Tdly values for the cells between 25% and 100% are limited in a shady region of Figure 3b. Please note that the impact of the cell current on Tdly depends on the position of the selected cell due to the difference in BL resistance between the sensing circuit and the selected cell. The cell at 25% of the BL has no significant variation, whereas that at 100% of the BL has significant variation due to the differences in data. One can find the worst case of Tdly to pick up the longest Tdly value at every Tpre value. Interestingly, a BLL of 100% does not always

determine Tdly. BL 100% determines Tdly when Tpre is <2.2 µs or >3.2 µs, whereas BL25% exhibits Tdly at 2.4 µs < Tpre < 3.0 µs.

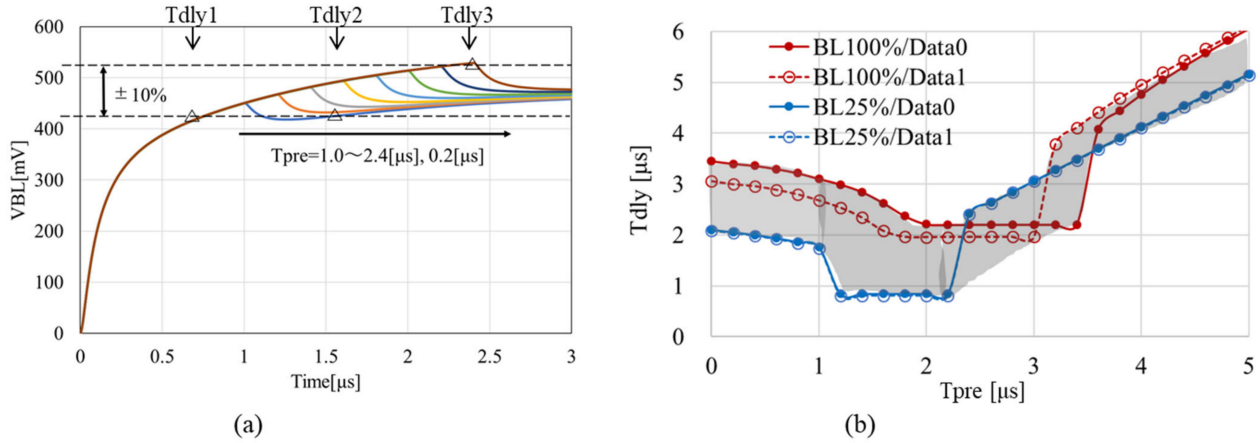

Figure 3. (**a**) BL voltage waveform with different PE pulse widths when the "0" cell at 25% of the BL is selected. (**b**) Delay time vs. PE pulse width.

Figure 4a shows the sensing current delay at different BL positions. In comparison with the BL voltage delay shown in Figure 3b, the current delay is more sensitive to Tpre. Note that the dependence of the position of the selected cell on Tdly for the sense current is quite different than that for the BL voltage. The current delay time in the worst case is determined in all the BL positions, resulting in Figure 4b. The optimum Tpre to minimize the current delay is about the same as the BL voltage delay.

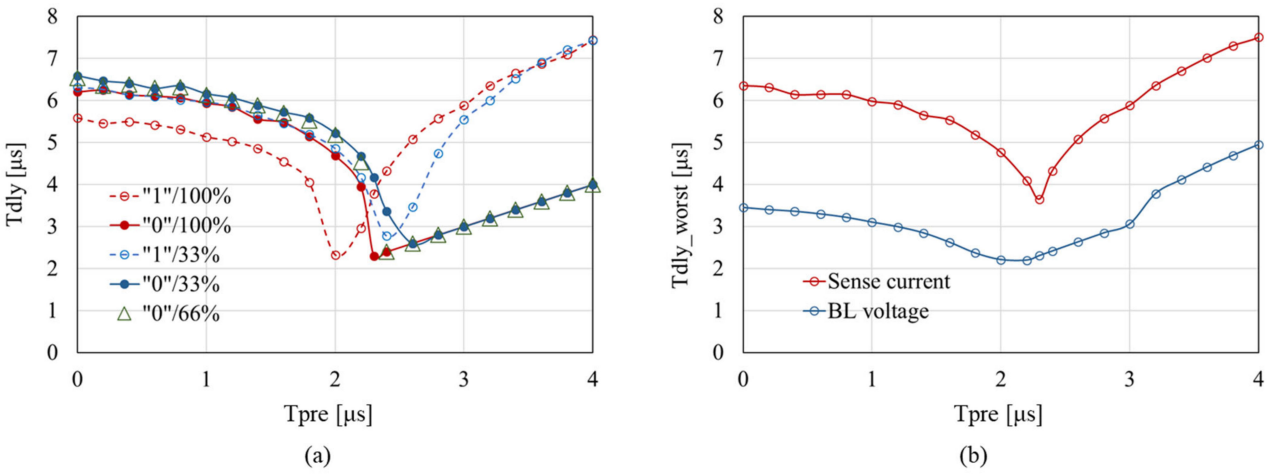

Figure 4. (**a**) Sensed current delay at different BL positions. (**b**) Worst delay time in all BL positions for the sensed current and BL voltage.

In order to understand the characteristics affecting the sensitivity of Tpre, the cell current (I_{CELL}) and the BL current (I_{BLF}) at the selected BL position were measured in addition to the sensing current (I_{SNS}), as shown in Figure 5.

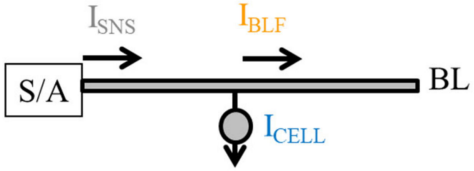

Figure 5. Definition of current components.

Figure 6 shows the BL voltage (upper) and current waveform (lower) with different Tpre (2.0 µs, 2.4 µs and 2.8 µs from left to right, respectively) values when the "1" cell at x = 25% is selected. The arrows in the upper graphs indicate the processing time to show how the charges at every BL node are redistributed after Tpre. The current delay is minimized when Tpre is 2.4 µs. I_{BLF} becomes very close to 0 nA as soon as PE pulsing is finished. Thus, the sense current becomes stable in a short time. One can notice that BL 66% does not change much over time. As concluded in [4], the RC delay line has a position of 2/3 with no change in time in the case where an optimum Tpre is used to minimize the voltage delay time in theory. Thus, the sensed current delay can be also minimized with the optimum Tpre for BL voltage delay. With Tpre values of 2.0 µs or 2.8 µs, the sensed current delay becomes much longer. With a shorter Tpre of 2.0 µs, the BL voltages are insufficient such that I_{BLF} becomes positive after the PE pulse, which in turn affects I_{SNS}. Conversely, with a longer Tpre of 2.8 µs, the BL voltages are more than sufficient such that the I_{BLF} becomes negative after a PE pulse, which in turn affects I_{SNS} as well. BL 66% with a Tpre of 2.0 µs or 2.8 µs changes significantly over time, which indicates that it takes more time for all the BL nodes to become stable.

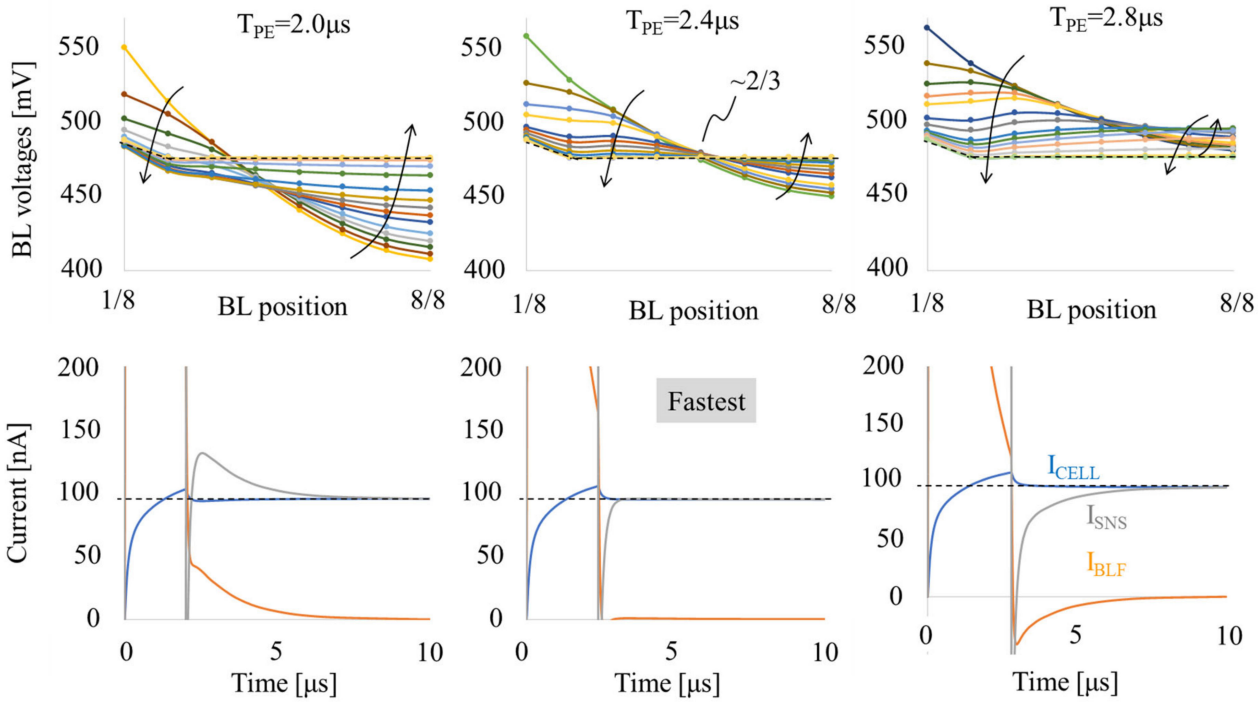

Figure 6. BL voltage (**upper**) and current waveform (**lower**) with different Tpre (2.0 µs, 2.4 µs and 2.8 µs from left to right, respectively) values when the "1" cell at x = 25% is selected.

Figure 7 shows the BL voltage (upper) and current waveform (lower) with different Tpre (2.0 µs, 2.4 µs and 2.8 µs from left to right, respectively) values when the "1"-cell at x = 100% is selected. Even though the optimum Tpre is different than that for the case where the cell located at BL 25% is selected, a Tpre value of 2.0 µs allows the BL voltage at 2/3 to become very stable over time and features the minimum sense current delay as shown in the left bottom graph.

Figure 8 shows the BL voltage (upper) and current waveform (lower) with different Tpre (2.0 µs, 2.4 µs and 2.8 µs from left to right, respectively) values when "0"-cell at x = 100% is selected. Even though the optimum Tpre is different than that for the case where the "1" cell located at BL of 100% is selected, a Tpre value of 2.4 µs allows the BL voltage at 2/3 to become very stable over time and features the minimum sense current delay as shown in the center bottom graph. A Tpre value of 2.8 µs or longer can be optimum

as well, because the excess pre-charging allows I_{SNS} to be <10 nA at any time after Tpre. If the value of I_{SNS} is <10 nA, the sensing circuit interprets the data as "0".

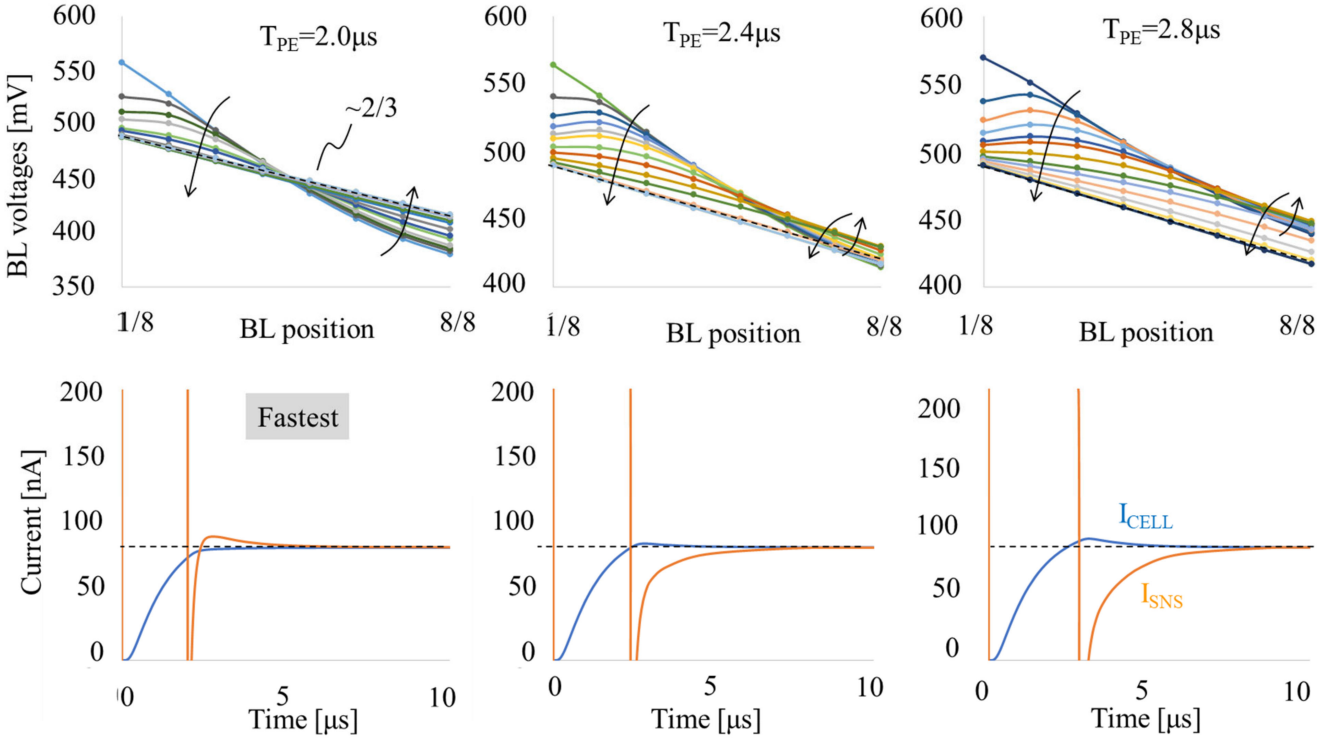

Figure 7. BL voltage (**upper**) and current waveform (**lower**) with different Tpre (2.0 µs, 2.4 µs and 2.8 µs from left to right, respectively) values when the "1" cell at x = 100% is selected.

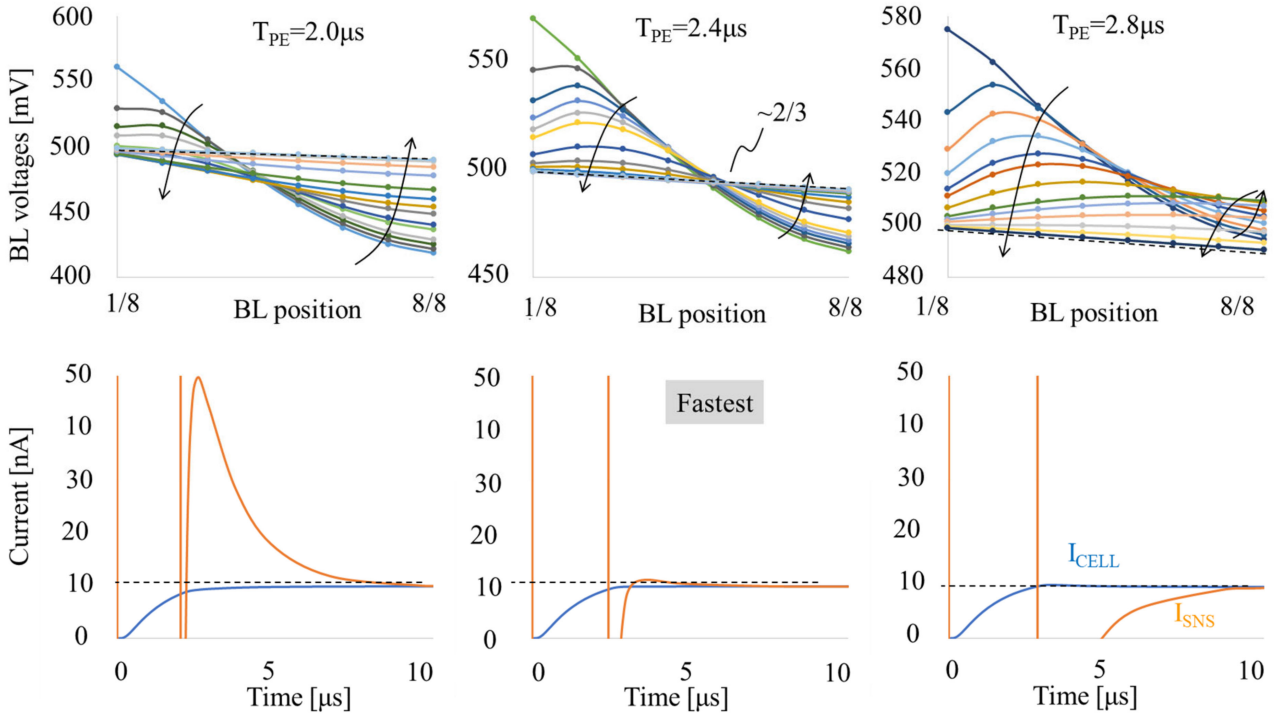

Figure 8. BL voltage (**upper**) and current waveform (**lower**) with different Tpre (2.0 µs, 2.4 µs and 2.8 µs from left to right, respectively) values when the "0" cell at x = 100% is selected.

3. Three-Lines Model (TLM)

Even when the total BL capacitance of the TLM is the same as that of SLM, the sensed current delay can be increased due to the capacitive coupling between next neighbor BLs in case of an ABL read operation. In this section, the three-line model is studied.

3.1. Tdly vs. Tpre

Figure 9 shows the address dependency of the sensed current delay in the fastest case (a) and the slowest case (b) with the three-line model. Fast corners, as shown by F0 and F1, have no significant dependence of Tdly on the selected address, whereas slow corners, as shown by S0 and S1, do feature dependence. The fast corners for "1" and "0" have data patterns of 111 and 000 for the three BLs. The slow corners for "1" and "0" have data patterns of 010 and 101 for the three BLs. The worst delay occurs when the farthest cell is selected. The worst delay is determined by S0 when Tdly <1.2 us and by S1 when Tdly >1.2 us.

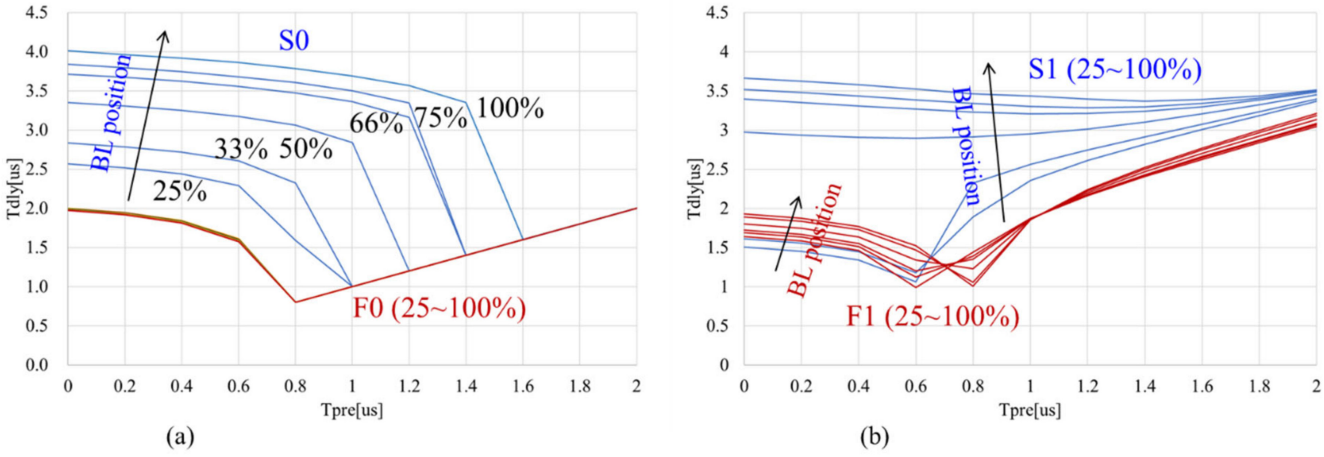

Figure 9. Address dependency of the sensed current delay in the fastest case (**a**) and the slowest case (**b**) with the three-line model.

Figure 10 shows the voltage and current delays in the worst cases as described by Vtdw (Voltage Tdly in the Worst case) and Itdw (Current (I) Tdly in the Worst case), respectively, with the single-line and three-line models (SLM/TLM). Even though the total capacitance defined by Cg + 2 Cc is common with 3 pF or both SLM and TLM, the minimum delay with the TLM is much faster than that with the SLM because Cc only needs to be charged to the voltage difference between the BL voltages for data "1" and "0", whereas Cg needs to be charged to the BL voltages. Thus, the total charge for the BL capacitance of the TLM is smaller than that of the SLM. Tables 2 and 3 summarize the reduction rates of Tdly_worst PE pulses and Tpre window in the case that a delay that is 20% longer than the minimum is acceptable. Thus, PE pulses are effective for reducing the sensing current as for the BL voltage. The sensitivity of Tdly_worst on Tre is quite large for the SLM and small for the TLM. The optimum Tpre to minimize Tdly_worst for the sensing current was about same as that for the BL voltage in case of the SLM, as shown by the curves in red. On the contrary, the optimum Tpre for the sensing current is longer by a factor of two than that for the BL voltage in case of the TLM, as shown by the curves in blue.

Table 2. Reduction in delay with optimum PE pulses.

	V_{BL} Delay	I_{SNS} Delay
SLM	36%	43%
TLM	28%	16%

Table 3. Tpre window in the case that "a delay that is 20% longer than the minimum" is acceptable.

	V_{BL} Delay	I_{SNS} Delay
SLM	0.6 µs	0.2 µs
TLM	0.4 µs	2.8 µs

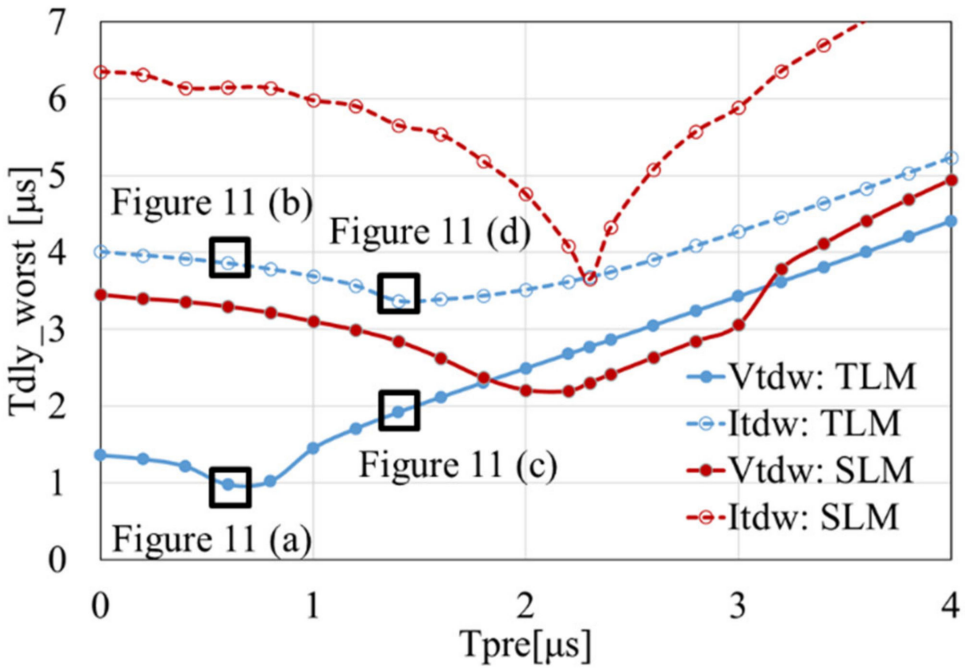

Figure 10. Worst case voltage and current delay (Vtdw/Itdw) with the single-line and three-line models (SLM/TLM).

Figure 11 shows voltage (a) and current (b) waveforms when the farthest "1" cell is selected with Tpre = 0.6 us and the worst data pattern of 010, and the voltage (c) and current (d) waveforms when the slowest "0" cell is selected with Tpre = 1.4 us and the worst data pattern of 101. Icell_n and Isense_n indicate the cell current and sensed current of the next neighbor BLs. In Figure 11a,c, the voltages at BL positions of 25%, 33%, 50%, 66%, 75% and 100% are shown. The condition for each graph is mapped in Figure 10. The condition for the minimum BL delay has the waveform shown in Figure 11a. The BL voltages move to stable states very quickly, even with a cell current of 100 nA. As shown in Figure 11b, the cell current moves to a stable state as quickly as the BL voltage because Icell is determined by the BL voltage at the selected address. On the other hand, the sensed current changes far slower because of the coupling capacitance Cc.

Let us consider that the condition for the minimum sense current delay has the waveform as shown in Figure 11d. Even though the delay time is at a minimum, the sensed current still has a significant impact in terms of Cc on the transient behavior. As a result, Tdly for the sense current is insensitive to Tpre, as shown by Figure 10. On the other hand, the BL voltages move to stable states very quickly even, with non-optimum Tpre, as shown by Figure 11c.

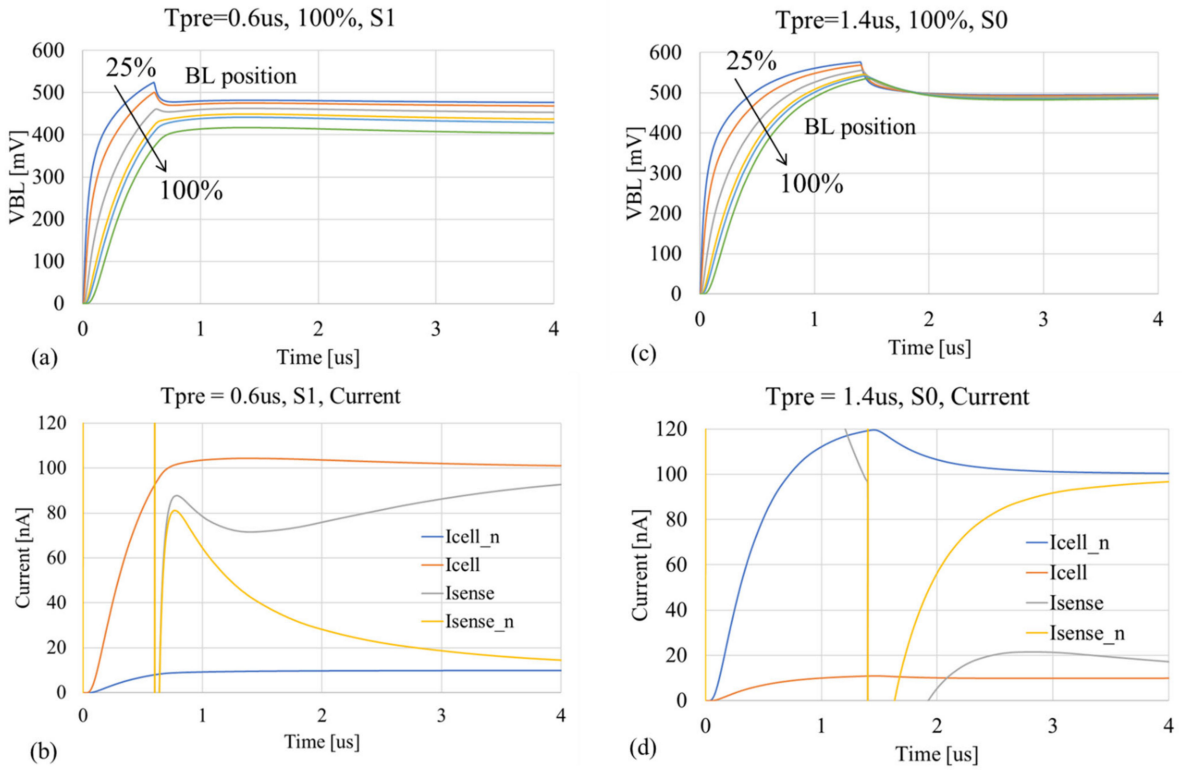

Figure 11. Voltage (**a**) and current (**b**) waveforms when the farthest "1" cell is selected with Tpre = 0.6 us and the worst data pattern of 010. Voltage (**c**) and current (**d**) waveforms when the slowest "0" cell is selected with Tpre = 1.4 us and the worst data pattern of 101.

3.2. *Effectiveness of Address Dependent Tpre*

Figure 12 shows the address-dependent optimum PE time (Topt) in blue and the delay time with Topt in orange for the BL voltage (a) and sensed current (b) with the three-line model. At each optimum point, Tdly for "1" is the same as that for "0". One can have the minimum BL voltage delay which is reduced in proportion to the selected BL address, approximately. One can also have the minimum sensed current delay with another set for optimum Tpre for BL33% and BL25%. The minimum sensed current delay has no significant change for a BL address of 50% or higher due to significant impact of coupling capacitance on the sensing current, especially when the selected cells are located far from the sensing circuit.

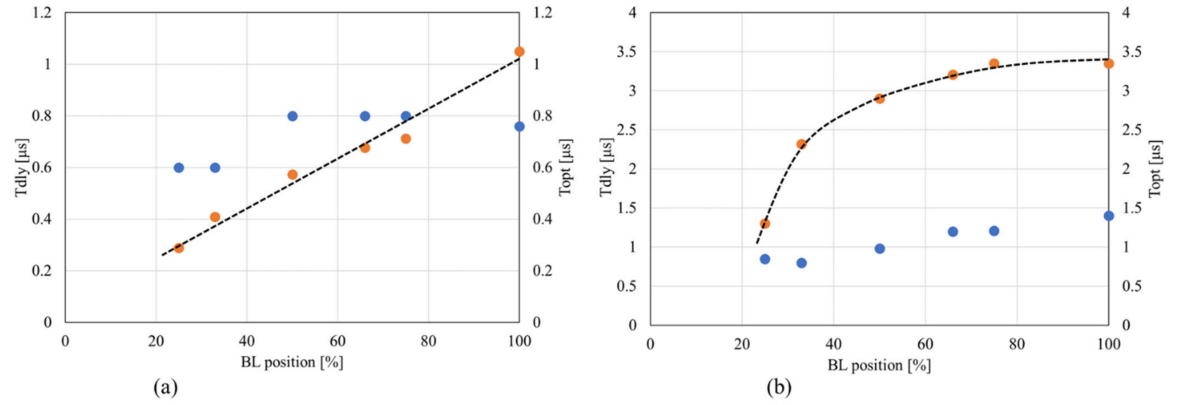

Figure 12. Address-dependent optimum PE time (Topt) in blue and the delay time with Topt in orange for the BL voltage (**a**) and the sensed current (**b**) with three-line model.

3.3. Impact of PASS Transistors on the Delay Time

To demonstrate how the output resistance of the PASS transistors affects the sensed current delay, a simulation was performed with a configuration as shown in Figure 2c, where 1.8 V transistors in a 180 nm CMOS were used, whose output resistance was 350 kΩ at the sense current of 100 nA. Therefore, in this demonstration, the ratio of the output resistance of PASS transistors on the BL resistance is 350 kΩ/1 MΩ = 0.35. Figure 13a shows the sensed current delay as a function of Tpre for the simulation, with and without PASS transistors. The effective resistance component for the RC time constant is increased with the PASS transistors. To check if the output resistance of PASS transistors simply increases the RC time constant, the values of Tpre and Tdly for the curves with PASS transistors were scaled by a factor of two, resulting in Figure 13b. Slow corners for "with transistors" were in good agreement with those for "without transistors", which indicates that the data and discussions so far can be valid in the case of transistors when a scaling factor is multiplied. The worst case for Tdly is compared in Figure 13c.

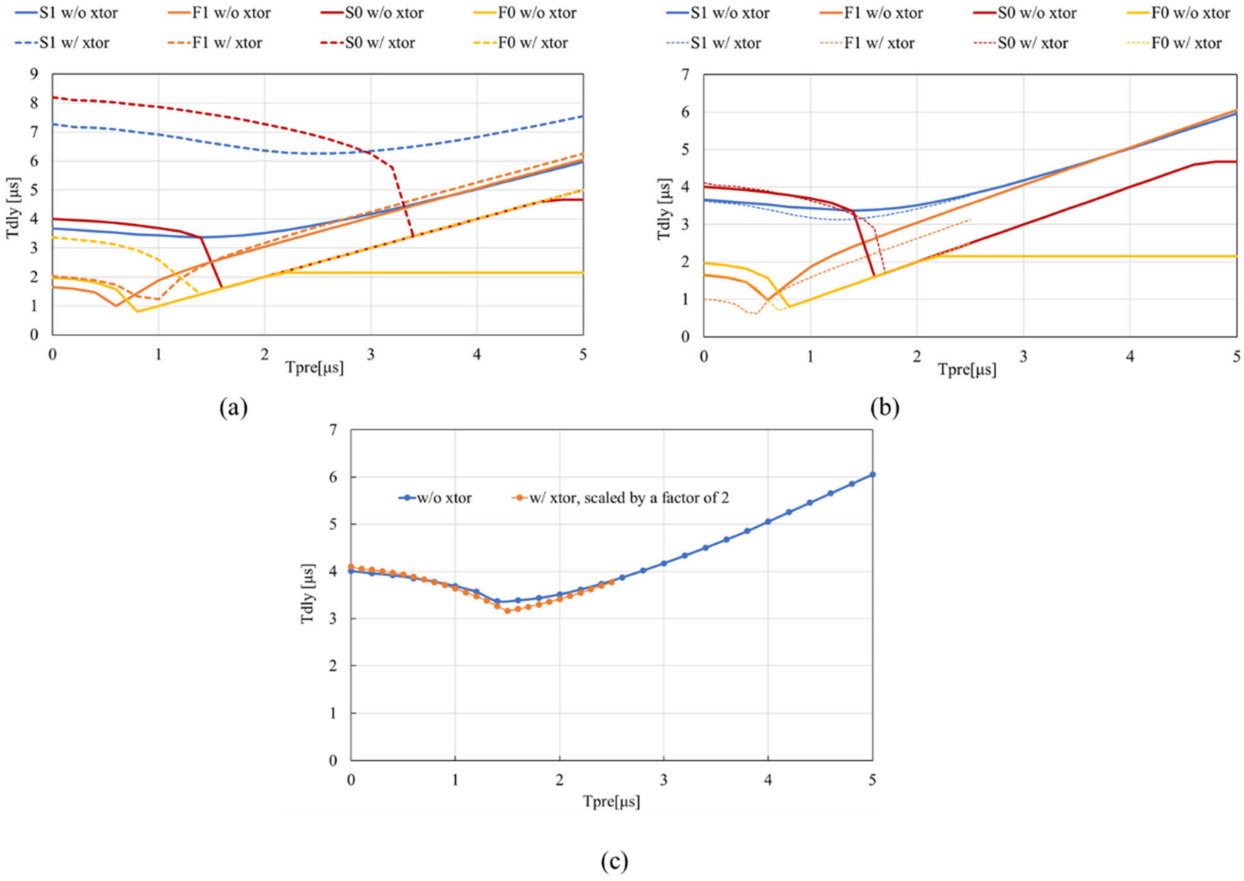

Figure 13. Sensed current delay as a function of Tpre for the netlist with and without PASS transistors with raw data (**a**) and with scaled data for "with transistors" (**b**). The worst case Tdly is compared in (**c**).

4. Conclusions

PE pulsing was studied to assess whether one can reduce the BL delay as well the WL delay. The sensed current delay can be reduced with PE pulses when optimum ones are used in both single-line and three-line models, though the effectiveness is different. Address-dependent PE pulses are effective for the cells located at BLs close to sensing circuits. The impact of PASS transistors has been investigated as well. Tpre and Tdly can be scaled by a factor depending on the ratio of the output resistance of PASS transistors

on the BL resistance. In the demonstration here, the scaling factor was two when the ratio was 0.35.

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