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A Low-Power ADPLL with Calibration-Free RO-Based Injection-Locking TDC for BLE Applications

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Abstract: This paper proposes a low-power all-digital phase-locked loop (ADPLL) with calibration-free ring oscillator (RO)-based injection-locking time to digital converter (TDC) for BLE applications. The RO is reused as the delay cell of TDC, and the quantization step of TDC is always tracked with the RO period; hence no calibration is needed in this architecture. We adopt RO tuning to lower the injection-locking bandwidth so as to decrease the power consumption of the injection current. Moreover, the fractional part of phase error detection is turned down in the coarse tuning of ADPLL to save power. An LC-based digital-controlled oscillator (LCDCO) with a 6.4 nH inductor and a resistive bias is used to have a low power and better phase noise performance. The ADPLL is fabricated in 40 nm CMOS with a 1 V supply and consumes 1.4 mW when it is locked. The measured phase noise is −114 dBc/Hz at 1 MHz offset. The test results show significant power saving. Thus, it can be a promising candidate for BLE applications.

Keywords: all-digital phase-locked loop (ADPLL); injection-locking time to digital converter (TDC); bluetooth low-energy (BLE); digital-controlled oscillator (DCO); phase noise; RO tuning; TDC calibration

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1. Introduction

With the increasing demand for the Internet-of-Things (IoT), Bluetooth Low-Energy (BLE) has become a popular solution for short-range communication of wireless applications, such as wearable devices, sensor monitoring platforms, and smart cities [1–5]. However, due to the limitations of application scenarios, BLE devices often have the characteristics of small volume and are easy to carry. Some even need to be implanted into the human body, which puts forward strict requirements for the battery life of these devices. The wireless communication module dominates the power consumption budget of the whole system [6]. Therefore, with a limited energy supply, the low-power wireless communication system design has become the most critical requirement of BLE devices. Thanks to the relatively simple FSK modulation, the architecture of the BLE transceiver is simplified. In a BLE transmitter, frequency modulation can be achieved by direct frequency synthesis through a phase-locked loop (PLL). Therefore, the frequency synthesizer and PA occupy most of the power consumption of the whole BLE transmitter. Among them, how to reduce the power consumption of the frequency synthesizer on the premise of meeting the requirements of phase noise has become the most challenging design.

An all-digital phase-locked loop (ADPLL) was used as a wireless communication module roughly a decade ago [7,8]. In recent years, the advantages of frequency synthesizers based on ADPLL have gradually emerged due to the development of CMOS technology, and it has become popular instead of the analog-based charge-pump phase-locked loop

(CPPLL). Figure 1 shows four different architectures of ADPLL. The divider-based ADPLL [9–11] in Figure 1a will cause additional quantization noise due to the sigma-delta modulator (SDM) for fractional operation. Moreover, this structure also has the problem of noise up-conversion caused by the time to digital converter (TDC) and divider. The counter-based ADPLL [12–16] shown in Figure 1b uses TDC to generate the fractional phase error directly. Thus, the additional divider noise will be removed, and only reference noise will be up-converted by the frequency multiplication ratio N. However, in this structure, TDC consumes much more power because of the extra normalization circuit caused by PVT variations. Figure 1c shows the counter-based ADPLL with embedded TDC [17]. Using the polyphase output characteristics of the RO, RO is reused as the delay unit of TDC. In this way, the quantization step of TDC always follows the cycle of RO output. Therefore, no additional normalization operation is required, and the power consumption is reduced. Based on this architecture, an ultra-low-power BLE transmitter is designed in [15]. It uses an RO-based wide bandwidth ADPLL working at 600 MHz and multiplies the frequency to 2.4 G through the edge combiner (EC). However, the design has poor phase noise performance, which limits the application of this structure. Moreover, to shorten the detection range of high-speed TDC, some architectures adopt a DTC-assisted TDC structure [14], which successfully reduces the complexity of the TDC circuit and uses TDC snapshotting to reduce the sampling rate to the reference frequency. However, the mismatch and nonlinearity between DTC and TDC will introduce spurs. At the same time, both DTC and TDC need calibration, resulting in additional power consumption.

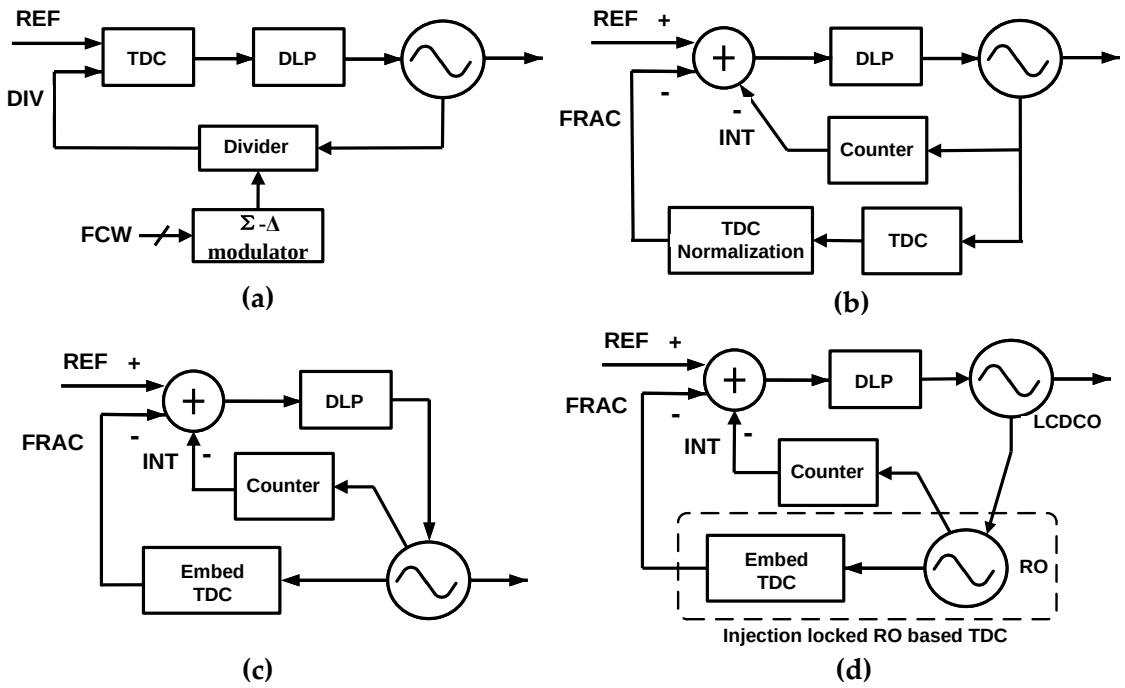

Figure 1. (**a**) Divider-based ADPLL; (**b**) Counter-based ADPLL; (**c**) Counter-based ADPLL with embed TDC; (**d**) Counter-based ADPLL with injection-locked RO based TDC.

Based on the embedded TDC, this paper proposes a low-power ADPLL architecture, as shown in Figure 1d, which uses LC digital-controlled oscillators (LCDCO) to inject the RO, and RO acts as the delay unit of TDC for fractional error operation. At the same time, type-I ADPLL is used to reduce the power consumption in the locking process, and the fractional error detection is turned down in the coarse tune process of the system. We use frequency tuning of RO, which has a 10 MHz tuning step to reduce the power consumption of injection locking and hence the DNL of injection-locked TDC.

This paper is organized as follows: Section 2 gives the analysis of the injection-locked RO and the calibration-free TDC. Then the overall architecture and system-level design considerations of the proposed ADPLL are presented. Section 3 talks about the detailed circuit implementation of the key building blocks. Section 4 demonstrates the measurement results and the comparison to the state-of-the-art. Finally, Section 5 draws the conclusion of the entire work.

2. Analysis and Design

2.1. Analysis of Injection-Locked RO

The injection-locking technique is widely used in the design of frequency synthesizers, dividers, and voltage-controlled oscillators (VCO) [18–21]. Figure 2 shows a typical N-stage single-end RO and its current vector diagram; N must be an odd number to avoid circuit latch-up. I_{OSC} is the RO current of each stage. To satisfy the Barkhausen criteria for oscillation, the overall phase shift of the oscillator loop must be an integer multiple of 2π. Therefore, the RC-loading phase shift of each stage will be π/N. Its open-loop transfer function can be expressed as:

$$H(j\omega) = -\frac{A_0^N}{\left(1 + j\frac{\omega_{RO}}{\omega_{BW}}\right)^N}. \tag{1}$$

where A_0 is the low-frequency gain of each stage, ω_{RO} is the free-running frequency of the RO, and ω_{BW} is the 3-dB bandwidth of every signal stage. The relationship between oscillation frequency and the phase shift can be given by:

$$\tan\frac{\pi}{N} = -\frac{\omega_{RO}}{\omega_{BW}}. \tag{2}$$

As for the N-stage single-end RO under injection locking, the injection current I_{inj} is directly added to the first stage. The RO and its current vector diagram are shown in Figure 3. The phase condition of oscillation can be expressed as:

$$\varphi + N\left(\frac{\pi}{N} + \theta + \pi\right) = 2k\pi. \tag{3}$$

where $k = 1, 2, 3\ldots$, φ and θ are the additional phase shifts in the first stage and the remaining stages. After injection locking, the phase shift caused by RC-loading of every stage is $(\pi - \varphi)/N$, so θ is equal to $-\varphi/N$. With a constant strength of injection current I_{inj}, the maximum phase shift $\varphi_{\max}$ will be satisfied when I_{inj} is orthogonal to the output current of the first stage (I_{load}). The current vector diagram is shown in Figure 3c.

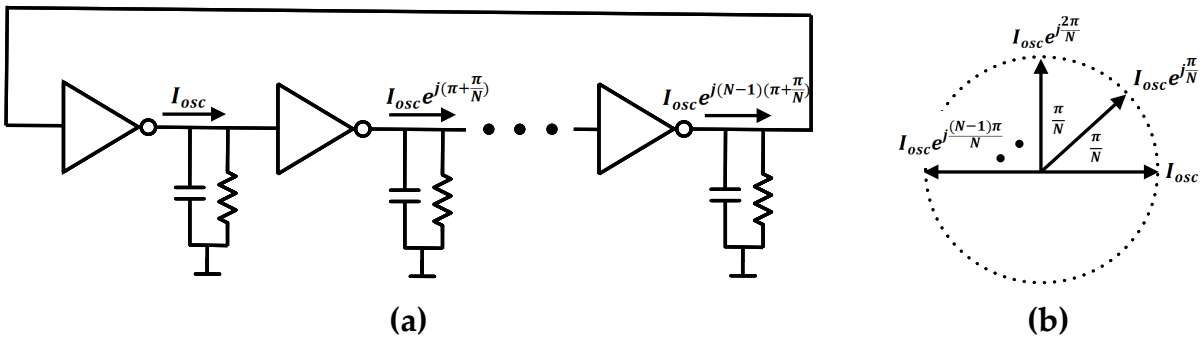

Figure 2. (**a**) N-stage single-end ring oscillator; (**b**) Current vector diagram.

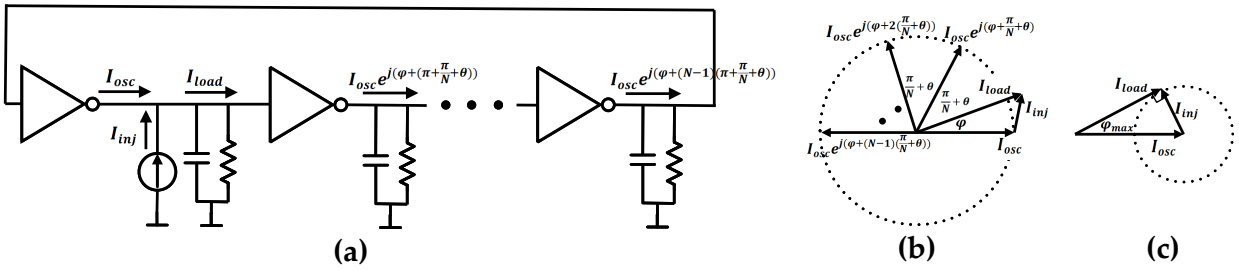

Figure 3. (**a**) N-stage single-end ring oscillator under injection locking; (**b**) Current vector diagram under injection locking; (**c**) Current vector diagram of the boundary of injection locking with given strength of the injection current.

We can infer from this diagram that:

$$\frac{|I_{inj}|}{\sin(\varphi_{\max})} = \frac{|I_{osc}|}{\sin(\pi/2)}. \tag{4}$$

Similarly, combined with (2), the open-loop transfer function of RO under injection locking is given by:

$$H(j\omega) = -\frac{A_0^N}{\left(1+j\frac{\omega_{inj}}{\omega_{BW}}\right)^N} = -\frac{A_0^N}{\left(1+j\frac{\omega_{inj}}{\omega_{RO}/\tan\frac{\pi}{N}}\right)^N}. \tag{5}$$

Therefore the phase shift caused by RC-loading of every stage can be expressed as:

$$\tan^{-1}\left(\frac{\omega_{inj}}{\omega_{RO}/\tan\frac{\pi}{N}}\right) = \frac{\pi}{N}+\theta. \tag{6}$$

By applying Taylor's formula, (6) can be approximated by:

$$\theta \approx \frac{\Delta\omega}{\omega_{RO}}\left(\sin\left(\frac{\pi}{N}\right)\cos\left(\frac{\pi}{N}\right)\right). \tag{7}$$

where $\Delta\omega = \omega_{inj} - \omega_{RO}$. Since $|\theta|$ is equal to $|\varphi|/N$, combining (7) and (4) we can infer that the injection locking bandwidth (ω_{BW_IL}) can be expressed as:

$$\frac{\Delta\omega}{\omega_{RO}} \le \frac{1}{N}\left(\frac{1}{\sin\left(\frac{\pi}{N}\right)\cos\left(\frac{\pi}{N}\right)}\right)\varphi_{\max} = \frac{1}{N}\left(\frac{1}{\sin\left(\frac{\pi}{N}\right)\cos\left(\frac{\pi}{N}\right)}\right)\sin^{-1}\left|\frac{I_{inj}}{I_{osc}}\right| = \frac{\omega_{BW\_IL}}{\omega_{RO}}. \tag{8}$$

From this expression, we can see that the injection locking bandwidth is related to the stages of RO and the injection current I_{inj}. Therefore, if a higher stage of RO is used, one can maintain the same ω_{BW} by increasing I_{inj}.

2.2. Calibration-Free RO-Based TDC

In counter-based ADPLL, TDC is used to quantize the time difference between the reference clock (FREF) and the DCO output clock (CKV). Figure 4a shows the structure of classical flash TDC. CKV passes through an inverter delay chain, and every output of the delay will be sampled by the same FREF. The output is then encoded and normalized to the range $(-1, 1)$ since one cycle of CKV is normalized to 1. Nevertheless, because of the PVT variation, the TDC quantization step must be calibrated so as to catch the CKV period [8]. Thus, this is a relatively power-hungry choice. However, as shown in Figure 4b, if we reuse RO as the TDC's delay chain, the flip flops directly sample every stage of the RO output. This structure is called embedded TDC [17]. In this situation, the TDC quantization step

will always track with the CKV period, which means no calibration is needed, and the power consumption is saved.

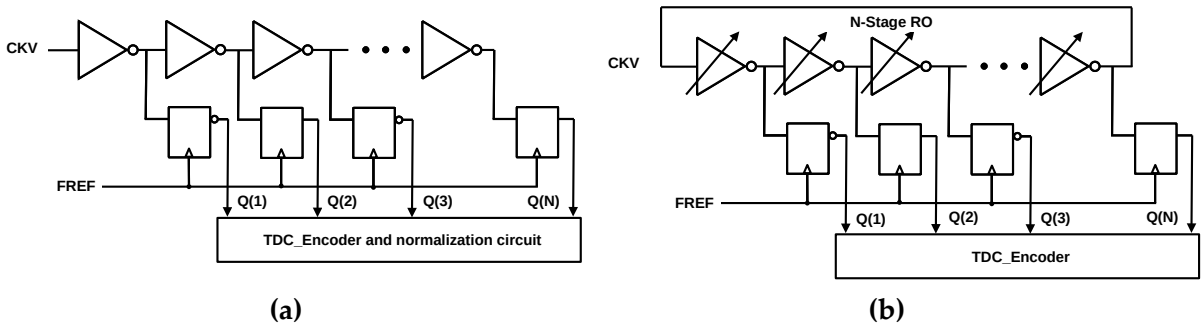

Figure 4. (**a**) Classical Flash TDC; (**b**) Embedded TDC.

As discussed in an earlier section, if RO is injection-locked, the phase shift among the stages of RO will be unequal, which will lead to differential nonlinearity (DNL) of the embedded TDC. The DNL of embedded TDC will cause spurious tones to the output of ADPLL. As shown in Figure 3, the phase shift of the injection stage (ϕ_1) and other stages (ϕ_2) can be expressed as:

$$\phi_1 = \frac{\pi}{N} + \theta + \varphi = \frac{\pi}{N} + (1 - N)\theta, \tag{9}$$

$$\phi_2 = \frac{\pi}{N} + \theta. \tag{10}$$

The definition of DNL of the TDC is:

$$DNL_k = \frac{\phi_k - \phi_{LSB}}{\phi_{LSB}}. \tag{11}$$

where (ϕ_{LSB}) is $\frac{\pi}{N}$, which is the nominal phase shift of embedded TDC when the RO is free running. By combining (7), (9)–(11), we have:

$$DNL_1 = \frac{N(1-N)}{\pi} \frac{\Delta\omega}{\omega_{RO}} \left(\sin\left(\frac{\pi}{N}\right) \cos\left(\frac{\pi}{N}\right)\right), \tag{12}$$

$$DNL_2 = \frac{N}{\pi} \frac{\Delta\omega}{\omega_{RO}} \left(\sin\left(\frac{\pi}{N}\right) \cos\left(\frac{\pi}{N}\right)\right). \tag{13}$$

From these two equations, we can see that with the given strength of injection locking, a larger frequency difference $(\Delta\omega)$ between the injection signal and free-running RO signal will make the embedded TDC DNL worse. If $\Delta\omega = 0$, there will be no DNL resulting from injection locking.

2.3. Proposed ADPLL with Calibration-Free RO-Based Injection Locking TDC

The overall architecture of the proposed type-I ADPLL is shown in Figure 5. To overcome the poor phase noise caused by RO, we use LCDCO to inject the embedded TDC. To achieve a wide output frequency range and high0output frequency accuracy at the same time, LCDCO will adopt three discrete frequency tuning modes: coarse mode, medium mode, and fine mode. The frequency tuning range of each mode will cover the frequency range of at least 6 LSBs of the previous mode. In order to overcome the PVT variations and cover the frequency range of 2.4–2.48 GHz in BLE, the coarse tuning range shall be at least 500 MHz. Based on Equation (8), if we apply $N = 6$ and $\omega_{BW} = 500$ MHz in this expression, we have $I_{inj}/I_{OSC} = 0.5$; this will inevitably increase the injection current and power consumption.

Since the coarse mode and medium mode in the ADPLL locking process have no requirements for phase noise, in order to further reduce the power consumption, the improved ADPLL locking process is as follows: When the loop enters the coarse and medium tuning mode, turn off RO and TDC, as shown in the dotted line in Figure 5, we use the output of LCDCO as the input of the high-speed counter, and the loop only calculates the integer part of the phase error. After the medium mode, the frequency accuracy of the target channel will reduce to a few megahertz. Then the RO tuning mode is on, and the output of one phase of RO is used as the input of the counter to calculate the integer phase error. After the coarse RO tuning finishes, the frequency difference between RO and LCDCO is only about 10 MHz, which leaves a small injection-locking bandwidth. Thus, the power consumption of the injection current can be reduced.

After the RO tuning control, the fine control mode is on to complete the final locking, the RO tuning control bits are fixed, and the injection locking path is turned on. Then the fractional phase error is calculated through injection-locked RO-based TDC. Figure 6 shows the functional diagram of different locking modes of the ADPLL.

Since the frequency of free-running RO and the injected source are close enough because of the RO tuning control, according to [22], the transfer function of the injection locking loop can be expressed as:

$$\frac{\phi_{\text{out}}(s)}{\phi_{\text{inj}}(s)} = H_{inj}(s) = \frac{\omega_{BW\_IL}}{s + \omega_{BW\_IL}}. \tag{14}$$

where $\phi_{\text{out}}(s)$ is the injected output phase and $\phi_{\text{inj}}(s)$ is the phase of the injection source. From this equation, we can see that the injection locking loop is low pass filtered. Figure 7 shows the phase domain model of the proposed ADPLL with major noise sources, including reference noise, TDC noise, DCO noise, and RO noise.

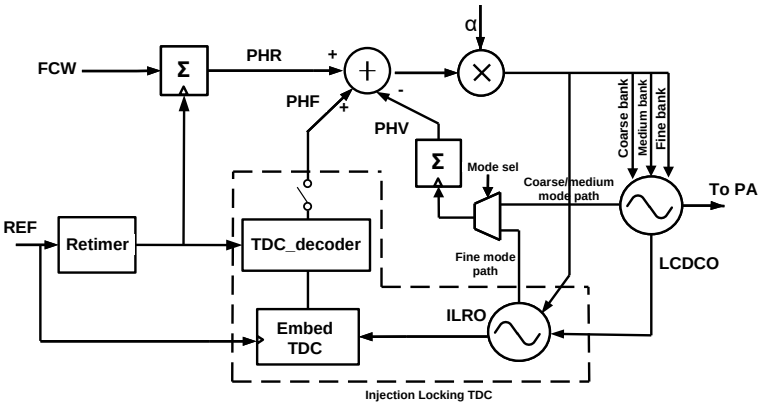

Figure 5. Block diagram of the proposed ADPLL.

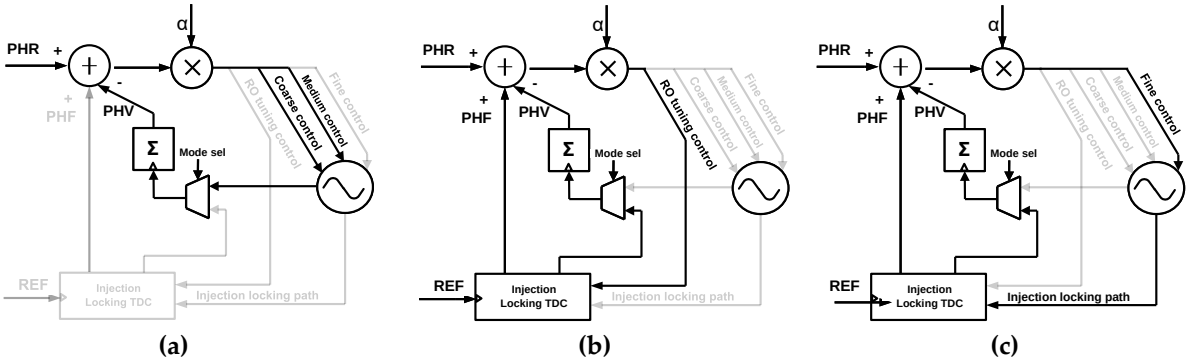

Figure 6. (**a**) Coarse mode and medium mode of the proposed ADPLL; (**b**) RO tuning mode of the proposed ADPLL; (**c**) Fine mode of the proposed ADPLL.

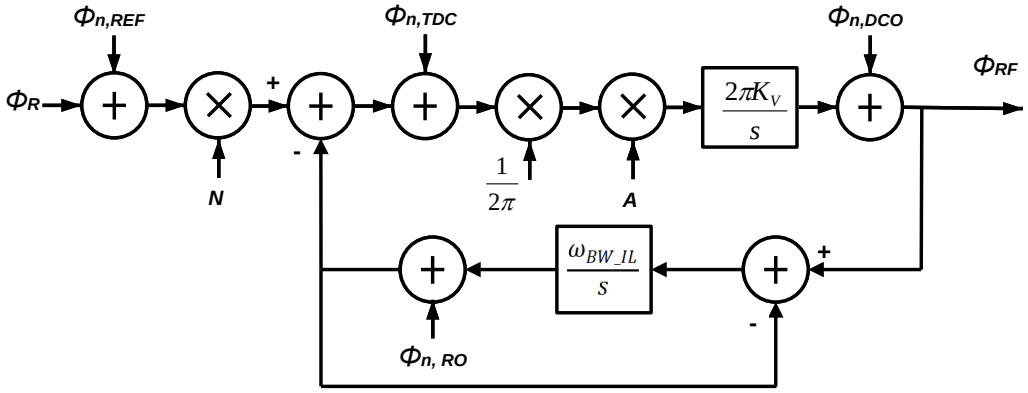

Figure 7. Noise model of the proposed ADPLL.

The open-loop transfer function can be written as:

$$H_o(s) = \frac{AK_v}{s}. \tag{15}$$

Then the closed-loop transfer function is:

$$H_c(s) = \frac{NH_o(s)}{1 + H_{\text{inj}}(s)H_o(s)} = \frac{NAK_V(s + \omega_{BW\_IL})}{s^2 + s\omega_{BW\_IL} + AK_v\omega_{BW\_IL}}. \tag{16}$$

where the damping factor ζ is $0.5\sqrt{\omega_{BW\_IL}/AK_v}$. The phase noise transfer functions of different noise sources are given by:

$$\frac{\phi_{RF}(s)}{\phi_{n,RO}(s)} = -\frac{AK_v s}{s^2 + s\omega_{BW\_IL} + AK_v\omega_{BW\_IL}}, \tag{17}$$

$$\frac{\phi_{RF}(s)}{\phi_{n,DCO}(s)} = \frac{s^2 + s\omega_{BW\_IL}}{s^2 + s\omega_{BW\_IL} + AK_v\omega_{BW\_IL}}, \tag{18}$$

$$\frac{\phi_{RF}(s)}{\phi_{n,TDC}(s)} = \frac{AK_v(s + \omega_{BW\_IL})}{s^2 + s\omega_{BW\_IL} + AK_v\omega_{BW\_IL}}, \tag{19}$$

$$\frac{\phi_{RF}(s)}{\phi_{n,REF}(s)} = \frac{NAK_v(s + \omega_{BW\_IL})}{s^2 + s\omega_{BW\_IL} + AK_v\omega_{BW\_IL}}. \tag{20}$$

These equations show that the noise contributions are all affected by the injection locking bandwidth ω_{BW_IL}. The simulated phase noise of DCO and RO to the ADPLL output with different ω_{BW_IL} is shown in Figure 8. It can be seen that with the constant AK_v, which determines the loop bandwidth of ADPLL, ω_{BW_IL} should not be too small because the loop will become unstable, and the phase noise of ADPLL will get worse by RO. With a proper set of ω_{BW_IL}, the noise floor of RO will have no influence on the total PN output.

Figure 9 shows total phase noise with TDC quantization and FREF noise considered. From (20), we can see that the phase noise of FREF will be up-converted by $20\log N$. However, because of the superior phase noise performance of the crystal oscillator, the output phase noise will still be below the DCO phase noise. The TDC resolution is equal to a single-stage RO delay t_{res} , which dominates the in-band phase noise of ADPLL. To have a better performance of in-band phase noise, one should increase the number of RO stages so as to decrease t_{res} . However, this will inevitably result in high power consumption.

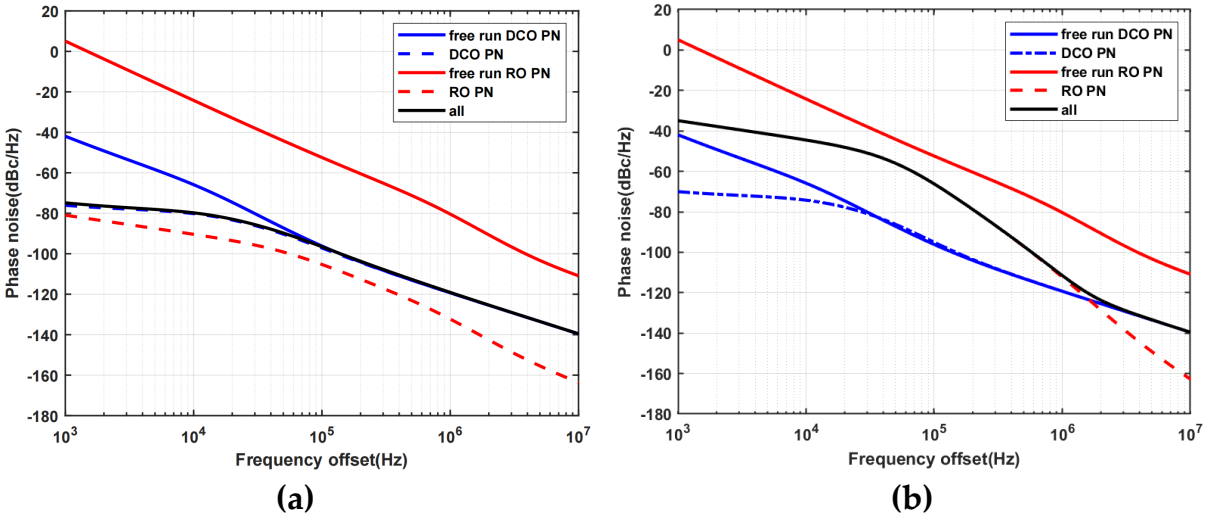

Figure 8. ADPLL phase noise contributed by DCO and RO with $AK_v = 160$ kHz. (**a**) $\omega_{BW\_IL} = 20$ MHz; (**b**) $\omega_{BW\_IL} = 100$ kHz.

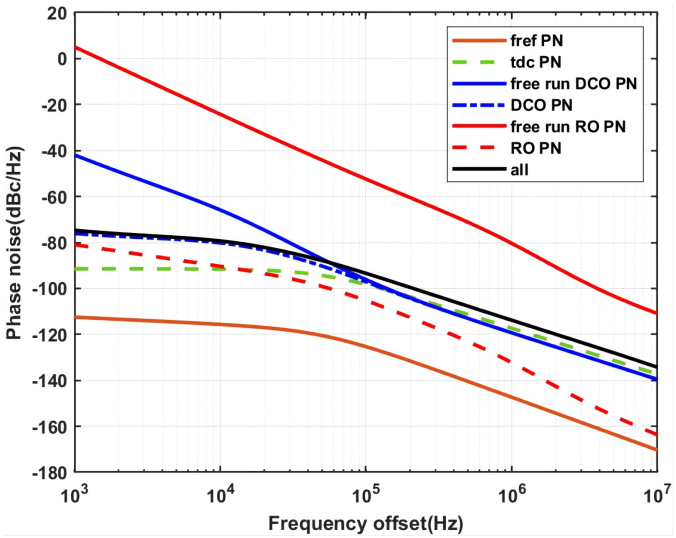

Figure 9. Total phase noise contribution of the proposed ADPLL.

3. Circuit Implementation

3.1. Ring Oscillator

The circuit implementation of injection-locked RO-based TDC is shown in Figure 10. We use a 6-stage pseudo-differential RO to oscillate at 2.4 GHz, which provides 12 TDC phases and $t_{res} = 34.7$ ps. This will result in -91 dBc/Hz in-band phase noise with a 32 MHz reference clock. The output of every phase of RO is connected to the buffer and sampled by FREF. Then the 12 bits output is encoded to roughly 3.5 bits as the fractional phase error of the phase detector. Another output of the RO is also buffered to the counter to accumulate as the integer phase error. To minimize the TDC DNL, every output of RO must connect to two buffers to balance the loading. Therefore, the buffers that are not used are connected to dummies. Since the capacitance loading will decrease the oscillation frequency, one must increase the current to obtain the same frequency. Therefore, the size of the buffer in the first stage is pretty small and increases stage by stage. Similarly, the RO delay cell we choose is two inverter stages with NMOS-only cross-coupled pairs instead of CMOS cross-coupled pairs, as shown in Figure 11. The layout of the RO should also be carefully designed to decrease any unwanted parasitic capacitance.

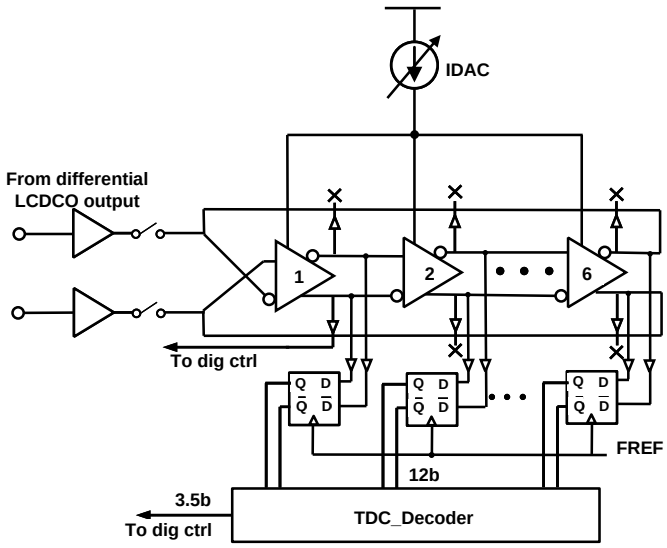

Figure 10. Circuit implementation of the injection-locked RO-based TDC.

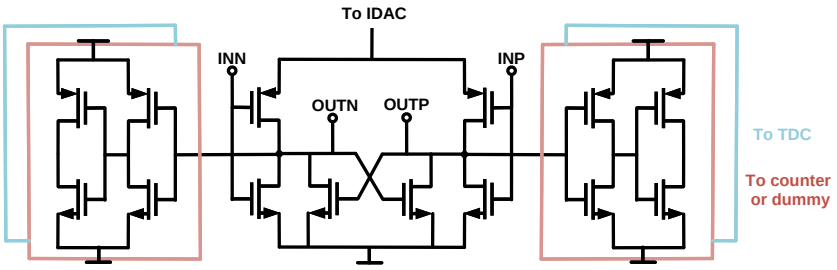

Figure 11. Circuit of the RO delay cell.

The oscillation frequency of RO is tuned by the current steering DAC that is shown in Figure 12. The length of these transistors should be wide to implement accurate, current replication. To realize a 10 MHz LSB tuning step of the DAC, we use six control bits to cover at least an 800 MHz tuning range.

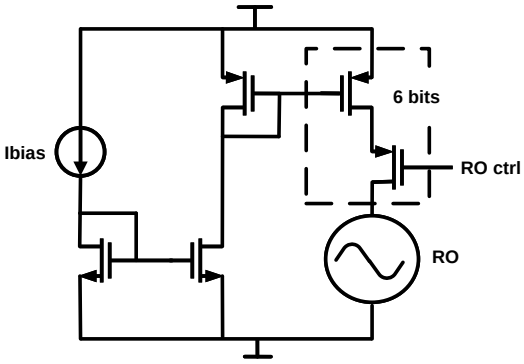

Figure 12. Circuit of the current steering DAC.

3.2. LC-Based DCO

The LCDCO we use is a typical CMOS architecture with both NMOS and PMOS cross-coupled pairs as the negative resistance stage and a digitally tuned resistor tail, as shown in Figure 13. Because of the flicker-noise up-conversion of MOS transistor bias, a poly-silicon resistor is adopted for biasing instead of a MOS-based current source [23]. The resistor only has the thermal noise and will be filtered by the added tail capacitor C_{tail}. The current of the LCDCO can be regulated by the resistor, which will result in the variation in output

amplitude and phase noise. This bias technique also saves a large amount of area compared to the current source bias.

The power consumption in the LC circuit needs the negative resistance to compensate so as to sustain the oscillation. To find the lower limit of power consumption of the LCDCO, we calculate the energy stored in the capacitor or the inductor that:

$$W(t) = \frac{1}{2}Li^2(t) = \frac{1}{2}Cv^2(t). \tag{21}$$

where $i(t)$ and $v(t)$ are the currents through the inductor and the voltage of the capacitance. Since the quality factor of an on-chip inductor is much worse than the capacitor banks, we make an assumption that the total equivalent parasitic resistance R_S is connected in series with the inductors. Combined with (21), the power loss due to R_S is equal to:

$$P_{\text{loss}} = \frac{1}{2}R_s i^2_{\text{max}} = \frac{1}{2}\frac{Cv^2_{\text{max}}R_s}{L}. \tag{22}$$

With the equation $f = \frac{1}{2\pi\sqrt{LC}}$ we can conclude that:

$$P_{\text{loss}} = \frac{1}{8\pi}\frac{v^2_{\text{max}}R_S}{f^2L^2} = \frac{1}{2}\frac{v^2_{\text{max}}}{L\omega Q_L}. \tag{23}$$

where Q_L is the quality factor of the inductor. We can see from this equation that the power loss is inversely proportional to the inductance if the operating frequency and the equivalent parasitic resistance are constant. However, if the inductance is too large, the tuning range of the capacitor banks will be reduced, and the self-resonant frequency will be decreased. Therefore, in this project, a value of 6.4 nH of inductance is chosen to balance these issues.

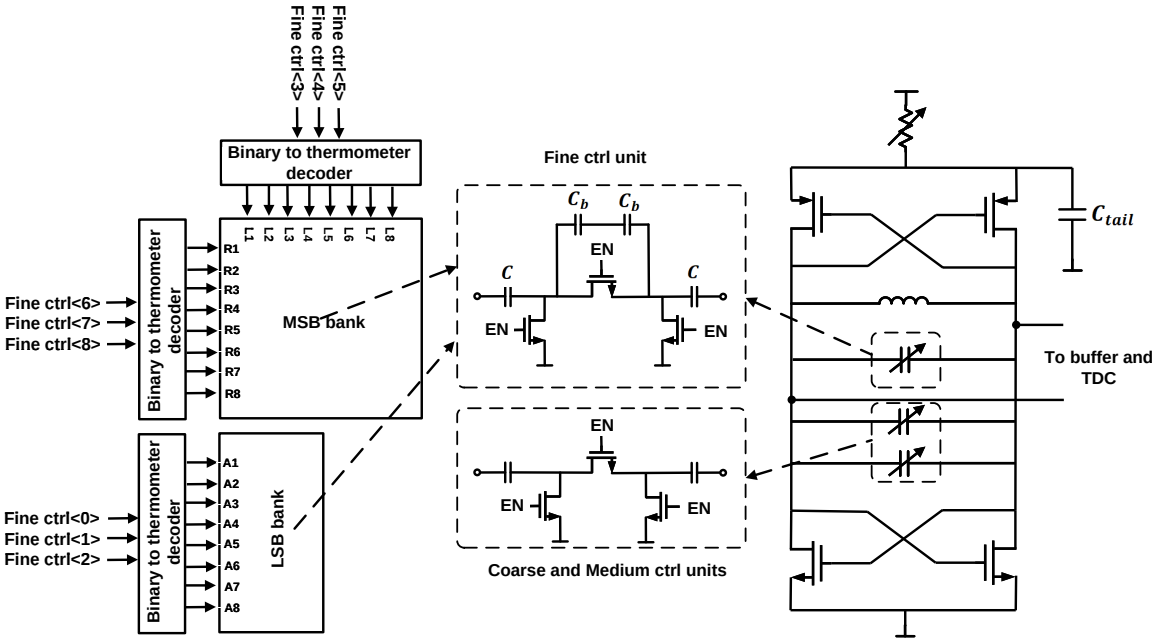

Figure 13. Circuit of the LCDCO.

The capacitor array of the LC tank in the LCDCO is composed of a coarse capacitor bank, medium capacitor bank, and fine capacitor bank. The control unit of each bank is shown in Figure 13. we use MOM capacitors instead of MOS varactors to realize these three banks because they are less sensitive to PVT variations. In the coarse mode, the unit capacitor of the coarse capacitor bank is set to 25 fF to achieve a 14 MHz tuning step,

and we use 6 bits binary control to achieve a 1 GHz tuning range. The control unit of the medium bank is the same as the coarse bank with a difference of a smaller unit capacitor of 3.3 fF to achieve a 2 MHz tuning step, and 6 bits binary control is also adopted to achieve a 120 MHz tuning range. The fine banks are 9 bits that can cover 16 MHz with a tuning step of 40 kHz, which needs a 23 aF capacitor unit. Two capacitors C_b with a large C_b/C ratio are used to create such a small change of capacitance in fine mode. The fine bank is thermometer-coded to implement an improved matching performance. However, a 9-bit fine bank with the thermometer coded needs 511 unit cells, and the area of each cell is large due to the large C_b. To reduce the large area caused by the fine bank, we divide the fine bank into 6 MSB bits and 3 LSB bits, each MSB cell with a step equal to eight times that of the LSB cell. This only produces 63 MSB unit cells and 7 LSB unit cells with a smaller C_b in MSB unit cells compared to the LSB unit cells, thus achieving a reduced area and parasites of the fine bank. The diagram of the fine capacitor bank is shown in Figure 13.

4. Simulation and Measurement Results

The proposed ADPLL was fabricated in a TSMC 40-nm CMOS process, and the layout photograph of the chip is shown in Figure 14. The core area of the ADPLL is 0.22 mm^2. Figure 15 shows the transient waveform of the ADPLL operation with post-layout simulation. The reference frequency is 32 MHz, and the target frequency is set to 2.414 GHz. The locking process of the ADPLL is divided into the coarse mode, medium mode, RO tuning mode, and fine mode. First, we set the target frequency to 2.414 GHz by manually adjusting the frequency division ratio. Then, the ADPLL works in the coarse mode; the loop is automatically calibrated with a given coarse mode loop bandwidth until the control bits toggle between two adjacent bits. After that, the ADPLL works in the medium mode with the coarse control bits fixed. The medium mode loop bandwidth of ADPLL is set lower compared to the coarse mode to ensure a smaller frequency resolution. After the medium mode, the frequency accuracy of the target frequency will reduce to a few megahertz. Then, the RO is on; the loop waits for 500 ns to make the RO stable. Then the RO tuning mode is on, and the target frequency is also set to 2.414 GHz. At the same time, the LCDCO keeps the tuning bits unchanged. After the RO tuning mode, the switch between the LCDCO and RO is on. The RO is injection-locked by LCDCO in fine mode. The fractional error is calculated by RO-based TDC to complete the final locking. As shown in Figure 15, the ADPLL will toggle between several control bits when the loop is locked. This is caused by the limited quantization error of TDC, and the noise will dominate the in-band phase noise of the ADPLL as the loop bandwidth is wider (e.g., 2 MHz, as shown in Figure 15).

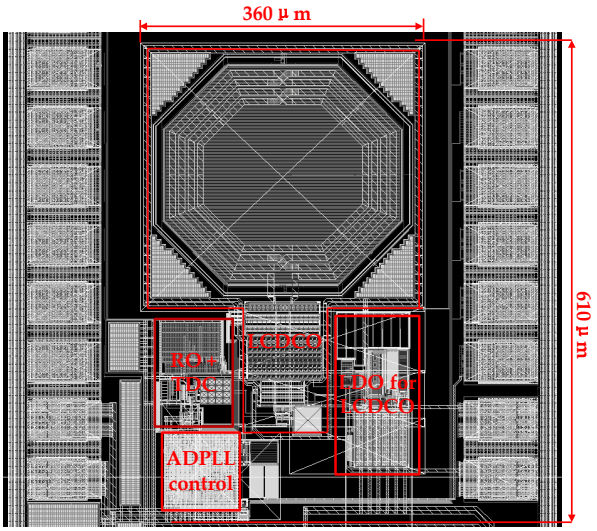

Figure 14. Layout photograph of the ADPLL chip.

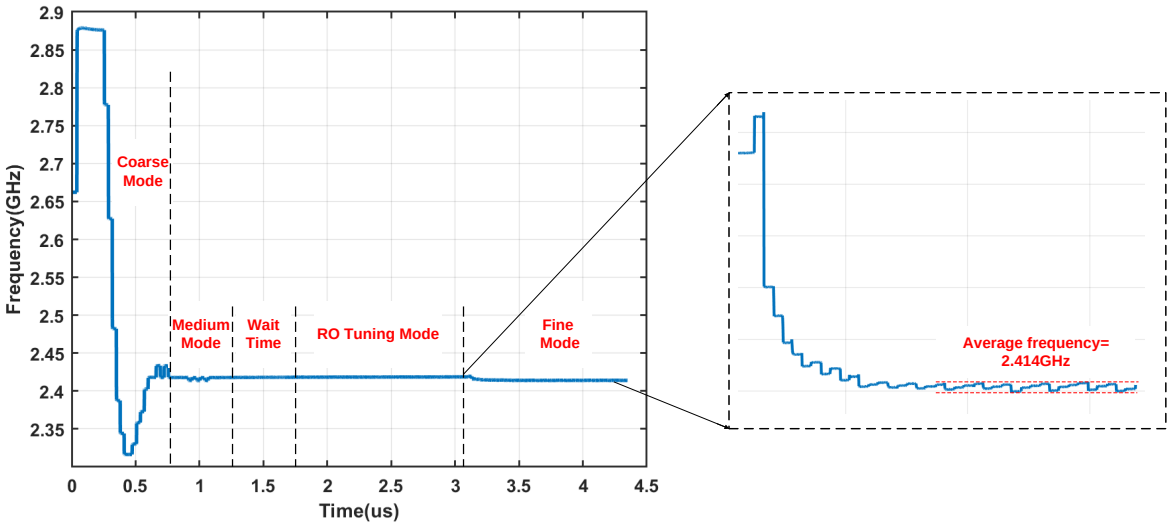

Figure 15. Transient waveform of the system operation with post-layout simulation.

Figure 16 shows the performance of injection-locked TDC after post-layout simulation. The oscillation frequency is set to 2.45 GHz. It can be seen that there are two positive peak values of DNL, which are caused by the differential input of the injection current. However, they are all less than 0.17 LSB, and the influence on ADPLL can be negligible.

To ensure the normal operation of ADPLL, the free oscillation frequency of RO needs to be tuned close to the locking frequency. Figures 17–19 shows the measured phase noise performance of the free-running RO, free-running DCO, and the locked ADPLL. We set the target locking frequency to 2.448 GHz. In the RO test mode, the frequency of RO is manually adjusted to the frequency closest to 2.448 GHz. The poor phase noise of RO is shown in Figure 17. We can see that the oscillation frequency of RO is 2.46 GHz, which has a 12 MHz difference compared to the target frequency. Then, the ADPLL skips the RO tuning mode and finally locks to 2.448 GHz. The loop bandwidth is set to 100 kHz to reduce the in-band phase noise of TDC. The phase noise performance of the closed-loop is shown in Figure 19, which is the same when the RO is set to auto-tuning mode, showing that with a proper setting, the phase noise of RO will not influence the total phase noise of ADPLL. The ADPLL spectrum output is shown in Figure 20, and the reference spur is −65 dBc.

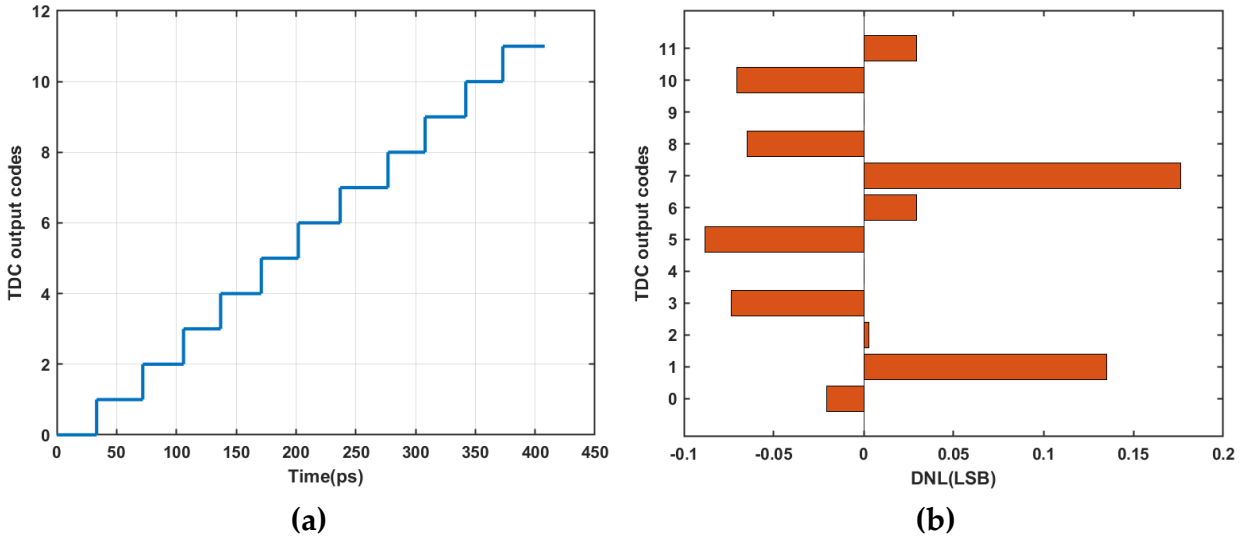

Figure 16. (**a**) TDC gain with post-layout simulation; (**b**)DNL performance of TDC.

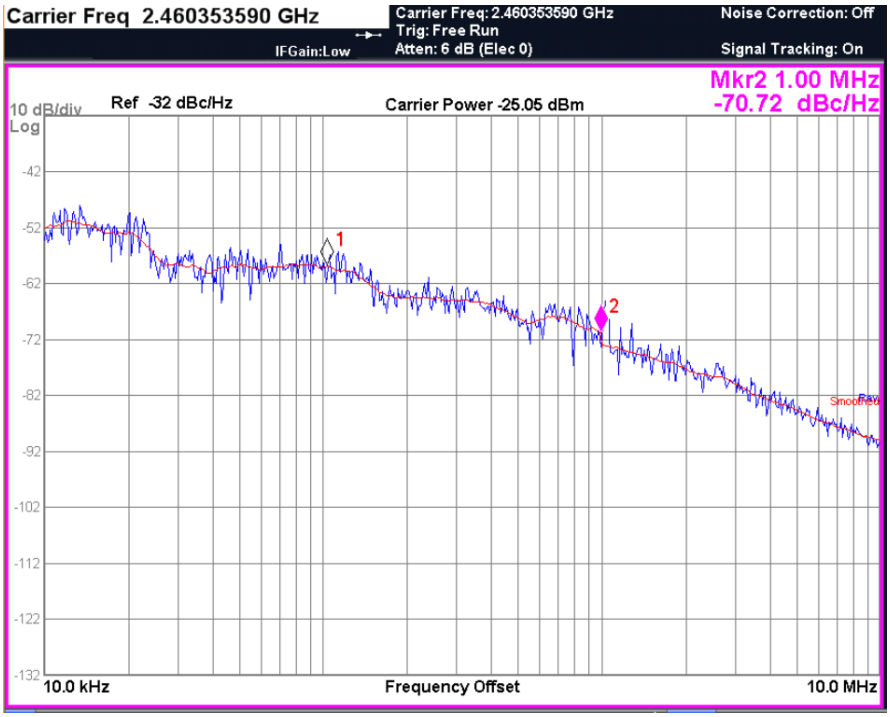

Figure 17. Measured phase noise performance of free-running RO.

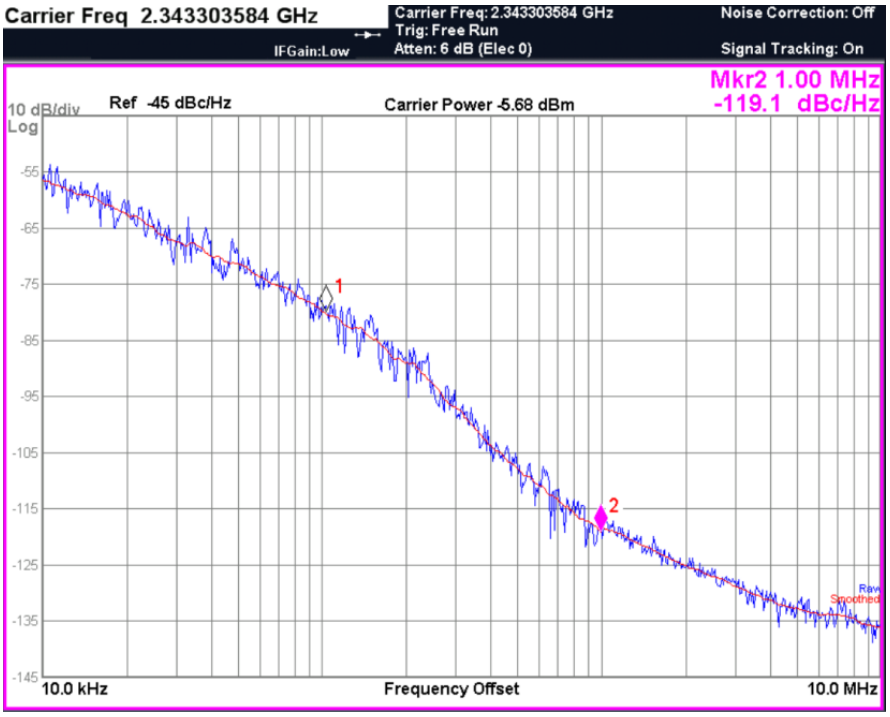

Figure 18. Measured phase noise performance of free-running DCO.

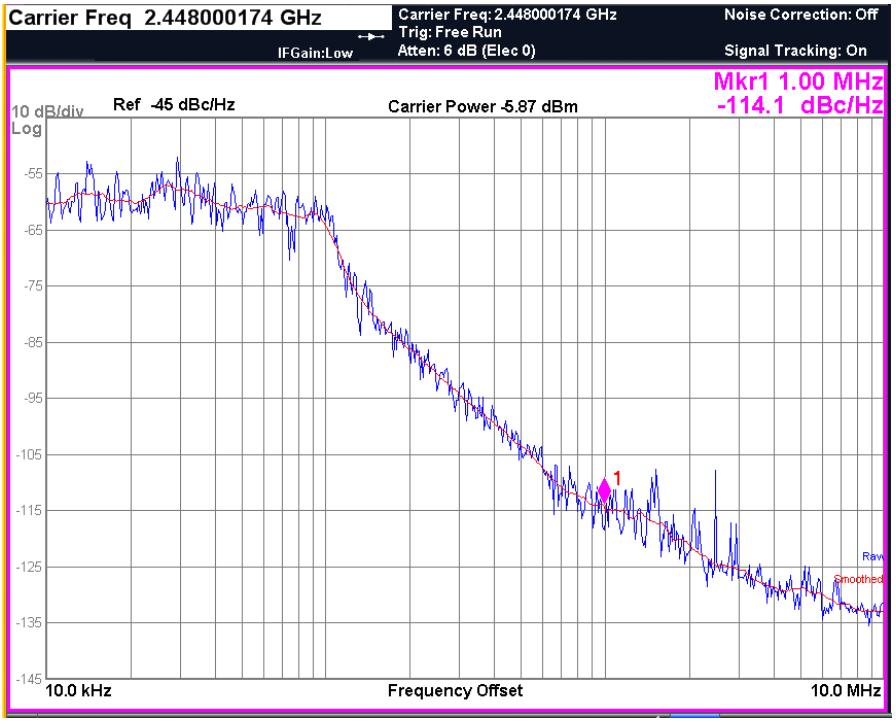

Figure 19. Measured phase noise performance of closed-loop ADPLL.

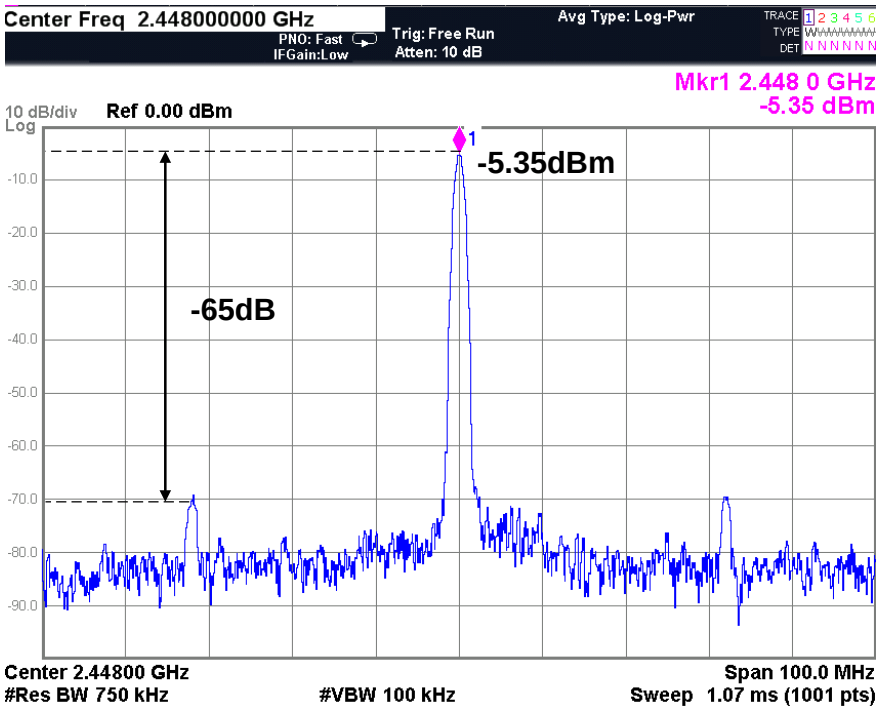

Figure 20. Measured ADPLL spurious performance.

The measured power consumption of the ADPLL with a 1 V power supply is shown in Figure 21. In coarse mode and medium mode, the RO is shut down, and the total power consumption is only 773 µW. In RO tuning mode and fine mode, the LCDCO and buffer consume 541 µW, and the RO and digital part consume 582 µW and 246 µW. The total power of ADPLL consumes 1.4 mW. Figure 22 shows the test environment. The external power supply consists of three separate parts. The digital part of the circuit is directly powered by an external 1 V supply, and the PA is a 1.5 V supply. To ensure the best

performance of the oscillator, the power supply of LCDCO and the RO are separated by two low-dropout (LDO) regulators. The LDO is powered by a 3 V supply, and the total current consumption is 2 mA, including the internal bandgap circuit. Table 1 shows the ADPLL performance compared with the state-of-the-art. The power consumption of the proposed work is only 1.4 mW, which is comparable with the advanced low-power ADPLL designs but with a better out-of-band phase noise [12,24]. The ADPLL of [15] consumes only 379 µW because of the ultra-low-power RO and reduced locking frequency. However, the much worse phase noise performance lowers the PLL FoM. The balanced performance of our work will be more attractive in a BLE transceiver design.

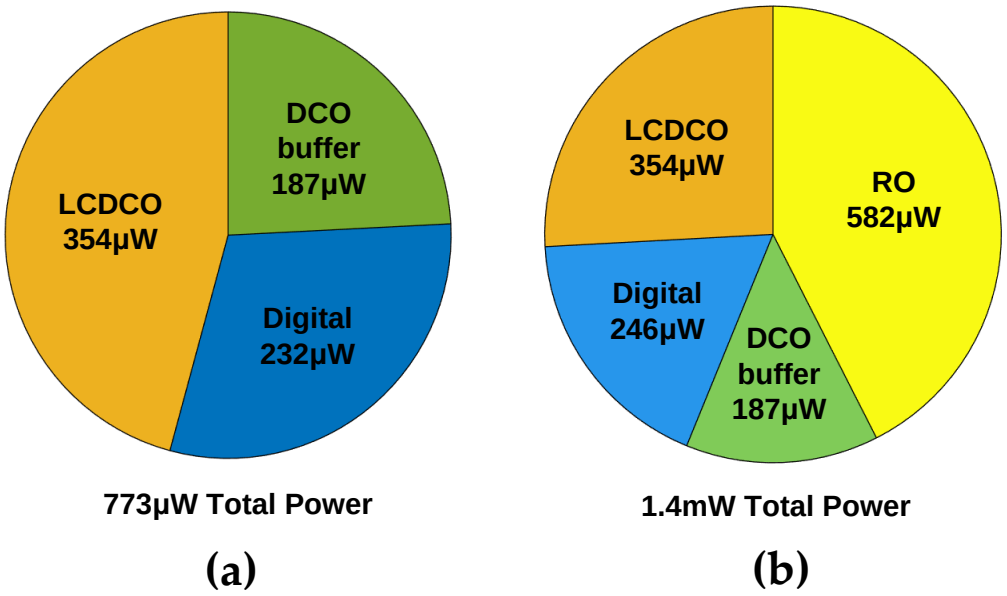

Figure 21. ADPLL power breakdown in (**a**) coarse mode, medium mode, and (**b**) RO tuning mode and fine mode.

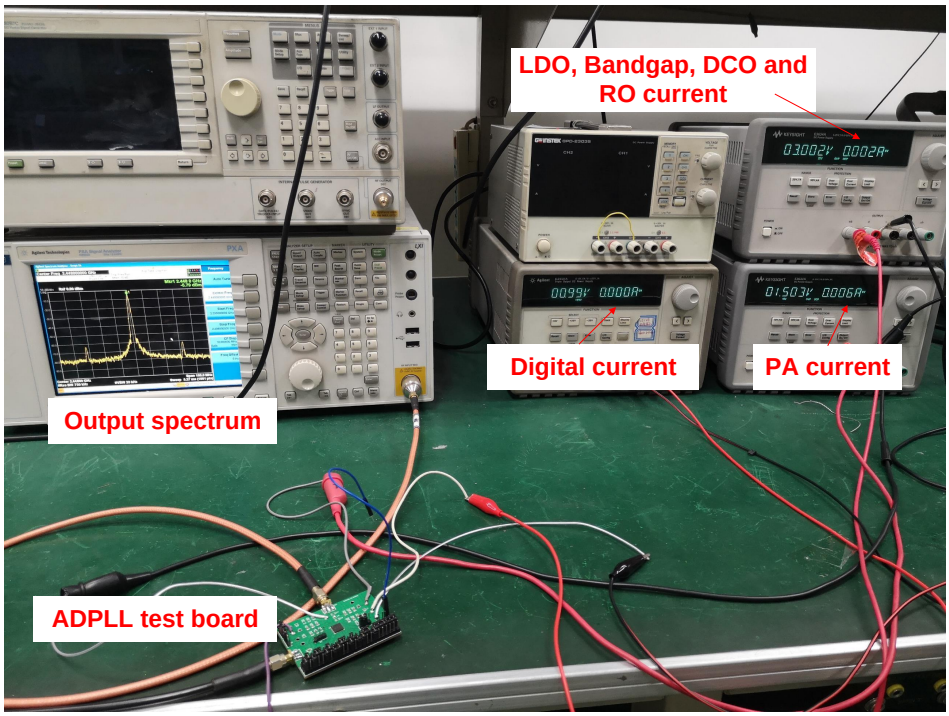

Figure 22. ADPLL test environment.

Table 1. Performance comparison with the state-of-the-art.

	TCAS-I 2016 [13]	JSSC 2019 [15]	TCAS-I 2017 [24]	JSSC 2020 [12]	This Work
Technology	65 nm CMOS	40 nm CMOS	40 nm CMOS	22 nm FD-SOI	40 nm CMOS
Frequency Range	2.7–4.8 G	2.4–2.48 G	1.7–2.7 G	2.4–2.48 G	2.4–2.48 G
PLL Architecture	LCDCO + Injection-locked RO	RO-based	LCDCO + Snapshot DTC-based TDC	LCDCO + SAR-ADC-based TDC	LCDCO + Injection-locked RO
Phase Noise	−90 dBc/Hz @40 kHz −128 dBc/Hz @3 MHz	−85 dBc/Hz @1 MHz	−109 dBc/Hz @1 MHz	−85 dBc/Hz @10 kHz −110 dBc/Hz @1 MHz	−114 dBc/Hz @1 MHz
Power Consumption	21.2 mW	379 µW	1.19 mW	1.25 mW	1.4 mW
PLL FoM [1]	N/A	−208.5	−234.6	N/A	−212.1

[1] $\text{FoM} = 10\log_{10}\left(\left(\sigma^2_{\text{jitter}}\right) * \left(\frac{P}{1mW}\right)\right)$.

5. Conclusions

In this paper, a low-power ADPLL with calibration-free RO-based injection-locking TDC is proposed. By analyzing the injection-locking behavior and its influence on phase noise and the TDC performance, we use six pseudo-differential stages RO as 3.5 bits TDC to balance the in-band phase noise and the power consumption. The injection-locking bandwidth is set to 10 MHz to minimize the injection current. The ADPLL is divided into four modes, and the fractional phase detection of the phase error is turned down to reduce power. The LCDCO is used to inject the RO-based TDC and consumes only 354 µW. The total power of 1.4 mW is achieved when the ADPLL is locked. Moreover, it can further benefit from technology scaling due to its digitally intensive nature.

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Conflicts of Interest: The authors declare no conflict of interest.

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