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A Fault Clearance and Restoration Approach for MMC-Based MTDC Grid

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Abstract: With the growth in continuous energy demand, high-voltage Multi-Terminal DC (MTDC) systems are technically and economically feasible to transmit bulk power and integrate additional energy sources. However, the high vulnerability of the MTDC systems to DC faults, especially pole-to-pole (P2P) faults, is technically challenging. The development of DC fault ride-through techniques such as DC circuit breakers is still challenging due to their high cost and complex operation. This paper presents the DC fault clearance and isolation method for an MMC-based MTDC grid without adopting the high-cost DC circuit breakers. Besides, a restoration sequence is proposed to re-energize the DC grid upon clearing the fault. An MMC-based four-terminal DC grid is implemented in a Control-Hardware-in-Loop (CHIL) environment based on Xilinx Virtex-7 FPGAs and Real-Time Digital Simulator (RTDS). The RTDS results show that the MTDC system satisfactorily rides through DC faults and can safely recover after DC faults.

Keywords: Modular Multilevel Converter (MMC); Multi-Terminal DC grid; MTDC; DC faults; protection strategy

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1. Introduction

Increasing energy demand is propelling more renewable energy-dominated power grids all around the globe. That is because renewable energy sources do not emit carbon dioxide (CO_2) and other greenhouse gases to contribute to the ongoing climate warming. However, due to insufficient infrastructure and independent operation, most power grids are not ready for bulk renewable energy penetration into their old fossil-based power generation systems. That is where the High Voltage Direct Current (HVDC) transmission system appears to accommodate more clean energy sources, carry bulk power long distances, and interconnect asynchronous or weak grids. The capital cost poses a significant limitation for HVDC transmission. Once cost-effective solutions are developed for the capital cost of the HVDC, it will be more cost effective than the commonly used High Voltage Alternating Current (HVAC). HVDC transmission is considered more cost effective for longer distances. After all, it has more minor capacitive losses than the HVAC, especially when the conductors are placed closer to the ground. Besides, reactive power compensation is not required along with the transmission as HVDC only transmits active power. Moreover, DC cables do not have frequency and there is no concern about corona effects. On the other hand, HVAC lines are usually bundled to increase the effective radius of the bundled conductors to reduce the corona discharge. Yet, this method increases the overall line capacitance. Lastly, DC transmission requires a single or double conductor per circuit, whereas AC transmission requires a three-phase circuit and more conductors overall. HVDC transmission lines do not have the same environmental, electro-magnetic, and visual issues while building new Right-of-Ways (ROW) as the HVAC lines. Moreover, HVDC lines can be placed on the existing AC transmission towers to reduce the build-out cost without any

mutual-coupling concern. The highly versatile structure of the HVDC transmission allows the integration of more renewable energy sources while satisfying the growing energy demand in a cleaner, cheaper, and more reliable way. Voltage Source-based Converter (VSC) topologies, especially the Modular Multilevel Converter (MMC), are a significant enabler of the HVDC transmission. One of the essential benefits of the MTDC grid is to transmit power to isolated, remote communities or different load centers while providing voltage stability and operational reliability to the entire system under AC transients. Several weak grids, renewable energy sources, or various asynchronous grids can be easily connected to an MTDC grid [1,2]. Unlike a two-terminal DC grid, an MTDC grid flexibly manages heavily loaded AC systems, configuring some terminals as an inverter to inject more power into the grid. Besides, MTDC grids are resilient to operate under catastrophic generator or line-outage conditions without completely stopping the power transmission at the healthy part of the system [3,4]. Concisely, an MTDC grid is quite favorable regarding stability, sustainability, operational cost, system reliability, and availability. Therefore, the MMC-based Multiterminal High Voltage DC (MTDC) grid application is becoming popular worldwide. In 2016, the world's first five-terminal MMC-based Zhoushan MTDC grid was commissioned to improve regions' supply quality with challenging geographical structures [5,6].

Nevertheless, DC fault clearance and protection are still significant challenges for MTDC development. DC fault requires fast, accurate, reliable detection and isolation. Traditionally, AC circuit breakers (ACCBs) are adopted to protect HVDC grids [7,8]. However, the operation time of ACCBs is between 50 to 100 milliseconds (ms) which is not fast enough to protect the solid-state power electronics components in the converter stations. Despite the slow operation, ACCBs are still adopted in MTDC protection in collaboration with the DC disconnectors [9]. However, a DC fault may cause a substantial fault current due to the small impedance of DC cables and the grounding methods before the ACCBs operate. Similarly, due to the DC fault current's fast propagation, the converter station's DC voltage may be reduced drastically.

Hence, HVDC transmission needs a proper, economic, and rapid DC fault detection and protection scheme. Different solid-state hybrid DCCBs are developed in [10–13]. However, on-state losses and the cost are the main challenge of the proposed DCCBs as high voltages, hence, researchers created alternative fault protection schemes. In [14–18], DC reactors are proposed to be placed at each end of the DC cables to limit the fault current and detect the rate of voltage change in the reactors. Nevertheless, high power loss in the reactors, fast sampling frequency requirement, and lower reliability of the voltage screening equipment are the main challenges of this technique.

A full bridge submodule (FBSM)-based MMC, which has the ability to block fault currents, is presented in this paper. When all MMC switches are turned off, the DC fault current is forced to flow through the SM capacitors; thus, the DC is blocked. In other words, the fault is cleared using the MMC converter. DC circuit breakers are not used in this paper as they are expensive and not fully developed. Instead, low-voltage disconnectors isolate the faulty line when the fault current reaches zero. The fault clearance time of the DC fault depends on the fault location and the total impedance (capacitance, inductance, and resistance) in the MTDC network. All storage elements temporarily behave as energy sources during the DC faults. Therefore, detecting and blocking the fault current is essential before it reaches a high level.

Due to the ultra-high voltage of the DC grid, the proposed fault clearance and restoration scheme cannot be tested in a laboratory environment because of safety hazards. Thus, the effectiveness of the proposed method is validated in a Control-Hardware-in-Loop (CHIL) environment in the Real-Time Digital Simulator (RTDS). The MMC terminals' detailed model and their controllers emulated Xilinx Virtex-7 FPGAs. The DC grid and the utility grids are modeled in the RTDS. A total of 12 Xilinx FPGAs are connected to the RTDS through fiber optic cables.

2. Modeling and Control of the MTDC System

A mesh-connected four-terminal MMC-based HVDC grid, shown in Figure 1, is adopted and investigated in this paper. All AC grids are modeled with a Short-Circuit Ratio (SCR) of 4 as strong grids and connected to an MMC system through a transformer. Each MMC arm consists of an N number of series-connected full bridge submodule (FBSM) and an inductor, as illustrated in Figure 2. The number of MMC SMs is different in each MMC. The MMC system parameters for each converter are tabulated in Table 1.

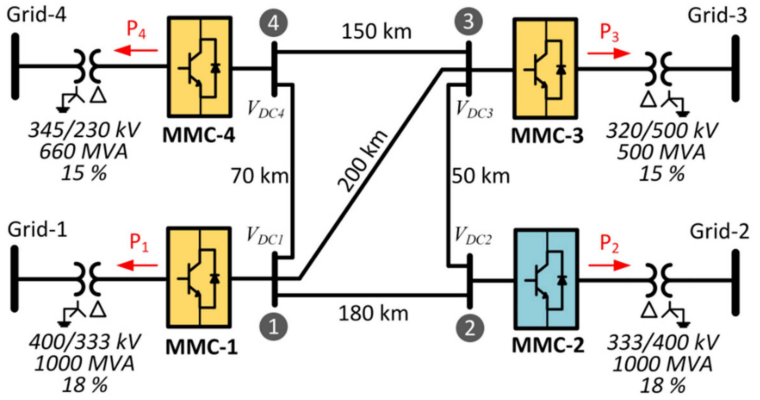

Figure 1. A mesh-connected four-terminal MMC system.

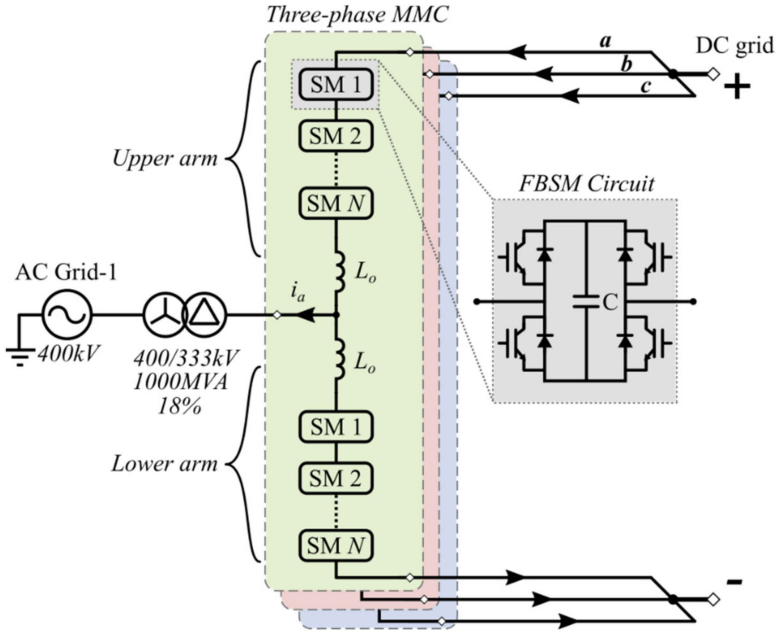

Figure 2. An FBSM structured three-phase MMC configuration (MMC-1).

Table 1. MMC parameters of the MTDC system.

Description	MMC-1	MMC-2	MMC-3	MMC-4
Rated power (MVA)	1000	1000	500	660
DC voltage (kV)	640	640	640	640
AC grid voltage (kV)	400	400	500	345
Transformer ratio	400/333	400/333	500/320	345/230
Number of SMs (*N*)	400	160	200	320
SM voltage (kV)	1.6	4	3.2	2
Arm inductance (mH)	50	50	55	30
SM capacitance (mF)	15	6	4	8

2.1. MMC System

The three-phase MMC circuit diagram, shown in Figure 2, consists of six arms. Each MMC phase contains an upper arm and a lower arm. Each arm comprises an N number of SMs and an inductor L_o. The dynamic equations of the upper-arm voltage $v_{u,x}$ and the lower-arm voltage $v_{l,x}$ of phase x are obtained as:

$$v_{u,x} = \frac{V_{DC}}{2} - L_o \frac{di_{u,x}}{dt} - R_o\, i_{u,x} - v_{m,x} \tag{1}$$

$$v_{l,x} = \frac{V_{DC}}{2} - L_o \frac{di_{l,x}}{dt} - R_o\, i_{l,x} + v_{m,x} \tag{2}$$

where the subscript x indicates the MMC phase number ($x \in a, b, c$), and $i_{u,x}$ and $i_{l,x}$ are the currents of the upper and lower arms, respectively; V_{DC} is the DC bus voltage; $v_{m,x}$ is the MMC AC-side interface voltage; and L_o and R_o represent the MMC arm impedance.

The upper- and lower-arm currents of phase x are defined as:

$$i_{u,x} = i_{z,x} + \frac{i_x}{2} \tag{3}$$

$$i_{l,x} = i_{z,x} - \frac{i_x}{2} \tag{4}$$

where i_x is the AC grid current of phase x and $i_{z,x}$ is the internal arm current of phase x.

The internal dynamic behavior of the MMC arms $v_{z,x}$ is obtained as:

$$v_{z,x} = L_o \frac{di_{z,x}}{dt} + R_o\, i_{z,x} = \frac{V_{DC}}{2} - \frac{v_{u,x} + v_{l,x}}{2} \tag{5}$$

The voltage references of the upper and lower arms of phase x are obtained by:

$$v^*_{u,x} = \frac{V_{DC}}{2} - v^*_{z,x} - v^*_{m,x} \tag{6}$$

$$v^*_{l,x} = \frac{V_{DC}}{2} - v^*_{z,x} + v^*_{m,x} \tag{7}$$

where $v^*_{z,x}$ represents the reference of the induced voltage of the arm inductor of phase x and $v^*_{m,x}$ is the reference of the MMC AC-side voltage.

Figure 3 shows the entire MMC control structure. The reference of the MMC AC-side voltage $v^*_{m,x}$ is provided from the main control obtained by considering the required active, reactive power and the DC bus voltage. This paper applies the conventional vector current control method-based d- and q-axes to develop the current control, as shown in Figure 3. The reference of the internal arm voltages $v^*_{z,x}$ is used to suppress the circulating currents. The circulating current suppression control (CCSC) method presented in [19] is applied in this paper. The nearest level modulation (NLM) technique is applied to the arm voltage reference $v^*_{k,x}$ ($k \in u, l$) to calculate the number of SMs required to be inserted into the system. The SM-level control, which includes SM voltage balancing, protection, and gate signal generating, presented in [20] is used in this paper to reduce the communication and computational burdens of controllers with a high number of SMs. The sorting-algorithm-based-voltage-balancing approach is used in this paper [4].

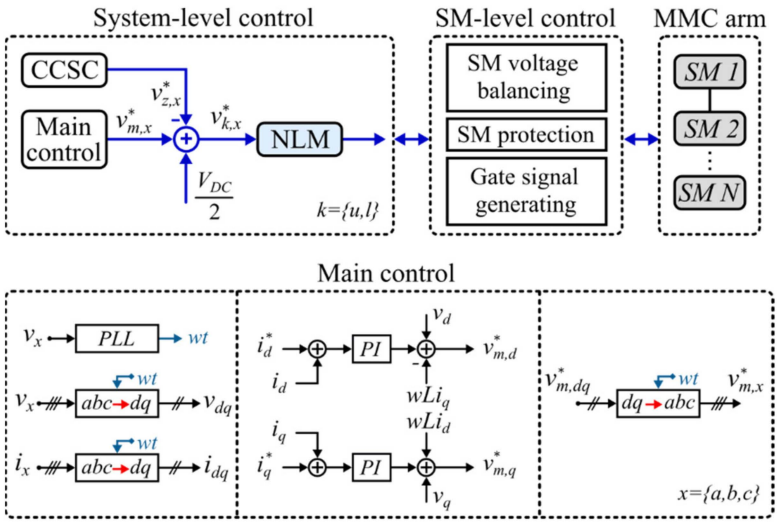

Figure 3. MMC control structure.

2.2. MTDC Grid

The MTDC system shown in Figure 1 consists of four MMC terminals, namely MMC-*i*, connected in a mesh configuration, where *i* indicates the terminal number (i.e., *i* = 1, 2, 3, and 4). The DC transmission lines' parameters are 0.025 Ω/km, 0.9356 mH/km, and 0.0123 μF/km. The length of TL_{ij} is illustrated on Figure 1, where TL_{ij} is the DC transmission line between terminals *i* and *j*.

The droop control, where several converters contribute to the DC bus voltage regulation, improves the DC grid reliability and stability. Figures 4 and 5 show the droop control block diagram and its characteristics applied to all MMCs. The power P_i is modified based on the droop characteristics R_i to control the DC voltage at the i^{th} terminal. If the steady-state error (*e*) is zero, the following equation is obtained:

$$V^*_{DCi} - V_{DCi} = R_i(P^*_i - P_i) \tag{8}$$

where R_i is the droop coefficient of the i^{th} terminal, which defines the sensitivity of the power change to the DC voltage change; P_i and V_{DCi} are the measured power and DC voltage, respectively, at the i^{th} terminal; and P^*_i and V^*_{DCi} refer to the power and voltage, respectively, for the i^{th} terminal.

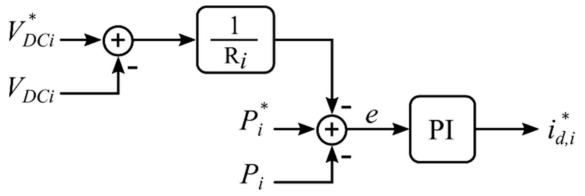

Figure 4. Droop control block diagram.

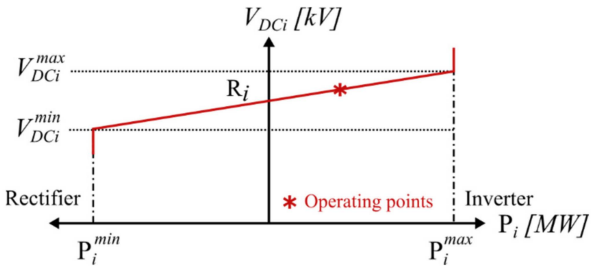

Figure 5. Droop control characteristics.

The power flow at the i^{th} terminal is defined as:

$$P_i = P_i^* - \frac{1}{R_i}(V_{DCi}^* - V_{DCi}) \tag{9}$$

In a large-scale MTDC system with long-distance transmission lines, the DC bus voltages of terminals might differ because of the voltage drop in the transmission lines. From (9), a large DC voltage difference $\left(V_{DCi}^* - V_{DCi}\right)$ results in a different power flow at the i^{th} terminal. The reference of the DC voltage of each converter station with droop control should be accurately obtained to precisely maintain the power flow amount under steady-state operating conditions. The power flow calculation of the DC network is required to obtain the operating points of each terminal in the DC network.

In this paper, terminal 2 is selected as a slack bus "V-bus" with prespecified DC voltage and the other terminals are identified as "P-bus" whose net injected power is known. Thus, the reference of the power P_i^* and DC voltage V_{DCi}^* for the i^{th} terminal is prespecified as follows:

$$P_i^* = \begin{bmatrix} P_1^* \\ P_2^* \\ P_3^* \\ P_4^* \end{bmatrix} = \begin{bmatrix} 800\ MW \\ Unknown \\ -300\ MW \\ 450\ MW \end{bmatrix} \tag{10}$$

$$V_{DCi}^* = \begin{bmatrix} V_{DC1}^* \\ V_{DC2}^* \\ V_{DC3}^* \\ V_{DC4}^* \end{bmatrix} = \begin{bmatrix} Unknown \\ 640\ kV \\ Unknown \\ Unknown \end{bmatrix} \tag{11}$$

The net injected power P_i into the DC grid from terminal i is obtained as follows:

$$P_i = V_{DCi} \sum_{j=1}^{4} Y_{ij} V_{DCj} \qquad i = 1,\ 2,\ 3,\ 4 \tag{12}$$

where Y_{ij} $(= \frac{1}{R_{ij}})$ is the admittance between the nodes i and j.

The nonlinear equation derived in (12) is solved with the Newton–Raphson method to calculate the unknown variables in (10) and (11) as follows [21]:

$$V_{DCi}^{(k+1)} = \begin{bmatrix} V_{DC1}^{(k+1)} \\ V_{DC3}^{(k+1)} \\ V_{DC4}^{(k+1)} \end{bmatrix} = \begin{bmatrix} V_{DC1}^{(k)} \\ V_{DC3}^{(k)} \\ V_{DC4}^{(k)} \end{bmatrix} + \mathcal{J}^{-1} \begin{bmatrix} P_1^* - P_1^{(k)} \\ P_3^* - P_3^{(k)} \\ P_4^* - P_4^{(k)} \end{bmatrix} \tag{13}$$

where $V_{DCi}^{(k)}$ and $V_{DCi}^{(k+1)}$ is the estimated DC voltage from the previous and current iteration, respectively; $P_i^{(k)}$ is the net injected power calculated from (12) using the estimated DC voltage $V_{DCi}^{(k)}$ from the previous iteration; and $\mathcal{J}$ is the Jacobian matrix.

After solving the nonlinear equation, the steady-state operating points of the MTDC system are obtained in Table 2. The power flow calculation results are reference set points for the droop controls to avoid power-sharing errors between the terminals.

Table 2. Power flow calculation of the MTDC grid.

Terminal #	Bus Type	DC Voltage	Net Injected Power
1	P-bus	633.053 kV	800 MW
2	V-bus "Slack"	640 kV	−962.906 MW
3	P-bus	638.168 kV	−300 MW
4	P-bus	632.984 kV	450 MW

3. Proposed DC Fault Clearance and Restoration Scheme

This section presents an MTDC grid protection strategy against permanent DC faults without the necessity of DC breakers. The protection approach mainly consists of the DC fault clearance and MTDC grid restoration strategy. The DC fault clearance stage includes fault detection, fault current I_f blocking, locating, and removing faulty line methods. The grid restoration strategy is initiated after clearing and isolating the DC fault completely. The DC fault clearance and grid restoration strategies are shown in Figure 6.

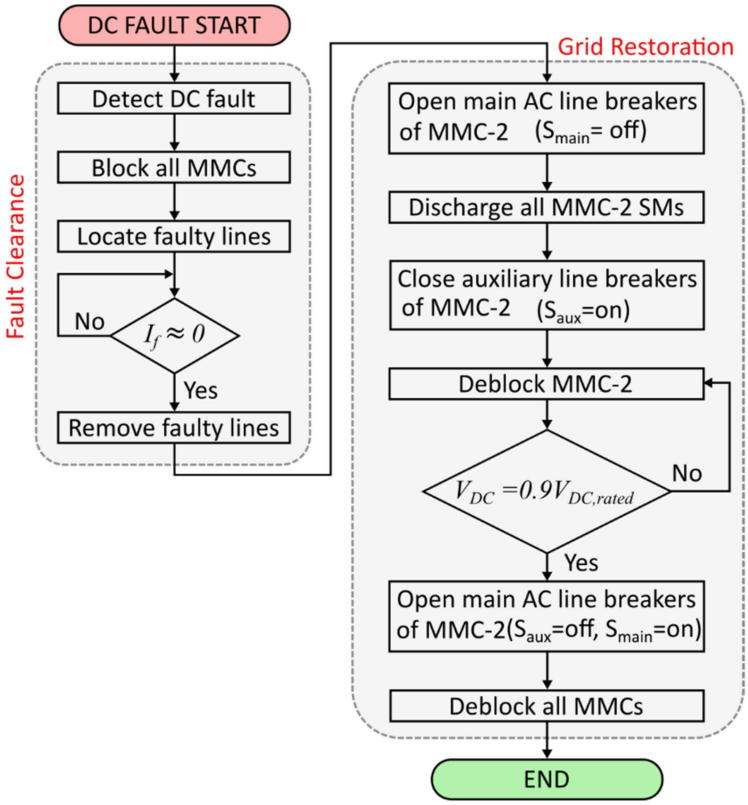

Figure 6. DC fault clearance and grid restoration flowchart.

3.1. DC Fault Detection

The DC current should always be maintained within prespecified thresholds to avoid an overcurrent issue in the system. If the DC current or voltage exceeds the prespecified threshold, action should be taken to prevent device damage. Typically, the DC current is substantially increased and the DC voltage is reduced during DC fault conditions. Thus, the DC fault can be independently detected from the DC current and voltage as follows [22]:

$$|I_{DCi}| > I_{thr,i} \quad or \quad |V_{DCi}| < V_{thr} \tag{14}$$

where I_{DCi} is the DC current of MMC-*i*. $I_{thr,i}$ and V_{thr} are the fault detection thresholds of the DC current and voltage, respectively.

If the DC current I_{DCi} is higher than the threshold value $I_{thr,i}$ of terminal *i*, or the DC voltage V_{DCi} is lower than the threshold value V_{thr} of terminal *i*, the MMC-*i* is blocked. The DC current and voltage fault detection thresholds are selected with an acceptable deviation for the operational deviations and safety margin. For instance, the DC current and voltage thresholds can be set as follows:

$$I_{thr,i} = 1.2 \times \frac{P_{rated,i}}{V_{DC,rated}} \tag{15}$$

$$V_{thr} = 0.85 \times V_{DC,rated} \tag{16}$$

where $P_{rated,i}$ is the rated power of MMC-*i* and $V_{DC,rated}$ is the rated DC voltage of the MTDC system.

3.2. DC Fault Clearance and Isolation

The FBSM-based MMC prevents the fault current from flowing from the AC to DC sides to protect the MMC and MTDC systems during DC faults. The DC fault current is forced to flow through the capacitors of the FBSM; thus, the DC current is blocked as in Figure 7. The FBSM–MMC circuits rapidly block the fault currents by generating reversed voltages when all switches are turned off. After clearing the DC current fault (i.e., $I_f \approx 0$), the faulted line is removed from the MTDC grid using disconnectors to isolate the DC fault completely. The MTDC system is then ready to be restored with the rest of the healthy DC transmission lines. The DC fault location method is required to determine the faulty line precisely. Several DC fault location methods are proposed based on DC current directions, voltage, and current transients, and traveling waves during DC faults in [17,23–28]. The DC fault is typically located in about 5 ms [29].

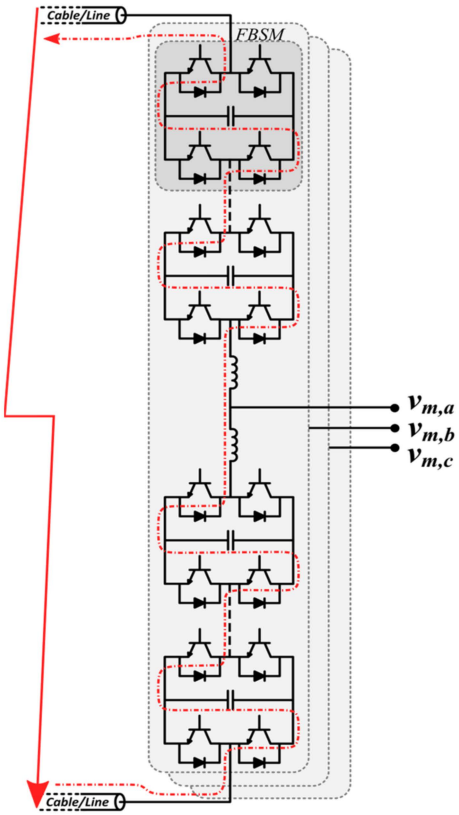

Figure 7. DC fault current flow in MMC-based FBSM circuits.

3.3. MTDC Grid Restoration Scheme

When a DC fault is cleared, the MTDC grid energy is completely absorbed. The stored energy in DC link capacitors and transmission lines is fully discharged. However, the MMC blocking action prevents MMC energy consumption. In other words, the SM capacitors of the MMC are charged with DC faults. The energy difference between the MMC and MTDC grid may cause a destructive inrush current when the MMC is deblocked. Figure 8 shows a simplified MTDC grid energy level after DC fault clearance. S_{MMC} represents the block/deblock status of the MMC. Thus, a discharging system is required to discharge the MMC energy. In addition, a pre-charge circuit is required to smoothly charge the MMC and MTDC systems during the restoration process. Note that the discharging system and the pre-charge circuit are only required with one MMC terminal to re-energize the MTDC

grid but not required with the other MMC terminals. In this paper, MMC-2 is assigned to re-energize the MTDC grid.

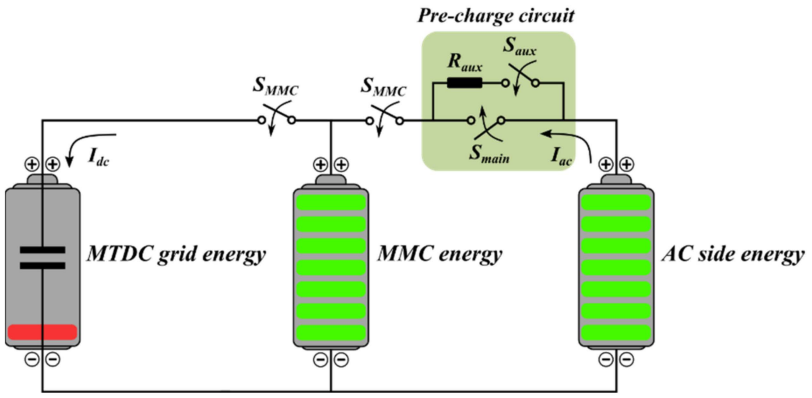

Figure 8. Simplified illustration of MTDC grid energy level after DC fault clearance.

3.3.1. Discharging System

To avoid the energy mismatch between the MMC and the MTDC grid, the SM capacitors of the MMC are discharged using a resistor connected in parallel with the SM capacitor, as shown in Figure 9a. After clearing the DC fault, the discharging switch $S_{discharge}$ is turned on to discharge the SM capacitor in the resistor. The discharging time constant τ is given as:

$$\tau = R_{discharge} \times C \quad (17)$$

where $R_{discharge}$ is the SM discharging resistance and C is the SM capacitance.

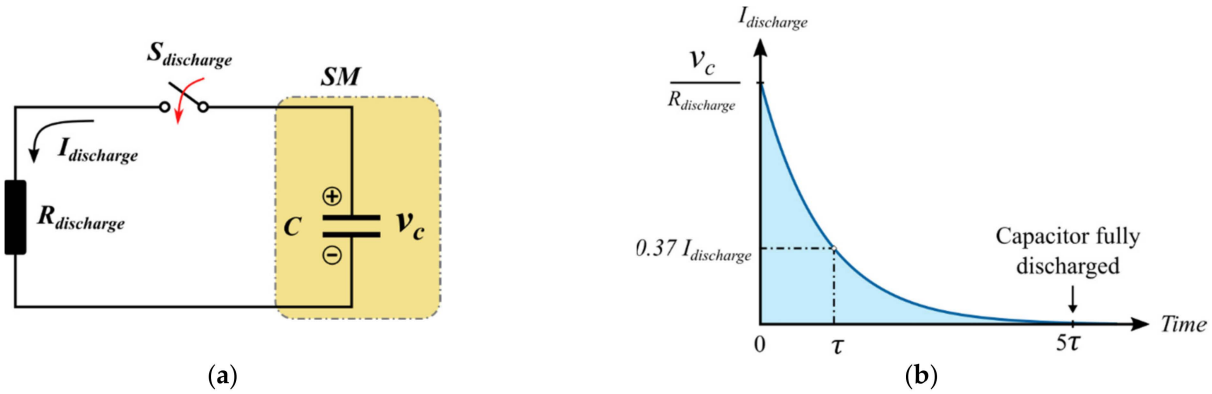

Figure 9. (**a**) Discharging system for single SM; (**b**) Capacitor discharging current.

The SM discharging resistance $R_{discharge}$ maintains the maximum discharge current $I_{discharge}$. A large SM discharging resistance may reduce the maximum discharge current, but it may take a very long time to discharge SM capacitors. Typically, the capacitor takes about 5τ to be fully discharged. Figure 9b shows the discharging current characteristics. The maximum discharge current is at the highest value at $t = 0$ when the capacitor voltage Vc is at the highest value. The discharging time of the SMs can take up to 100 ms. In such cases, the DC fault is cleared and the MMC is then prepared for a restoration.

3.3.2. Pre-Charge Circuit

Although the MMC and MTDC energy are discharged, the AC grid energy may cause an inrush current when deblocking the MMC because of the high capacitance at the MMC and MTDC systems. A pre-insertion resistor installed at the AC side of the MMC is required to charge the MMC and MTDC systems smoothly. The pre-charge circuit is shown in Figure 8. R_{aux} is a relatively high resistance connected in parallel with the AC line to

safely charge capacitors during the start-up process. The switches S_{main} are switched on during the normal and safe operation, while S_{aux} is only switched on during the start-up and restoration process.

After completely discharging the SM capacitor voltages, the auxiliary switch S_{aux} is connected to charge the MMC and MTDC systems. The MMC-2, which is assigned to re-energize the MTDC grid, is deblocked to begin the charging process. The MMC-2 system operates in the charging mode until the DC bus voltage reaches 90% of the rated DC voltages. The main switch S_{main} is then turned on for the normal operation, and all other blocked MMCs are deblocked.

4. RTDS Results

4.1. CHIL Implementation

The four-terminal MMC-based HVDC network, seen in Figure 1, is modeled in the Real-Time Digital Simulator (RTDS) systems, PB5 and NovaCor RTDS, and Xilinx Virtex 7 FPGA boards [30,31]. All MMC systems are emulated in the FPGAs with a time step of 2 microseconds (μs). Each MMC emulator requires two FPGA-based arm controllers for upper- and lower-valve arms. Therefore, four MMC emulators and eight Xilinx Virtex 7 type FPGA-based arm controllers are adopted to realize the switching model of the MTDC system. On the other hand, the AC grid sides, including the transformers and system-level controls, and the DC transmission lines are modeled in the RTDS systems with a time step of 50 μs. Due to the limitation of the computation resources of the RTDS, the MTDC network is modeled through inter-rack communication. To accommodate the MTDC network in the RTDS racks, the DC line between terminals 1 and 3 is divided into two racks. The two RTDS devices are optically connected using a fiber optic cable to synchronize the entire MTDC network. A photo of the CHIL set-up for the MMC–MTDC grid is shown in Figure 10.

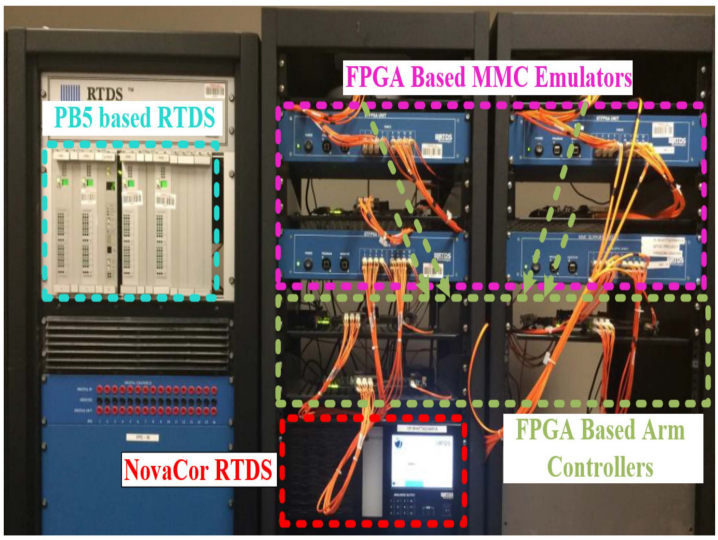

Figure 10. CHIL implementation set-up for MTDC grid.

4.2. Verification of the DC Fault Clearance and Grid Restoration Scheme

The dynamic performance of the MMC-based four-terminal DC grid is evaluated under pole-to-pole (P2P) DC fault conditions. In this case scenario, three different fault locations are considered (F1, F2, and F3), as illustrated in Figure 11. At the F1 location, the P2P DC fault occurs in the middle of the transmission lines connecting MMC-1 and MMC-3 terminals. At the F2 location, the DC fault occurs near the MMC-2 terminal on the DC transmission lines connecting MMC-2 and MMC-3. At the F3 location, the DC fault occurs at the MMC-1 terminal on the DC transmission lines connecting MMC-1 and MMC-2.

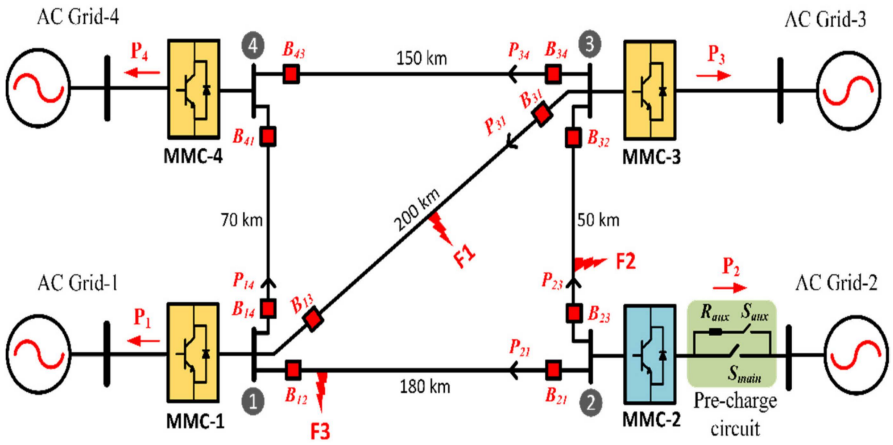

Figure 11. MMC-based MTDC system for the DC fault study.

4.2.1. DC Fault at the F1 Location

A P2P DC fault is initiated at F1 at t = 0.2 s. The terminals' DC voltage significantly reduces and the DC currents rise quickly. When the DC fault is detected, gate signals of MMC switches are turned off to protect the converter components against overcurrent. The blocking action of MMCs depends on the DC current magnitude and DC bus voltage. If the DC grid current exceeds the threshold value (e.g., 120% of the MMC DC current rating) or the DC voltage of the MMC terminal falls below the threshold value (e.g., 85% of DC bus voltage rating), the gate signals of the MMCs are turned off immediately. As shown in Figure 12, MMC-1 is blocked when the DC bus voltage of the MMC-1 terminal reaches the threshold value (i.e., 544 kV). When the DC current of MMC-2 I_{dc2} exceeds the limit, MMC-2 is blocked. MMC-3 is blocked when MMC-3 DC current I_{dc3} reaches the threshold value. MMC-4 is blocked when the DC bus voltage of the MMC-1 terminal reaches the threshold value.

The faulted line isolation time relies on the DC fault current decay performance. When the fault current decays to zero, the transmission line is removed from the MTDC grid by opening the disconnectors (B13 and B31). The fault current dynamic performance is shown in Figure 13, where the fault currents flow from the positive and negative poles in both directions. It takes about 128.9 ms to isolate the faulted lines from the MTDC grid, which is the total DC current to decay to zero after gate blocking. After isolating the faulted lines, the SM capacitor voltages of MMC-2 are discharged. The discharging time of the SMs is 100 ms, estimated by designing the time constant of the discharging circuit when assuming a maximum discharging current of 1.2 kA.

After completely discharging the SMs, MMC-2 is deblocked to charge the MTDC grid through the pre-charge circuit. Charging the MMC SM capacitors and the MTDC system takes about 712.6 ms to reach 90% of the rated DC voltage. The MTDC charging time depends on the pre-insertion resistance R_{aux} and the equivalent capacitance of the MMC and MTDC grid. When the DC bus voltage reaches 90% of the rated DC voltage (i.e., 576 kV), all other MMCs are deblocked to operate in safe and normal operating conditions. Figure 14 shows the fault clearance and restoration performance for the DC currents, DC voltages, and MMC-2 SM capacitor voltages. Figure 15 shows the DC fault clearance and restoration time for all the MMC terminals. It can be seen that the critical condition is concise, but the restoration process takes more time to safely operate the MTDC system again. The faulty line is removed from the MTDC network within 128.9 ms after the fault current becomes zero. The fault current takes 128.9 ms because the storage elements energized the MTDC network. Thus, the faulty line isolation time depends on the MTDC transmission line parameters.

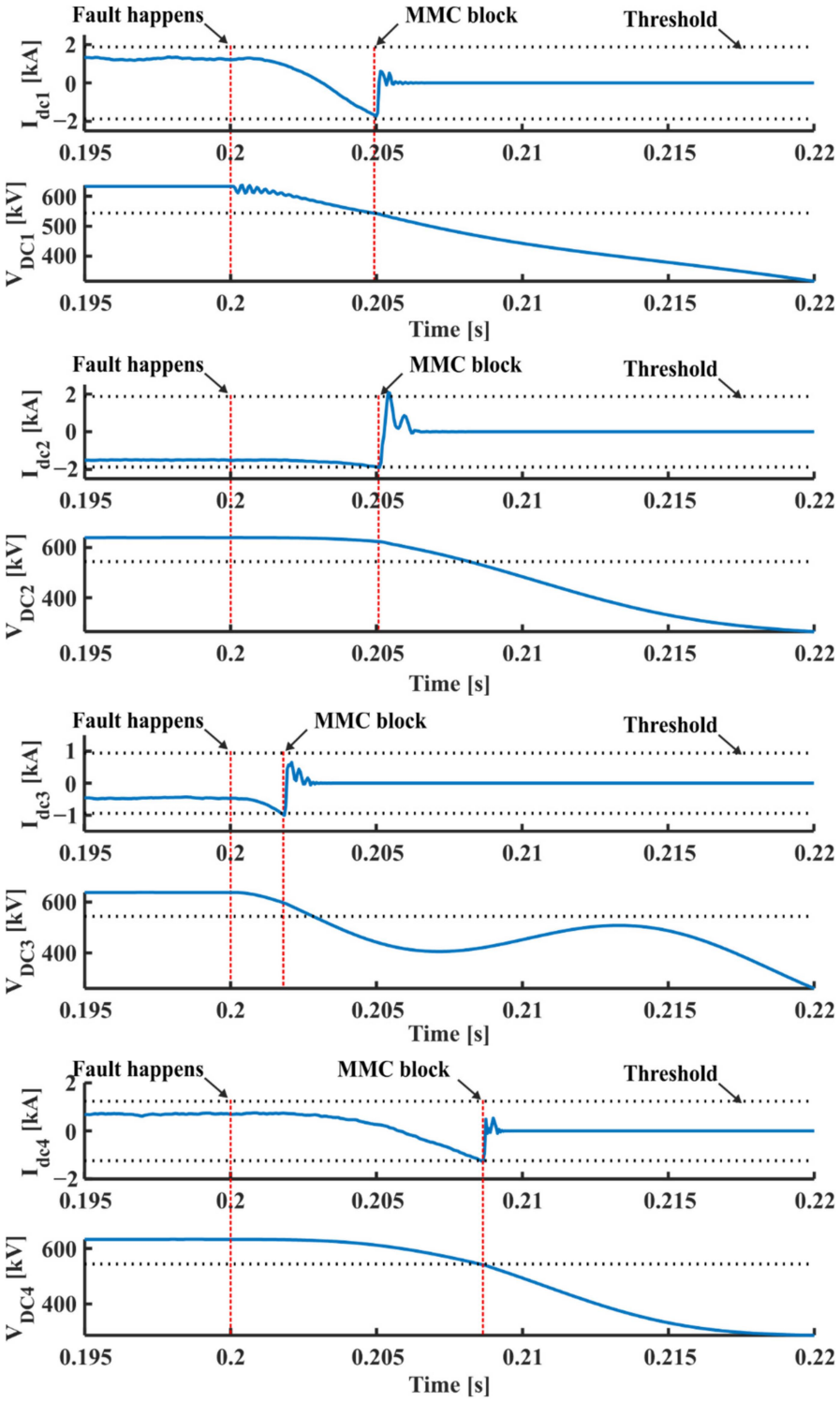

Figure 12. DC currents and voltages of MMCs with P2P DC fault at location F1.

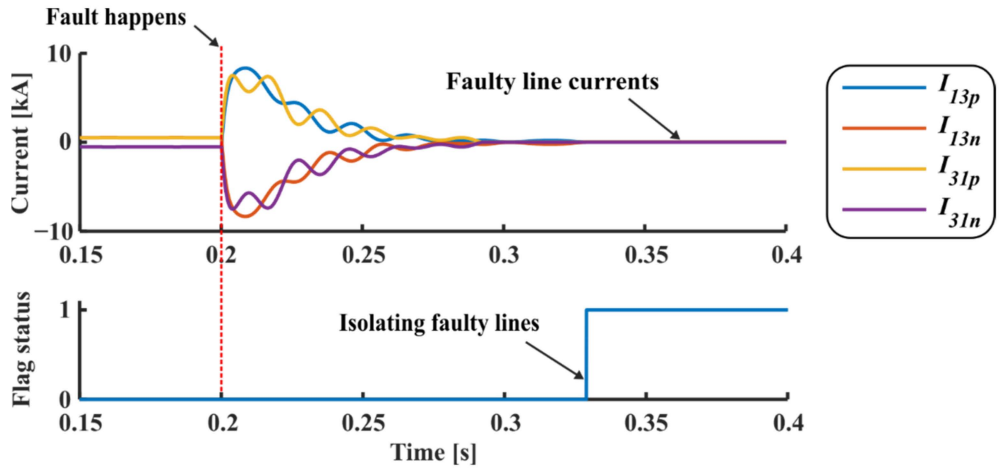

Figure 13. Fault currents and isolation status with DC fault at location F1.

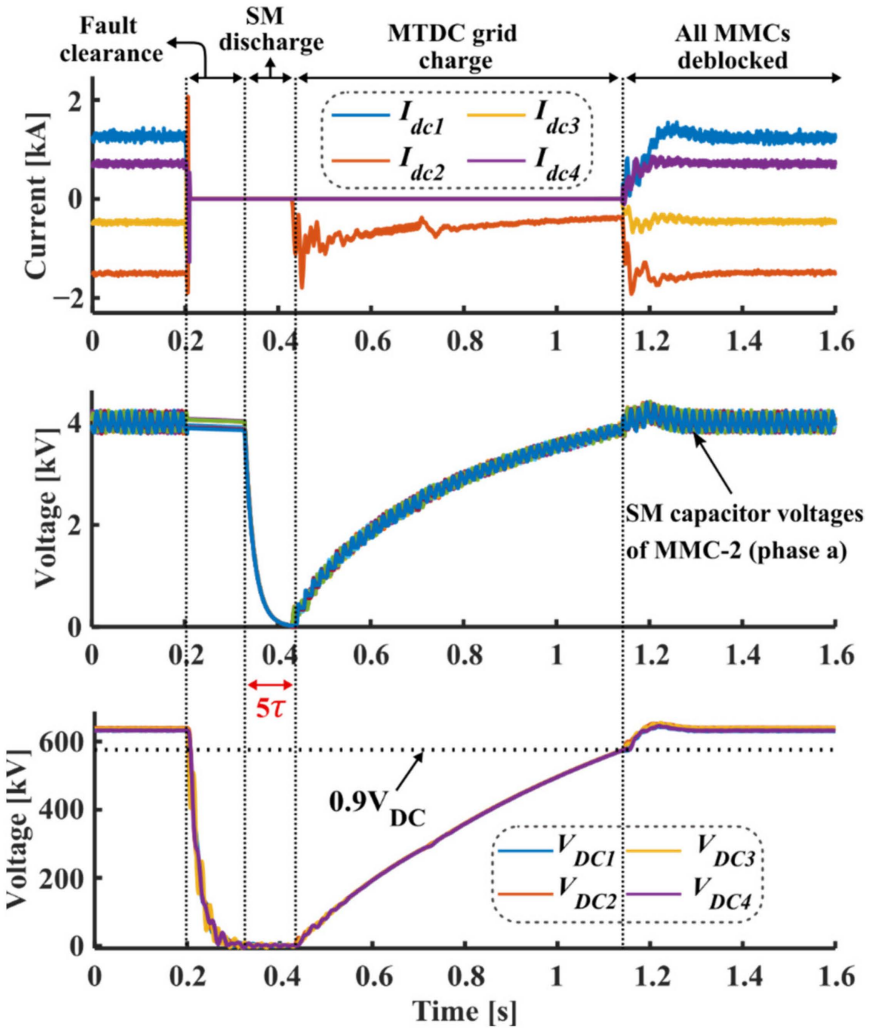

Figure 14. DC currents, voltages, and MMC-2 SM voltages with fault at location F1.

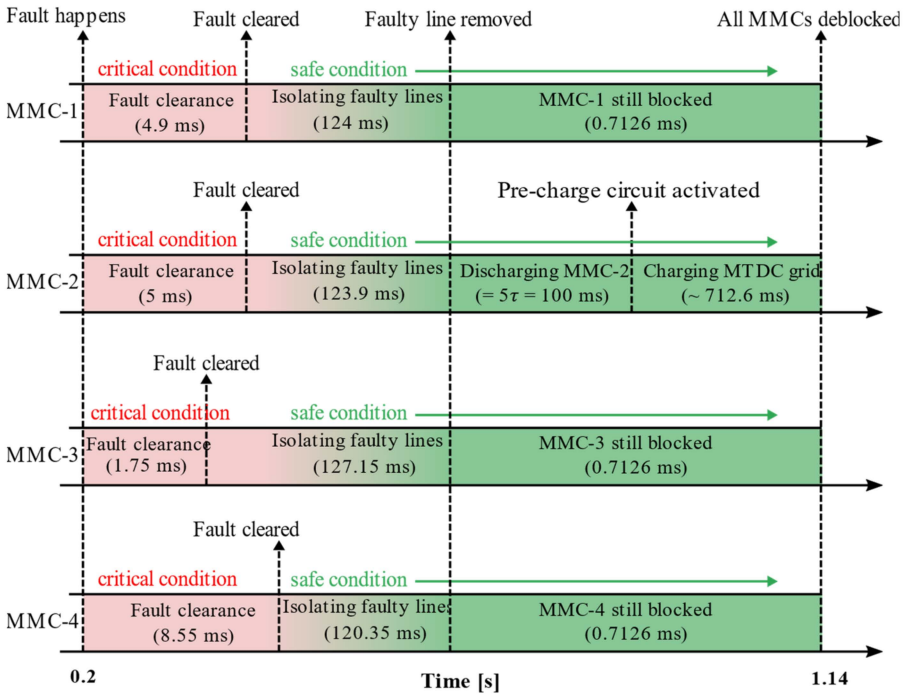

Figure 15. Fault clearance and restoration time of MMCs under DC fault at location F1.

4.2.2. DC Fault at the F2 Location

In this case, a P2P DC fault occurs near the MMC-2 terminal on the DC transmission lines connecting MMC-2 and MMC-3 (TL_{23}). The DC fault is triggered at t = 0.2 s. The clearance and restoration strategies used in the previous case are adopted. When the faulted line currents decay to zero, the transmission line is removed from the MTDC grid by opening the disconnectors (B_{23} and B_{32}).

In this case, the transmission line TL_{12} will carry the entire power amount produced by the MMC-2 terminal because TL_{12} is the only way to transfer power to the other terminals. The DC power of the MTDC transmission lines is shown in Figure 16. The DC grid current dynamic performances of the MMC terminals are shown in Figure 17. The power flow of MTDC terminals is controlled within reasonable boundaries, as shown in Figure 18. The DC fault keeps the DC grid currents within the threshold current limits. After the DC fault, the entire MTDC grid is safely restored to its normal operation.

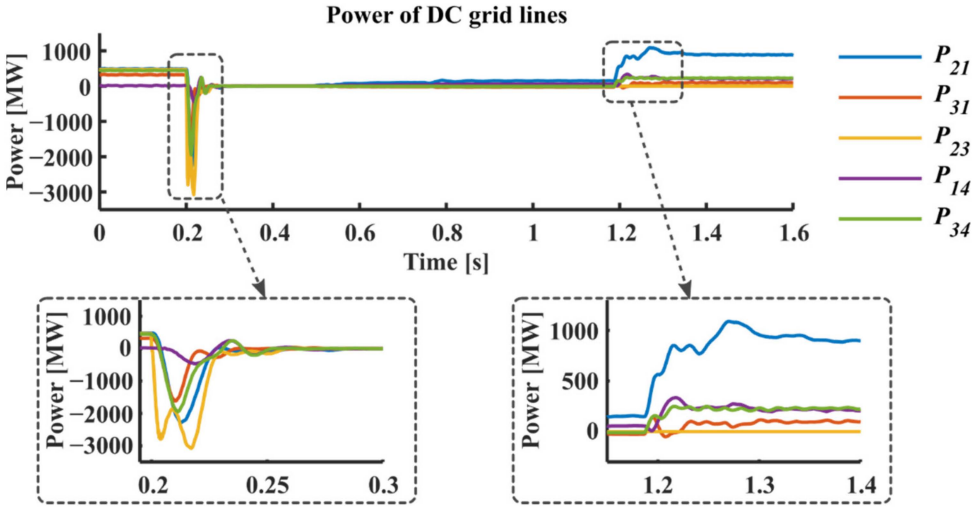

Figure 16. Power flow in the DC transmission lines with fault at location F2.

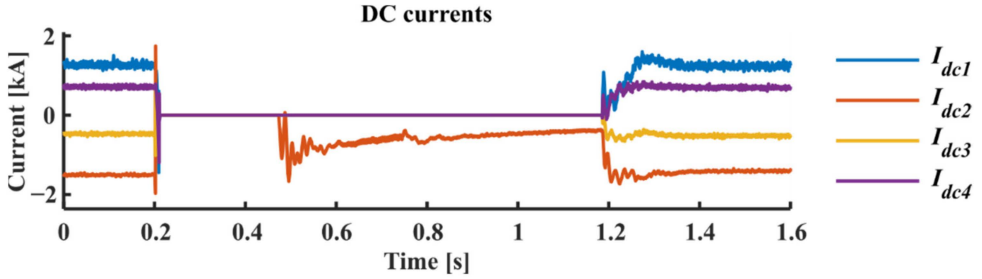

Figure 17. DC currents of the MTDC terminals with DC fault at location F2.

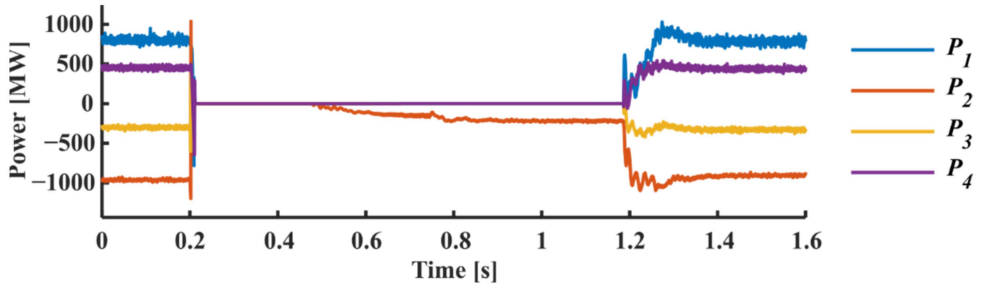

Figure 18. Net injected power P_i into the MMC terminals with DC fault at location F2.

4.2.3. DC Fault at the F3 Location

In this case, a P2P DC fault occurs near the MMC-1 terminal on the DC transmission lines connecting MMC-1 and MMC-2 (TL_{12}). The DC fault occurs at t = 0.2 s. The clearance and restoration strategies used in the previous cases are adopted. The DC grid current dynamic performances of the MMC terminals with P2P DC fault are shown in Figure 19. The DC power of the MTDC transmission lines is shown in Figure 20. The time required to detect DC faults is different for each MMC terminal based on the fault location. The removal time of faulty DC lines depends on the fault current decay, which eventually depends on the transmission line parameters. The MMC and MTDC grid charging time depends on the pre-charge circuit resistance and the MMC and MTDC grid capacitance. The times required to detect DC faults, isolate faulty lines, and charge the MMC and MTDC grid with the three DC fault cases (F1, F2, and F3) are tabulated in Table 3.

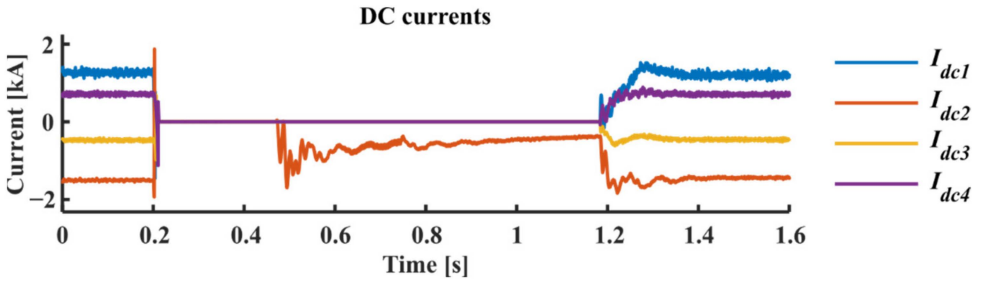

Figure 19. DC currents of the MTDC terminals with DC fault at location F3.

Table 3. Fault clearance and restoration time at different fault locations.

		DC Fault Location		
		F1	**F2**	**F3**
Fault clearance (ms)	MMC-1	4.9	9.2	3.9
	MMC-2	5	1.8	1.9
	MMC-3	1.75	1.9	5.9
	MMC-4	8.55	10.1	10.5
Faulty line isolation (ms)		128.9	172.7	171.4
MTDC grid charging (ms)		712.6	713	712.2

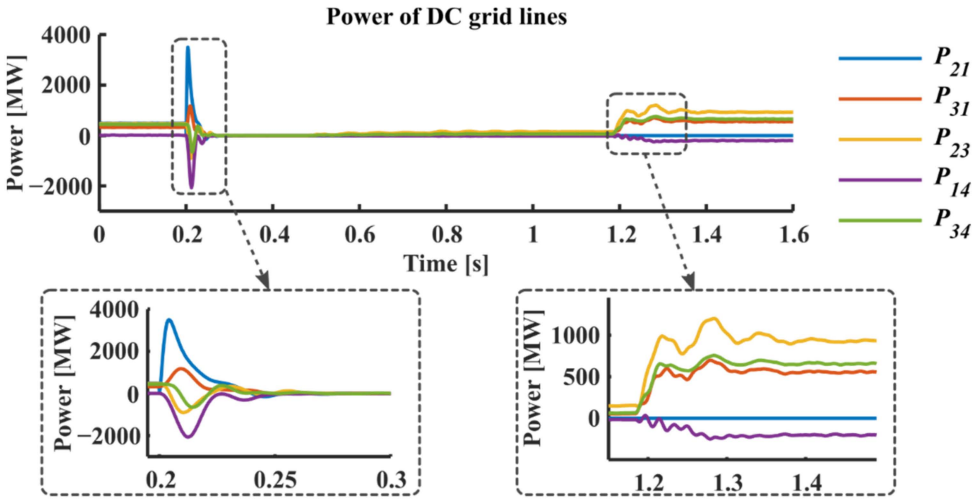

Figure 20. Power flow in the DC transmission lines with fault at location F3.

4.3. Power Flow Assessment of the MTDC Grid under Different Disconnected DC Lines

In meshed MTDC configurations, the MTDC system can transmit power under permanent DC faults when the faulted lines are removed from the DC grid. However, the remaining transmission line power may compensate for the disconnected line power. When a DC fault occurs at F1, the transmission line connecting terminals 1 and 3 is disconnected. Compared to the power flow in the regular operation, the DC power flow of P_{21}, P_{41}, and P_{34} with TL_{31} removed is increased by 145.4 MW, 157.1 MW, and 158 MW, respectively. Similarly, when the DC fault occurs at location F2, transmission line TL_{23} is removed. As a result, the DC power flow P_{21} is significantly increased because the total power generated from terminal 2 is transmitted through TL_{12}. Table 4 shows the steady-state DC transmission line power with different removed DC transmission lines.

Table 4. DC transmission power flow with different removed lines.

Removed Line	DC Transmission Power (MW)				
	P_{21}	P_{31}	P_{14}	P_{23}	P_{34}
TL_{12}	0.0	553.4	−201.8	926.0	653.0
TL_{13}	634.1	0.0	−143.7	308.8	599.6
TL_{14}	483.1	317.2	0.0	474.4	454.1
TL_{23}	888.1	99.2	208.3	0.0	230.2
TL_{34}	671.7	539.8	431.4	261.7	0.0
Normal operation	488.7	323.7	13.4	468.6	441.6

5. Conclusions

This paper studies a four-terminal high-voltage (640 kV) MTDC transmission grid for DC fault isolation and grid restoration. MMC-based terminals are modeled using a full bridge SM (FBSM) circuit based on detailed modeling on Xilinx Virtex 7 FPGAs. Each MMC is modeled non-uniformly based on a different number of SMs to test the proposed isolation and restoration method. One MMC terminal and its controller require three Virtex-7 FPGAs for modeling, so twelve Virtex-7 FPGAs are utilized and connected with the RTDS. It is well known that the FBSM circuit-based MMC can block DC short-circuit fault currents. DC fault current is forced to flow through the capacitors of the FBSM; thus, the DC current is blocked. This paper adopts the FBSM to benefit its fault-blocking feature. In addition, the proposed DC fault clearance and restoration method are presented to protect the MTDC grid and safely re-energize after clearing the fault. The operation and control of the MMC-based four-terminal HVDC system are investigated with the droop control scheme under pole-to-pole DC faults. The power flow calculation based on the

Newton–Raphson method is used to determine the safe threshold value of the DC power and DC voltage terminals to ensure accurate power sharing and DC voltage control with the droop control method. Further, a power flow assessment for the MTDC transmission system after removing a faulty transmission line is also presented. The RTDS results showed that the MTDC system satisfactorily rides through DC faults and can safely recover after a DC fault.

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Abbreviations

The following abbreviations are used in this manuscript

MTDC	Multiterminal High Voltage DC
P2P	Pole-to-Pole
CHIL	Control-Hardware-in-Loop
RTDS	Real-Time Digital Simulator
CO_2	Carbon Dioxide
HVDC	High Voltage Direct Current
HVAC	High Voltage Alternating Current
ROW	Right-of-Ways
VSC	Voltage Source-based Converter
MMC	Modular Multilevel Converter
ACCB	AC Circuit Breaker
SCR	Short-Circuit Ratio
FBSM	Full Bridge Submodule
CCSC	Circulating Current Suppression Control
NLM	Nearest Level Modulation

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