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A Wideband 6-Bit Digital Attenuator in a GaAs pHEMT MMIC

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Abstract: A low insertion loss, wideband 6-bit digital step attenuator is implemented in the 0.25-µm GaAs pHEMT process. Modified π- or T-type attenuator structures are adopted to expand the operation frequency bandwidth and reduce the insertion phase violation. Furthermore, the through-wafer via (TWV) is analyzed to reduce the influence of the parasitic effect on the high-frequency performance of the attenuator. The depletion mode single-gate switch transistors are used to control the on-off state of the attenuator, which provides low insertion loss and high isolation. The step of the attenuator is 0.5 dB, and the attenuation range is 31.5 dB. The measurement results show a maximum root mean square (RMS) attenuation error of 0.51 dB and RMS phase error of 6.6 degrees from DC-18 GHz. The chip area is 1.8 × 0.6 mm^2.

Keywords: digital step attenuator; phase variation compensation; pHEMT; wideband; through-wafer via

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1. Introduction

The attenuator is one of the key devices in phased array systems, which is mainly used for amplitude adjustment and damage protection [1]. The digital step attenuator (DSA) using π- or T-type units has the advantages of a wideband, high precision, high linearity, being bidirectional, and a small amplitude error [2,3]. In recent years, several technologies have been used in wideband DSA aimed at reducing the phase error and increasing the working bandwidth [4–9]. The internal switched π- or T-type attenuator with passive compensation components is popular for compact chip sizes. The passive components are added into the π- or T-type structure to form low-pass characteristics in both the reference and attenuation states. Therefore, the phase–frequency curves of the two states decrease similarly with the increase in the frequency, and the phase difference is reduced.

However, the performance of the low-pass network adopted in the π- or T-type attenuators is always influenced by the parasitic component of the passive devices. The low Q factor inductance would induce additional insertion loss, and it would also be limited by the operating frequency. A good solution to avoid using inductance is to assign the capacitors in parallel with the shunt resistors of the π- or T-type attenuator [7]. The bypass compensation capacitors play the role of low-pass components, and they also expand the operation frequency. Unfortunately, when using relatively large transistors as series switches, the bypass compensation capacitors would cause attenuation degradation at high frequencies when needing a large value to reduce the phase error. In addition, a larger capacitance in the shunt branches will also increase the insertion loss at high frequencies.

Compared with the CMOS process, attenuators based on the gallium arsenide (GaAs) process have low insertion loss at high frequencies [10]. However, the performance at high frequencies will also be affected by the parasitic components. It is still difficult to reduce the attenuation and phase errors at the same time, even if compensation capacitances are

adopted. The size of pHEMT is not as flexible as MOSFET, which leads to many difficulties in balancing the attenuation and phase error.

In this paper, a wideband digital step attenuator is implemented in 0.25-μm GaAs pHEMT technology. A modified π-type attenuator structure with additional compensation capacitance is adopted. The middle capacitance between the shunt branch of the π-type attenuator adds a new degree of freedom in optimizing the phase and attenuation error. The parasitic effect of through-wafer via (TWV) is also analyzed and optimized to improve the performance. The implementation of the circuit is introduced in Section 2. The fabrication and measurement results are shown in Section 3. Finally, Section 4 concludes the performance of the attenuator.

2. Implementation of the Attenuator Circuit

Figure 1 is the diagram of the proposed attenuator circuit, which combines six π- or T-type attenuation units in cascade. To minimize the chip size and keep good matching and attenuation performance, different types of attenuation units are used to implement various values, and inter-stage inductances are added to the large value attenuator cells. The small attenuation elements adopt a reduced T-type structure, while the medium elements adopt a bridged T-type structure and the larger cells, such as those of 8 dB and 16 dB, adopt a π-type structure.

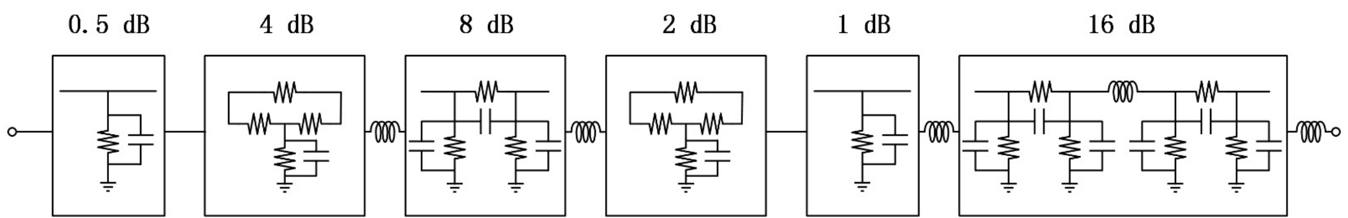


Figure 1. The diagram of the proposed attenuator circuit with the switches neglected.

T-type, bridged T-type, and π-type attenuators can achieve better matching and attenuation performance. To avoid the use of an extreme resistance value, the bridged T-type attenuator is used to achieve 2-dB and 4-dB attenuation units, while the π-type one is used for 8 dB and 16 dB, of which 16 dB is achieved by 2 8-dB units in cascade.

In addition, to reduce the insertion phase shift between the reference and the attenuation states, bypass capacitors are paralleled with the resistors in the shunt branches of the bridged T-type, π-type, and reduced T-type structures, which are shown in Figure 2a–c. The bypass capacitors will change the attenuator into low-pass characteristics in both the reference and attenuation states, which leads to similar phase curves. The phase error is reduced, and the operating bandwidth is also expanded [7].

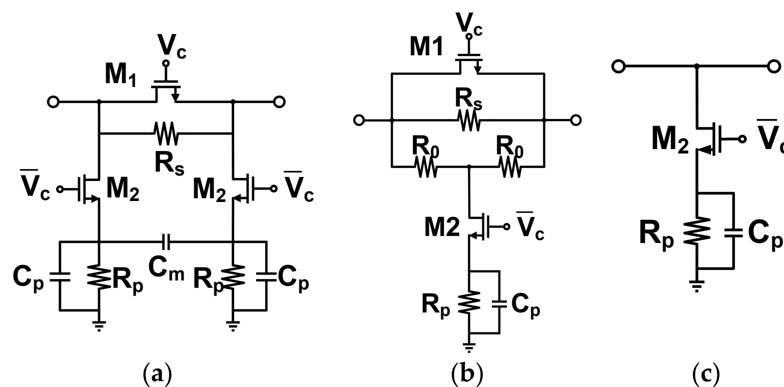


Figure 2. (**a**) The modified π-type for the large value attenuator. (**b**) The modified bridged T-type for the middle value attenuator. (**c**) The modified reduced T-type attenuator for the small value attenuator.

For large value attenuation units with a π-type structure, the phase difference is relatively high, which requires a larger value capacitor for compensation. However, the introduced bypass capacitor will increase the transmission loss at high frequencies, and the attenuation curve thus deteriorates. To alleviate this problem and further increase the working bandwidth of the attenuator, a compensation capacitor C_m in the middle of the parallel branch is introduced. The capacitor C_m can adjust the transmission curve of the attenuation state, and it hardly affects the reference state. By using the capacitor flexibly, both the attenuation and phase error of the attenuator can be minimized. Aside from the bypass capacitor, this can lead to gaining an extra degree of freedom in designing the attenuator [9]. The capacitor C_m actually adjusts the locations of the zeros and poles in the attenuation state. A larger C_m will decrease the phase difference and the attenuation in the middle frequency of the attenuator. Compared with simply increasing C_p, the phase difference is reduced at the cost of continuously increasing the high-frequency attenuation. The additional C_m capacitance allows for more freedom in the attenuator's design.

All the circuits are grounded to the bottom metal plane of the chip by a through wafer via (TWV). The TWV also has a great influence on the high-frequency response of the attenuator. It can be modeled as shown by the equivalent circuit in Figure 3. The inductor L_p and resistor R_p are used to model the reactive and inactive behavior of the main body of the TWV. The resistor R_{sub} and capacitor C_{sub} are implemented to account for the parasitic effect of the substrate. Small inductors L_s act as the inductive part of the top metal pad. The TWV is simulated by electromagnetic (EM) simulation tool, and the S-parameter file is extracted. All the parameters are optimized to make the model closed to the simulation results.

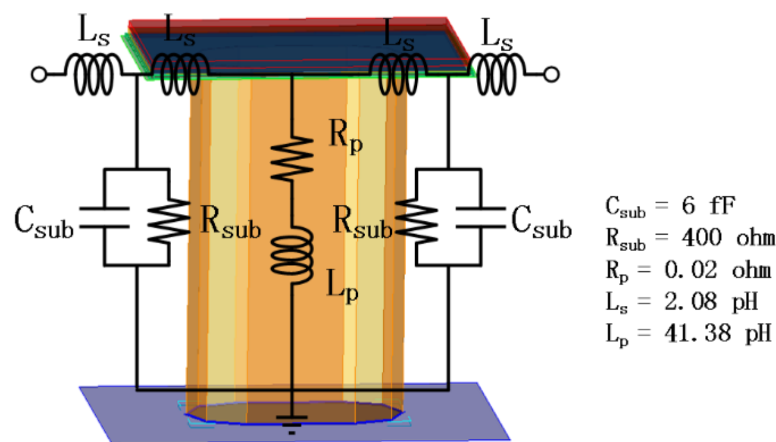


Figure 3. The equivalent circuit of the TWV.

The shunt branches of the attenuators are grounded by TWVs, so the attenuators are not grounded ideally. Additional parasitic components would worsen the performance at high frequencies, especially in large attenuation units. To reduce the influence of the TWV on the attenuator, multiple TWVs are connected in parallel by the underlying metal layer. The number of the paralleled TWVs is optimized to satisfy the performance and chip size. It can be seen in Figure 4 that the attenuation curve of the 8-dB attenuator with two TWVs in parallel decreases first and then increases, being much flatter than that with just one TWV. At the same time, the phase difference is adjusted to a small value at high frequencies. Similarly, the 16-dB attenuator cells consist of two 8-dB cells, and all four TWVs are connected in parallel.

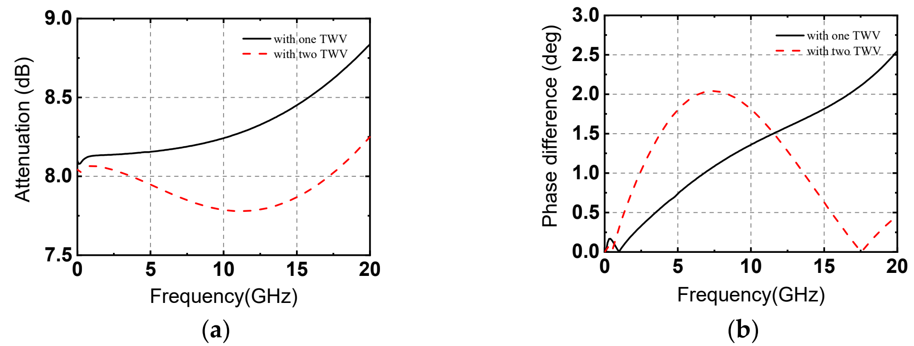


Figure 4. (**a**) The attenuation and (**b**) phase difference of the 8-dB cells with one and two TWVs.

3. Fabrication and Measurement Results

The proposed attenuator circuit was fabricated by a GaAs 0.25-µm pHEMT process. The chip photo is shown in Figure 5, and the size was 1.8 × 0.6 mm^2 including the pads. The 6-bit attenuator was controlled by voltages of 0 or −5 V. The switch pHEMTs had gates with a 0.5-µm gate length in this work, and the widths were in different series and parallel branches. Except for the reduced T-structure attenuator, the control voltages of the series and parallel transistors were logically opposite, with 0 V for on and −5 V for off. The input and output ports were ground-signal-ground (GSG) pads, and both ground pads were grounded by TWVs. The chip was fixed to the ground plane of the PCB using conductive silver glue, and all the control pads were bonded to the PCB by gold wire. The DC to DC chip provides −5V negative voltage, and multiple switches control the corresponding logical voltage in the control PCB. The diagram of the measurement setup is shown in Figure 6, including network analyzer, DC power, RF probe station, measurement PCB, device under test (DUT) and control PCB.

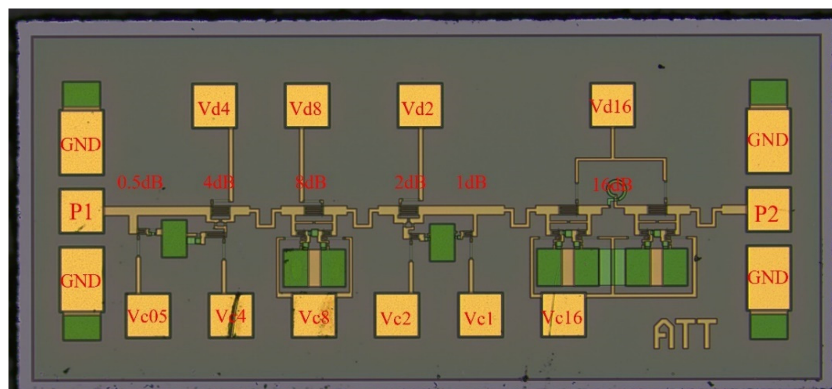


Figure 5. Photo of the proposed attenuator.

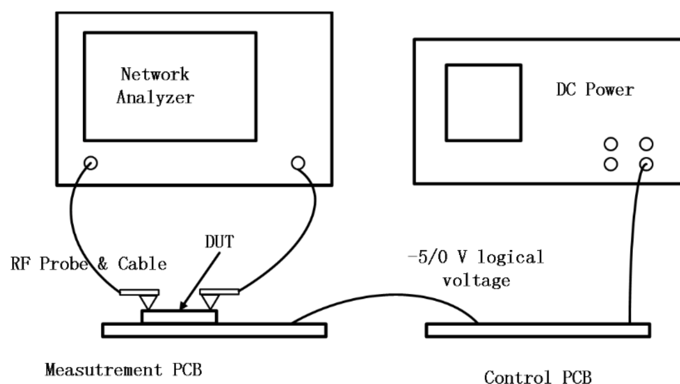


Figure 6. The diagram of the measurement setup.

The chip was measured on-chip with a microwave probe station and Keysight N5247B network analyzer. The measured transmission curves of all attenuation states are shown in Figure 7, and the insertion loss of the reference state was 2.6~3.6 dB. The attenuation and relative phase differences of the main states are shown in Figure 8. The reflection coefficients of both the input and output ports were less than −11 dB, as shown in Figure 9. The root mean square (RMS) errors of the attenuation and insertion phase shift are shown in Figure 10, where the RMS error of attenuation was less than 0.51 dB and the RMS error of the insertion phase shift was less than 6.6 degrees. A comparison between the attenuators of different technologies and topologies is shown in Table 1. The work had good insertion loss performance compared with the CMOS process and relatively low phase and attenuation errors in such a frequency bandwidth.

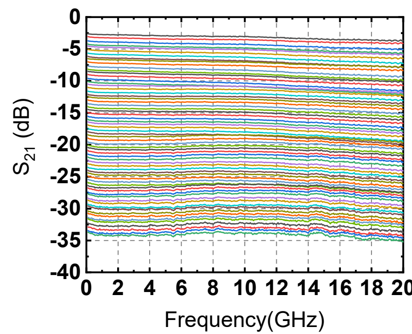
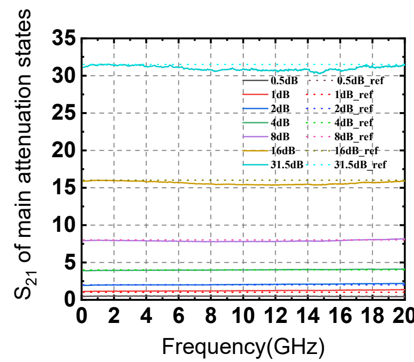
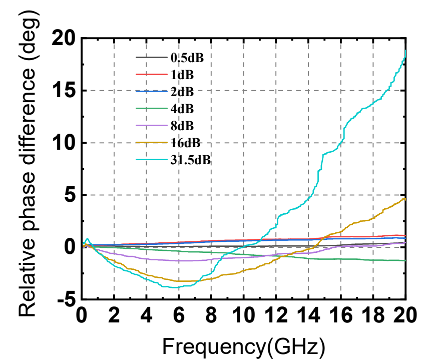


Figure 7. Measurement results of the S21 in all states.

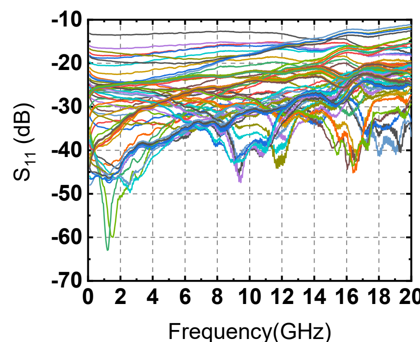


(**a**)

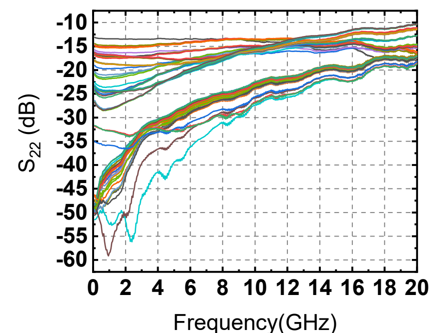


(**b**)

Figure 8. (**a**) Measurement results of the S21 in the main states. (**b**) The relative phase difference curve of the main states.



(**a**)



(**b**)

Figure 9. (**a**) Measurement results of the S11 and (**b**) S22.

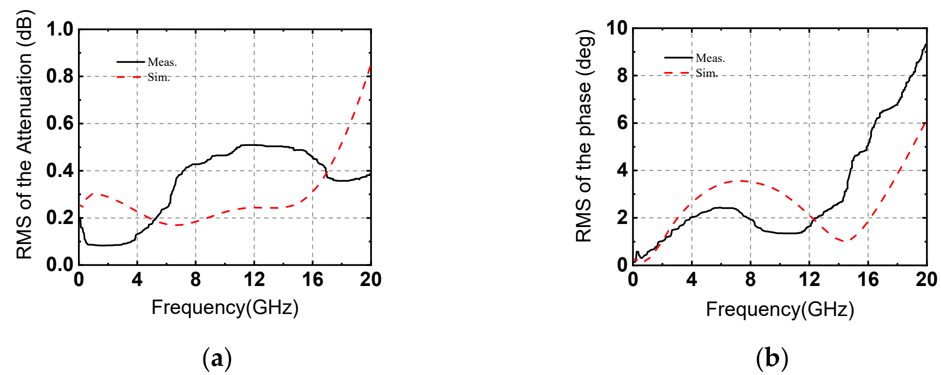


Figure 10. (**a**) Measurement and simulation results of the attenuation RMS error. (**b**) RMS error of the insertion phase shift.

Table 1. Performance comparison of the attenuator circuits.

Ref	[7]	[6]	[10]	This Work
Technology	0.13 µm SiGe BiCMOS	0.18 µm CMOS	0.5 µm GaAs	0.25 µm GaAs
Frequency (GHz)	DC-20	19–21	2–18	DC-18
Topology	Switched T-type with capacitive compensation	Switched π- or T-type with tail cap. compensation	Switched π- or T-type and path selection	Switched π- or T-type with capacitive compensation
Attenuation Range (dB)	31.5 (6 bits)	31.5 (6 bits)	31.5 (6 bits)	31.5 (6 bits)
Insertion Loss (dB)	1.7–7.2	7.2–8	<5.71	2.6–3.6
Return Loss (dB)	>12	>12	>10	>11
Amplitude Error (dB)	<0.37	<0.6	<2.3 [1]	<0.51
RMS Phase Variation (deg.)	<4	<3.8	<3.51 [1]	<6.6
Chip Size (mm^2)	0.14	0.45	3.5 [2]	1.08 [2]

[1] Main state accuracy. [2] Including pads.

4. Conclusions

This paper proposed a wideband, low phase variation 6-bit step attenuator. Modified reduced T-type, bridged T-type, and π-type attenuators were used to implement attenuators of the corresponding values. The pHEMTs act as switches and offer low insertion loss and good isolation. By adding different compensation capacitances properly, the phase difference between states was lower, and the bandwidth was expanded. The parasitic effect of the TWV was alleviated by having several in parallel. The attenuator had a low insertion loss of 2.6~3.7 dB, and the attenuation range was 31.5 dB with a step of 0.5 dB. The attenuation RMS error was less than 0.51 dB, and the phase RMS error was less than 6.6 degrees. Considering the inaccuracy of the process model, there was a certain deviation between the simulation results and the test results, but this paper still provides some attempts to improve the working bandwidth and phase error of the attenuator.

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