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Voltage Ripple Suppression Methods for the Capacitor in Modular Multilevel Converter Submodules Employing a Reversed Pulse Width Modulation-Switching Channel

Wenguang Yang, Fei Yao * and Yongyang Zhou

College of Information Science and Technology, Donghua University, Shanghai 201620, China; wg_yang@mail.dhu.edu.cn (W.Y.); 2211994@mail.dhu.edu.cn (Y.Z.)
* Correspondence: fyao@dhu.edu.cn

Abstract: Modular multilevel converters (MMCs) will be widely applied in onboard integrated power systems due to their high levels of electric power output and good-quality sine waveform outputs. However, the capacitor voltage of MMCs fluctuates greatly because the charge–discharge process of the capacitor is continuous when the system is working. In order to reduce voltage ripples efficiently, a capacitor voltage ripple-suppression strategy employing a reversed PWM switching channel is proposed in this paper. For one pair of the upper and lower arm submodules, a switching channel is built. Then, the highest ripple voltage possible can be offset since the voltage fluctuation direction of the upper and the lower arm capacitors would be reversed. In addition, a clamping capacitor is added to the switching channel to further suppress the fluctuation voltage by 78%. Compared to traditional large capacitance suppression methods, only 12% capacitance is used in the proposed method. The reliability and power density of the proposed MMC both increased, and there are no additional losses compared with previous voltage ripple suppression methods. The effectiveness of the proposed voltage ripple suppression strategy is verified by simulation results.

Keywords: modular multilevel converter; capacitor voltage; voltage ripple suppression; switching channel; onboard integrated power system

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1. Introduction

All-electric ships represent an important developmental direction for ships. Thus, onboard integrated power systems have recently become a research focus [1,2]. Faced with the characteristics of high power and medium-high voltage, multilevel converters have been widely applied in onboard integrated power systems because they do not require large filters and can provide good-quality sine waveform outputs [3–5]. Compared to other converters, MMCs have the advantages of having a high degree of modularity, low redundancy costs, and high efficiency; thus, it has great developmental prospects [6–8]. However, the capacitor voltages of MMCs fluctuate greatly since the capacitors are always charged or discharged during operation, and the voltage ripple amplitude is inversely proportional to the operating frequency of the MMC [9]. Excessive voltage fluctuations lead to power imbalances within the MMC and may even deteriorate the output waveform of the MMC. In addition, the capacitor voltages in the submodules of each arm are unequal due to the existence of the capacitor parameter difference as well as the difference of the capacitor charge rate. This is called capacitor voltage imbalance, which affects the safety and the stability of the MMC system. These defects limit the use of MMCs in onboard integrated power systems. The voltage fluctuation problem not only exists in submodule capacitors but also exists in the DC output side when the MMC is used as a rectifier, especially when operating in the renewable energy system. Normally, the DC output voltage fluctuates with the change in the input power relative to the MMC rectifier. Currently, the sliding mode control has been used for stabilizing the output DC voltage in the series microgrid system under island mode [10]. Since the outputted DC voltage fluctuation is not the main problem in the onboard MMC integrated power system, it is not discussed in this paper.

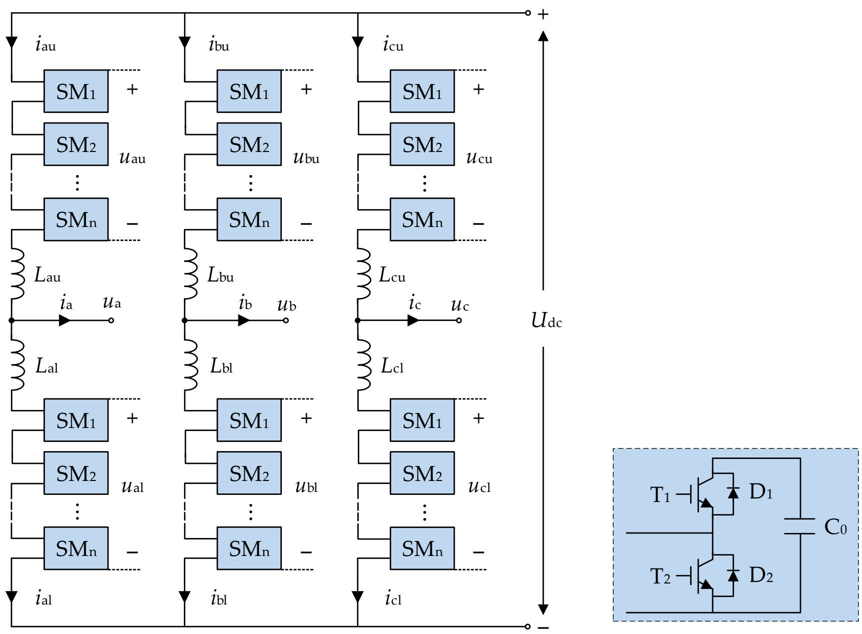
The traditional method for resolving the capacitor voltage imbalance problem is the voltage-sorting method. Recently, many novel voltage-balancing methods are proposed by scholars to improve the traditional voltage-balancing method. For reducing the switching frequency of the converter, a modified capacitor voltage-balancing method based on the control algorithm of the expert system is proposed in [11]. It modifies the traditional voltage-balancing method by retaining the previous state of the submodule. Normally, large capacitors are used to suppress the voltage ripple in an MMC. In [12], a super-capacitor-based MMC topology was proposed, and the super capacitor was added in each submodule. However, a large number of submodules are usually cascaded to achieve a high voltage level in the MMC, resulting in MMCs with expensive large capacitors. Currently, many scholars have carried out research on how to suppress voltage fluctuations in MMC capacitors. The main methods include high-frequency harmonic injection and power channel transfer.

The main idea of the high-frequency harmonic injection method is to introduce the high-frequency component into the arm voltage and arm current at the same time to suppress the low frequency fluctuations in the submodule capacitor. The method was first proposed for application in MMCs by ABB [13]. Later, many scholars put forward improvements to the method, such as changing the injected high-frequency sine wave into a sine wave in addition to a third harmonic, quasi-square wave or square wave to reduce the current stress of the device [14–19] or by introducing a d-q synchronous rotation coordinate system to complete the injection method [20]. In [19], the third-order harmonic voltage and second-order harmonic current are injected in the MMC to reduce capacitor voltage ripples. In this method, the injection of the common-mode voltage is not required in the circuit of the AC side. Thus, the amplitude of the injected second-order harmonic current could be reduced, which could decrease the current stress of the injected harmonic current. However, the current stress caused by these high-frequency harmonic injection methods is still large and will increase additional losses, especially at high frequency levels [21]. The model predictive control method has been proposed by scholars for reducing the amount of calculations [22]. However, this method will also increase additional losses when the fluctuations of the capacitor voltages become large. The main reason is that, in this situation, it exhibits a similar operating pattern with the high-frequency harmonic injection method for reducing capacitor voltage ripples. Therefore, we propose a capacitor voltage-suppression method that is realized by a power channel. Here, the power channel is built between the submodules to form a path to exchange electric power [23–26]. Since the voltage fluctuation directions of the capacitors in the upper and lower arms are reversed, the power channel can be used to offset the ripple voltage. This approach experiences no current stress or additional losses but increases the number of devices. Depending on the control method, a power channel can be added between the upper and lower arms in each phase [23,24] or between the three phases [25,26]. However, these capacitor voltage ripple suppression methods have to use a DC–DC converter and a high-frequency transformer to construct the power channel to connect the submodules, which is not only complicated to control but is also more expensive. In [27], another arm, which is the same as the original arm, is added between upper and lower arms as a physical power transfer channel in each phase. Then, a cross-connected topology is constituted. This method does not require additional DC–DC converters and transformers, but the control algorithm of the power devices on the added arms is complex. In [28], the added arm in the topology of [27] was replaced by a capacitor. The circuit is simpler and costs decreased. However, it requires high frequency common-mode voltage injection and circulating current injections when in operation, which could produce additional losses.

In this paper, a novel capacitor voltage ripple suppression method employing the reversed-PWM switching channel is proposed. The capacitor voltage fluctuations of the submodules in the upper and the lower arms are analyzed. Then, a switching channel is constructed between the upper and lower submodules to form a path through which the charge in the capacitors with the potential difference can flow freely. Additionally, a clamping capacitor is added to the switching channel to further suppress the voltage ripple. Capacitors can be also used to compensate for reactive power and for introducing load balance. In [29], capacitors are used as the negative- and zero-sequence compensator topology for three-phase unbalanced loads in the distribution networks. The capacitor connection modes are controlled to switch between phase-to-phase and phase-to-ground by using intelligent grouping compound switches. Compared to traditional voltage ripple suppression strategies, the circuit topology used in this novel method is simple, and the costs are low due the removal of the DC–DC converter and the high-frequency transformer. In addition, compared with previous voltage ripple suppression methods, there are no additional losses in the proposed novel MMC. With the proposed voltage ripple suppression method, the voltage ripples of the submodule capacitors are greatly reduced. In addition, the reliability and power density of the proposed MMC also increased. The remainder of this article is organized as follows: In Section 2, the voltage ripples of the capacitors in the upper and the lower arms are analyzed. In Section 3, the submodule topologies employing the reversed PWM-switching channel are provided. The realization of this novel capacitor voltage ripple suppression method is described in Section 4. Additionally, the simulation results regarding capacitor voltage fluctuation suppression are shown in Section 5. Finally, the conclusion is provided in Section 6.

2. Analysis of the Capacitor Voltage Ripple

The typical topology of the MMC is shown in Figure 1a. An MMC has three phases, and each phase is divided into an upper arm and a lower arm. Each arm consists of a number of submodules and an arm inductor in series. The arm's inductance can restrain the circulating current.



(**a**) (**b**)

Figure 1. Topology of MMC: (**a**) three-phase MMC topology; (**b**) topology of a half-bridge submodule (SM_n).

Figure 1b shows the topology of the half-bridge submodule, which is the most commonly used submodule. The submodule has three operating modes: an input mode, bypass mode, and removal mode. In Figure 1b, T_1 and T_2 are IGBTs, and D_1 and D_2 are antiparallel diodes. When T_1 and T_2 are switched off at the same time, the submodule is cut off; i.e., it is in a hot standby state. When T_1 is switched off and T_2 is switched on, the operating state of the submodule is called the bypass state. When T_1 is switched on and T_2 is switched off, the submodule begins its operation. In this state, the capacitor of the submodule is connected in series with the capacitors of the other submodules in operation. The sum of the series capacitor voltages is the arm voltage. The difference-mode component of the arm voltages of the upper and lower arms is the AC voltage output of each phase. It can be seen from the MMC topology that the sum of the capacitor voltages of the input submodules in each phase is equal to the DC voltage. The numbers of the input submodules of the upper and lower arms of each phase vary with time, but their sum is constant, and it is equal to the number of the submodules used in each arm.

The output voltage of each phase in the MMC is expressed as follows:

$$u_{\mathrm{x}} = M\frac{U_{\mathrm{dc}}}{2}\sin(\omega t + \theta_{\mathrm{x}}) = U_{\mathrm{x}}\sin(\omega t + \theta_{\mathrm{x}}) \tag{1}$$

where M is the voltage modulation ratio, U_{dc} is the DC voltage, U_{x} is the AC voltage amplitude, and θ_{x} is the AC voltage phase angle [28].

The output current of each phase is expressed as follows:

$$i_{\mathrm{x}} = I_{\mathrm{x}}\sin(\omega t + \theta_{\mathrm{x}} - \varphi) \tag{2}$$

where I_{x} is the amplitude of the AC current, and φ is the load impedance angle [28].

The instantaneous output power of each phase is as follows.

$$p_{\mathrm{x}} = u_{\mathrm{x}} i_{\mathrm{x}} \tag{3}$$

Combining (1) and (2) into (3) obtains the following.

$$\begin{cases} p_{\mathrm{a}} = \frac{MU_{\mathrm{dc}}I_{\mathrm{x}}}{4}\cos\varphi - \frac{MU_{\mathrm{dc}}I_{\mathrm{x}}}{4}\cos(2\omega t + 2\theta_{\mathrm{x}} - \varphi) \\ p_{\mathrm{b}} = \frac{MU_{\mathrm{dc}}I_{\mathrm{x}}}{4}\cos\varphi - \frac{MU_{\mathrm{dc}}I_{\mathrm{x}}}{4}\cos(2\omega t + 2\theta_{\mathrm{x}} - \varphi + \frac{2}{3}\pi) \\ p_{\mathrm{c}} = \frac{MU_{\mathrm{dc}}I_{\mathrm{x}}}{4}\cos\varphi - \frac{MU_{\mathrm{dc}}I_{\mathrm{x}}}{4}\cos(2\omega t + 2\theta_{\mathrm{x}} - \varphi - \frac{2}{3}\pi) \end{cases} \tag{4}$$

It can be seen from (4) that the power of each phase of the MMC includes a DC component and secondary negative sequence component. The DC component is the active part of the output power, and the secondary component is stored in the capacitors of the submodules or in the DC side of the MMC.

The arm voltage of the MMC is usually controlled as follows:

$$\begin{cases} u_{\mathrm{xu}} = \frac{1}{2}U_{\mathrm{dc}} - u_{\mathrm{x}} = \frac{1}{2}U_{\mathrm{dc}}[1 - M\sin(\omega t + \theta_{\mathrm{x}})] \\ u_{\mathrm{xl}} = \frac{1}{2}U_{\mathrm{dc}} + u_{\mathrm{x}} = \frac{1}{2}U_{\mathrm{dc}}[1 + M\sin(\omega t + \theta_{\mathrm{x}})] \end{cases} \tag{5}$$

where u_{xu} is the upper arm voltage, and u_{xl} is the lower arm voltage of the x phase (x = a, b, c).

The output current can also be expressed as follows:

$$i_{\mathrm{x}} = i_{\mathrm{xu}} - i_{\mathrm{xl}} \tag{6}$$

where i_{xu} and i_{xl} are the upper arm current and lower arm current of the x phase (x = a, b, c), respectively.

Define the common-mode component of the upper and lower arm currents as the circulating current i_{xc}.

$$i_{\mathrm{xc}} = \frac{1}{2}(i_{\mathrm{xu}} + i_{\mathrm{xl}}) \tag{7}$$

According to (6) and (7), the arm current can be expressed as follows.

$$\begin{cases} i_{\mathrm{xu}} = i_{\mathrm{xc}} + \frac{1}{2}i_{\mathrm{x}} \\ i_{\mathrm{xl}} = i_{\mathrm{xc}} - \frac{1}{2}i_{\mathrm{x}} \end{cases} \tag{8}$$

The power of the upper arm and the lower arm in each phase is expressed as follows.

$$\begin{cases} p_{\mathrm{xu}} = u_{\mathrm{xu}} i_{\mathrm{xu}} \\ p_{\mathrm{xl}} = u_{\mathrm{xl}} i_{\mathrm{xl}} \end{cases} \tag{9}$$

Combining (1), (2), (5), and (8) into (9) obtains the following.

$$\begin{cases} p_{\mathrm{xu}} = & \frac{U_{\mathrm{dc}}}{2} i_{\mathrm{xc}} + \frac{U_{\mathrm{dc}} I_{\mathrm{x}}}{4} \sin(\omega t + \theta_{\mathrm{x}} - \varphi) - \frac{MU_{\mathrm{dc}}}{2} i_{\mathrm{xc}} \sin(\omega t + \theta_{\mathrm{x}}) \\ & -\frac{MU_{\mathrm{dc}} I_{\mathrm{x}}}{4} \sin(\omega t + \theta_{\mathrm{x}}) \sin(\omega t + \theta_{\mathrm{x}} - \varphi) \\ p_{\mathrm{xl}} = & \frac{U_{\mathrm{dc}}}{2} i_{\mathrm{xc}} - \frac{U_{\mathrm{dc}} I_{\mathrm{x}}}{4} \sin(\omega t + \theta_{\mathrm{x}} - \varphi) + \frac{MU_{\mathrm{dc}}}{2} i_{\mathrm{xc}} \sin(\omega t + \theta_{\mathrm{x}}) \\ & -\frac{MU_{\mathrm{dc}} I_{\mathrm{x}}}{4} \sin(\omega t + \theta_{\mathrm{x}}) \sin(\omega t + \theta_{\mathrm{x}} - \varphi) \end{cases} \tag{10}$$

The first and the fourth terms of p_{xu} are in phase with p_{xl} in (10), and the second and the third terms are reversed with p_{xl}. Since circulating current i_{xc} mainly contains the DC component and the secondary component, the fundamental ripple of the upper and lower arm power is inverse, and the double-frequency ripple is in phase. The power ripple leads to the voltage ripple of the capacitor. Since the fundamental frequency component occupies the largest proportion in the arm power, the capacitor voltages of the upper and lower arms fluctuate inversely at the fundamental frequency.

The further analysis of (10) shows that the fluctuation amplitude is proportional to the output current amplitude and is inversely proportional to the output frequency. The large voltage fluctuation of the capacitor will challenge the withstanding voltage capability of the capacitors and the power switching devices, and it will aggravate the power imbalance inside the MMC and even deteriorate the output waveform. In order to reduce the capacitor voltage ripple of the submodule without using large-size capacitors, a new submodule topology employing a switching channel is proposed in this paper. The switching channel is constructed between the submodules of the upper and lower arms. Since the channel forms a path for charge to flow freely, it can realize the self-charge and self-discharge between the capacitors of the submodules at both sides of the channel. Thus, voltage fluctuations can be greatly reduced.

3. Submodule Topologies Employing the Reversed-PWM Switching Channel

According to the above analysis, the capacitor voltages of the submodules in the upper and lower arms demonstrate inverse fluctuations at the fundamental frequency, which will lead to periodic potential differences. If the switching channel is built between the submodules at the same position of the upper and lower arms, the charge of the capacitor with higher voltage in the upper (lower) arm can flow to a capacitor with lower voltage in the lower (upper) arm. Then, the self-charging (discharging) ability of the capacitors between the upper and lower arms can be realized. This decreases the capacitor's voltage when it is higher than the reference voltage and increases the capacitor's voltage when it is lower than the reference voltage. The voltages of both capacitors become close to the reference value at the same time, which means that capacitor voltage fluctuation suppression is realized.

Figure 2a is the schematic diagram of the switching channel between the arms. On the left is the submodule of the upper arm, and on the right is the submodule of the lower arm. The channel between the two submodules provides a path for the charge to flow freely between the capacitors.

Because of the additional physical connection between the upper and lower arms, MMC will not work properly if the switching channel is not controlled. Moreover, we want the channel to be simple and effective, and the best method to achieve this is to limit the additional control costs added to the MMC system. In this manner, the proposed switching channel only uses the switching device to control the charge's flow. Only when the submodules at both sides are in the bypass state at the same time does the channel input switch, and it is kept off at other times to ensure the normal operation of the MMC.

In addition, a clamping capacitor is added in the channel to further limit the voltage fluctuations to a smaller range. The submodule topology employing the switching channel with the clamping capacitor is shown in Figure 2c. The MMC topology based on the proposed submodule is shown in Figure 3.

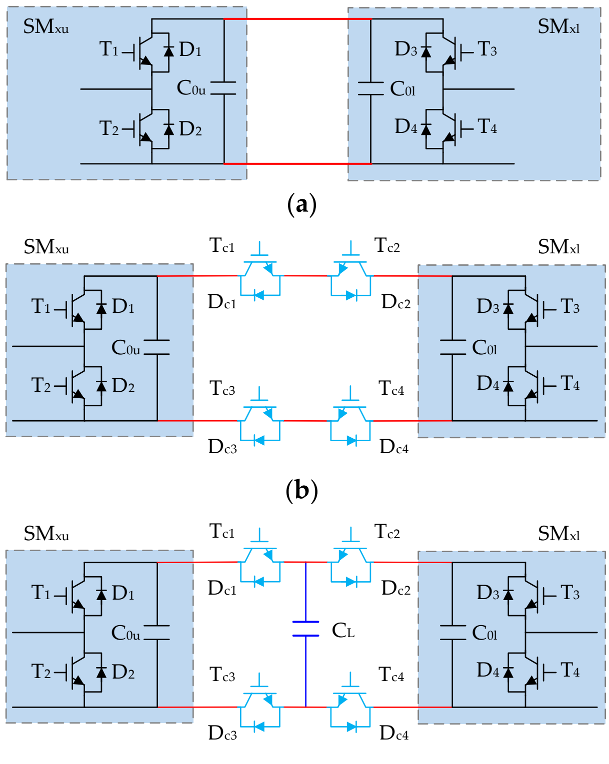


Figure 2. Proposed submodule topology: (**a**) schematic diagram of the switching channel; (**b**) submodule employing the switching channel; (**c**) submodule employing the switching channel with the clamping capacitor.

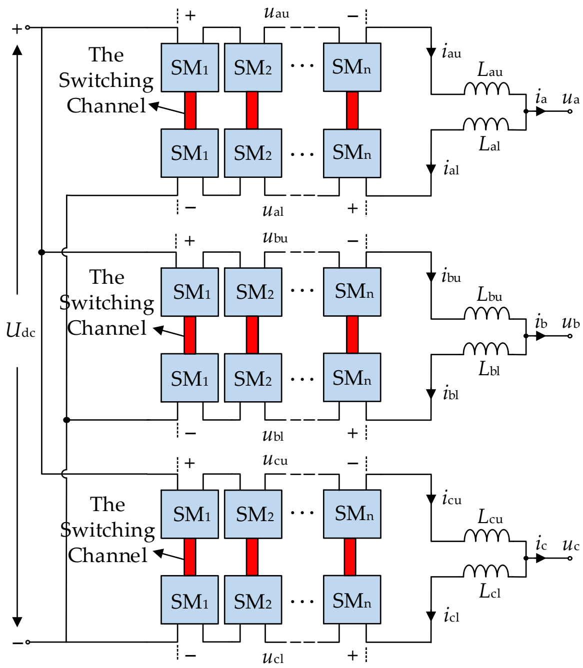


Figure 3. MMC topology based on new submodules.

4. Realization of the Capacitor Voltage Ripple Suppression Method with the Switching Channel

In order to realize the proposed capacitor voltage fluctuation suppression strategy, the control method and operating principle of the channel switches are both described in detail. The clamping capacitor is added in the channel for stabilizing the submodule capacitor voltage. In addition, for reducing the number of the switch devices used in the switching channel, the same position connection method and the symmetrical connection method are both provided and discussed.

4.1. Control of the Channel Switches

Since the proposed switching channel is connected to the upper and lower arms in the same phase, a new path is added to the original topology of the MMC. In order to ensure the normal operation of the MMC employing the switching channel, the on–off modes of the channel require additional control. The on–off logic of the switching channel is shown in Table 1. Only when the submodules at both ends of the channel are in bypass state will the channel be switched on. During this period, the capacitor of the submodule has no arm current flowed through and is connected to the other capacitor of the submodule at the end of the channel in parallel for charging or discharging.

Table 1. Power channel control logic.

SM_u	SM_l	Power Channel
input	input	off
input	bypass	off
bypass	input	off
bypass	bypass	on

Since the turn-off signal of the switching channel is obtained by the NAND logic calculation of the trigger pulses of the submodule switch devices, when the switching channel is about to be switched off, the channel will not receive the turn-off signal until the two terminal submodules of the channel are put into operation. During this period, the submodule and the switching channel are put into operation at the same time, which leads to the abnormal operation of the MMC.

In order to solve the above-mentioned timing problem, one idea is to add a dead zone before the switches in the channel are switched off. Then, we can ensure that the channel is switched off during the period after the submodule is put into operation to prevent the simultaneous operation of the submodule and the channel. However, since the input and bypass of the submodule are controlled by the capacitor voltage balance control system, predicting the bypass time of the channel in advance is difficult, so the added dead time cannot be estimated. To perform this, the dead time can be added at the end of each channel switch's switching cycle, as shown in Figure 4. However, this method will increase the switching loss in the switches used in the channel.

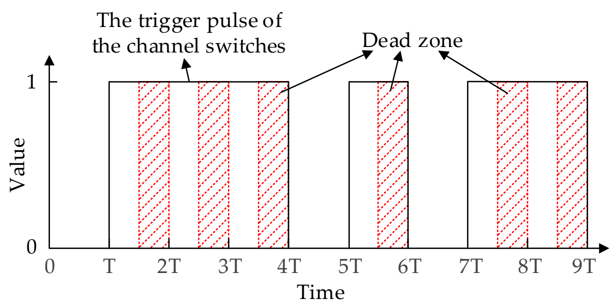


Figure 4. Position of the dead zone of the channel switch trigger pulse.

In order to ensure the high efficiency and low loss of the switching channel, interlocking switches are added into the submodules to solve the above timing problem. As shown in Figure 5, S_c is the switch used in the channel, and S_L is the interlocking switch. Trigger pulses of the S_L and S_c are kept opposite to one another at all times. It is ensured at the hardware level that the submodules and the channel will not be put into operation at the same time. In this manner, the frequency of the channel switch is not too high, and there are no increases in switching loss.

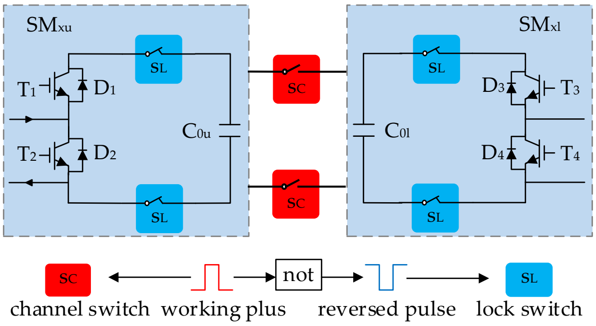


Figure 5. Submodule based on interlocking switches.

4.2. Operating Principle of the Switching Channel

It can be seen from Formula (10) that the submodules of the upper and lower arms contain fluctuating power in the opposite direction at the fundamental frequency. The capacitor voltage fluctuations in the traditional submodules during the operation are shown in Figure 6a. It can be seen in the figure that periodic reverse ripples above and below the reference voltage value can be observed in the capacitor voltages. The voltage fluctuation could result in a periodic potential difference in the capacitors of the upper and lower arms, respectively. If the switching channel is built between the capacitors in the upper and lower arms, the capacitor with the higher voltage will charge the capacitor with lower voltage. Then, both voltages will approach the reference value at the same time, and the voltage fluctuation suppression effect is achieved.

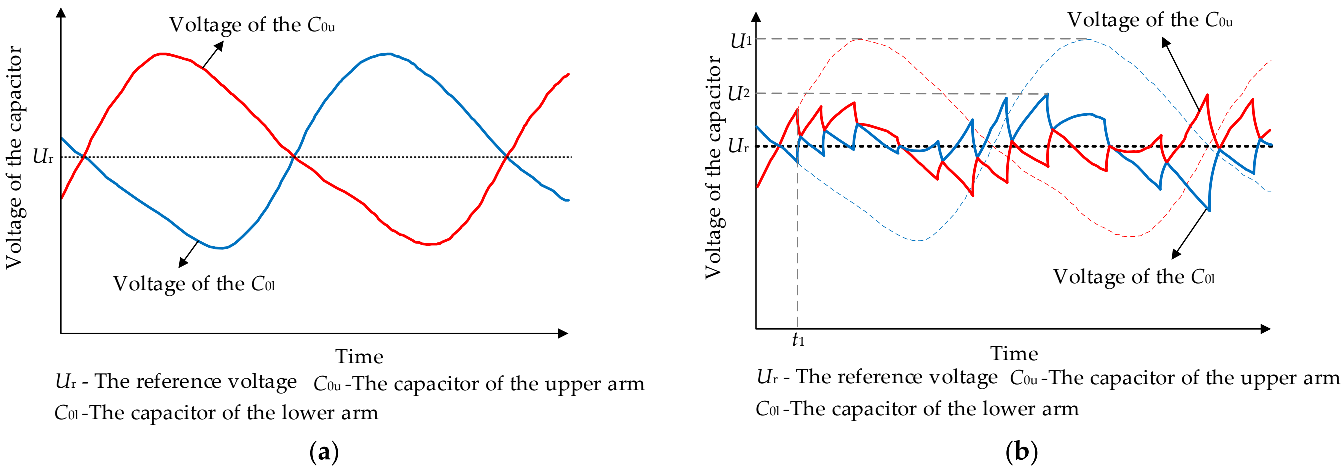


Figure 6. Schematic diagram of voltage suppression: (**a**) schematic diagram of capacitor voltage fluctuation without suppression method; (**b**) schematic diagram of capacitor voltage fluctuation with proposed suppression method.

The capacitive voltage ripples employing the switching channel are shown in Figure 6b, in which the maximum value of the voltage fluctuation is suppressed from U_1 to U_2. At time t_1, both terminal submodules of the channel are bypassed at the same time, and the switching channel is introduced. A path is formed between the capacitors of the two submodules. Since the potential of the C_{0u} is higher than that of C_{0l}, the charge flows from

C_{0u} to C_{0l}. Then, C_{0l} voltage increases, and C_{0u} voltage decreases until the two capacitor potentials are equal.

Since the voltage of capacitor cannot be changed suddenly, it takes time for the two capacitors to reach the same voltage. We call this period of time Δt, which is affected by the capacitance time' constant. Additionally, we could call each duration in which the channel is in the input state time t_c, which is determined by the capacitor's voltage-balance control system. This means that t_c is the duration of both the submodules at the two sides of the channel in the bypass state.

In Table 2, N_{SMxu} and N_{SMxl} are the number of the submodules in the input state of the upper arm and the lower arm, respectively. T_s is the duration of this stage, and T is the MMC working cycle. Additionally, P is the probability of the two-terminal modules of the channel, and it is in the bypass state at the same time. The product of T_s and P is the operating time t_c of the channel at this stage. According to Table 2, the minimum non-zero value of t_c is described as follows.

$$t_{cmin} = \frac{(n-1)T}{n^2(n+1)} \tag{11}$$

Table 2. Input probability of the switching channel.

N_{SMxu}	0	1	2	...	n
N_{SMxl}	n	$n-1$	$n-2$	...	0
T_s	$\frac{T}{n+1}$	$\frac{T}{n+1}$	$\frac{T}{n+1}$	...	$\frac{T}{n+1}$
P	0	$\frac{n-1}{n} \cdot \frac{1}{n}$	$\frac{n-2}{n} \cdot \frac{2}{n}$	...	0

To ensure that the energy channel works as expected, $t_{cmin} > \Delta t$ should be ensured.

4.3. Voltage Stabilizing Effect of the Clamping Capacitor

It can be obtained from the capacitor characteristics that, when the capacitance is constant, the voltage increase in the capacitor is proportional to the increase in the charge [30], which can be represented as follows.

$$\boldsymbol{\Delta} u = \frac{\boldsymbol{\Delta} Q}{C} \tag{12}$$

From (12), we know that when the amount of transferred charge in the switching channel remains unchanged, an additional capacitor can be placed in the switching channel in order to further reduce fluctuations in the capacitor voltage. In addition, the added capacitor can also further clamp the capacitor's voltage to the reference voltage U_{C0}.

4.4. Connection Method of the Switching Channel

The switching channel is in parallel with several cascaded submodules. When the switching channel is in the off state, the voltage resulting from the channel switches is the sum of the capacitor voltages of the input submodules in parallel with it.

If the switching channel is connected with the submodules at the same position, as shown in Figure 7a, then the maximum voltage borne by each channel is nU_C, i.e., DC voltage U_{dc}. MMC is usually used in medium- and high-voltage systems; thus, U_{dc} is generally large. It is necessary to connect multiple switch devices in the channel in series so that they can share the voltage and adopt the corresponding device voltage equalization technology.

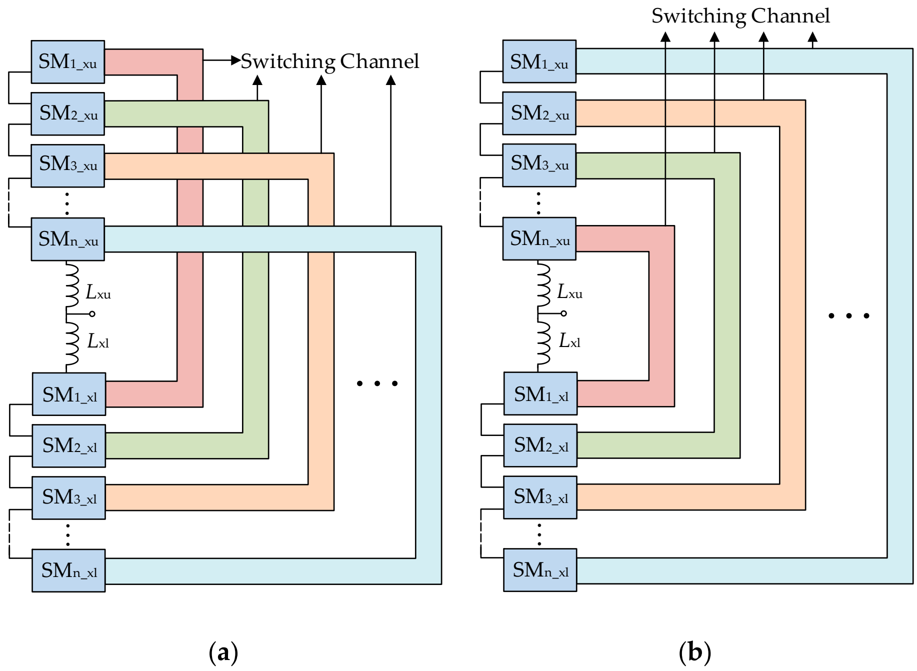


Figure 7. Two connection modes: (**a**) same position connection method; (**b**) symmetrical connection method.

To reduce costs, thyristors can be used in series as pressure-containing devices. The charge can only flow in one direction in the thyristor, but the switching channel requires two-way movements of the charge; thus, the thyristors in the channel need to be doubled and used in reverse parallel orientations. At the same time, since thyristors are semi-controllable devices, there must be at least two reversed IGBTs or other fully controlled devices in series in the channel to realize the full control of the input and the removal of the channel.

It is worth noting that the number of the voltage-withstanding devices used for different channel connections varies. When the same-position connection mode shown in Figure 7a is used, the maximum voltage resulting from each channel is nU_C. Assuming that the withstanding voltage value of each withstanding voltage device is U_T and considering a margin of 1.5 times, the total number of withstanding voltage devices required for n channels is described as follows.

$$K = \frac{3n^2 U_C}{U_T} \tag{13}$$

If the channel connection mode is changed to the symmetrical connection, as shown in Figure 7b, the maximum withstanding voltage varies from $2U_C$ to nU_C due to the different numbers of submodules in parallel with each channel, and the number of withstanding voltage devices required for this connection mode is described as follows.

$$K = \frac{2.25n^2 U_C}{U_T} + \frac{1.5nU_C}{U_T} \tag{14}$$

Compared to the same-position connection mode, the symmetric connection mode reduces the number of used devices by the following.

$$\mathrm{m} = (0.75n^2 - 1.5n)\frac{U_C}{U_T} \tag{15}$$

The proportion of the saved devices is $(25 - \frac{50}{n})\%$. Thus, it can be concluded from Formula (15) that when more submodules are used in the MMC with the symmetrical connection mode, the proportion of the saved devices becomes larger.

5. Simulation Results

In order to verify the effectiveness of the proposed voltage ripple suppression strategy, MMC models based on the traditional submodule and submodules employing a switching channel without a clamping capacitor and with a clamping capacitor were built in MATLAB/Simulink according to Figure 8. The MMC in the simulation is used as an inverter, and the DC side is the power supply. A phase-disposition pulse width modulation strategy is adopted. The voltage-balancing strategy used in this simulation comprises the traditional voltage-sorting method. When the arm current is positive, the submodules with the lowest capacitor voltages are put into operation and then the corresponding submodule capacitors charge, while the submodules with the highest voltage are put into operation and the corresponding submodule capacitors discharge when the arm current is negative. The system parameters of the three models are consistent and shown in Table 3.

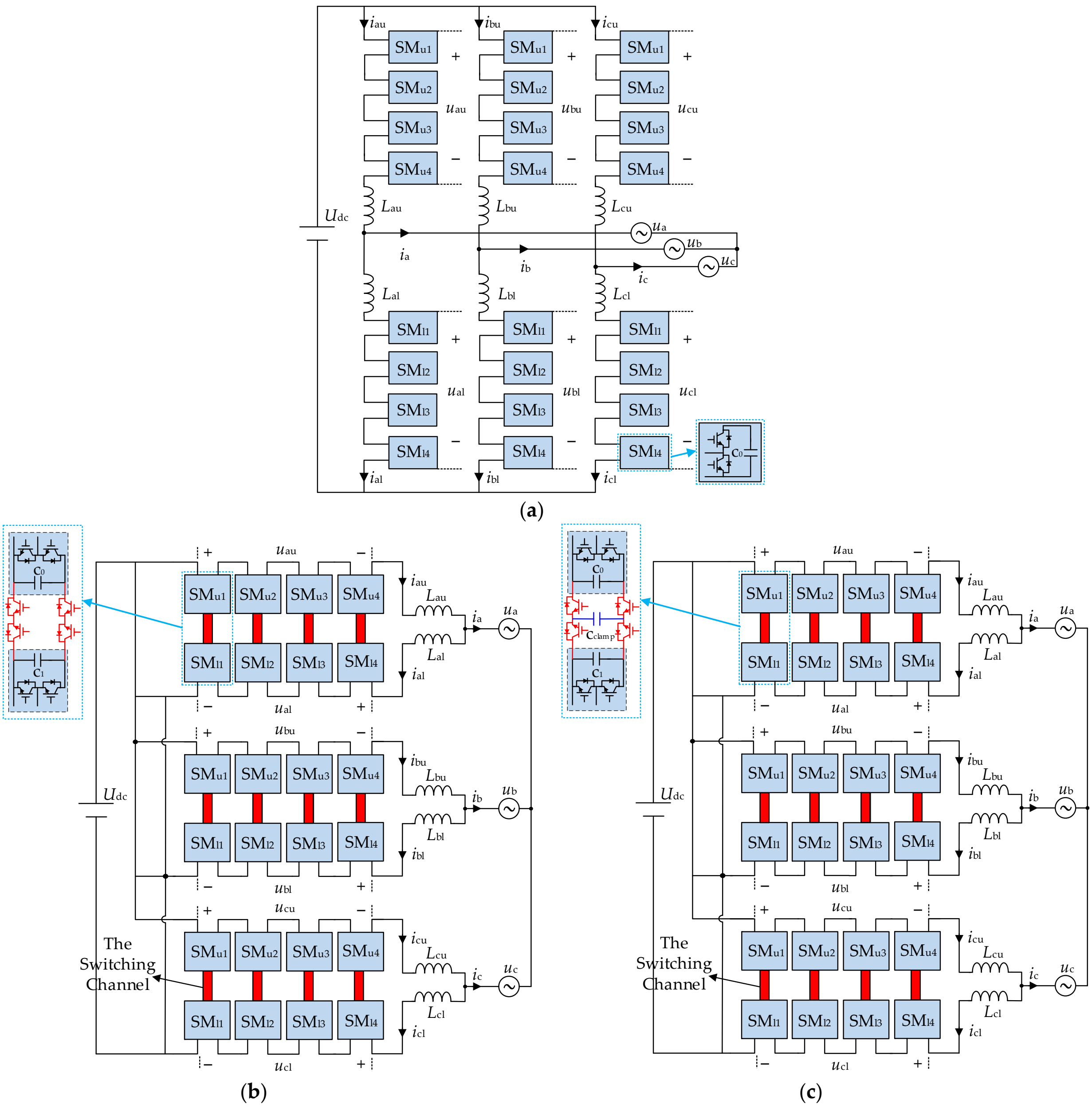


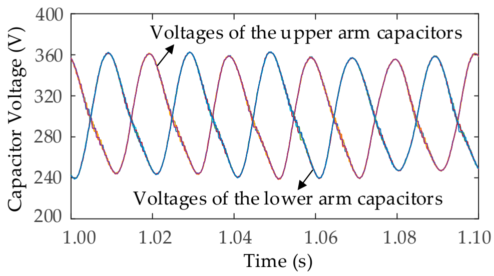
Figure 8. Simulation models of the MMC: (**a**) MMC based on the traditional submodule; (**b**) MMC based on the submodules employing a switching channel without a clamping capacitor; (**c**) MMC based on the submodules employing a switching channel with a clamping capacitor.

Table 3. Parameters of the simulation model.

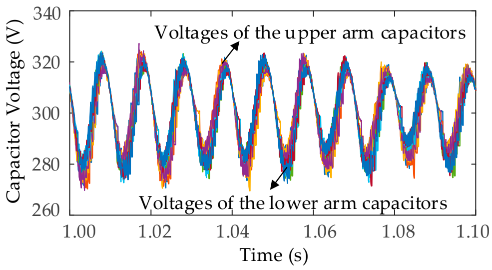
Symbol	Parameter	Value
U_{dc}	DC bus voltage	1200 V
N	Number of submodules per arm	4
$U_{C0,C1}$	Reference capacitor voltage	300 V
$C_{0,1}$	Submodule capacitor	666 µF
C_{clamp}	Clamping capacitor	666 µF
$L_{au,bu,cu}$	Inductance of the upper Arm	4 mH
$L_{al,bl,cl}$	Inductance of the lower Arm	4 mH
$I_{a,b,c}$	Rated amplitude of AC current	60 A
$U_{a,b,c}$	Rated amplitude of AC voltage	400 V
f	Rated frequency	50 Hz
f_s	Switching frequency	2 kHz

5.1. Suppression Results of the Capacitor Voltage Ripple

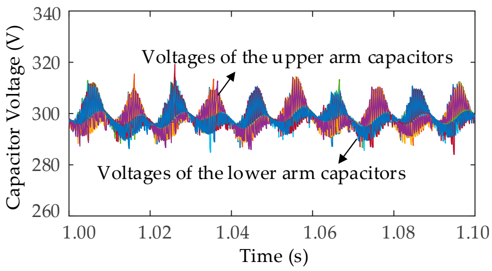
Figure 9 shows the capacitor voltages of the submodules with three different topologies. Figure 9a shows the capacitor voltages of the traditional submodules. We can observe from Figure 9a that the capacitor voltages demonstrate periodic fluctuations at the frequency of 50 Hz, and the capacitor voltages of the upper arm and the lower arm fluctuate in the reversed direction. Additionally, the waveforms of the capacitor voltages of the upper and the lower arms are approximately symmetrical with respect to the reference voltage value (U_{C0} = 300 V). The waveform of the capacitor voltage is consistent with that of the theoretical analysis in Section 2. The peak-to-peak value of the voltage fluctuation is about 121.6 V, as seen in Figure 9a.



(**a**)



(**b**)



(**c**)

Figure 9. Voltages of the submodule capacitors: (**a**) traditional submodule; (**b**) submodule employing a switching channel without the clamping capacitor; (**c**) submodule employing a switching channel with the clamping capacitor.

Figure 9b shows the capacitor voltages of the submodules employing a switching channel without a clamping capacitor. Since the switching channel provides a physical path for the charge flow between the capacitors of the upper and lower arms, the voltage fluctuations are suppressed. The peak-to-peak value of the capacitor voltage of the submodule employing the switching channel without the clamping capacitor is 56.7 V, which is 53.37% lower than that of the traditional submodule. It can also be seen from Figure 8b that the ripple directions of the capacitor voltages of the upper and lower arms is the same, which is due to the in-phase component of the upper and lower arm power.

Figure 9c shows the capacitor voltages employing the switching channel with the clamping capacitor. Additionally, the peak-to-peak voltage value of the submodule employing the switching channel with the clamping capacitor is only 25.8 V, which is 78.78% lower than that of the traditional submodule and 54.50% lower than that of the submodule employing a switching channel without a clamping capacitor. It can be seen from the capacitor voltage suppression results of the three different topologies that the proposed voltage ripple suppression strategy performs well. Thus, in the case of a same level output voltage, the submodule capacitance of the MMC with the proposed method can be reduced greatly compared to that of the MMC without a voltage ripple suppression strategy.

5.2. The Effect of the Clamping Capacitor

Figure 10 shows the details of the capacitor voltages of the submodules employing a switching channel during the charging and discharging process. It can be seen that there are many burrs on the capacitor's voltage waveforms, which is the key to suppressing voltage fluctuations. Burrs can be divided into two parts: one part deviating from the reference voltage value (U_{C0} = 300 V), and the other part approaching to the reference voltage value. When the submodule is put into operation, an arm current flows through the capacitor, and the capacitor is charged (or discharged) away from the reference voltage. When the switching channel is put into operation, the capacitor is charged or discharged by another capacitor of the submodule connected with the channel because of the potential difference between the two capacitors, and the voltages of the two capacitors become close to the reference value.

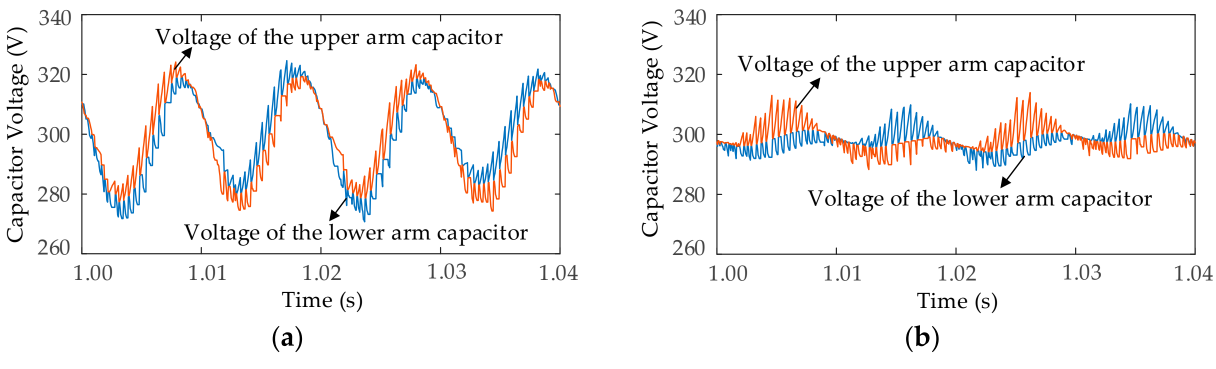


Figure 10. The capacitor voltages of the submodules employing the switching channel during charging and discharging process: (**a**) the capacitor voltages of the submodules employing a switching channel without a clamping capacitor; (**b**) the capacitor voltages of the submodules employing a switching channel with a clamping capacitor.

It can be seen from Formula (10) that the power of the upper and lower arms has an inverted fundamental component and an in-phase secondary component. The secondary component of the power will cause in-phase voltage fluctuations in the capacitors, and this fluctuation cannot be offset by the switching channel. Therefore, the voltages as a whole exhibit in-phase fluctuations with a double fundamental frequency in Figure 10a. In Figure 10b, the capacitor's voltage fluctuations are suppressed compared to those in the submodules employing a switching channel without a clamping capacitor. This is because the clamping capacitor increases the total capacitance in the charging path while the quantity of the electric charge required to flow through the path is the same.

5.3. Analysis of the Output AC Currents

Figure 11 shows the output AC currents of the MMC with three different topologies. Figure 11a,c,e show the waveforms of the output AC currents of the MMC with three different topologies, respectively. The THD analysis results of the phase A output currents of the aforementioned three different MMCs are shown in Figure 11b,d,f. It can be seen that the THD of the phase A output current of the conventional MMC is 2.04%, while the corresponding results of the MMCs employing the switching channels without and with a clamping capacitor are 1.75% and 1.55%, respectively. The output AC current THD of the proposed MMC employing the switching channel with a clamping capacitor decreases 24.02% compared with the traditional MMC. Thus, the waveform of the output current of the MMC employing the switching channel with the clamping capacitor has the best sine quality compared to the other two MMC topologies. This is because this kind of MMC has the smallest capacitor voltage ripple during operation.

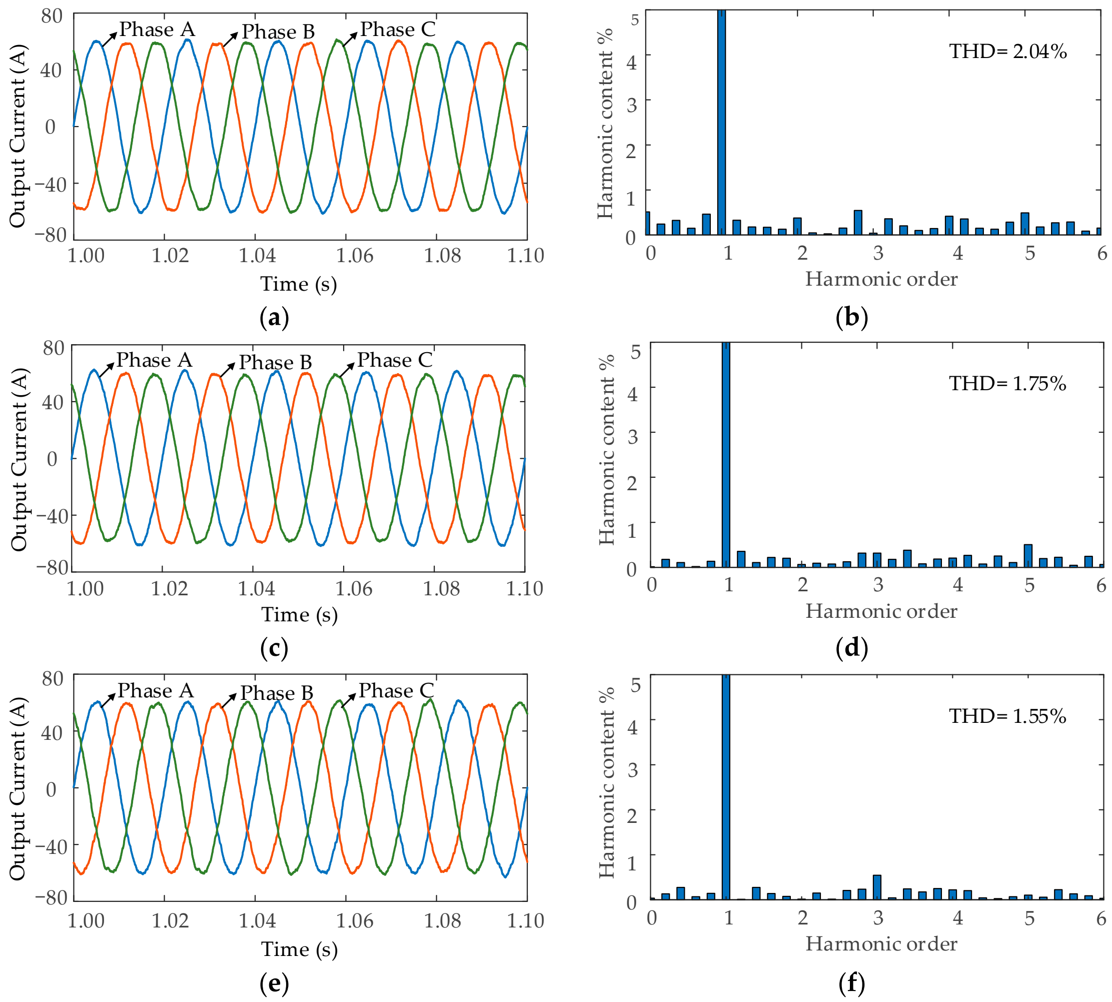


Figure 11. The output AC currents of the MMC with three different topologies: (**a**) the output AC current of the MMC with the traditional submodule; (**b**) THD of the output AC current of the MMC with traditional submodule (phase A); (**c**) the output AC current of the MMC employing the switching channel without a clamping capacitor; (**d**) THD of the output AC current of the MMC employing the switching channel without a clamping capacitor (phase A); (**e**) the output AC current of the MMC employing a switching channel with a clamping capacitor; (**f**) THD of the output AC current of the MMC employing a switching channel with a clamping capacitor (phase A).

6. Conclusions

A voltage ripple-suppression strategy employing a reversed PWM switching channel is proposed in this paper. The capacitor voltages of the submodules in the upper and lower arms are analyzed. It was found that the voltage fluctuation directions are inversed. The proposed switching channel provides a charge path between the submodules of the upper and lower arms. Then, the voltage fluctuations could be partially offset. In addition, a clamping capacitor was added to the channel's DC bus to further suppress fluctuation voltages by approximately 78% together with the effect of the aforementioned switching channel. Therefore, the total capacitance used in the proposed method is more reduced than that of the capacitance used in the traditional capacitor voltage ripple suppression strategy. Additionally, the power density increased. Because of these advantages, the proposed switching-channel capacitor voltage-suppression method has good application prospects in onboard integrated power systems. The shortcoming of the proposed method in this paper is that only capacitor voltage-fluctuation suppression schemes under power frequency (50 Hz) situations were considered. Thus, the operating frequency of the MMC is limited. The future work will focus on widening the operating frequency of the MMC system and suppressing capacitor voltage fluctuations when the MMC is working at lower frequencies. In this case, the MMC can be used for driving high-power level motors and working in a wider range of frequencies.

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Nomenclature

MMC	Modular multilevel converter
SM_{un}	The upper arm submodule of the MMC
SM_{ln}	The lower arm submodule of the MMC
M	Voltage modulation ratio
U_{dc}	DC voltage (V)
U_x	The amplitude of the AC voltage ($x = a, b, c$) (V)
U_C	Capacitor voltage (V)
U_{C0}	Reference capacitor voltage (V)
u_{xu}	Upper arm voltage of the x phase ($x = a, b, c$) (V)
u_{xl}	Lower arm voltage of the x phase ($x = a, b, c$) (V)
I_x	The amplitude of the AC current ($x = a, b, c$) (A)
i_{xu}	Upper arm current of the x phase ($x = a, b, c$) (A)
i_{xl}	Lower arm current of the x phase ($x = a, b, c$) (A)
i_{xc}	Circulating current ($x = a, b, c$) (A)
φ	Load impedance angle (rad)
θ_x	AC voltage phase angle of the x phase ($x = a, b, c$) (rad)
p_x	The instantaneous output power of the x phase ($x = a, b, c$) (W)
p_{xu}	The power of the upper arm of the x phase ($x = a, b, c$) (W)
p_{xl}	The power of the lower arm of the x phase ($x = a, b, c$) (W)
T	MMC working cycle (s)
T_s	Duration of each stage of the submodule (s)
P	Probability of the two-terminal modules of the channel in the bypass state at the same time
t_c	Duration of the channel in the input state each time (s)
Δt	Duration of the capacitors to reach the same voltage (s)
N	Number of submodules per arm
U_T	The withstanding voltage value of each withstanding voltage device (V)
K	The total number of withstanding voltage devices required

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