electronics

Article

A Track-and-Hold Circuit with Tunable Non-Linearity and a Calibration Loop for PAM-8 SerDes Receivers

Alessio Di Pasquo [1,2,*], Enrico Monaco [2], Nicola Ghittori [2], Claudio Nani [2] and Luca Fanucci [1]

[1] Department of Information Engineering, University of Pisa, 56122 Pisa, Italy; luca.fanucci@unipi.it
[2] Marvell Semiconductor, 27100 Pavia, Italy; emonaco@marvell.com (E.M.); nghittori@marvell.com (N.G.); nclaudio@marvell.com (C.N.)
* Correspondence: alessio.dipasquo@phd.unipi.it

Abstract: In this brief, we propose a 60 GS/s high-linearity two-stage 8 × 8 time-interleaved track-and-hold circuit where it is possible to tune the static non-linearities of the second-stage buffer by applying a proper bias voltage. This allows us to maximize the static linearity of the buffer or introduce effects that counterbalance the non-linearities of other blocks of the analog front-end. To validate the proposed circuit, a prototype in TSMC 5 nm technology is designed and a linearity calibration loop is proposed for a Pulse Amplitude Modulation SerDes receiver. For the analog buffer, circuit-level simulations are performed in Cadence Virtuoso, while the calibration loop is simulated in MATLAB. The optimal bias voltage value can be found by modeling the track-and-hold linearity using a Taylor series and implementing the linearity calibration loop in MATLAB. By applying this result to the circuit-level simulation, we obtain a total harmonic distortion of over 50 dB, which matches with the maximum value achievable across the complete bias voltage control range. Lastly, the linearity of the system is also verified using a PAM-8 pseudorandom stream signal.

Keywords: PAM-8; SerDes receivers; track-and-hold; time-interleaved; linearity

Citation: Di Pasquo, A.; Monaco, E.; Ghittori, N.; Nani, C.; Fanucci, L. A Track-and-Hold Circuit with Tunable Non-Linearity and a Calibration Loop for PAM-8 SerDes Receivers. *Electronics* **2022**, *11*, 2199. https://doi.org/10.3390/electronics11142199

Academic Editors: Costas Psychalinos, Ahmed S. Elwakil, Abdelali El Aroudi and Esteban Tlelo-Cuautle

Received: 6 June 2022
Accepted: 10 July 2022
Published: 13 July 2022

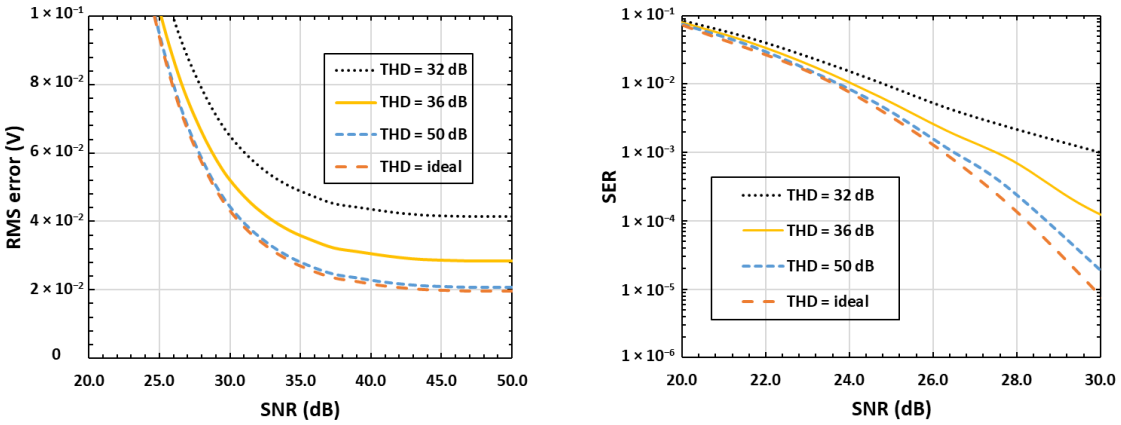
1. Introduction

Over the last few years, there has been a strong increment in internet traffic. This led to a rising interest in high-speed wireline communication systems with ever-increasing data rates, especially in data center applications. As of now, the most employed modulation in SerDes transceivers is Pulse Amplitude Modulation with four levels (PAM-4) [1–3], which allows doubling the data rate using the same symbol rate compared to Non-Return-to-Zero (NRZ) modulation. To achieve even higher data rates, the symbol rate of the system can be increased, but this approach is limited by the bandwidth of the channel. To overcome this problem, a higher-order modulation can be used. Examples of these modulations are PAM-8 [4–6], and other eight-symbol modulations such as [7] that increment the data rate by 50% compared to PAM-4, while using the same symbol rate.

On the other hand, PAM-8 introduces other challenges. Indeed, due to the high number of voltage levels required, it is much more sensitive to non-idealities such as noise, non-linearities, and Inter-Symbol Interference (ISI) that reduce the eye aperture. This directly affects the Bit Error Rate (BER) of the receiver, reducing the performance of the overall link. While the noise can be theoretically reduced by increasing the power consumption of the analog front-end and the ISI can be compensated by more complex equalization techniques, the non-linearities are difficult to address. Due to the low supply voltages of scaled CMOS technology nodes, it is challenging to achieve a high voltage swing for a good Signal-to-Noise Ratio (SNR) while maintaining a suitable total harmonic distortion (THD). Figure 1a shows the simulated root mean square (RMS) error at the slicer input, including the contribution of noise, residual ISI, and distortion, as a function of SNR (due to additive noise at receiver input) for different levels of receiver (RX) static THD

derived using a MATLAB simulation of a PAM-8 receiver. For THD values of approximately 32 dB and 36 dB [3], as used in typical PAM-4 receivers, the system shows a higher value of MSE compared to the 50 dB case which resembles the error in the case of an RX with ideal linearity. The same behaviors are visible in Figure 1b where the SER was obtained for a lower range of input SNR. This range was used to give evidence of the system behavior while not having to perform time-consuming simulations which can give a statistically relevant number of points to calculate the SER for high SNR values.

Because of the difficulties in achieving a high THD, the need arises for calibration to maximize the linearity, especially for the track-and-hold (TH) sampling stages of time-interleaved (TI) ADCs commonly used for wireline receivers. Indeed, as these blocks typically work with a large signal swing to maximize ADC loading, they are a significant contributor to overall THD. While many techniques can be found in the literature to reduce the non-linearities introduced by the TI ADC interleaving mismatches [8,9], there are relatively few examples of systems that address the non-linearities of the analog front-end. In [10,11], such systems make use of complex algorithms in the digital domain.



(**a**) (**b**)

Figure 1. (**a**) RMS error (in volts from the ideal reconstruction of the digital values with a swing of 2 V_{pp}) and (**b**) SER as a function of SNR for different levels of AFE static THD, derived using a MATLAB simulation of a PAM-8 receiver.

This paper proposes a TH circuit with tunable non-linearities and a simple calibration loop that allows maximizing the static linearity of the analog front-end by controlling a bias voltage in the analog domain. This could either improve the BER of the receiver or relax the constraint on the SNR for the same value of BER required.

2. TH Sampler

Figure 2 shows the top block diagram of the TH sampler. The circuit samples the input signal on 64 TI capacitances with a sampling speed of 60 GS/s. This is achieved through two cascaded time-interleaved stages. The signal is first sampled on eight different capacitances by the first stage, and then this process is repeated by the second stage for each of the eight sampled values. The sampling speeds of the two stages are 7.5 GS/s and 937.5 MS/s, respectively.

2.1. Circuit Description

The first stage is implemented through the sampling buffer described in [12]. In the second stage, eight interleaved buffers are used. Each one is followed by eight time-interleaved sampling switches to reach the desired interleaving factor, equal to 64. These eight buffers must support an input common-mode around half of the supply voltage to accommodate the output common-mode of the previous stage. Suitable solutions are the

ones used in [13,14], which are *gm-gm* inverter-based topologies. These topologies are very simple to design while having good speed and linearity.

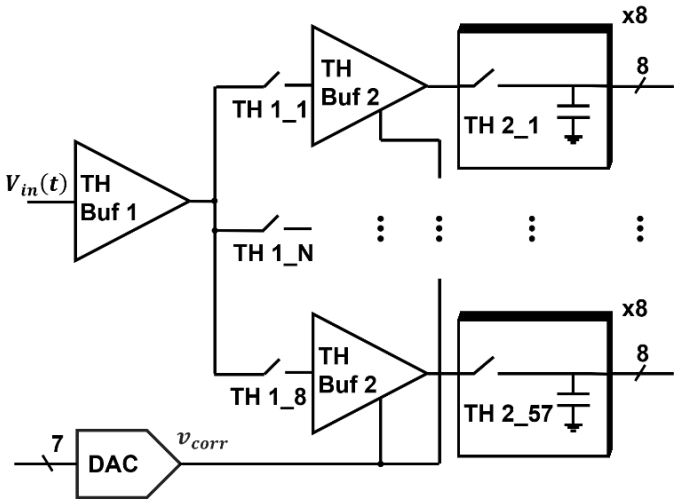


Figure 2. An 8×8 time-interleaved two-stage track-and-hold circuit and DAC for non-linearity calibration.

The linearity performance of this circuit stems from the opposite behavior of the inverter and diode. While the inverter compresses the signal, the diode load provides decompression. These two effects tend to cancel each other, resulting in overall good linearity. Nonetheless, this solution shows some limits due to the imperfect matching of the non-linearities. This is especially true across process corners and temperatures in which the behaviors of the inverter and the diode are significantly different, thus reducing the linearity.

For this reason, the solution shown in Figure 3 is proposed. It consists of a simple inverter for the first *gm* stage, followed by a differential current-controlled inverter closed in a diode configuration as load. The gate voltage v_{corr} of the tail transistor M_{nt} can be tuned to change the non-linearities of the diode and cancel the transconductor ones.

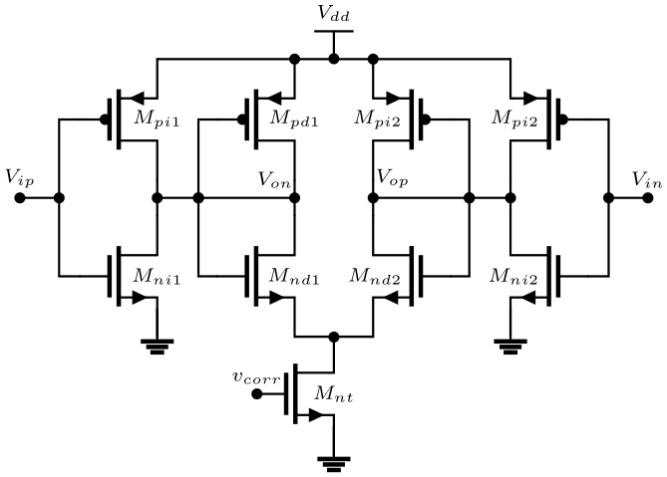


Figure 3. Second-stage *gm-gm* buffer.

2.2. Second-Stage Buffer Linearity Behavior

The relative non-linearity error (ε_r) of the buffer static input–output characteristic is defined as follows and it is shown in Figure 4 for different values of v_{corr}:

$$\varepsilon_r = \frac{V_{outd} - G_{AC} V_{ind}}{G_{AC} V_{ind}}, \tag{1}$$

where V_{outd} and V_{ind} are the output and input differential signal, respectively, while G_{AC} is the linear gain of the buffer.

The transfer function of the second stage can be made linear, compressive, or decompressive depending on the value of the bias voltage v_{corr}.

The value of v_{corr} which maximizes the linearity of the buffer across temperature and process corners is shown in Figure 5. The optimum has the same trend with temperature, but the temperature coefficient may be quite different for different process corners. A bias circuit that allows the buffer to work in the optimum condition across PVT is thus not straightforward, and hence a calibration is required.

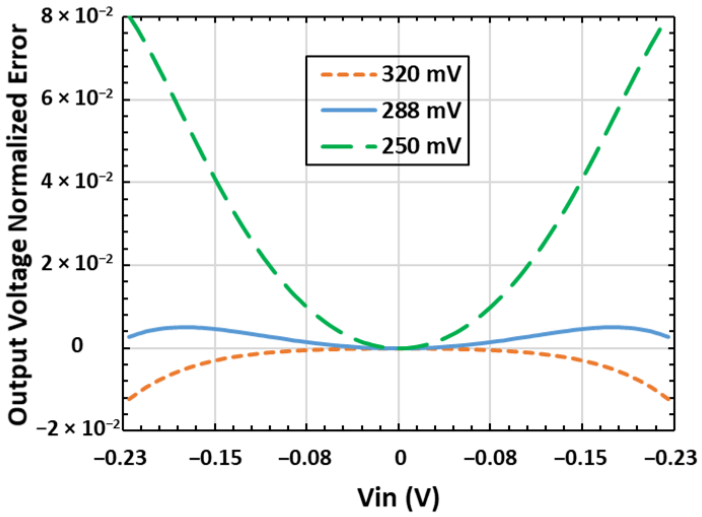


Figure 4. Relative non-linearity error of the second-stage buffer for different values of v_{corr}.

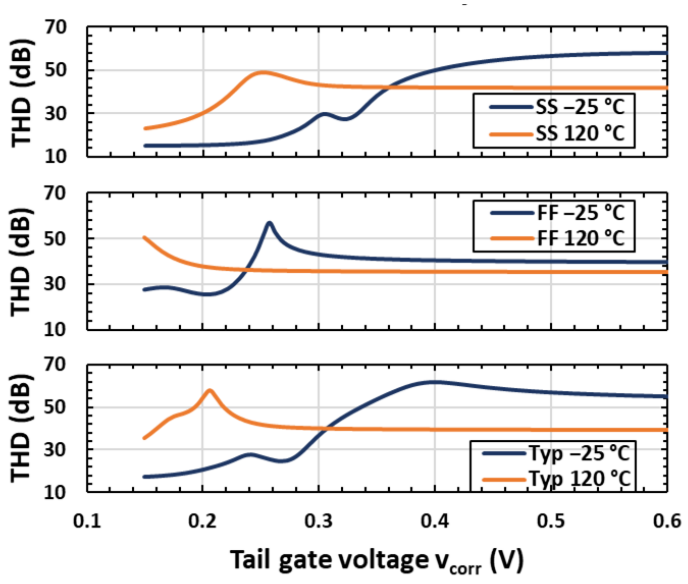


Figure 5. Second-stage buffer linearity characterization for different PVT conditions.

Another observation is that through the correct choice of the second buffer bias point, the non-linearities of the previous or successive stages can be compensated for. To perform this operation, a calibration is required to identify the non-linearity of the analog chain and find the correct value of v_{corr}. This allows maximizing the THD performance of the overall analog front-end.

3. Linearity Calibration Loop

The actual implementation of the linearity calibration loop strongly depends on the system in which the TH circuit is implemented. In this paper, the circuit is employed in a PAM-8 receiver, and a calibration feedback loop suitable for such receivers is presented.

A PAM-8 receiver can be represented using the block diagram in Figure 6. The channel symbol models the transmitter filter, the transmission channel, and the analog front-end of the receiver using their combined impulse response (h_{ch}). The non-linearities of the AFE are modelized in the subsequent block. The transmitted symbols filtered by h_{ch} are then fed to the TH, which is composed of two stages. The non-linear input–output characteristic of the circuits will be described by the coefficients of a Taylor approximation in the developed model as discussed in the next section. Moreover, for the second-stage buffer, the coefficients are dependent on the value of v_{corr}.

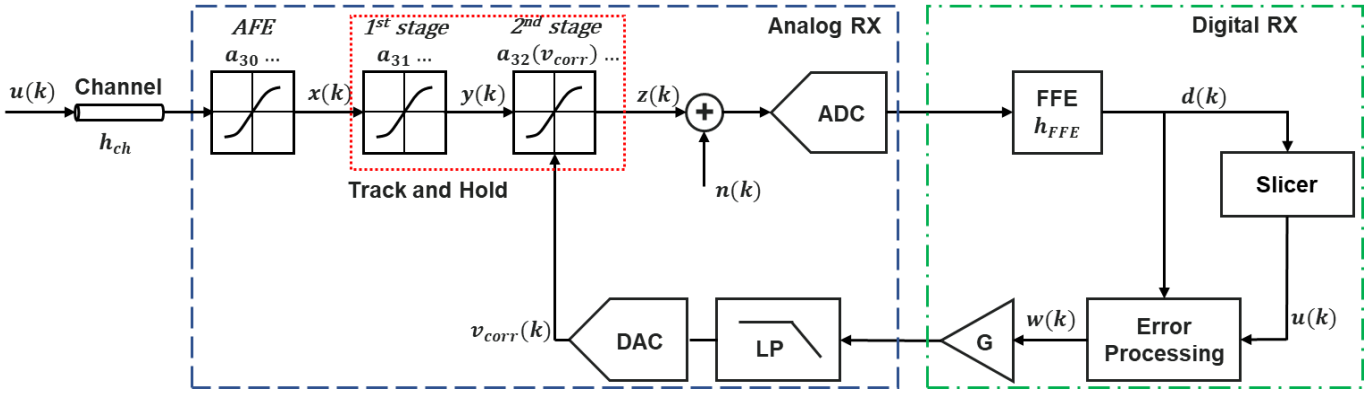


Figure 6. Block diagram of the receiver and of the proposed feedback loop to maximize linearity.

After the second-stage buffer, the equivalent noise of the receiver is added to the samples and the signal is quantized by the ADC. A Feed-Forward Equalizer (FFE) is then used to remove the ISI introduced by the channel. Finally, the slicer makes the hard decisions given the soft decisions as its input. By the proper digital processing of soft and hard decisions, information about the optimum value of v_{corr} can be extracted in order to minimize the receiver non-linearity errors.

The ADC and the DAC used in this model are ideal. Typically, the ADC introduces non-linearities that are neglectable compared to the ones of the track-and-hold circuit, meaning they do not have great impact on the overall system. On the other hand, the DAC does not need to be linear as long as its input–output characteristic is monotone because the feedback loop will drive the DAC to the optimal value of v_{corr}.

3.1. Taylor Approximation Validation

The non-linear input–output characteristic of the second-stage buffer can be analytically described using the Taylor expansion. Neglecting the even terms due to the differential nature of the circuit, the following expression can be written:

$$V_{outd}(t) = \sum_{i=0}^{\infty} a_{2i+1} V_{ind}^{2i+1}(t), \tag{2}$$

where a_1 is the linear gain of the buffer and a_{2i+1} represents the odd-order distortion coefficients. To verify the validity of the analytical model, the relative non-linear error ε_r of the second-stage buffer, obtained through a DC sweep of the input signal, is compared with a polynomial fitting of the characteristic with $i \leq 3$. As shown in Figure 7, the Taylor expansion up to coefficient a_7 gives a good approximation of the non-linear error, as long as the input signal is included in the range between -220 mV and 220 mV. This corresponds to the maximum voltage amplitude allowed by the second stage.

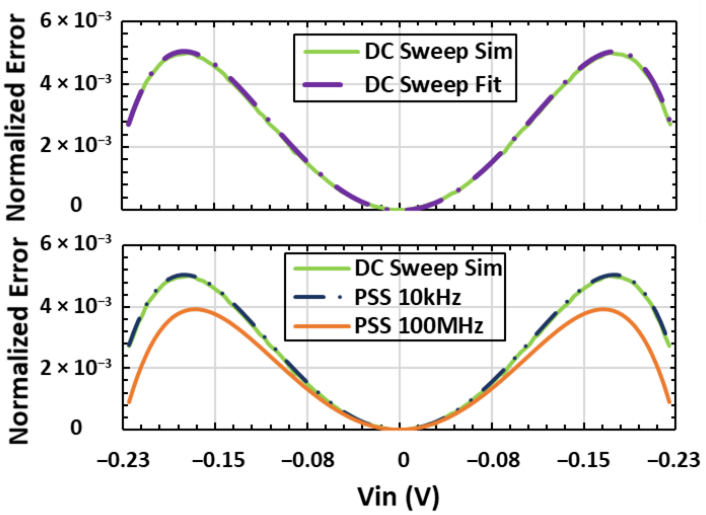


Figure 7. Relative error of the input–output characteristic obtained through DC sweep simulation and polynomial coefficient from DC sweep fitting and from harmonics of PSS simulation.

The polynomial approximation is also verified for different input signal frequencies F_{in}, performing Periodic Steady State (PSS) simulations of the second-stage buffer for F_{in} = 10 kHz and F_{in} = 100 MHz. From the non-linear output of the PSS simulation, the polynomial distortion coefficients a_{2i+1} are calculated (with $i \leq 3$). The relative error arising from the coefficients is then compared to the DC sweep simulation (Figure 7). For an input signal frequency up to 100 MHz, the Taylor expansion described above gives a good approximation of the non-linearities of the second-stage buffer. Higher frequencies were not considered because, as we will see in further sections, a DC characterization of the non-linearity still allows the system to converge to an optimal value of v_{corr}.

3.2. Calibration Loop Operation

Indicating with $u(k)$ the PAM-8 symbols sent by the transmitter, the signal $x(k)$ at the first-stage buffer input is $x(k) = u(k) \otimes h_{ch}(k)$. The signal $z(k)$ at the TH output is then:

$$z(k) = x(k) + a_3x^3(k) + a_5x^5(k) + a_7x^7(k) \tag{3}$$

where a_3, a_5 and a_7 are the coefficients which describe the non-linearities introduced by the cascade of the two buffers and of every component of the AFE chain depicted in Figure 6.

Assuming an optimal FFE, and thus a negligible residual ISI, the signal $d(k)$ at the slicer input can be written as:

$$d(k) = u(k) + a_3u^3(k) + a_5u^5(k) + a_7u^7(k) + n(k) \tag{4}$$

where $n(k)$ is the equivalent thermal and quantization noise of the analog circuit, which has zero mean value.

Assuming the slicer hard decision is equal to the transmitted symbol $u(k)$, the following expression can be obtained by multiplying the slicer error $d(k) - u(k)$ by $u(k)$:

$$w(k) = u(k)\left\{a_3u^3(k) + a_5u^5(k) + a_7u^7(k) + n(k)\right\} \tag{5}$$

The resulting signal $w(k)$ is multiplied by a gain G, low-pass filtered, and fed into a 7b DAC obtaining the correction voltage $v_{corr}(k)$. As the terms with zero mean value are suppressed by the low-pass filtering, the voltage $v_{corr}(k)$ can be expressed in the first approximation as:

$$v_{corr}(k) \approx G\frac{[a_3 + a_5 + a_7]}{2} \tag{6}$$

Therefore, the system can detect the non-linearity coefficients of the TH. The feedback loop will then set the value of v_{corr} to minimize the error induced by such coefficients. The third harmonic of the input signal, whose amplitude H3 is proportional to:

$$H3 \propto 0.8a_3 + a_5 + 1.02a_7 \tag{7}$$

is therefore minimized. This approximation can be obtained by sending a sinusoidal input signal with unitary amplitude $\sin(2\pi f_{in})$. Its Fourier transform can then be calculated after it is distorted by the sampling stages, obtaining:

$$S(f) = -\frac{1}{128}((64 + 48a_3 + 40a_5 + 35a_7)\delta(f - f_{in}) + (16a_3 + 20a_5 + 21a_7)\delta(f - 3f_{in}) + \ldots) \tag{8}$$

By normalizing the coefficient of the third harmonic $H3$, we obtain Equation (7).

In real applications, residual ISI is present even after the FFE. This means that the main cursor is not equal to the transmitted symbol value and therefore it cannot be canceled from the soft decision $d(k)$ by subtracting the slicer output from it. To show this, we can first assume that $a_5,\ a_7 = 0$ for simplicity, and define $h_e = h_{ch} \otimes \mathrm{h_{FFE}}$, with $\sum_i h_e(i) = 1$. If $h_e(1)$ is the impulse response element corresponding to the main cursor, the value of v_{corr} is also dependent on the residual ISI component $(h_e(1) - 1)$ that hides the non-linearities:

$$v_{corr}(k) \approx \frac{G[h_e(1) - 1]}{2} + \frac{Ga_3C_h}{2} \tag{9}$$

where C_h is a coefficient dependent on the channel and FFE. A possible solution to this problem is processing the signal with the method in Figure 8. The errors of N_{post} successive and N_{pre} previous samples are subtracted from $e(k)$, removing the residual main cursor:

$$v_{corr}(k) \approx \frac{G[h_e(0) + h_e(1) + h_e(2) - 1]}{2} + \frac{Ga_3C_h'}{2} = \frac{Ga_3C_h'}{2} \tag{10}$$

The components of the error signal dependent on other samples are filtered due to their lack of correlation with the desired symbol. This method allows a correct operation of the feedback loop without previous knowledge of the channel.

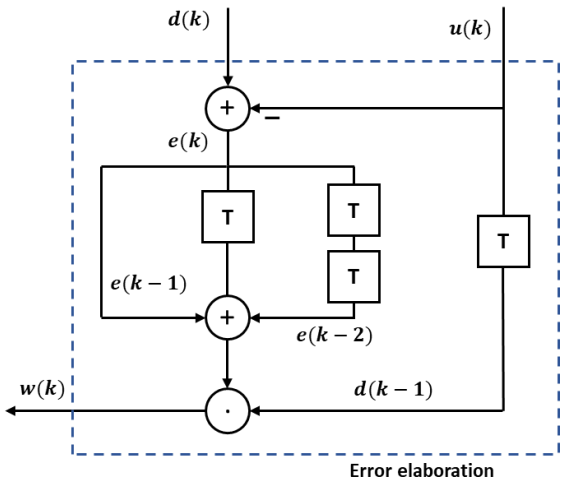


Figure 8. Error processing block to eliminate residual ISI effect (in the example, there is only one precursor and one post-cursor).

4. Simulation Results

To validate the proposed calibration loop, the TH circuit was designed in TSMC 5 nm FinFET technology. The circuit was simulated with parasitic R and C, whose values were derived from actual back annotations. In particular, they are based on previous chip measurements and post-layout simulations, allowing the prediction of the post-layout

behavior with reasonable accuracy. These added R and C take into account both higher and lower metal level contributions. The circuit can operate with a sampling frequency of 60 GS/s with a gain of 6 dB at Nyquist, resulting in an output signal of 505 mV_{ppd}. The power consumption of all the track-and-hold buffers from the 0.93 V voltage supply is 17.2 mW while driving the 64 ADCs load capacitances of 45 fF.

For two different PVT combinations, the distortion coefficients of the TH first and second stages were obtained from circuit-level simulations. These values were used in a MATLAB time-based model PAM-8 RX implementing the loop to derive the expected steady value of v_{corr} for these two scenarios. In the model, the second-stage dependency on $v_{corr}(t)$ is also included and an AFE with ideal linearity was used.

Then, transient simulations of the overall system were performed using an input sinusoidal signal of 252 mV_{ppd} at 1 GHz, with a source resistance of 25 Ω. Figure 9 shows the THD of the TH output as a function of v_{corr} for typical and fast process corner. The maximum linearity of over 50 dB was obtained for a value v_{corr} which almost matches the one obtained through the MATLAB simulation (given the small differences between the circuit and the modeling), meaning that the calibration loop can maximize the linearity of the overall TH circuit.

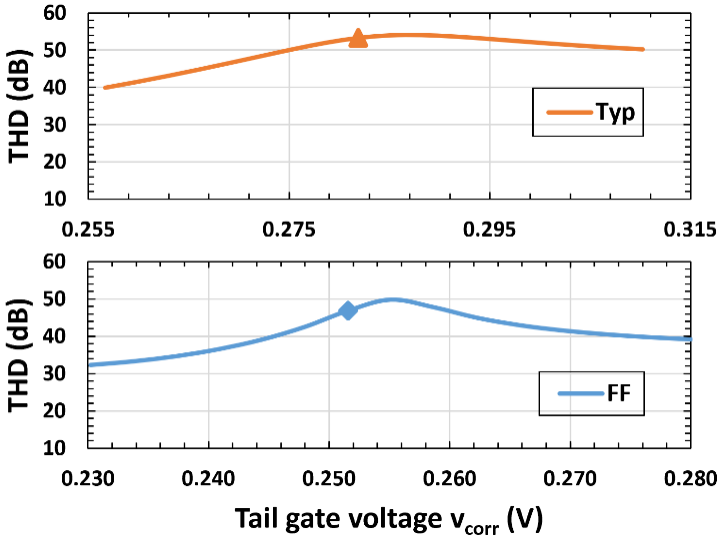


Figure 9. THD of the track-and-hold circuit from transient simulation for typical and fast process corner. The markers denote the v_{corr} voltage obtained by the MATLAB model.

To further validate the performance improvements stemming from the proposed calibration loop, a PAM-8 Pseudo-Random Binary Stream (PRBS) input signal with a −30 dB channel attenuation at Nyquist was used. The signal was sent with two amplitudes, full scale and a tenth of the full scale, obtaining the outputs v_{o1} and v_{o10}. Afterwards, the following operation was performed on the output signals to verify the linearity of the circuit:

$$er_{rms} = rms(v_{o10} - 10 \cdot v_{o1}) \tag{11}$$

The value of the RMS error gives us an assessment of the system linearity with a PRBS input signal. In Figure 10, we can see that the MATLAB model gives us a value of v_{corr} which can almost minimize the RMS error and therefore the non-linearity, even though the model does not include the dynamic non-linearities present in the circuit simulation.

To further validate the proposed linearity calibration technique, the same MATLAB PAM-8 RX model simulation was repeated with the same TH distortion coefficients and adding an AFE with 32 dB and 36 dB THD performance. In these cases, the calibration loop converges to a v_{corr} value that maximizes the overall linearity of the RX chain including the AFE. The resulting MSE at the slicer input shown in Figure 11a shows a behavior of

the calibrated systems akin to the ideal RX linearity case. The same results are visible in Figure 11b, where the SER is very similar to the case in which the RX linearity is ideal.

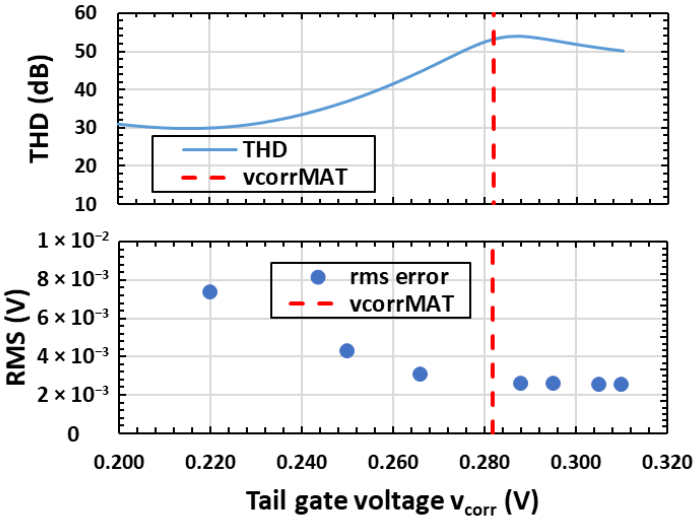
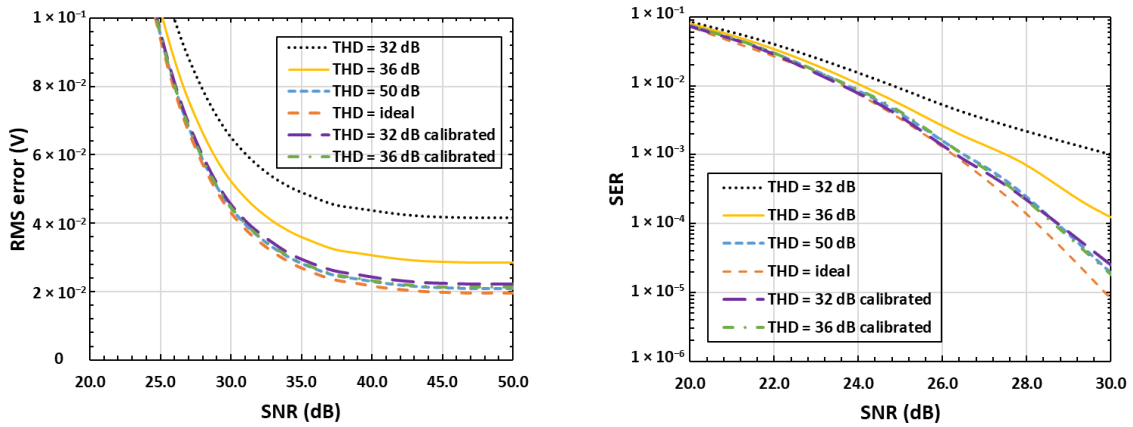


Figure 10. THD of the track-and-hold circuit (**top**) and RMS error given by non-linearities for PRBS input signal (**bottom**) in typical PVT condition.



(**a**) (**b**)

Figure 11. (**a**) MSE (in volts from the ideal reconstruction of the digital values) and (**b**) SER as a function of SNR for different levels of AFE static THD and for two AFE THD values after calibration derived using a MATLAB simulation of a PAM-8 receiver.

5. Conclusions

This paper proposes a 60 GS/s 8 × 8 time-interleaved TH circuit in 5 nm FinFET technology with a gain of 6 dB at Nyquist and tunable non-linearities. A calibration feedback loop for a PAM-8 receiver is proposed and modeled in MATLAB, which allows maximizing the linearity of the TH. From the simulation of the MATLAB model, the voltage calibration bias of the second-stage buffer was extrapolated. Then, the bias voltage was used to perform transistor-level simulations of the analog track-and-hold buffer, obtaining a THD of over 50 dB in typical process corner with a 1 GHz, 252 mV_{ppd} sinusoidal input. The linearity of the system was also verified using a PAM-8 pseudorandom stream signal showing that the RMS error is indeed minimized. Lastly, the MATLAB simulation of the PAM-8 RX with a 36 dB THD AFE model shows the possibility of using this calibration technique to compensate for AFE non-linearities as well. In future works, the performances of the pro-

posed TH circuit and calibration loop will be further verified using post-layout simulations and HDL implementation, respectively, and eventually with silicon implementation.

Author Contributions: Conceptualization, A.D.P., E.M. and N.G.; methodology, A.D.P., E.M., N.G. and C.N.; validation, A.D.P., E.M., N.G. and C.N.; formal analysis, A.D.P., E.M., N.G. and C.N.; investigation, A.D.P., E.M. and N.G.; data curation, A.D.P.; writing—original draft preparation, A.D.P.; writing—review and editing, A.D.P., E.M., N.G., C.N. and L.F.; supervision, C.N. and L.F. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Bailey, J.; Shakiba, H.; Nir, E.; Marderfeld, G.; Krotnev, P.; LaCroix, M.-A.; Cassan, D.; Tonietto, D. A 112-Gb/s PAM-4 Low-Power Nine-Tap Sliding-Block DFE in a 7-nm FinFET Wireline Receiver. *IEEE J. Solid-State Circuits* **2021**, *57*, 32–43. [CrossRef]
2. Krupnik, Y.; Perelman, Y.; Levin, I.; Sanhedrai, Y.; Eitan, R.; Khairi, A.; Landau, Y.; Virobnik, U.; Dolev, N.; Meisler, A.; et al. 112 Gb/s PAM4 ADC Based SERDES Receiver for Long-Reach Channels in 10nm Process. In Proceedings of the 2019 Symposium on VLSI Circuits, Kyoto, Japan, 9–14 June 2019. [CrossRef]
3. Pisati, M.; Minuti, A.; Bollati, G.; Giunco, F.; Massolini, R.G.; Cesura, G.; De Bernardinis, F.; Pascale, P.; Nani, C.; Ghittori, N.; et al. A 243-mW 1.25–56-Gb/s Continuous Range PAM-4 42.5-dB IL ADC/DAC-Based Transceiver in 7-nm FinFET. *IEEE J. Solid-State Circuits* **2019**, *55*, 6–18. [CrossRef]
4. Foley, D.; Flynn, M. A low-power 8-PAM serial transceiver in 0.5-µm digital CMOS. *IEEE J. Solid-State Circuits* **2002**, *37*, 310–316. [CrossRef]
5. Chong, E.; Musa, F.A.; Mustafa, A.N.; Gao, T.; Krotnev, P.; Soreefan, R.; Xin, Q.; Madeira, P.; Tonietto, D. A 112 Gb/s PAM-4, 168 Gb/s PAM-8 7 bit DAC-Based Transmitter in 7nm FinFET. In Proceedings of the ESSCIRC 2021—IEEE 47th European Solid State Circuits Conference (ESSCIRC), Grenoble, France, 13–22 September 2021; pp. 523–526. [CrossRef]
6. Chun, Y.; Megahed, M.; Ramachandran, A.; Anand, T. A PAM-8 Wireline Transceiver with Linearity Improvement Technique and a Time-Domain Receiver Side FFE in 65 nm CMOS. *IEEE J. Solid-State Circuits* **2022**, *57*, 1527–1541. [CrossRef]
7. Megahed, M.; Chun, Y.; Wang, Z.; Anand, T. A 27 Gb/s 5.39 pJ/bit 8-ary Modulated Wireline Transceiver Using Pulse Width and Amplitude Modulation Achieving 9.5 dB SNR Improvement over PAM-8. In Proceedings of the 2021 Symposium on VLSI Circuits, Kyoto, Japan, 13–19 June 2021. [CrossRef]
8. Li, J.; Wu, S.; Liu, Y.; Ning, N.; Yu, Q. A Digital Timing Mismatch Calibration Technique in Time-Interleaved ADCs. *IEEE Trans. Circuits Syst. II Express Briefs* **2014**, *61*, 486–490. [CrossRef]
9. Hung, T.-C.; Liao, F.-W.; Kuo, T.-H. A 12-Bit Time-Interleaved 400-MS/s Pipelined ADC With Split-ADC Digital Background Calibration in 4000 Conversions/Channel. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1810–1814. [CrossRef]
10. Zhao, H.; Diaz, J.C.G.; Hoyos, S. Multi-Channel Receiver Nonlinearity Cancellation Using Channel Speculation Passing Algorithm. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *69*, 599–603. [CrossRef]
11. Bocco, A.F.; Solis, F.; Reyes, B.T.; Morero, D.A.; Hueda, M.R. Background Compensation of Static TI-ADC Nonlinearities in Coherent Optical Receivers. In Proceedings of the 2021 Argentine Conference on Electronics (CAE), Bahia Blanca, Argentina, 11–12 March 2021; pp. 45–49. [CrossRef]
12. Di Pasquo, A.; Nani, C.; Monaco, E.; Fanucci, L. A High Linearity Driver with Embedded Interleaved Track-and-Hold Array for High-Speed ADC. In Proceedings of the 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 22–28 May 2021; pp. 1–5. [CrossRef]
13. Mattia, O.E.; Murmann, B. 80 GS/s 5.5 ENOB time-interleaved inverter-based CMOS track-and-hold. *Electron. Lett.* **2020**, *56*, 328–329. [CrossRef]
14. Zheng, K.; Frans, Y.; Ambatipudi, S.L.; Asuncion, S.; Reddy, H.T.; Chang, K.; Murmann, B. An Inverter-Based Analog Front-End for a 56-Gb/s PAM-4 Wireline Transceiver in 16-nm CMOS. *IEEE Solid-State Circuits Lett.* **2019**, *1*, 249–252. [CrossRef]