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Experimental Realization of 16-Pixel Terahertz Receiver Front-End Based on Bulk Silicon MEMS Power Divider and AlGaIn/GaN HEMT Linear Detector Array

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Abstract: A 16-pixel terahertz (THz) receiver front-end working at room temperature was designed, built, and measured in this paper. The designed receiver front-end is based on the antenna-coupled AlGaIn/GaN high-electron-mobility transistor (HEMT) THz linear detector array (TeraLDA) and a 16-way THz power divider. The local oscillator (LO) signal is divided by the power divider into 16 ways and transmits to the TeraLDA. Each detector contains a planar unified antenna printed on a 150 μm -thick sapphire substrate and a transistor fabricated on AlGaIn/GaN heterostructure. There are 16 silicon hemispheric lenses located on the TeraLDA to increase the responsivity of the TeraLDA. The focus of each lens is aligned in the center of the TeraLDA pixels. Depending on different read out circuits, the receiver front-end could work in homodyne and heterodyne modes. The 16-way power divider is a four-stage power divider that consists of fifteen same 2-way dividers, and was fabricated by bulk silicon microelectromechanical systems (MEMS) technology to achieve low insertion loss (IL). This designed receiver front-end could be a key component of a THz coherent focal plane imaging radar system, that may play a crucial role in nondestructive 3D imaging application.

Keywords: terahertz; receiver front-end; power divider; waveguide; heterodyne; MEMS

1. Introduction

The terahertz (THz) wave is an electromagnetic wave that lies between infrared light and millimeter wave. Comparing with the millimeter wave at frequencies between 30 and 300 GHz, THz wave has a higher bandwidth leading to a better resolution in imaging system. In contrast to the light beyond 10 THz, THz waves can penetrate non-polar, non-conducting materials such as clothing, paper, masonry, or plastic, which give rise to THz imaging systems will play a key role in non-destructive imaging applications, such as, human imaging [1] or cloud and rain detection [2].

Terahertz imaging is currently being performed using both non-coherent and heterodyne coherent methods [3]. Coherent radar systems illuminate the subjects with THz radiation and detect the echo signals using heterodyne configuration, whereas non-coherent radar systems merely receive the reflected THz radiation or the naturally occurring radiation from the subject. Heterodyne coherent detection has a excellent frequency resolution,

which can obtain more targets' information through the echo signals' frequency and phase, and great prospects in the fields of THz astronomy and THz imaging, etc.

Currently, THz non-coherent (homodyne) focal plane array (FPA) imaging radar system is well-developed as a result of that the large-scaled homodyne FPA have a ready solution of array and silicon readout circuit [4–6]. There are 8712 detectors in a FPA with the dimensions of $100 \times 200 \text{ cm}^2$ in [7].

For heterodyne coherent FPA, there are many challenges in developing large-scale FPAs. The main issues relating to the FPA architecture are the mixer array, local oscillator (LO) power injection, and the readout circuit. For heterodyne FPA imaging radar system, transmitting same amplitude and in-phase LO power to detectors is difficult for quasi-optical feeding method. Feeding LO signals to detectors by power divider tends to perform better. There are some cooled heterodyne FPAs in THz astronomy [8–10]. However, the high complexity of such systems, which operate in low-temperature environments, prevents them from being widely used.

A CMOS solution in room temperature had been proposed in [11]; the 32-unit array consists of mixers, THz LO sources, and intermediate frequency (IF) multiplexers in-pixel. An 8-pixel 340 GHz mixer array worked for standoff personnel screening was reported in [12] with pixel-to-pixel spacing of 12 mm.

At present, air-filled rectangular waveguide (RWG) is a mainly structure to design high-performance low-loss transmission lines, couplers, or dividers in THz band. In THz band, silicon micromachined waveguide technology offers a number of advantages for fabrication of the air-filled RWG [13–15]. Several waveguide power dividers had been manufactured with silicon micromachined technology [16–18] with 2-way or 4-way.

In this work, a 16-pixel THz heterodyne receiver front-end working at room temperature was designed, built, and characterized. The designed receiver front-end consists of silicon lens array, antenna-coupled AlGaIn/GaN high-electron-mobility transistor (HEMT) THz linear detector array (TeraLDA), and a 16-way MEMS power divider. The design details of the proposed TeraLDA and the MEMS power divider, and the measurement and experiment results are presented.

This paper is organized as follows: Section 2 explains the architecture of the proposed terahertz heterodyne receiver front-end. Section 3 introduces the design of the THz linear detector array. Section 4 describes the design of the MEMS power divider. Section 5 illustrates the assembly and experimental results. Finally, Section 6 concludes this work.

2. The 16-Pixel Terahertz Receiver Front-End Architecture

The receiver front-end is a key part of a THz radar system, used in multi-target tracking and imaging systems. The front-end is placed in the focal plane of a multi-beam reflector antenna. The off-axial defocusing of the reflector antenna can produce multiple high-gain fixed beams with different directions, which cover a one-dimensional field of view and could significantly increase the imaging speed of the system.

Figure 1 shows the architecture of the proposed terahertz heterodyne receiver front-end, which includes a hemispheric silicon lens array, a 16-pixel TeraLDA and a 16-way THz MEMS power divider. The hemispheric silicon lens array is used to focus the incident THz beam to enhance the TeraLDA responsivity. The pixel of the TeraLDA is the antenna-coupled AlGaIn/GaN HEMT heterodyne detectors, which are designed based on the localized mixing model and a unified antenna [19]. The 16-way power divider which fabricated by bulk-silicon MEMS technology is used to split the LO signal into 16 ways and transmits the LO signal to each pixel of the TeraLDA. The proposed receiver front-end is able to work in homodyne and heterodyne modes, depending on the read-out circuit and IF amplification chains. This proposed receiver front-end design is simple in structure, and easy to implement and assemble.

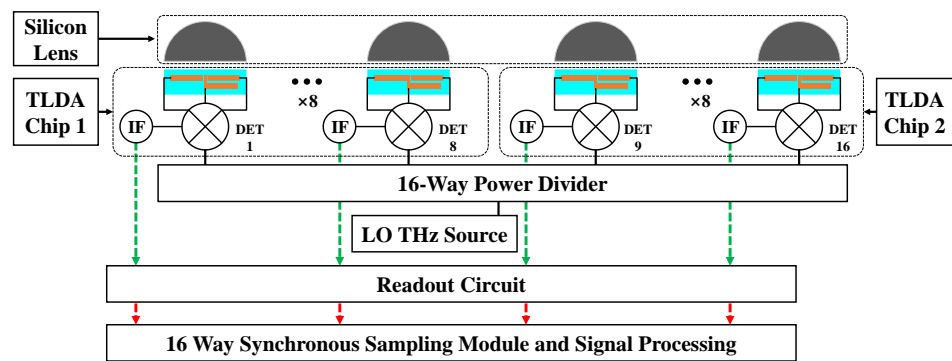


Figure 1. The architecture of the proposed terahertz heterodyne receiver front-end.

3. Theory and Design of the TeraLDA Based on HEMT

3.1. The Pixel Detector and TeraLDA Design

The THz antenna-coupled AlGaIn/GaN HEMT detector is designed based on the localized mixing model and is manufactured from the AlGaIn/GaN heterostructure. Due to spontaneous and piezoelectric polarizations in the AlGaIn/GaN heterostructure, two-dimensional electron gas (2DEG) is generated 25 nm below the surface. The proposed detector consists of an asymmetric antenna and HEMT that was connected to the antenna. The asymmetrical antenna is made up of three $\lambda/4$ monopole antennas. They are connected to the HEMT source, drain, and gate, as shown in Figure 2a. This kind of antenna will generate an induced electric field under the surface. The asymmetry of the electric field will drive the 2DEG to generate photoresponse. Detail studies of the principle of the THz photoresponse under the gate were depicted in our previous work [20,21].

Each TeraLDA pixel consists of two HEMT detectors, as shown in the enlarged view of Figure 2b. According to the localized mixing model, the pair of two rotationally symmetrical HEMT detectors will generate the differential signals. The differential signals are amplified by differential amplifier in read-out circuit to suppress the common-mode noise and increase the responsivity.

Based the antenna principle and the localized mixing model, the optimal antenna length is $A = 130 \mu\text{m}$, the width is $W = 12 \mu\text{m}$. The gap between the gate and source is $D = 600 \text{ nm}$, and the gate length is $L = 600 \text{ nm}$, which were limited by the fabrication process. In this work, the whole 16-pixel TeraLDA was divided into two 8-pixel TeraLDAs to reduce production difficulties. Figure 2b shows the optical microscope image of the 8-pixel TeraLDA chip.

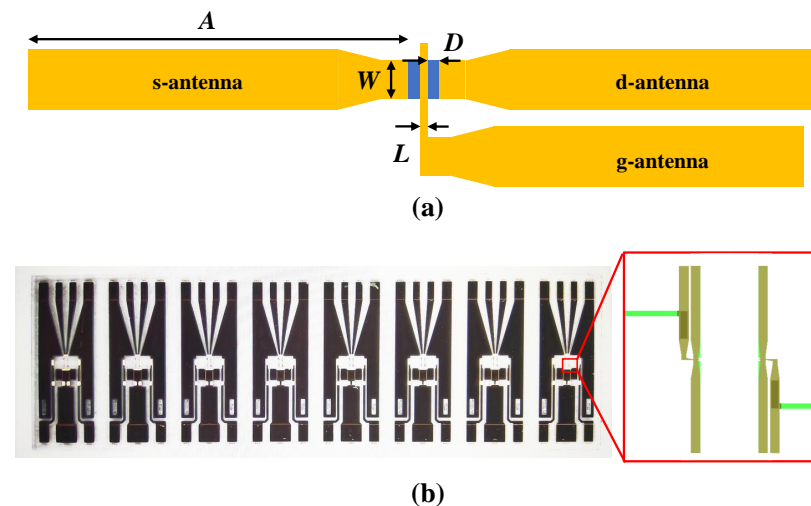


Figure 2. (a) The top view of the pixel of the TeraLDA. (b) Optical microscope image of the 8-pixel TeraLDA chip.

3.2. The Design of the Silicon Lens Array

Due to the 2 mm gap between the pixel detectors and the pixel detector planar size of $265 \mu\text{m} \times 30 \mu\text{m}$, the TeraLDA chip can only receive a small fraction of the terahertz echo signal. Therefore, the hemispheric silicon lenses with a diameter of 2 mm are used to focus the THz beam onto the TeraLDA chip pixel. The each silicon lens is located on the center of THz each pixel detector.

A commercial electromagnetic (EM) simulation software CST Studio Suite CST was used to carry out the simulation and verify the validity of the silicon lens. Figure 3 shows the simulation model and the results of a single TeraLDA pixel with an integrated silicon lens. The strength of the incident THz plane wave in the CST is set to 1 V/m. Based on the EM simulation, the average electric field strength at the THz detectors' antenna is increased by a factor of about 6 with respect to the electric field strength of the incident THz plane wave. The largest factor of more than 16 could be found near the waveguide wall in Figure 3. It can be seen that the silicon lens placed in front of the TeraLDA could significantly increase the detector's ability to receive incident terahertz energy.

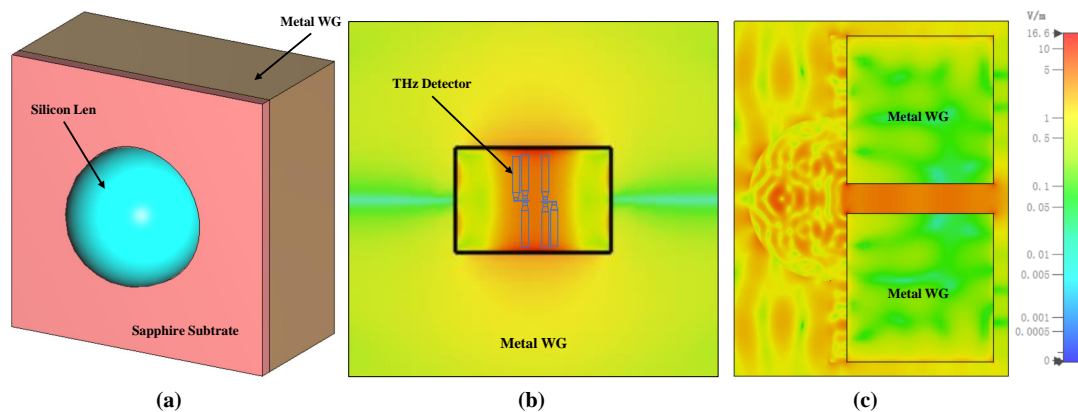


Figure 3. (a) The simulated model in CST, which consists of silicon lens, sapphire substrate and metal waveguide. (b) The electric field distribution on the surface of THz detector. (c) The electric field distribution on the E-plane of the metal waveguide.

3.3. Terahertz HEMT Detector Fabrication Process

The TeraLDA were fabricated based on ultraviolet lithography technology using the AlGaIn/GaN heterostructure, which is grown by metal organic chemical vapor deposition (MOCVD) on a 2 inch sapphire substrate. Figure 4 shows the complete fabrication process of the THz HEMT detector. The main processes are as follows.

1. Titanium tungsten (TiW) alloys are grown on the wafer surface as lithographic alignment markers using magnetron sputtering technology.
2. Using fluorine ion implantation to destroy the 2DEG outside the transistor channel region to form the active region.
3. Four metal layers of Ti, Al, Ni and Au are grown sequentially in source and drain regions using electron-beam evaporation technology and annealed at 880°C under nitrogen atmosphere to form ohmic contact for connecting the active region and the electrodes.
4. Growth of Ni and Au by electron-beam evaporation to build the gate to modulate 2DEG and antennas to receive terahertz radiation.
5. Thickening of Ni and Au metal in the bonding area to prevent destroying the metal during packaging.

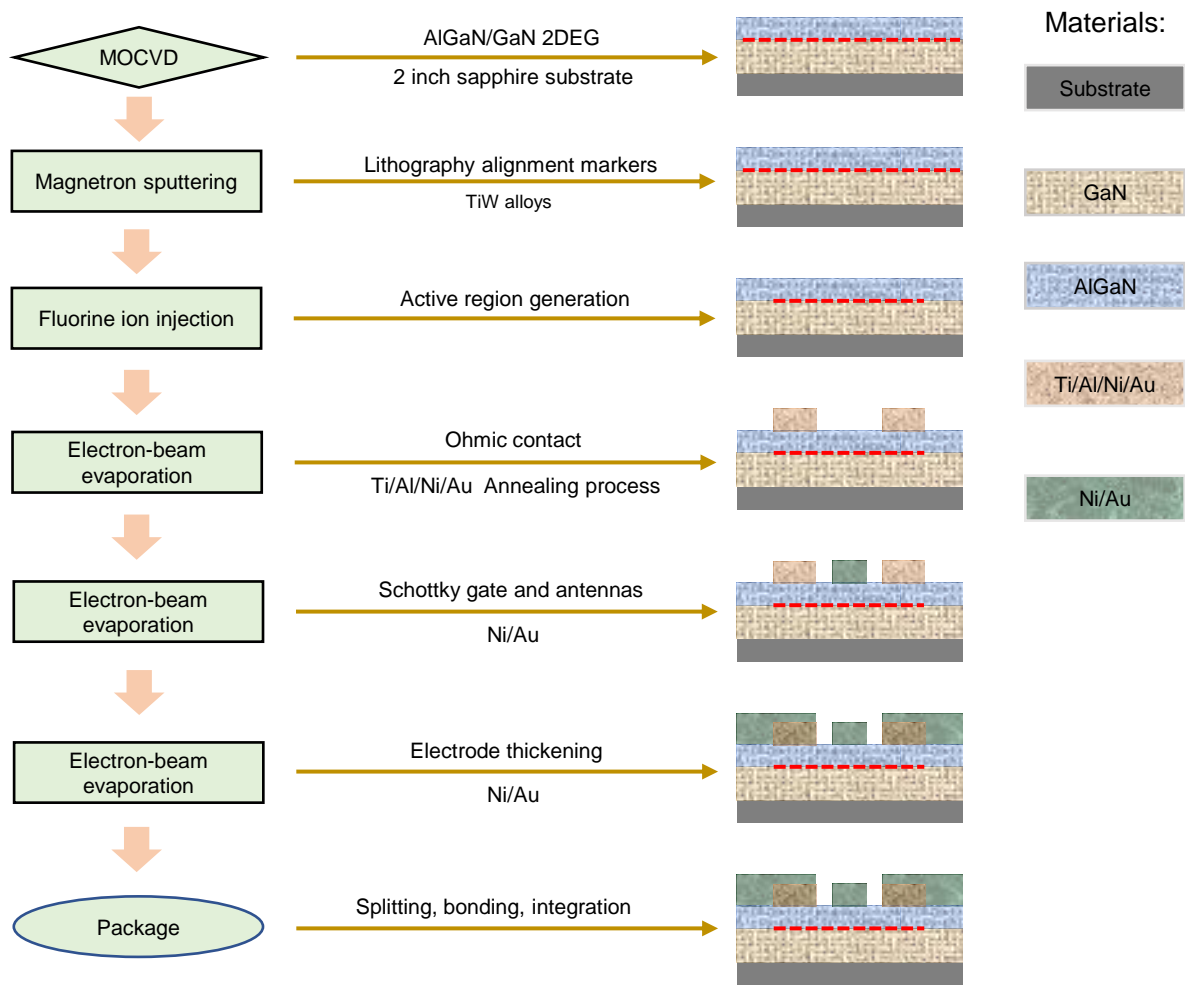


Figure 4. Schematic of the complete fabrication process of the THz HEMT detector.

3.4. Measurements and Results

The current–voltage (I – V) curves measurement was carried out first to check whether the HEMT detector was working properly, especially to check if the gate control is normal. For I – V measurement, the drain was biased to a small voltage (10 mV) by source measure unit (Keithley 2400) and the gate was biased to a specific gate voltage while the source was grounded. Figure 5 shows the results of the source-drain conductance.

From Figure 5, it can be seen that the electrical performance of the array detector chip is normal, with a good conductivity consistency of the 16 array pixels and operating voltages range from -3.84 V to -3.98 V.

Table 1 shows the comparison of the theoretical noise of 16 detector channels at a gate voltage of -3.90 V with the noise measured by the FFT spectrum analyzer (Stanford Research SR770). From Table 1, it can be found that the noise of DET 1 and DET 16 is much higher than the theoretical noise, while the theoretical and measured noise of other channels is comparable.

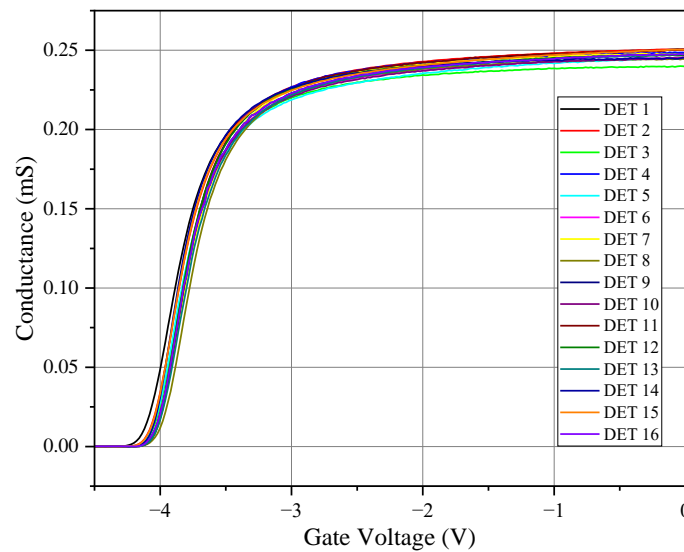


Figure 5. The conductance of the 16 pixels of the TeraLDA.

Table 1. Comparison of the theoretical noise and the measured noise.

Detector	Theoretical Thermal Noise	Measured Thermal Noise
DET 1	22.4 nV/Hz ^{1/2}	33.2 nV/Hz ^{1/2}
DET 2	22.9 nV/Hz ^{1/2}	24.1 nV/Hz ^{1/2}
DET 3	25.9 nV/Hz ^{1/2}	28.4 nV/Hz ^{1/2}
DET 4	23.0 nV/Hz ^{1/2}	25.9 nV/Hz ^{1/2}
DET 5	24.5 nV/Hz ^{1/2}	25.2 nV/Hz ^{1/2}
DET 6	23.2 nV/Hz ^{1/2}	26.2 nV/Hz ^{1/2}
DET 7	21.8 nV/Hz ^{1/2}	24.1 nV/Hz ^{1/2}
DET 8	25.0 nV/Hz ^{1/2}	28.0 nV/Hz ^{1/2}
DET 9	18.2 nV/Hz ^{1/2}	23.5 nV/Hz ^{1/2}
DET 10	19.3 nV/Hz ^{1/2}	23.2 nV/Hz ^{1/2}
DET 11	18.2 nV/Hz ^{1/2}	23.8 nV/Hz ^{1/2}
DET 12	18.5 nV/Hz ^{1/2}	26.5 nV/Hz ^{1/2}
DET 13	19.3 nV/Hz ^{1/2}	22.9 nV/Hz ^{1/2}
DET 14	19.2 nV/Hz ^{1/2}	26.7 nV/Hz ^{1/2}
DET 15	19.5 nV/Hz ^{1/2}	24.9 nV/Hz ^{1/2}
DET 16	17.8 nV/Hz ^{1/2}	38.1 nV/Hz ^{1/2}

4. Theory and Design Process of The MEMS Power Divider

4.1. Overall Design

The silicon-based semiconductor process, which has emerged in recent years, has a large number of terahertz devices made by this process because of its excellent dimensional control capability, good conductor surface roughness. However, there are some design limitations. The layer thickness of the wafer cannot be arbitrary, and the edges of the MEMS chip are relatively rough due to the scribing process. By avoid the above disadvantages, we designed and fabricated a 16-way MEMS power divider. The proposed power divider was constructed by three fundamental units: the waveguide H-plane Tee junction (T-junction) 2-way power divider, transition between standard RWG and non-standard waveguide, and the 90° waveguide bend. All three units are designed to operate in a wide frequency range. The fundamental T-junction 2-way power divider can be cascaded to achieve 16 output ports. The designed power divider has simple geometrical features for MEMS fabrication.

The geometry of this 16-way power divider is illustrated in Figure 6. The LO signal inputted from Input RWG port is divided into 16 ways, and outputs from output RWG ports. The 16 output ports are arranged at equal intervals of 2 mm.

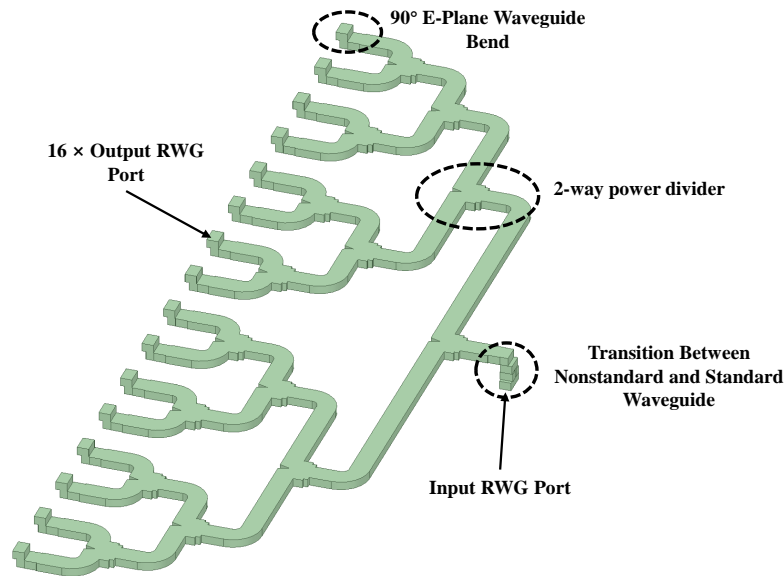


Figure 6. The complete 16-way power divider design.

4.2. Design of 2-Way Power Divider

The designed waveguide power divider is shown in Figure 7a. The waveguide 2-way divider is an H-plane T-junction. The H-plane T-junction was chosen rather than E-plane T-junction is that the output signals are in phase, while they would be out of phase in an E-plane design. The H-plane T-junction is matched by shaping the walls with multi-step and triangular protrusion at the symmetry plane. The multi-step impedance transformation is also used to achieve a broadband match to the output ports.

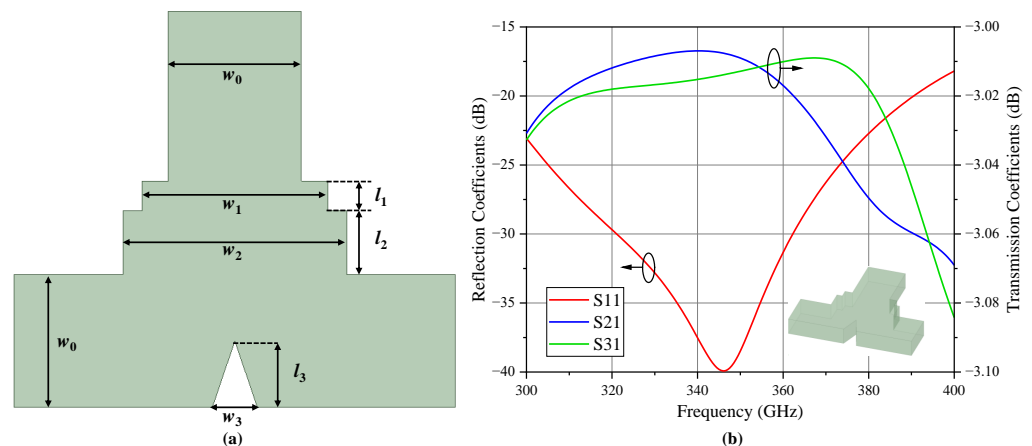


Figure 7. (a) The configuration of the 2-way waveguide power divider. (b) The simulation resulted of the above power divider.

Due to the limitations of the fabrication process, the thickness of each silicon substrate is 260 μm , which includes silicon wafer (250 μm), gold layer (3 μm each side) and bonding layer (2 μm each side). The size of the waveguide is not standard waveguide to match the width of the 90° E-Plane waveguide bend, that its size is 604 $\mu\text{m} \times 260 \mu\text{m}$. The operating range of the nonstandard waveguide is 310.2 to 469.0 GHz. The optimal dimensions of the 2-way power divider are: $w_0 = 604 \mu\text{m}$, $w_1 = 844 \mu\text{m}$, $w_2 = 1016 \mu\text{m}$,

$w_3 = 205 \mu\text{m}$, $l_1 = 135 \mu\text{m}$, $l_2 = 290 \mu\text{m}$, $l_3 = 302 \mu\text{m}$. Figure 7b shows its simulated S-parameters. The passive devices are reciprocal, which means that the transmission of a signal between any two ports does not depend on the direction of propagation, the input and output ports are interchangeable. Therefore, the scattering parameters are equal to their corresponding transposes, such as $S_{12} = S_{21}$. In follow S-parameters results, the S_{12} will be hidden for clarity. The simulated return loss is less than -20 dB in 300–380 GHz. The simulated results show good electrical performance around 340 GHz. Based on the H-plane T-junction power divider, an 16-way power divider can be designed.

4.3. Design of the 90° E-Plane Waveguide Bend and the Transition between Nonstandard and Standard Waveguide

For the proposed 16-way power divider, the RWG ports are located on the top and bottom plate of the MEMS stack. A transition was designed to couple the EM wave that passes through the divider to the output ports. For the input and output from the MEMS chip surface, a 90° WG bend was designed. Because the layer thickness of the silicon substrate is only $260 \mu\text{m}$, which differs from the height of the standard WR-2.8 RWG. Therefore, for the impedance matching, the broad wall width of the transition is reduced to $535 \mu\text{m}$.

Full-wave EM simulation of the bend transition design was performed with HFSS. the optimal dimensions are obtained as $w_1 = 535 \mu\text{m}$, $w_2 = 560 \mu\text{m}$, $w_3 = 604 \mu\text{m}$, $l_0 = 125 \mu\text{m}$, $l_1 = 250 \mu\text{m}$, $l_2 = 370 \mu\text{m}$, $l_3 = 300 \mu\text{m}$. Figure 8a shows the configuration of the transition. Figure 8b shows the the simulated S-parameters results. The return loss is less than -15 dB and the insertion loss is better than -0.15 dB from 300 to 380 GHz.

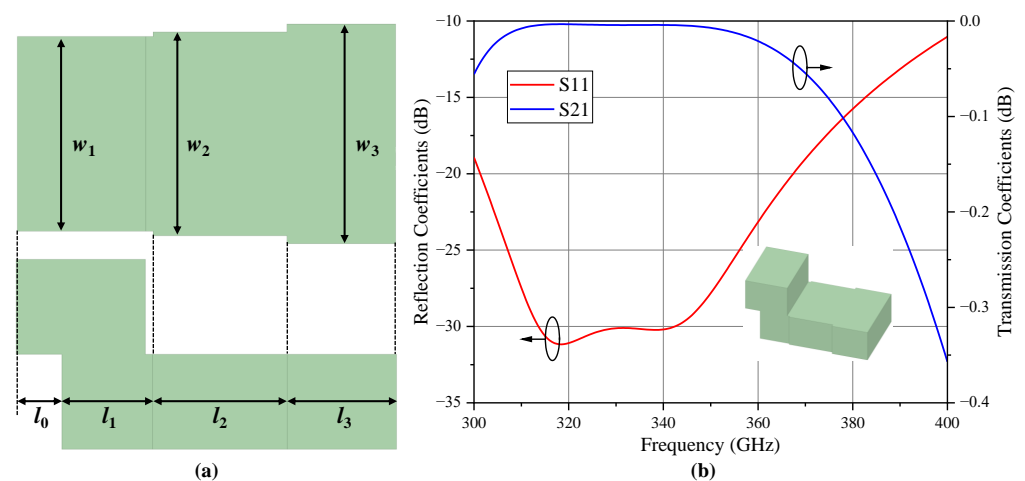


Figure 8. (a) The configuration of the proposed 90° E-plane waveguide bend. (b) The S-parameters simulation results of the 90° E-plane waveguide bend.

Figure 9a shows the configuration of the transition between nonstandard and standard waveguide. Figure 9b shows the simulation results for the S-parameters. The optimal dimensions are obtained as $w_1 = 710 \mu\text{m}$, $w_2 = 500 \mu\text{m}$, $w_3 = 550 \mu\text{m}$, $w_d = 65 \mu\text{m}$, $h_d = 59 \mu\text{m}$, $h_1 = 355 \mu\text{m}$, $h_2 = 400 \mu\text{m}$. The return loss is less than -15 dB and the insertion loss is better than -0.15 dB from 300 to 380 GHz.

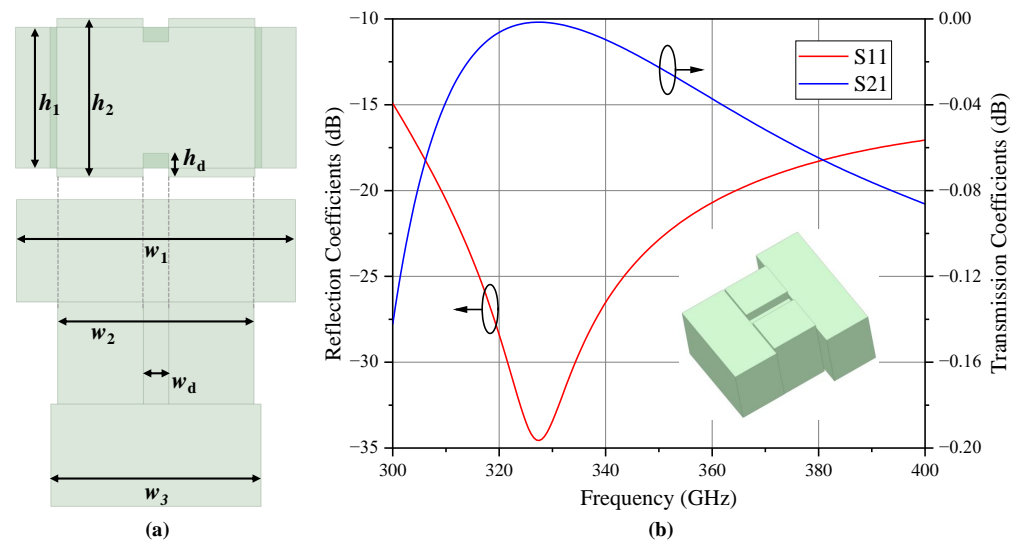


Figure 9. (a) The configuration of the transition between nonstandard and standard waveguide. (b) The S-parameters simulation results of the above waveguide transition.

Based on the 2-way T-junction power divider, the 90° E-plane waveguide bend and the transitions, a 16-way power divider was designed. The 16 output ports are arranged at equal intervals (2 mm). Figure 10 shows the simulated S-parameters of the power divider. It can be seen that S11 is better than -10 dB in 300 GHz to 380 GHz, and the 16 outputs are in-phase and with same magnitude.

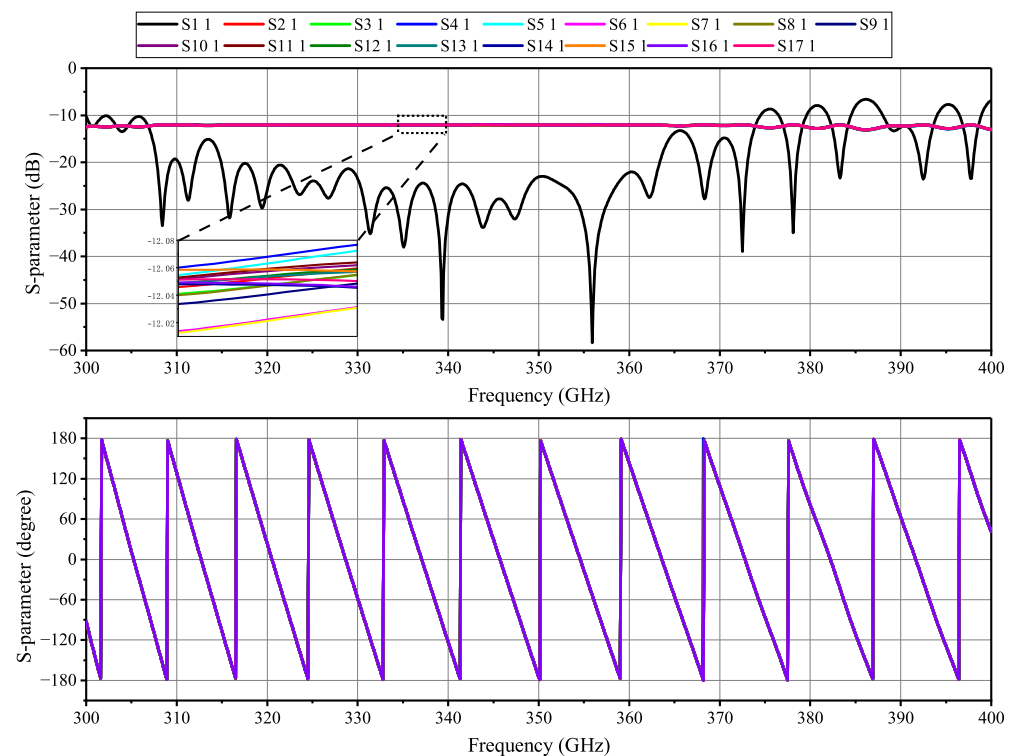


Figure 10. The S-parameters simulation results of the designed 16-way power divider.

4.4. MEMS Fabrication Process

The proposed divider has been fabricated using bulk silicon MEMS technology. The main process flow is as follows, shown in Figure 11:

I. A 6-inch high-resistance silicon (the deep gray layer in Figure 11) was selected as the substrate with resistivity of $10,000\sim 20,000 \Omega \cdot \text{cm}^2$.

II. After surface treatment, the passivation layer (the green layer in Figure 11) SiO_2 of thickness $1\sim 2\ \mu\text{m}$ was prepared on the wafer.

III–IV. The needed patterns were built on passivation layer by photolithography and buffered oxide etching (BOE) techniques. The black layer in Figure 11 III represents the mask. The blue arrows indicate the deep UV light.

V. The potassium hydroxide (KOH) etching process was used to remove the corresponding part of the silicon wafer in $50\ ^\circ\text{C}$.

VI. The remaining SiO_2 layers are removed by BOE and wet etching process.

VII. The metal seed layer (Cr/Au) is prepared by a sputtering process, and the $3\ \mu\text{m}$ thick metal patterns have been achieved by an electroplating process.

VIII. Multi-layer silicon wafers are bonded together using a hot pressing process.

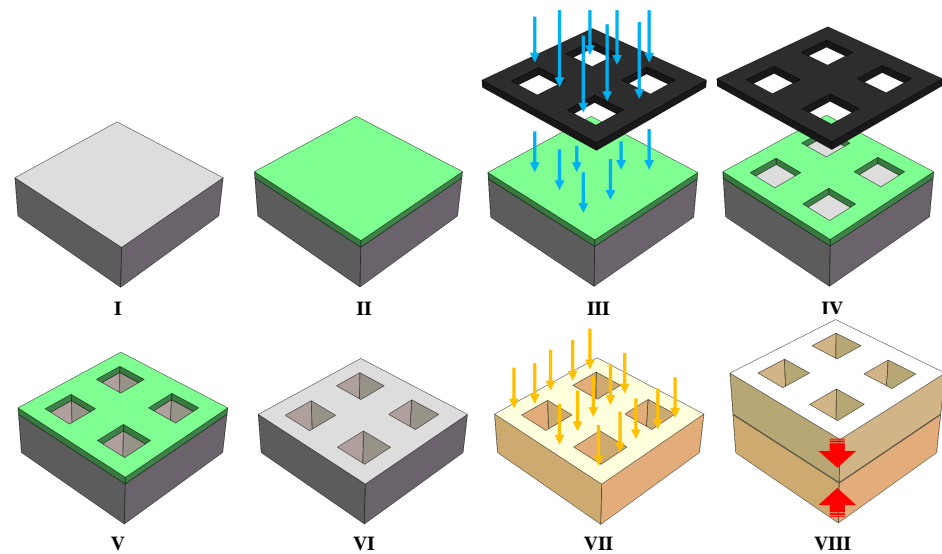


Figure 11. Fabrication process for the MEMS waveguide power divider.

Finally, the multi-layer silicon wafer is cut through a wafer dicing system.

According to the MEMS process, the power divider was divided into five same-thickness layers. Figure 12 depicts the geometry of the proposed 16-way power divider.

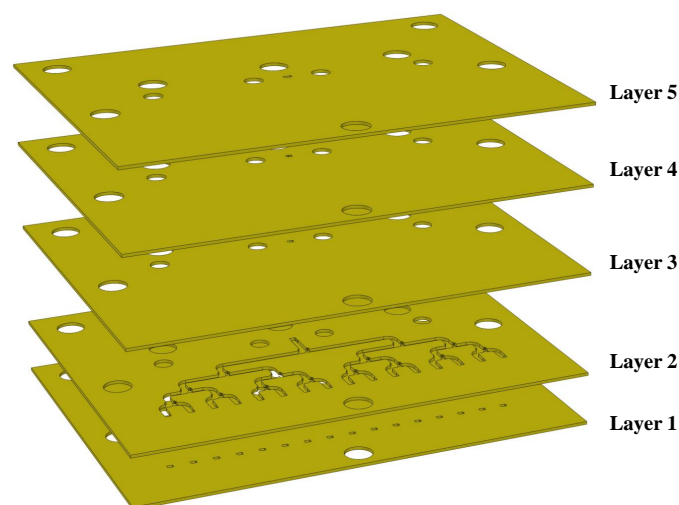


Figure 12. Exploded view of the five-chip stack forming the 16-way power divider.

Layer 1 contains 16 output ports whose sizes are non-standard, which also work as parts of the 90° transitions. Layer 2 is the air-filled 16-way RWG power divider, which

contains four stages 2-way power divider. Layer 3 contains input port whose size is non-standard, which also works as parts of the 90° transitions. Layer 4 contains the transition between the non-standard waveguide and the standard waveguide. Layer 5 contains a standard WR-2.8 waveguide as input port of the 16-way power divider.

Figure 13a,b show the photographs of the fabricated MEMS 16-way power divider and the enlarged views of the waveguide ports. The enlarged views were captured by Nikon SMZ25, the measured w_{rg1} is $712\ \mu\text{m}$ and w_{rg2} is $353.8\ \mu\text{m}$. Because the power divider needs to assemble with flange of the feeding waveguide, some holes are designed for location pins and screws. Figure 13c shows the top view of the support package of the 16-way power divider. Limited by the mill processing, the wall of the waveguide has four filleted corners which has a radius of $r_{rg_cnc} = 92\ \mu\text{m}$. By the enlarged view in the above figure, the verticality and roughness of the waveguide edge made by the MEMS process are much better than the CNC process.

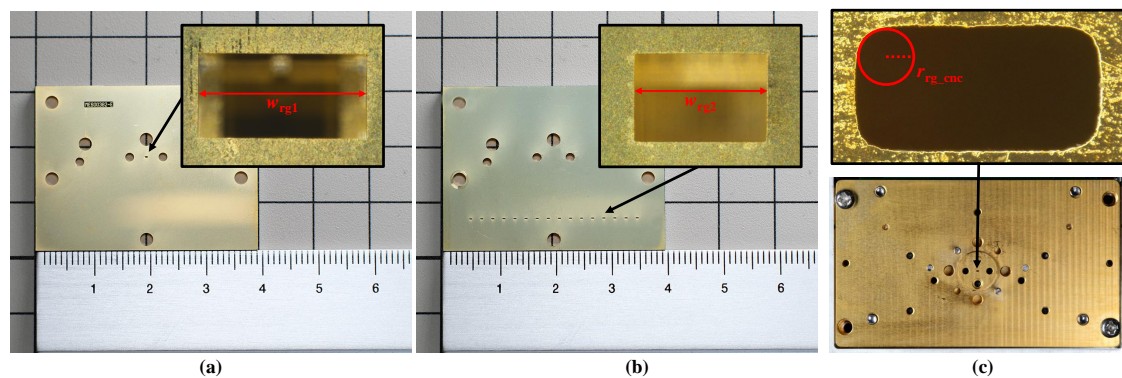


Figure 13. (a) The input port of the fabricated 16-way power divider. (b) The output ports of the fabricated 16-way power divider. (c) The input port of the fabricated metal adopter.

4.5. Measurements and Results

The 16-way power divider is not a chance to measure the output ports separately, because it has too many output ports which are in close proximity. We measured the S-parameters of the back-to-back structure combined by two 16-way power dividers to characterize the proposed power divider for insertion loss.

The designed power divider was tested using Keysight PNA-X N5247A vector network analyzer (VNA) with two VDI WM-570 (WR-2.2) frequency extenders, the lowest frequency of the measured result is limited at 330 GHz, and the simulated result shows that the power dividers also works well in 300–330 GHz. To analyze the 16-way power divider, a couple of metal waveguide adopters are made using a precision milling to connect with the waveguide ports of the vector network analyzer.

The simulation results were found using HFSS. The transition between WR-2.8 and WR-2.2 was considered in the EM simulation. The finite conductivity boundary and surface roughness model on the wall of the waveguide power divider is used to simulate actual materials. The material of the dividers is gold, of which the relative permeability is 0.99996 and the bulk conductivity is 4.1×10^7 siemens/m. The Grosse model was chosen as the surface roughness model with the surface roughness of 50 nm.

Figure 14c shows the results of S_{11} and S_{21} of the back-to-back structure combined by two 16-way power dividers. The measured S_{11} is below -10 dB over the 330–380 GHz. The S_{21} varied in the range of -2 dB and -3 dB, within in the same bands. The above results show the good agreement between the simulation and measurement due to the MEMS process.

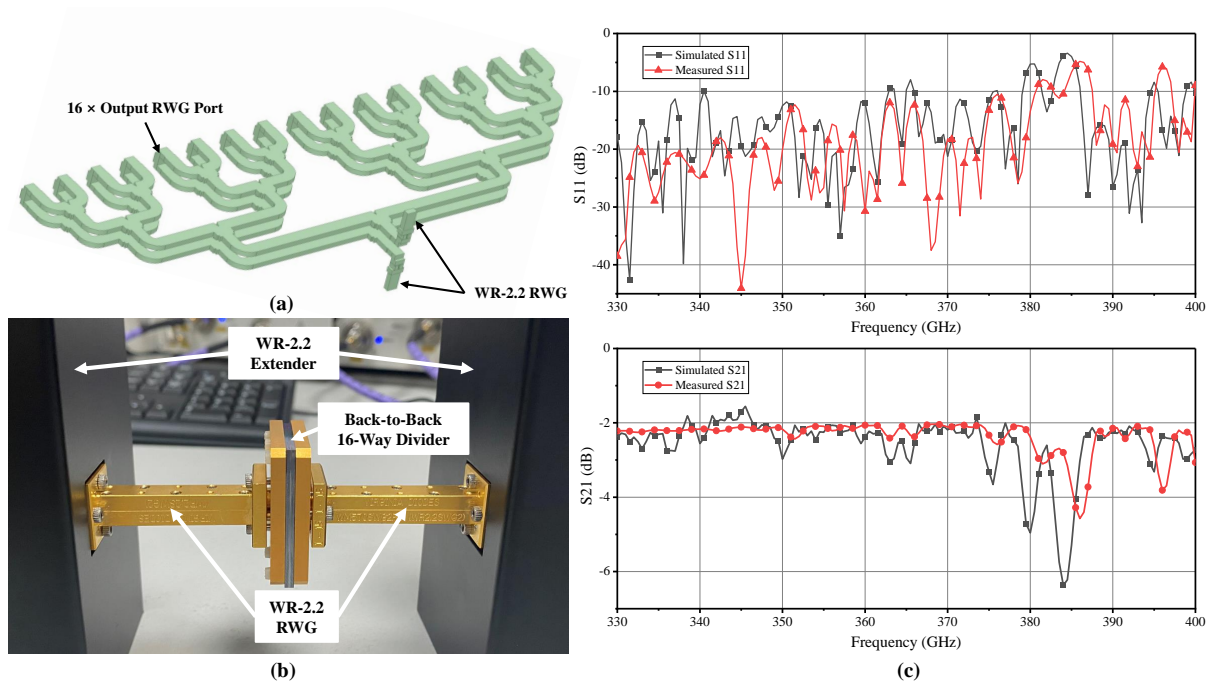


Figure 14. (a) The simulation model of the back-to-back 16-way power divider in HFSS. (b) The measurement setup of the back-to-back 16-way power divider. (c) The measured vs. simulated insertion loss and return loss for the back-to-back 16-way power divider.

5. Integration and Measurements of the Receiver Front-End

5.1. Integration of the Receiver Front-End

The designed receiver front-end consists of a silicon lens array, a 16-pixel TeraLDA combined with two 8-pixel TeraLDAs, a 16-way power divider, and 16-way read-out circuit. The exploded view of the receiver front-end is shown in Figure 15a.

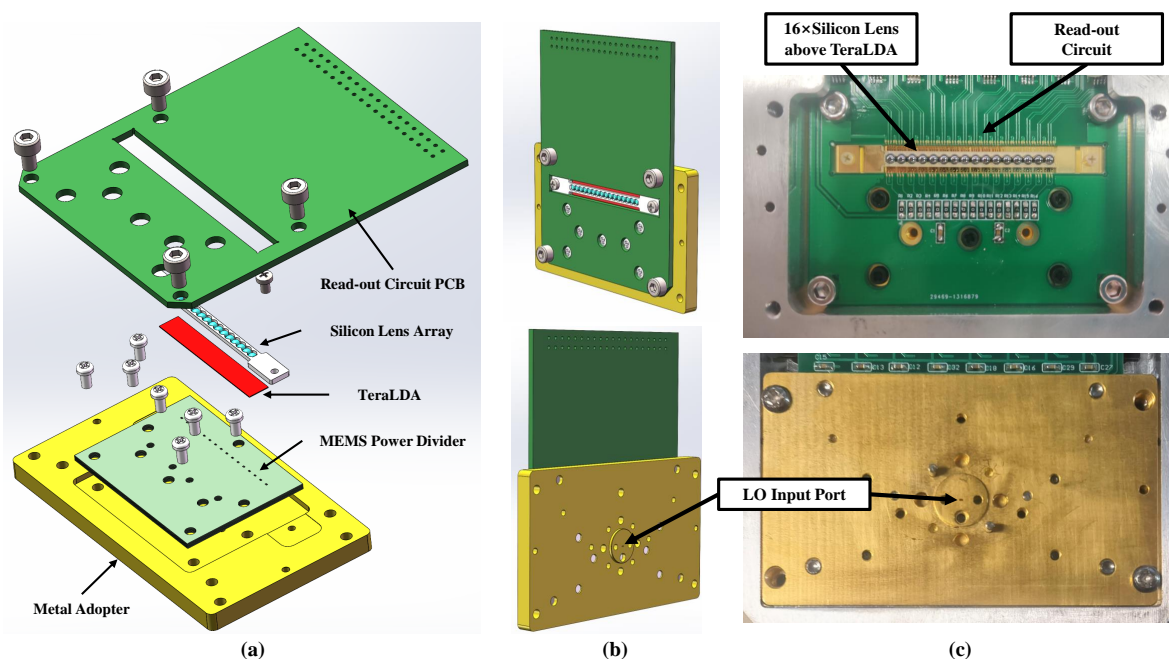


Figure 15. (a) Exploded view of the THz heterodyne receiver front-end. (b) The overall view of the THz heterodyne receiver front-end. (c) Photograph of the THz heterodyne receiver front-end.

First, the MEMS power divider was screwed to the metal adapter with nylon screws to prevent from crushing the divider. Then, two 8-pixel TeraLDAs were stuck to the divider practically using photoresist, as shown in Figure 16(b-I). The 16 silicon lenses are assembled on the array mold with the mirror frame (Figure 16a) and the silicon lens array was placed on the TeraLDA (Figure 16(b-II)). Finally, the read-out circuit PCB was screwed to the metal adapter, and the TeraLDA was bonded to the read-out circuit PCB with gold wires (Figure 16(b-III)). Figure 15c shows the image of the assembled receiver front end with stainless steel frame.

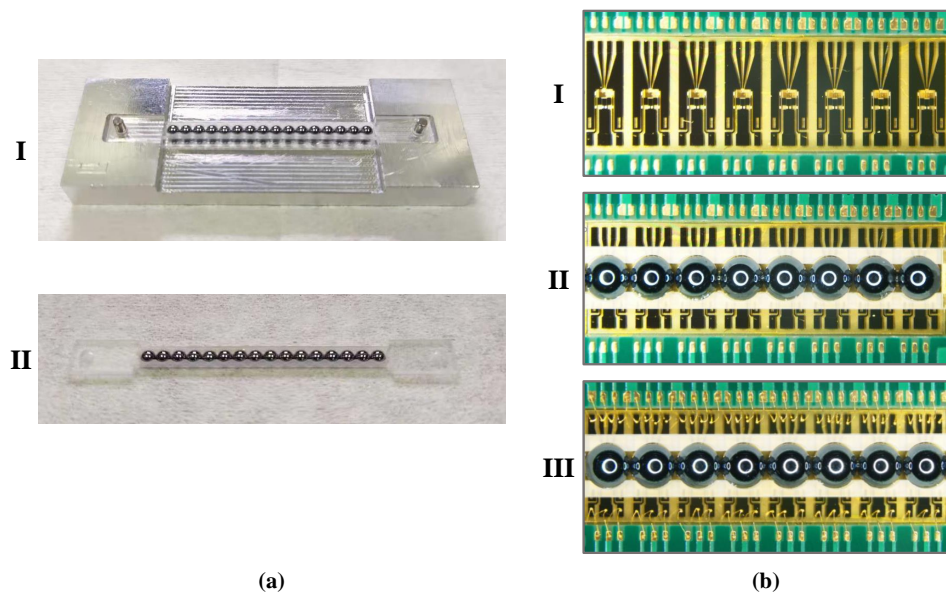


Figure 16. (a) Details of the assembly for silicon lens array. (b) Details of the assembly for TeraLDAs and silicon lens array (8-pixel of the whole array).

5.2. Receiver Front-End Experiments and Results

Figure 17 shows the experimental setup to characterize the performance of the designed receiver front-end at heterodyne mode. The two independent frequency multiplier chains, driven by two separate signal generators, generated RF ($f_{RF} = 32 \times f_{MG3692A}$) and LO ($f_{LO} = 27 \times f_{E8257D}$) THz signals near 340 GHz. The two signal generators were synchronized by 10 MHz reference clock. A pair of two off-axis parabolic mirrors (OAPs) focused the THz RF beam from THz source #1 on the one pixel of the TeraLDA. A diagonal horn was used in THz source #1 as transmit antenna, which had a 3 dB beamwidth of 22° and a gain of 23 dB. THz source #2 provided LO signals to the TeraLDA through the designed power divider. The power of both THz sources at different frequencies were measured by a THz power meter (VDI Erickson PM5B). The read-out circuit used the ADA4807-4ARUZ operational amplifier (op-amp) to make a transimpedance amplifier, which had a high gain-bandwidth product (GBWP) and low input bias current and bias voltage. The differential signals of the TeraLDA were first passed through a voltage follower (AD8066ARMZ) to reduce the impedance, while the amplitude and phase of the IF signal remained unchanged. The signals from the voltage follower are amplified 2.5 times by the op-amp. After that, the post-stage in phase amplification chain amplifies the amplified signal to 40 times. To sum up, the read-out circuit provided a voltage gain of 40 dB. The output signal of the read-out circuit was measured by a spectrum analyzer (Tektronix RS306B).

The heterodyne noise-equivalent power (NEP) was obtain from [22]:

$$\text{NEP}(\text{dBm}/\text{Hz}) = P_{\text{RF}}(\text{dBm}) - \text{SNR}(\text{dB}) - 10 \lg B(\text{Hz}) \quad (1)$$

where P_{RF} is the power of the incident THz wave, SNR is the signal-to-noise ratio of the IF signal, B is resolution bandwidth (RBW) in spectrum analysis.

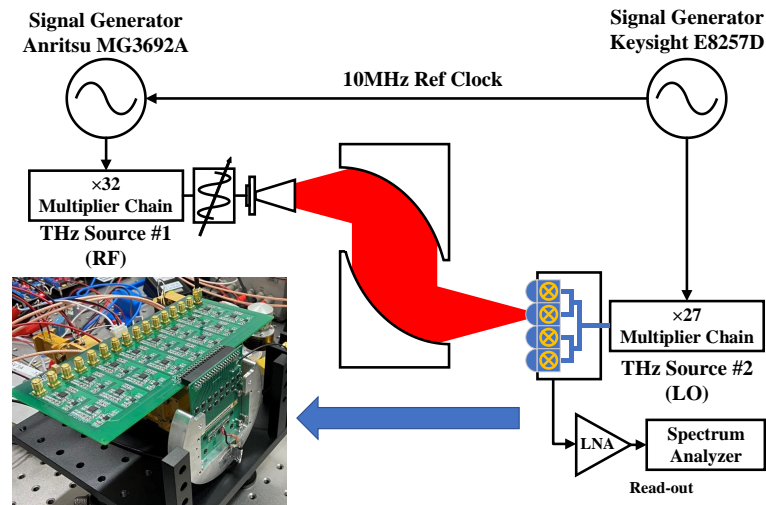


Figure 17. The measurement setup of the designed receiver front-end.

Figure 18 shows the measured IF signal and noise at different gate voltages. The RBW is 100 Hz. It can be seen that the IF signal from DET 1 and DET 16 is different from other detectors. The noise level of DET 1 is abnormal. These phenomena indicated that the DET 1 and DET 16 do not work properly, even if their I–V characteristics were normal before assembly. Figure 19 shows the measured SNR and NEP at different gate voltages. By calculating the NEP of TeraLDA, the best NEP is -92 dBm/Hz with DET 8 at optimal gate voltage of -3.76 V. The average NEP of the TeraLDA pixels is -87.6 dBm/Hz. The LO power from $\times 27$ multiplier chain is 1.2 mW. According to the above power divider measurement results, the LO power on the power divider output port is about -13.75 dBm.

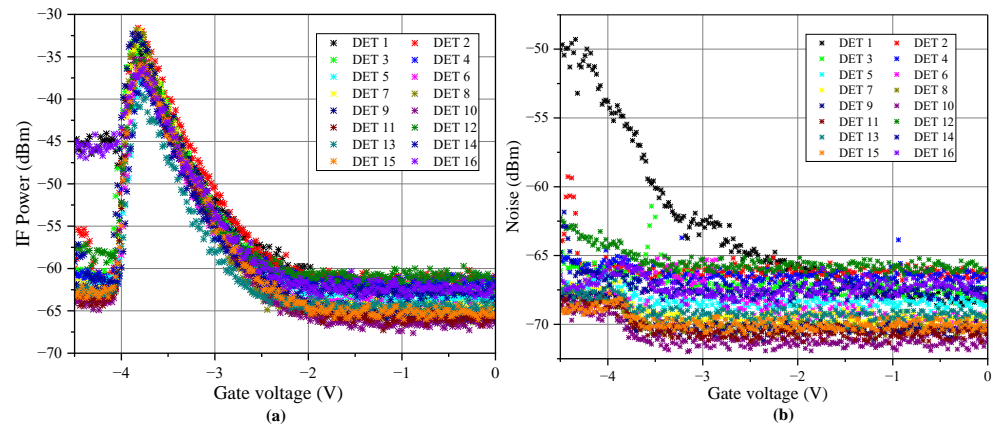


Figure 18. (a) IF signal and (b) noise power at IF frequency of 1.6 MHz, LO frequency of 331.52 GHz.

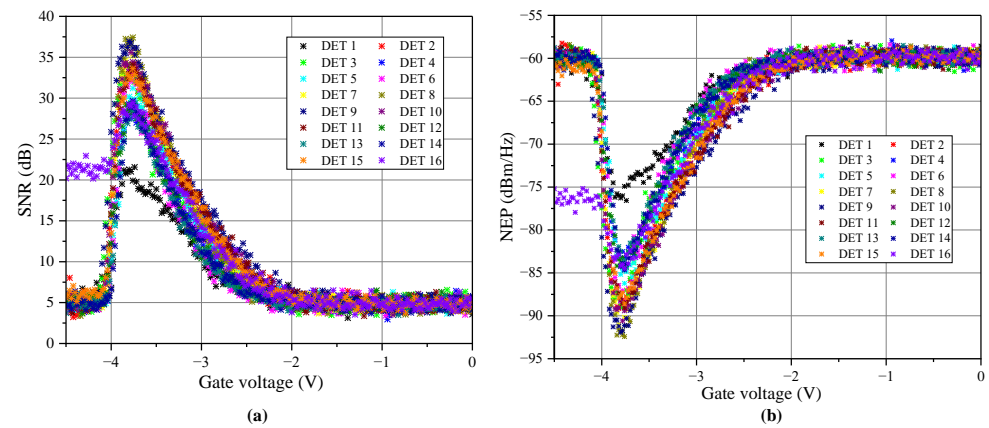


Figure 19. (a) SNR and (b) NEP at IF frequency of 1.6 MHz, LO frequency of 331.52 GHz.

Table 2 lists the comparison of the presented THz heterodyne array receiver front-end. Through the comparison, it can be seen that the proposed receiver front-end has the compact structure with multi-pixel and works at room temperature, which makes it suitable for non-destructive testing and miniaturized compact radar applications.

Table 2. Comparison among the presented terahertz heterodyne array receiver front-end.

Ref.	Type	Frequency	Pixel	Pixel Pitch	Operating Temp	LO Injection
[23]	SIS ¹	230 GHz	1 × 4	~8 mm	4 K	RWG
[24]	SIS	660 GHz	4 × 4	6 mm	4 K	Q-O ²
[25]	HEB ³	1.6 THz	1 × 3	6 mm	6 K	Q-O
[26]	SIS	350 GHz	8 × 8	~10 mm	4 K	Q-O
[27]	SIS	145 GHz	2 × 2	~28 mm	4 K	RWG
[28]	HEB	up 4.7 THz	4 × 2	~10 mm	4.2 K	Q-O
[29]	Schottky	850 GHz	2 × 2	~3 mm	~290 K	MS ⁴
[12]	Schottky	340 GHz	1 × 8	~12 mm	~290 K	RWG Probe
This Work	HEMT	340 GHz	1 × 16	~2 mm	~290 K	RWG

¹ Superconductor-Insulator-Superconductor. ² Quasi-Optical. ³ Hot Electron Bolometer. ⁴ Microstrip.

Figure 20a illustrates a simple ranging experimental scenario using the proposed receiver front-end. A frequency synthesizer based on ADF4159 from Analog Devices was used as a signal generator to generate a frequency modulated continuous wave (FMCW) LO signal. Linear sawtooth frequency modulation was used in this experimental. The parameters of the FMCW waveform are listed in Table 3.

It is about 3 m from the target (yellow door) to the radar system. The IF beat frequency (f_b) was calculated from the distance as Equation (2).

$$f_b = \frac{\Delta f}{\Delta t} \frac{2R}{c} = 160.0 \text{ kHz} \tag{2}$$

Table 3. The parameters of FMCW waveform.

Parameter Name	Value
Center Frequency f_c (GHz)	340
Sweep Bandwidth Δf (GHz)	4
Sweep time Δt (μ s)	200

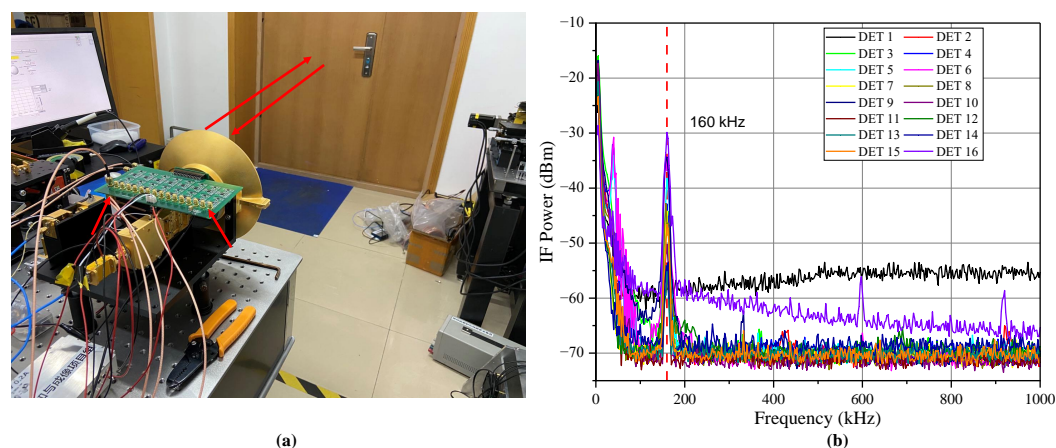


Figure 20. (a) The setup of the ranging experiment using the proposed receiver front-end. (b) The IF spectrum of the ranging experiment.

Figure 20b shows the IF spectrum of the receiver front-end. Furthermore, the center frequency of IF signal is 160 kHz. The results correspond to the above calculation.

6. Conclusions and Future Work

A 16-pixel THz heterodyne receiver front-end working at room temperature is presented and demonstrated the use of silicon micromachining for compact multi-output power divider and the array configuration of the TeraLDA. A compact 2 mm pixel spacing is achieved. The main components of the receiver have been discussed in detail. The TeraLDA based on the AlGaIn/GaN heterostructure was fabricated on a sapphire substrate. It works in a heterodyne mode on the basis of the local mixing principle. In addition, a silicon lens array is placed on the TeraLDA to further increase the responsivity. The 16-way power divider of the air-filled waveguide was designed, and characterized. The proposed power divider was stacked by five silicon layers, and each layer was fabricated by bulk silicon MEMS technology. A good agreement was observed between simulation and measurement. The designed receiver front-end offered a average heterodyne NEP of -87.6 dBm/Hz with a LO power of -3 dBm. It finally has been demonstrated that the implemented TeraLDA is capable of terahertz multi-pixel ranging. The receiver front-end design provides a possible solution for terahertz room-temperature focal plane imaging with a compact pixel spacing. Future work is ongoing to integrate our latest nano-gate detector array into this receiver front-end [22], that detectors have higher responsivity and assemble the new front-end into the 340 GHz heterodyne FPA imaging radar system which is under development.

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