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Analysis and Verification of a Half-Dual Bridge Resonant Converter with Voltage Match Modulation

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Abstract: To overcome the weakness of the narrow conversion gain of dual bridge resonant converter, a half-dual bridge resonant converter (H-DBRC) with voltage match modulation (VMM) is proposed and implemented for wide voltage range applications. The H-DBRC, including a full bridge on the primary side and a half bridge on the secondary side, is adopted to realize the bidirectional power flow and wide voltage operation. Owing to the synergy between the H-DBRC structure and VMM strategy, the converter can operate in full-bridge state and half-bridge state with maximized ZVS (zero-voltage switching) operation and minimized circulating current. The steady-state analysis is performed and the solutions for both forward and backward modes could be obtained uniformly by using the fundamental harmonics approximation approach. The soft-switching characteristics, implementation process and design example are analyzed in detail. Finally, to confirm the theoretical analysis and feasibility, both simulation and experimental verifications are demonstrated in this paper. Since the converter consistently achieves voltage-matching operation, the optimal ZVS range can be obtained when the voltage gain M is between 0.5 to 1. Moreover, the economic cost and control complexity are greatly reduced because only six switches are required in the converter.

Keywords: bidirectional resonant DC-DC converter; zero-voltage switching (ZVS); wide voltage range

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1. Introduction

Due to the features of electrical isolation, bidirectional energy flow, high power density and ability to achieve soft-switching, the dual active bridge DC-DC converters (DAB) and dual bridge resonant converters (DBRC) are widely used in a series of applications such as electric vehicles (EVs) [1,2], smart grids [3], energy storage systems (ESS) [4], and renewable energy systems. To meet the requirements of battery applications, converters should operate with bidirectional power transfer and soft-switching in a wide voltage range [5]. The conventional modulation strategy of a DAB or DBRC is the single phase shift (SPS) modulation [6,7]. The power flow direction and amplitude can be regulated just by controlling the phase shift between the primary side bridge and the secondary side bridge. When voltage gain is equal to 1, the converter has good performance, such as the lowest current stress and widest zero-voltage switching (ZVS) range. However, when voltage gain is far from 1, ZVS operation is hard to realize and circulating current increase dramatically [8].

To improve the converter performance under wide voltage variation conditions, plenty modulation strategies extended from SPS are proposed [9]. By adding inner phase shift in the primary side bridge or secondary side bridge of DAB or DBRC, SPS is changed to extended phase shift (EPS) [10,11], dual phase shift (DPS) [12,13], and triple phase

shift (TPS) [14,15] modulation. At the same time, the analysis and implementation of the converter with these modulations becomes complex due to the existence of more control variables [16–18]. In [19,20], an asymmetric pulse width modulation (APWM) is proposed for DBRC and a control route with minimized rms tank current is developed to decrease the conduction power loss. Similarly, an extended pulse width modulation (EPWM) with three control variables is proposed to extend ZVS range at light load [21]. The main problem of the two modulations is that ZVS operation for all eight switches can not be realized. A hybrid modulation is proposed in [22], when the normalized voltage gain is 0.5 or 1, the performance of DAB can be enhanced. However, when voltage gain is between 0.5 and 1, the modulation strategy is invalid.

In addition to optimizing the modulation strategies, large numbers of converters with variant topologies are proposed to enhance performance under wide voltage variation conditions [23–25]. An asymmetrical dual bridge converter based on dual transformers with secondary-side phase-shift control strategy is proposed in [26]. A hybrid-bridge DAB using voltage match control is proposed in [27], which has an auxiliary half-bridge structure on the primary side. In addition, a hybrid-bridge DBRC used in photovoltaic solar panel applications of bidirectional power flow and wide voltage range is proposed in [28]. The main drawback of these converters is that the additional switches and components will result in cost increase and control complexity. A simpler hybrid-bridge converter with six switches is proposed in [29], when voltage gain varies from 0.5 to 1, the performance of the converter can be improved. However, due to the non-resonant topologies, a dc blocking capacitor is needed to absorb the voltage offset. In [30], a dual-transformer based inductor-inductor-capacitor (LLC) resonant converter is proposed, the soft-switching range is extend over a wide input voltage and load level. However, the structure of two transformers will cause low power density and design difficulty. In order to realize wider operation range of input/output voltage, LLC resonant converters with serial and parallel topologies are analyzed in [31,32]. The main problem of these converters is that they can not realize bidirectional power flow.

To achieve wide voltage gain operation for bidirectional power flow applications, a half-dual bridge resonant converter (H-DBRC) with voltage match modulation (VMM) is presented in this paper. It is called half-DBRC because the topology is composed of a full bridge in the primary side and a half bridge in the secondary side. In addition, the two bridges are connected with a high-frequency transformer and a LC resonant tank. Moreover, VMM is employed to realize optimal performance with maximized ZVS operation and minimized circulating current in a wide range of voltage variation. The main idea of VMM is to keep the equivalent voltage gain equal to 1, more specifically, the equivalent amplitude of the primary ac voltage and secondary ac voltage are forced to be equal. Therefore, the primary-side ac voltage is modulated to an unbalanced waveform, to guarantee the voltage match with secondary-side ac voltage. The waveform has unbalanced characteristic because the negative pulse width is always equal to π while the positive pulse width is an adjustable value. The dc bias voltage is naturally balanced due to the existence of resonant capacitor. And the output power is still regulated by phase shift between primary side bridge and secondary side bridge. Since voltage match is realized for H-DBRC with VMM over the entire voltage range, a wide ZVS range can be achieved and the circulating current is naturally reduced.

Owing to the synergy between the H-DBRC structure and VMM strategy, high performance of the converter in a wide voltage range can be achieved. The merits and contributions of this paper are as follows:

(1) The structure of H-DBRC requires only six switches, that means the economic cost and control complexity can be greatly reduced. And wide-voltage-range operation can be realized in a cost-efficient way.

(2) Since the converter consistently achieves voltage matching with VMM strategy when the voltage gain M is between 0.5 and 1, ZVS of all the switches is achieved in a wide range.

(3) The optimal ZVS range and minimum circulating current can be obtained in both full-bridge and half-bridge states when $M = 1$ and $M = 0.5$.

(4) The proposed converter can realize bidirectional power transmission with similar characteristics under a unified model.

This paper is organized as follows. Section 2 describes the topology of proposed H-DBRC and the operation principle of two modes. Section 3 presents the steady-state snalysis of H-DBRC with VMM and soft-switching conditions. Then in Section 4, a design example is given, simulation and experimental results are included to verify the theoretical analysis. Section 5 concludes the paper.

2. Topology and Operation Principle of H-DBRC

The topology of the H-DBRC is shown in Figure 1. The converter consists of a full bridge, a half bridge, a series resonant tank with a inductor (L_r) and a capacitor (C_r), and a high-frequency (HF) transformer (T_r). $S_1 \sim S_6$ are six switches, $D_1 \sim D_6$ and $C_1 \sim C_6$ are the body diodes and parasitic capacitors respectively, C_{o1} and C_{o2} are output capacitors. v_{AB} and v_{CD} are the ac voltages on the primary side and secondary side, respectively. V_{in} is input voltage and V_{out} is output voltage. The leakage inductance of the HF transformer can be regarded as part of the resonant inductor (L_r). In addition, the resonant capacitor C_r is connected in series with the transformer, which can act as a DC blocking capacitor to prevent saturation of the HF transformer. The primary-side full bridge can be configured as a half bridge, when S_3 is always on and S_4 is always off. Beyond that, the converter allows power to flow forward and backward, which results in bidirectional energy transfer.

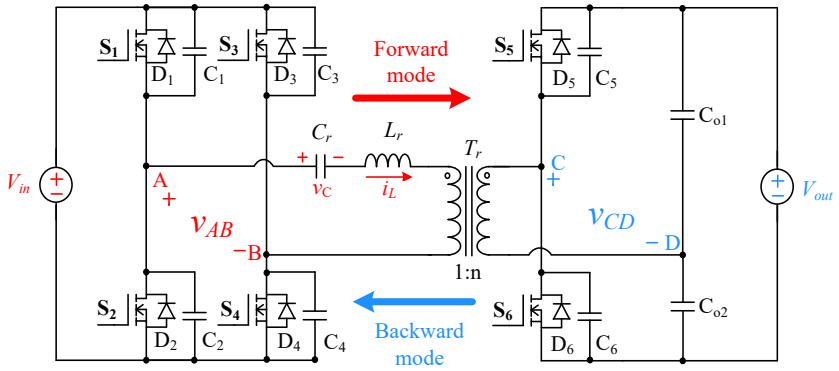


Figure 1. Topology of the proposed Half-Dual Bridge Resonant Converter.

2.1. Forward Mode

The steady-state waveforms of H-DBRC in forward mode are shown in Figure 2. With VMM strategy, S_1 and S_2 are operated with 50% duty cycle. The on-time duration of S_4 in one HF period is decreased to δ while the on-time duration of S_3 is increased to $2\pi - \delta$, the range of δ is $[0, \pi]$. Therefore, an unbalanced three-level waveform voltage v_{AB} with adjustable pulse-width δ is generated. It has a positive pulse-width δ, a zero-voltage portion $\pi - \delta$, and the negative pulse width is always equal to π. Switches S_5 and S_6 are also operated with 50% duty cycle, therefore, v_{CD} is constantly a square-wave voltage signal. In addition, there is a phase-shift angle φ between the two bridges that directs the power flow from one side to the other. It is defined as the angle by which the gating signal of S_1 leads that of S_5. It can be seen from Figure 2 that there are 7 different intervals in one switching cycle. Figure 3 shows equivalent circuits during various intervals.

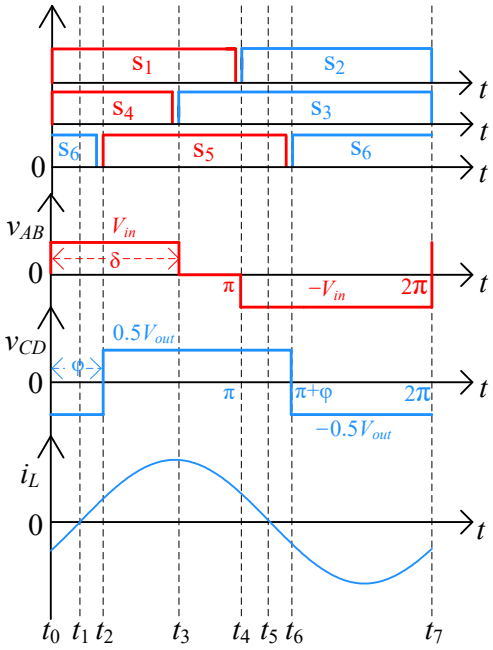


Figure 2. The steady-state waveforms of H-DBRC in forward mode.

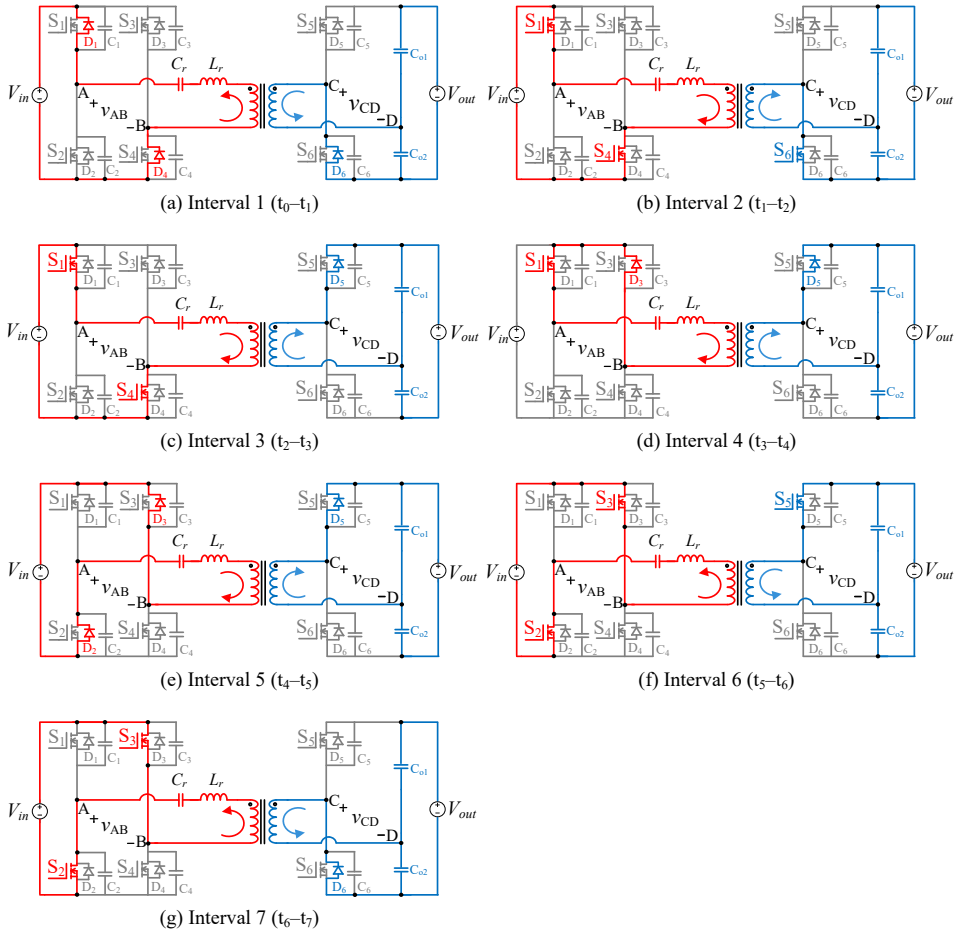


Figure 3. Equivalent circuits during different time intervals in forward mode.

(1) Interval 1 (t_0–t_1)

As shown in Figure 2, at t_0, S_2 and S_3 are turned off, S_1 and S_4 are turned on. Due to the resonant current i_L is negative, the current flows through D_1, D_4, and the ac voltage of the primary side $v_{AB} = +V_{in}$. The current flows through D_6 and C_{o1}, C_{o2} on the secondary side. Therefore, the ac voltage $v_{CD} = -0.5V_{out}$. The equivalent circuit for interval 1 is depicted in Figure 3a.

(2) Interval 2 (t_1–t_2)

The resonant current i_L increases to 0 at time t_1. In this interval, the resonant current i_L is positive. The resonant current flows through switches S_1, S_4 on the primary side, and the voltage $v_{AB} = +V_{in}$. The current flows through S_6 and C_{o1}, C_{o2} on the secondary side. Therefore, the ac voltage $v_{CD} = -0.5V_{out}$. This interval ends when S_6 is turned off. The equivalent circuit for interval 2 is depicted in Figure 3b.

(3) Interval 3 (t_2–t_3)

At t_2, switches S_6 is turned off, and S_5 is turned on. The resonant current i_L still keeps increasing. The primary-side full bridge has the same state as interval 2 and the voltage $v_{AB} = +V_{in}$. The current flows through the D_5 and C_{o1}, C_{o2} on the secondary side. Therefore, the ac voltage $v_{CD} = +0.5V_{out}$. The equivalent circuit for interval 3 is depicted in Figure 3c.

(4) Interval 4 (t_3–t_4)

As shown in Figure 2, at t_3, S_4 is turned off, and S_3 is turned on. On the primary side, v_{AB} is equal to 0 since it is shorted by S_1 and D_3. The current gradually decreases in this interval. The secondary-side bridge has the same state as interval 3 and the voltage $v_{CD} = +0.5V_{out}$. The equivalent circuit for interval 4 is depicted in Figure 3d.

(5) Interval 5 (t_4–t_5)

When $t = t_4$, S_1 turned off, and S_2 turned on. The resonant current i_L still keeps dropping until it reaches 0 in this interval. On the primary side, the current flows through D_2, D_3, and the voltage $v_{AB} = -V_{in}$. On the secondary side, the current flows through the D_6 and C_{o1}, C_{o2}, the voltage $v_{CD} = +0.5V_{out}$. The equivalent circuit for interval 5 is depicted in Figure 3e.

(6) Interval 6 (t_5–t_6)

In this interval, the polarity of the resonant current i_L changes and it begins to increase in reverse. So, the current is negative. On the primary side, the current flows through S_2, S_3, and the voltage $v_{AB} = -V_{in}$. On the secondary side, the current flows through the S_5, the voltage $v_{CD} = +0.5V_{out}$. The conducting devices and current path are shown in shown in Figure 3f.

(7) Interval 7 (t_6–t_7)

After switch S_5 is turned off and S_6 is turned on, the voltage of v_{CD} changes from $+0.5V_{out}$ to $-0.5V_{out}$. As shown in Figure 3g, on the primary side, the resonant current i_L flows through S_2, S_3. The current flows through the D_6, on the secondary side.

2.2. Backward Mode

The steady-state waveforms of H-DBRC in backward mode are shown in Figure 4. The converter is still controlled with VMM strategy. The primary-side switches are operated in the same state of forward mode, and the secondary-side switches S_5 and S_6 are still operated at 50% duty cycle. The difference is the gating signal of S_5 leads that of S_1 in a certain angle in backward mode. Since there is no change of the definition of angle φ, the phase shift between S_1 and S_5 is $-\varphi$. There are also 7 different intervals during one switching cycle in this mode. Figure 5 shows the equivalent circuit during the different time intervals.

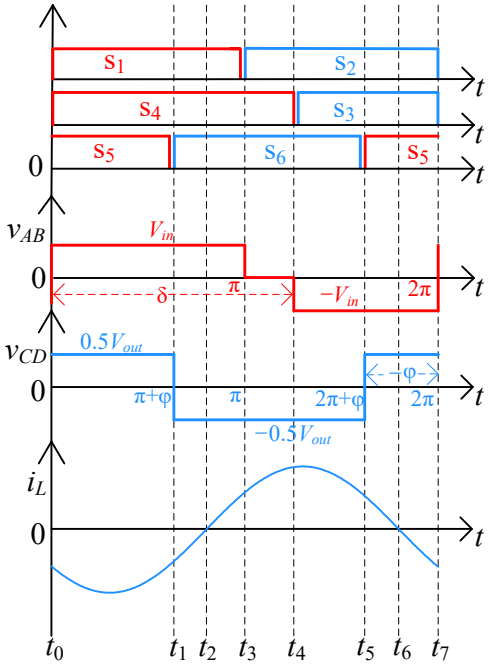


Figure 4. The steady-state waveforms of H-DBRC in backward mode.

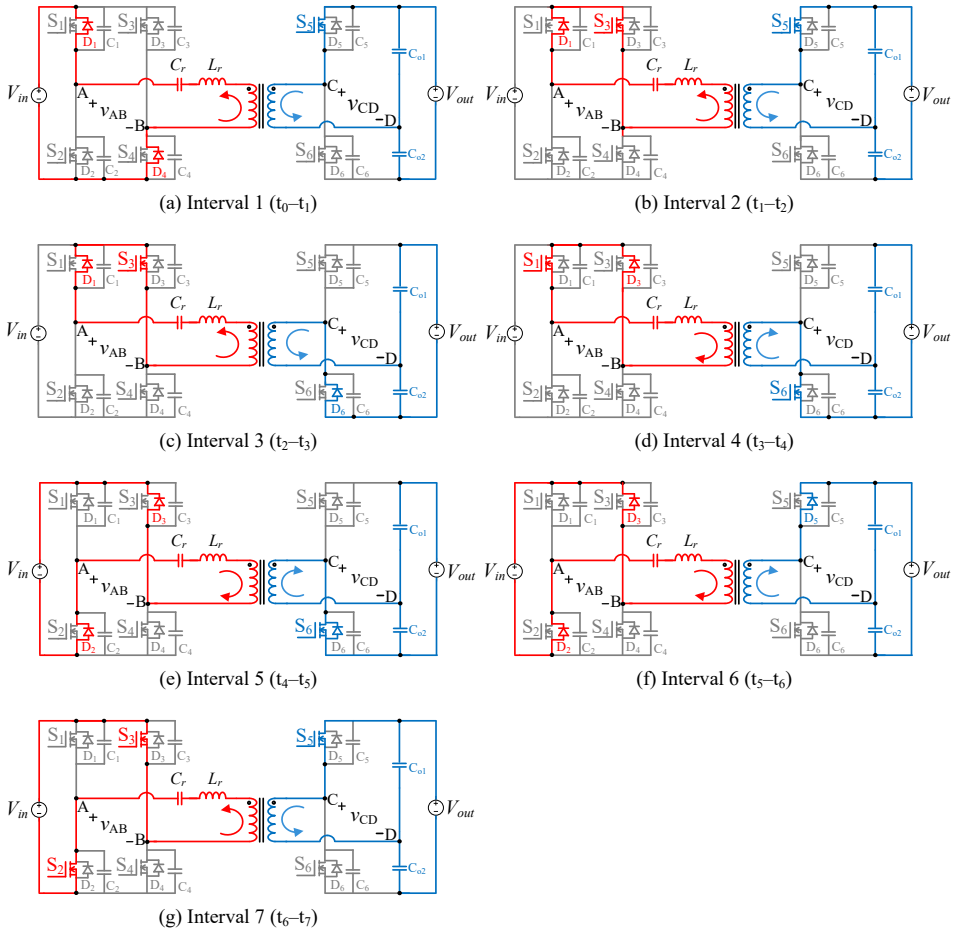


Figure 5. Equivalent circuits during different time intervals in backward mode.

(1) Interval 1 (t_0–t_1)

As shown in Figure 4. This interval begins when S_2, S_3 are turned off and S_1, S_4 are turned on at t_0. Since the resonant current i_L is negative, the current flows through D_1, D_4 on the primary side, and the voltage $v_{AB} = +V_{in}$. On the secondary side, the current flows through the switch S_5, the voltage $v_{CD} = +0.5V_{out}$. The equivalent circuit for interval 1 is depicted in Figure 5a.

(2) Interval 2 (t_1–t_2)

When $t = t_1$, S_4 turned off and S_3 turned on. On the primary side, the resonant current i_L flows through D_1, S_3, and the voltage $v_{AB} = 0$. The current gradually increases in this interval. On the secondary side, the current flows through the switch S_5 and C_{o1}, C_{o2}, the voltage $v_{CD} = +0.5V_{out}$. This interval ends when S_5 is turned off. The equivalent circuit for interval 2 is depicted in Figure 5b.

(3) Interval 3 (t_2–t_3)

In this interval, the resonant current i_L increases to 0 from t_2 to t_3. After switch S_5 is turned off and switch S_6 is turned on, v_{CD} is equal to $-0.5V_{out}$. As shown in Figure 5c, The primary-side full bridge has the same state as interval 2 and the voltage $v_{AB} = 0$. The current flows through D_6 and C_{o1}, C_{o2} on the secondary side.

(4) Interval 4 (t_3–t_4)

This interval begins when the resonant current i_L reaches 0 at t_3. Although the voltage v_{AB} is still equal to 0, the resonant current flows through S_1, D_3 on the primary side. On the secondary side, the current flows through the switch S_6, the voltage $v_{CD} = -0.5V_{out}$. The equivalent circuit for interval 4 is depicted in Figure 5d.

(5) Interval 5 (t_4–t_5)

At t_4, S_1 turned off and S_2 turned on, the resonant current i_L is positive in this interval. The primary current flows through anti-parallel diodes D_2 and D_3, the voltage $v_{AB} = -V_{in}$. On the secondary side, the current flows through the switch S_6 and C_{o1}, C_{o2}, the voltage $v_{CD} = -0.5V_{out}$. The conducting devices and current path for interval 5 are depicted in Figure 5e.

(6) Interval 6 (t_5–t_6)

When $t = t_5$, S_6 is turned off and S_5 is turned on. The resonant current i_L keeps dropping until it reaches 0 in this interval. The primary-side full bridge has the same state as interval 4 and the voltage $v_{AB} = -V_{in}$. On the secondary side, the current flows through the D_5, the voltage $v_{CD} = +0.5V_{out}$. The equivalent circuit for interval 6 is depicted in Figure 5f.

(7) Interval 7 (t_6–t_7)

The polarity of the resonant current i_L changes and the current is negative in this interval. On the primary side, the current flows through S_2, S_3, the voltage $v_{AB} = -V_{in}$. On the secondary side, the current flows through the switch S_5, the voltage $v_{CD} = +0.5V_{out}$. The equivalent circuit for interval 7 is depicted in Figure 5g.

3. Steady-State Analysis of H-DBRC with VMM

To facilitate the calculation and design, all equations presented are normalized with the base values given later. All parameters in the secondary side have been transferred to the primary side, which is denoted by the superscript " ′ ".

$$V_B = V_{in}, \quad Z_B = R'_L = \frac{R_L}{n^2} = \frac{(0.5V_{out})^2}{n^2 P_{rate}}, \quad I_B = \frac{V_B}{Z_B} \tag{1}$$

where P_{rate} is rate power, R_L is the equivalent output load, $1 : n$ is the turns ratio of the transformer. The normalized switching frequency is given by:

$$F = \frac{\omega_s}{\omega_r} = \frac{f_s}{f_r} \tag{2}$$

where $f_r = \omega_r/2\pi = 1/(2\pi\sqrt{L_rC_r})$ is the resonant frequency and $f_s = \omega_s/(2\pi)$ is the switching frequency. Then normalized impedance of the resonant tank are given by:

$$\begin{aligned} X_{Lr,pu} &= QF, \quad X_{Cr,pu} = -\frac{Q}{F} \\ X_{s,pu} &= X_{Lr,pu} + X_{Cr,pu} = Q(F - \frac{1}{F}) \end{aligned} \tag{3}$$

where Q is the quality factor and is defined as follows:

$$Q = \frac{\omega_r L_r}{R'_L} \tag{4}$$

The Fundamental Harmonics Approximation (FHA) approach can simplify the calculation for the steady-state analysis. The equivalent circuit of the converter in the phasor domain is depicted in Figure 6, and the two fundamental voltage phasors are shown as follows:

$$\begin{aligned} \overline{V}_{AB} &= \frac{\sqrt{10 - 6\cos\delta}}{\pi} \angle \arctan\frac{\sin\delta}{3 - \cos\delta} - \frac{\pi}{2} \\ \frac{\overline{V}_{CD}}{n} &= \frac{4M}{\pi} \angle -\varphi - \frac{\pi}{2} \end{aligned} \tag{5}$$

where M is the voltage gain of the converter and is defined as:

$$M = \frac{V'_o}{V_{in}} = \frac{0.5V_{out}}{nV_{in}} \tag{6}$$

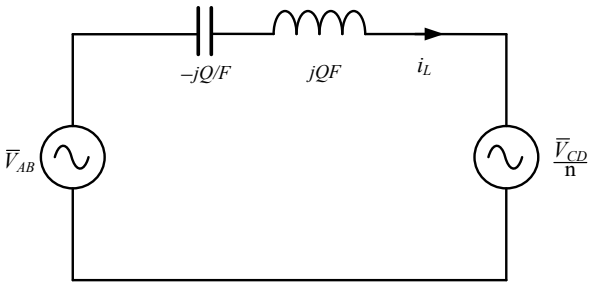


Figure 6. The equivalent circuit in the phasor domain.

According to the equivalent circuit shown in Figure 6, the normalized inductor current $i_{L,pu}$ expression can be written as:

$$i_{L,pu}(t) = I_{L,pu,p} \cdot \cos(\omega_s t + \angle i_{L,pu}) \tag{7}$$

where the peak current $I_{L,pu,p}$ and the phase angle $\angle i_{L,pu}$ are:

$$I_{L,pu,p} = \frac{\sqrt{16M^2 + 10 - 6\cos\delta + 8M[\cos(\delta - \varphi) - 3\cos\varphi]}}{\pi X_{s,pu}} \tag{8}$$

$$\angle i_{L,pu} = \arctan\frac{\sin\delta + 4M\sin\varphi}{3 - \cos\delta - 4M\cos\varphi} \tag{9}$$

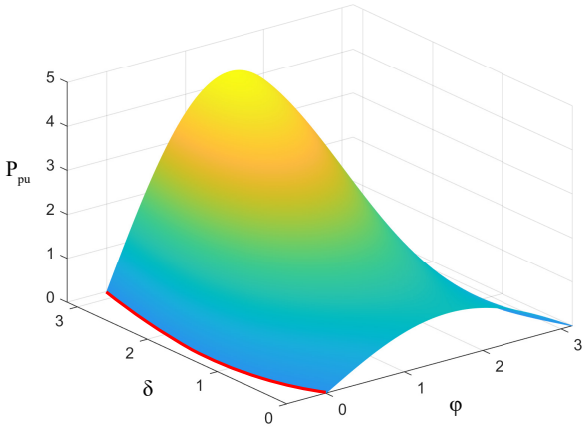
Then, the normalized power expression can be derived as:

$$P_{pu} = \frac{2M}{\pi^2 Q(F - \frac{1}{F})}[\sin(\delta - \varphi) + 3\sin\varphi] \tag{10}$$

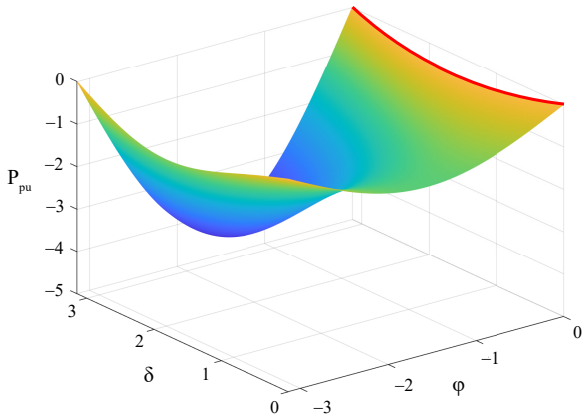
Since the definition of φ between forward mode and backward mode is the same, the expression of output power can be unified. And the boundary condition of the two modes can be obtained:

$$\varphi = -\arctan\frac{\sin\delta}{3-\cos\delta} \tag{11}$$

When $\varphi > -\arctan\left(\sin\delta/(3-\cos\delta)\right)$, the converter operates in forward mode. When $\varphi < -\arctan\left(\sin\delta/(3-\cos\delta)\right)$, the converter operates in backward mode. Figure 7a,b show the 3-dimensional plots of the normalized power with the control of δ and φ in forward and backward modes, respectively, in which the red curves are their boundary.



(**a**)



(**b**)

Figure 7. 3-dimensional plots of normalized power: (**a**) Fordward mode, (**b**) Backward mode.

3.1. Implementation of the Proposed VMM Strategy

VMM is employed to realize optimal performance with maximized ZVS operation and minimized circulating current in a wide range of voltage variation. The main idea of VMM is to keep the equivalent voltage gain equal to 1, more specifically, the equivalent amplitude of the primary-side ac voltage and secondary-side ac voltage are forced to be equal. Therefore, the following equation can be obtained:

$$\frac{V_{in}}{\pi}\sqrt{10-6\cos\delta} = \frac{4}{\pi}\left(\frac{0.5V_{out}}{n}\right) \tag{12}$$

Further, the equation can be simplified and voltage gain M can be expressed as:

$$M = \sqrt{\frac{5-3\cos\delta}{8}} \tag{13}$$

When a fixed voltage gain M is given, the angle δ can be calculated. Then, the optimum operation condition can be obtained. Since the range of δ is $[0, \pi]$, the proposed H-DBRC with VMM realizes a general voltage match when $0.5 \leq M \leq 1$.

By combining Equations (10) and (13), another control variable φ can be easily calculated at a given voltage gain M and power ratio K:

$$\varphi = \begin{cases} \arcsin\left[\frac{K\pi^2 Q(F-\frac{1}{F})}{8}\right] - \arctan\left[\frac{\sqrt{(4M^2-1)(1-M^2)}}{1+2M^2}\right] & \text{Forward mode} \\ -\arcsin\left[\frac{K\pi^2 Q(F-\frac{1}{F})}{8}\right] - \arctan\left[\frac{\sqrt{(4M^2-1)(1-M^2)}}{1+2M^2}\right] & \text{Backward mode} \end{cases} \quad (14)$$

where $K = P_o / P_{rate}$ is the power ratio.

The diagram of the implementation of the proposed VMM strategy is presented in Figure 8. Firstly, the input voltage and output voltage are measured by voltage sensors. Then the PI output P_{pu} and voltage gain M are calculated. After that, the control variables φ and δ can be calculated by VMM strategy. Finally, the gating singles are generated by a PWM unit according to the control variables. The entire control loop is straightforward and does not need any complex calculation since the analytical solution of the control variables can be expressed with VMM strategy.

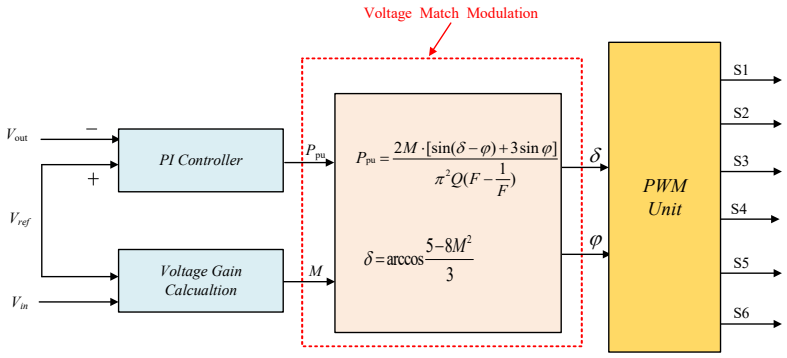


Figure 8. Implementation of the proposed VMM strategy.

For further explanation of VMM strategy, the converter operation at different voltage gains are illustrated in detail. Taking forward mode as an example, the typical waveforms are shown in Figure 9. For the case of $M = 0.5$ and $M = 1$, the obtained ac voltage v_{AB} and v_{CD} are both square waves, the converter operates at the optimal operating point with voltage match. Like SPS, only the outer phase shift angle φ between the primary-side and the secondary-side bridges is used to modulate the power transfer. When $M = 0.5$, as Figure 9a shows, the converter operates in half-bridge state, in which S_3 is always on and S_4 is always off. The ac voltage v_{AB} is a two-level wave of $-V_{in}$ and 0. The dc bias voltage of v_{AB} is naturally balanced by the resonant capacitor and ZVS operation is realized over the entire load range. When $M = 1$, as shown in Figure 9c, the converter works in full-bridge state. v_{AB} is a two-level wave and the voltage amplitude is $\pm V_{in}$. In addition, ZVS can be ensured for whole load rang. As shown in Figure 9b, when $0.5 < M < 1$, the converter works in the intermediate state, and the value of δ is between 0 and π. Therefore, v_{AB} becomes an unbalanced three-level waveform of $\pm V_{in}$ and 0. The dc bias voltage can also be balanced by the resonant capacitor.

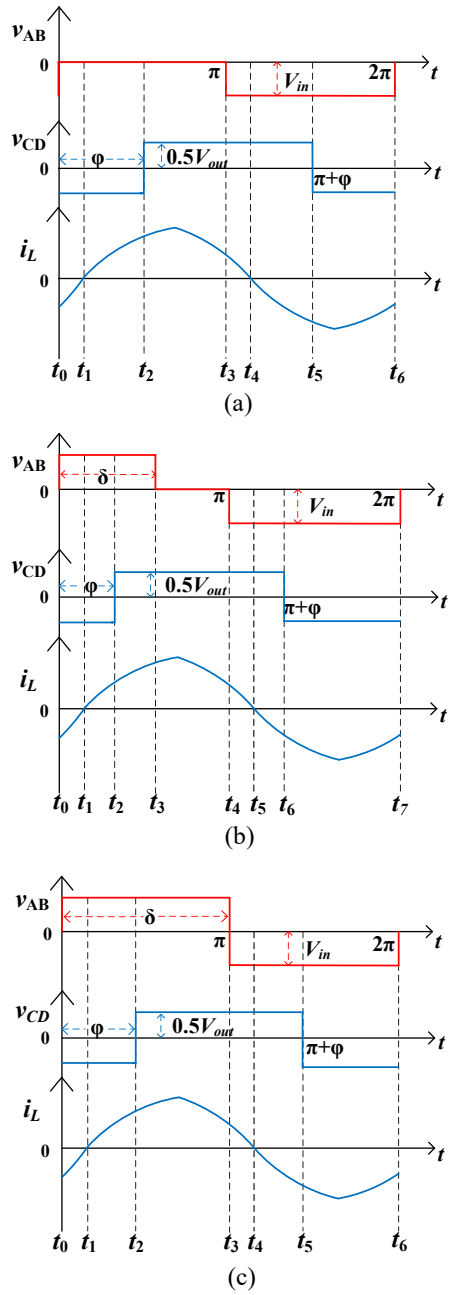


Figure 9. Typical waveforms at different voltage gains: (**a**) $M = 0.5$; (**b**) $M = 0.6$; (**c**) $M = 1$.

3.2. Soft Switching Analysis

When the current flows through anti-parallelled diodes of MOSFETs, it ensures that the switches can realize ZVS operation. So, the basic principle to achieve ZVS is that the current direction needs to be against the voltage direction when the switch is turned on. Therefore, the ZVS conditions of $S_1 \sim S_6$ in H-DBRC with VMM are shown in Table 1.

Table 1. ZVS conditions.

Switches	ZVS Conditions
S_1 S_2 S_4	$3 - \cos\delta - 4M\cos\varphi > 0$
S_3	$1 - 3\cos\delta + 4M\cos(\delta - \varphi) > 0$
S_5 S_6	$\cos(\delta - \varphi) - 3\cos\delta + 4M > 0$

From another perspective, the ZVS conditions can be illustrated graphically. Figure 10 shows the ZVS region with regard to the two control variables at different voltage gains. In each subfigure, the ZVS boundaries of different switches are shown for a particular voltage gain M, and the full ZVS region are shaded. The blue dashed line is an equal-power line, and the red point on the line indicates the working point with VMM strategy under the particular power level.

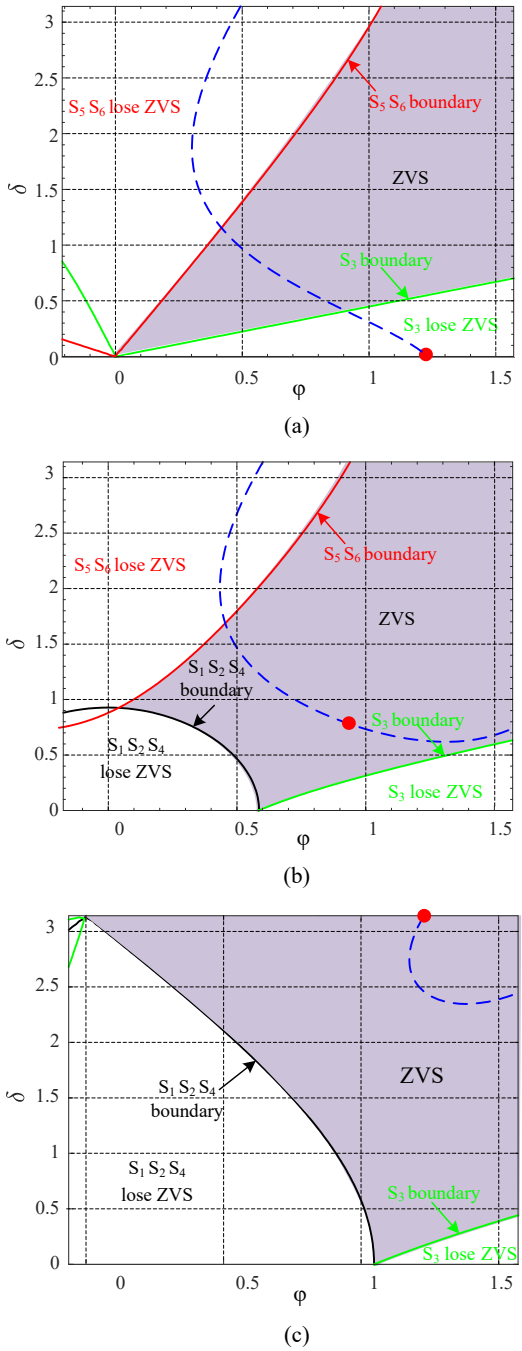


Figure 10. ZVS Region with different voltage gains: (**a**) $M = 0.5$, (**b**) $0.5 < M < 1$, (**c**) $M = 1$.

Figure 10a shows the ZVS region at $M = 0.5$. The equal-power line and working point can be obtained according to Equations (10) and (14). Since the control variable δ is always equal to 0, the converter is operating in the half-bridge state with VMM strategy, which means S_3 is always on and S_4 is always off. Although the working point is not in the full ZVS region, the switching loss can be neglected due to S_3 is not operating at

high frequency. From this point of view, the best ZVS performance can be obtained when $M = 0.5$. Figure 10b shows the ZVS region when $0.5 < M < 1$. Since it is an intermediate state, ZVS region is constrained by the converter working state, which is depend on the output power and voltage gain. In general, ZVS of all switches is easy to achieve in high power level due to a large φ. When $M = 1$, as shown in Figure 10c, the converter is operating in the full-bridge state and δ is always equal to π. It can be seen that the full ZVS operation is achieved. Although VMM strategy is similar to conventional SPS modulation when $M = 1$, full ZVS operation is lost in SPS when M deviates from 1. Therefore, when the proposed VMM strategy is compared with SPS, it has an extended ZVS range. Furthermore, it is worth noting that, when voltage match is satisfied, a low circulating current is achieved. As all knows, the circulating current will increase the RMS value of resonant current and is no use for the output power. Therefore,the conduction loss and magnetic loss can be decreased by VMM strategy.

4. Simulation and Experimental Verification

4.1. Design Example

To validate the theoretical analysis of the converter with VMM strategy, H-DBRC was subjected to a number of experiments in the laboratory and computer simulations. Firstly, the specifications of the converter are determined as follows: V_{in} is 75 V to 150 V, V_{out} is 100 V, the switching frequency f_s is 100 kHz and the rated power P_{rate} is 200 W. To achieve better performance, the design point is chosen at the maximum voltage gain $M_{max} = 1$, i.e., the minimum input voltage $V_B = V_{in\,\min} = 75$ V. The converter is tested with three different values of voltage gain: the maximum gain at 1 ($V_{in} = 75$ V, $V_{out} = 100$ V), the minimum gain at 0.5 ($V_{in} = 150$ V, $V_{out} = 100$ V), and $M = 0.6$ ($V_{in} = 125$ V, $V_{out} = 100$ V).

Moreover, to have a certain soft-switching margin for the above resonant operation, the normalized frequency F is chosen to be 1.35. Therefore, according to Equation (6) the transformer turns ratio can be derived:

$$1 : n = (M \cdot V_{in\,\min}) : 0.5V_{out} = 1 : 0.6667 \tag{15}$$

The base impedance Z_B is:

$$Z_B = \frac{(0.5V_{out})^2}{n^2 \cdot P_{rate}} = 28.125\ \Omega \tag{16}$$

It is selected to adopt a full-load quality factor Q of 1. The resonant inductor and capacitance parameters can be calculated as follows:

$$\begin{aligned} L_r &= \frac{Q \cdot F \cdot Z_B}{\omega_s} = 60.43\ \mu\text{H} \\ C_r &= \frac{F}{Q \cdot \omega_s \cdot Z_B} = 76.39\ \text{nF} \end{aligned} \tag{17}$$

4.2. Simulation Results

Before the experimental validation of the prototype, simulations were performed using PSIM software. Table 2 displays the specifications of the components in PSIM software. The steady-state operating waveforms of the forward mode using the proposed VMM strategy with different voltage gain M at rate power $P_{rate} = 200$ W as Figure 11 illustrated. Energy is transferred from V_{in} to V_{out} in the forward mode. The steady-state waveform at $M = 0.5$, with $V_{in} = 150$ V and $V_{out} = 100$ V, is depicted in Figure 11a–c. The plots in Figure 11a are, from top to bottom, as follows: output voltage V_{out}, v_{AB} and v_{CD}, resonant current i_L. Figure 11b are the current of $S_1 - S_3$ and the plots shown in Figure 11c are the current of $S_4 - S_6$. It can be seen that both v_{AB} and v_{CD} are square waves with 50% duty cycle, the resonant current i_L is approximately sinusoidal. Since the converter is operating in half-bridge state, switch S_4 is always closed and S_3 is always

turned on. The optimal performance with full ZVS operation and low circulating current is realized. Figure 11d–f shows the steady-state waveforms at $M = 0.6$. It can be seen that v_{AB} is a three-level waveform with a maximum value of 125 V, while v_{CD} is still a square waveform with an amplitude of 50 V and a duty cycle of 50%. The resonant current i_L is approximately sinusoidal and ZVS is achieved for all six switches. Figure 11g–i shows the steady-state waveforms at $M = 1$, it can be seen that v_{AB} and v_{CD} are square waves with no dc bias, where v_{AB} has an amplitude of 75 V and v_{CD} has an amplitude of 50 V. The optimal performance is achieved with full ZVS operation and low circulating current due to voltage match.

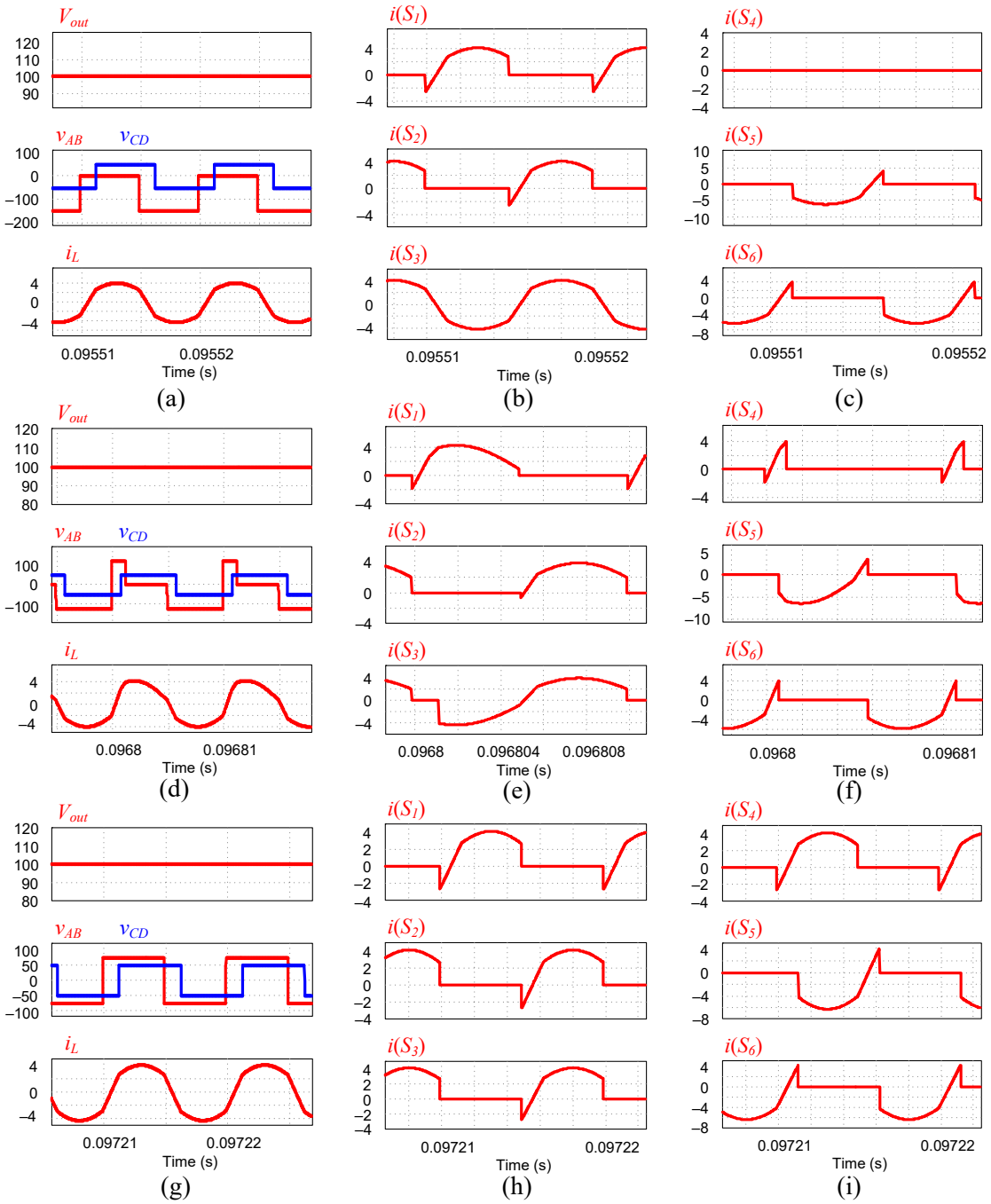


Figure 11. Simulation results of forward mode with different voltage gain M: (**a**–**c**) $M = 0.5$; (**d**–**f**) $M = 0.6$; (**g**–**i**) $M = 1$.

In order to validate the feature of bidirectional power flow, the backward mode with different voltage gain M is also tested. Figure 12 shows the steady-state operating waveforms at rate power $P_{rate} = -200$ W. Figure 12a–c shows the steady-state waveforms at $M = 0.5$ and Figure 12d–f shows the steady-state waveforms at $M = 1$. It can be found that the voltage gain is extend from 1 to 0.5 with full ZVS operation and low circulating current by using VMM strategy.

Table 2. The specifications of the components in simulation.

Parameter	Value
Turns ratio of the transformer (1:n)	9:6
Resonant inductor (L_r)	60.43 μH
Resonant Capacitor (C_r)	76.39 nF
Output Capacitors (C_{o1} and C_{o2})	200 μF
On Resistance of MOSFETs (S_1∼S_6)	600 mΩ
Parasitic Capacitors (C_1∼C_6)	0.2 nF
Forward Voltage of Body Diodes (D_1∼D_6)	1.2 V

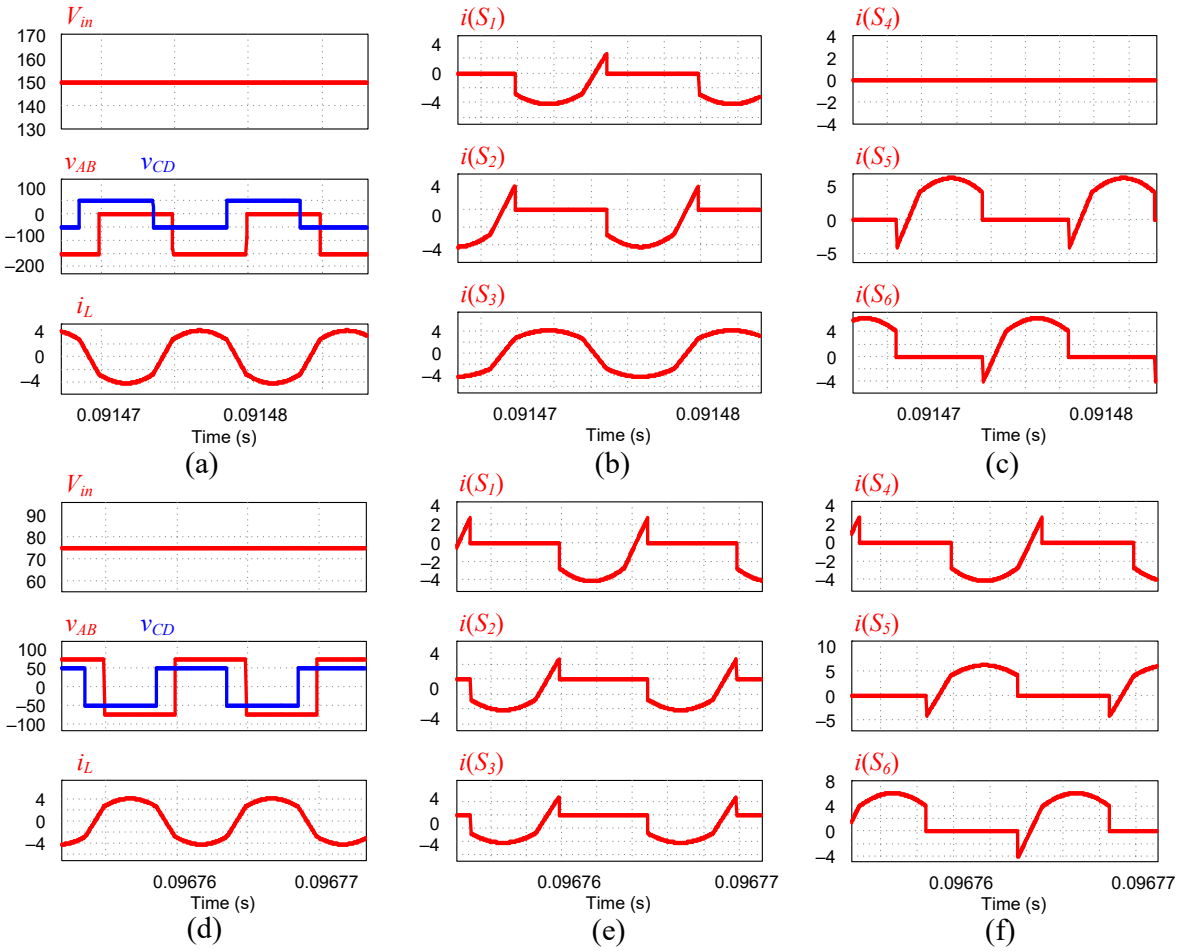


Figure 12. Simulation results of backward mode with different voltage gain M: (**a**–**c**) $M = 0.5$; (**d**–**f**) $M = 1$.

4.3. Experiment Results

To validate the effectiveness of the presented H-DBRC with the VMM strategy, a 200 W prototype is designed. Figure 13 shows the experimental prototype, which can be divided into four parts: the FPGA controller, the primary-side bridge, the HF transformer and LC

resonant tank, and the secondary-side bridge. The key parameters of the prototype are listed in Table 3. The primary-side MOSFETs ($S_1 - S_4$) are SIHP10N40D and the secondary-side MOSFETs ($S_5 - S_6$) are IPP320N20N3. L_r consists of a transformer leakage inductor and an external inductor.

Table 3. Parameters of the Experiment.

Parameter	Value
Input voltage (V_{in})	75 V∼150 V
Output voltage (V_{out})	100 V
Rated Power (P_{rate})	200 W
Switching frequency (f_s)	100 kHz
Turns ratio of the transformer (1:n)	9:6
Resonant inductor (L_r)	60.43 µH
Resonant Capacitor (C_r)	76.39 nF
The primary switches (S_1∼S_4)	SIHP10N40D (400 V/10 A)
The secondary switches (S_5∼S_6)	IPP320N20N3 (200 V/34 A)
Output Capacitors (C_{o1} and C_{o2})	200 µF

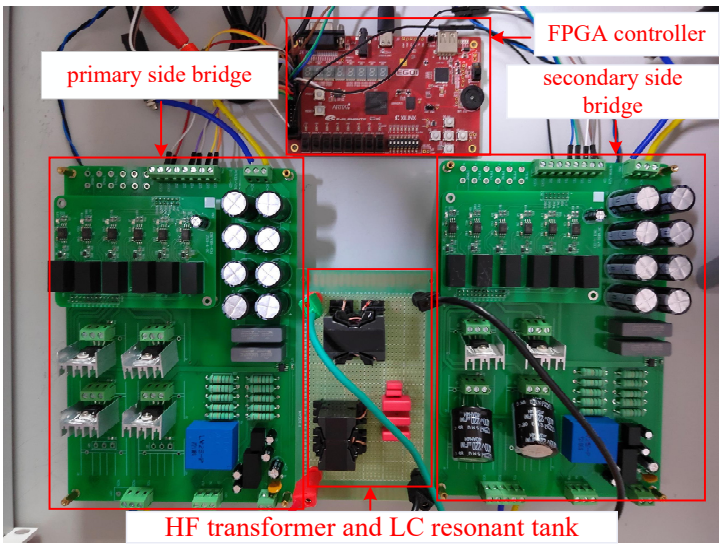


Figure 13. Picture of the designed converter.

The experimental waveforms under different power levels are presented in Figures 14–17 for different voltage gains. In each case, the waveforms recorded from top to bottom are v_{AB}, v_{CD}, resonant current i_L and resonant capacitor voltage v_C, respectively. As shown in Figure 14, when $M = 0.5$, the waveforms obtained from experimental tests match the simulation plots. ZVS operation of all switches is realized during full power range. H-DBRC functions as a half bridge converter and resonant capacitor absorbs half of the primary side dc voltage. Thus, it can be found that v_C has a dc offset of 75 V. The converter operates in low circulating current situation. The RMS value of i_L at $P_o = 200$ W, 150 W, 100 W, 50 W are 3.67 A, 2.39 A, 1.58 A, and 0.79 A, respectively, which is consistent with the theoretical data. The experimental waveforms for $M = 0.6$ with different power levels are shown in Figure 15. The dc bias is also absorbed by resonant capacitor. Since it is a intermediate state, the ZVS range is relatively narrow. It can be seen that all switches can achieve ZVS at $P_o = 200$ W and 150 W, while switches S_2 and S_5 lose ZVS operation at light load. The RMS values of i_L at different power levels are slightly greater than theoretical values. The reason is that, in this situation, v_{AB} is no longer a square wave. Therefore, the weight of high-order harmonics of v_{AB} increases, which brings more deviations when using FHA. When $M = 1$ in Figure 16, the converter operates in full-bridge state. The optimal performance with full ZVS operation and low circulating

current is realized. The RMS value of i_L at P_o = 200 W, 150 W, 100 W, 50 W are 3.80 A, 2.39 A, 1.58 A, and 0.77 A, respectively, which is consistent with the theoretical data. As shown in Figure 17, the experimental waveforms with different M under −200 W are illustrated, which indicates the converter operates in backward mode. It can be observed that v_{AB} lags v_{CD} in some degrees and i_L is almost antiphase with v_{AB}. All experimental results match the theory and simulation well.

The conversion efficiency of the H-DBRC with proposed VMM strategy in forward mode are recorded and plotted in Figure 18. It can be seen that the efficiency is almost the same between $M = 0.5$ and $M = 1$, because v_{AB} and v_{CD} are both square waves and the voltages are well matched in the two case. The highest efficiency is 93.43% at 150 W when $M = 1$. It should be noted that the efficiency decreases in light load, although ZVS operation is always realized. The reason is that the conduction loss is the main part of power loss in light load condition, which may be further reduced by using SiC power transistors.

Eventually, the H-DBRC with VMM strategy is compared with some previous works, as listed in Table 4, from various perspectives. Excellent performance in many ways is demonstrated in the proposed H-DBRC. It has the minimum number of switches and diodes compared with previous works, which can significantly reduce the economic cost and control complexity. Besides, the voltage range and the ZVS range are broad, under the control of the VMM strategy.

Table 4. Comparisions between the previous works.

	[26]	[27]	[28]	[29]	[30]	**This Work**
Voltage gain	0.82–1.15	0.5–1	0.92–2.38	0.5–1	1–2	0.5–1
Degrees of freedom	1	2	1	2	2	2
The number of switches (MOSFETs)	6	8	12	6	4	6
The number of diodes	4	0	0	0	4	0
Transformer	2	1	1	1	2	1
Switching frequency	Fixed	Fixed	Variable	Fixed	Fixed	Fixed
Resonant Tank	No	No	LC	No	LLC	LC
Soft-switching range	Narrow	Wide	Wide	Medium	Wide	Wide

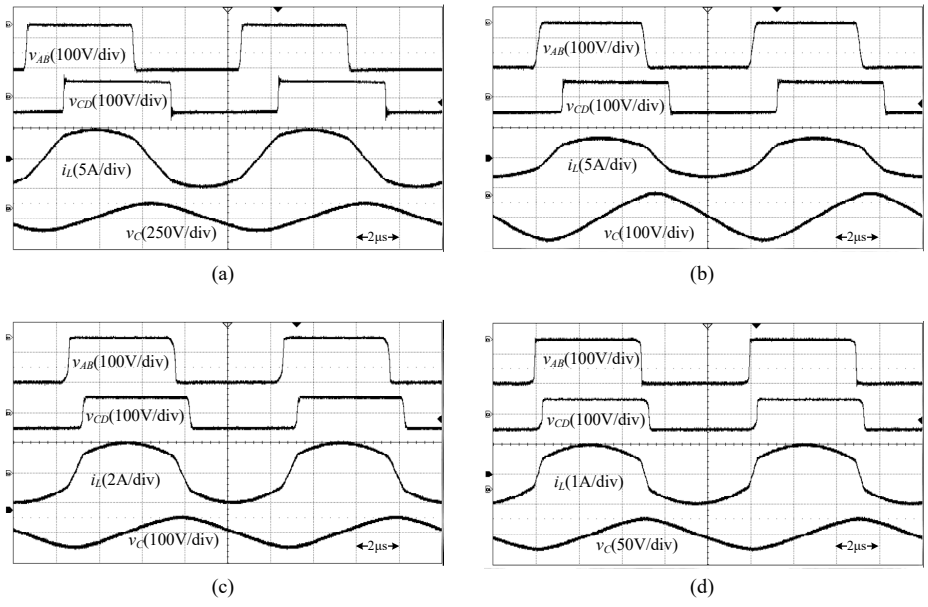


Figure 14. Experimental waveforms of different power levels when $M = 0.5$: (**a**) P_o = 200 W, (**b**) P_o = 150 W, (**c**) P_o = 100 W, (**d**) P_o = 50 W.

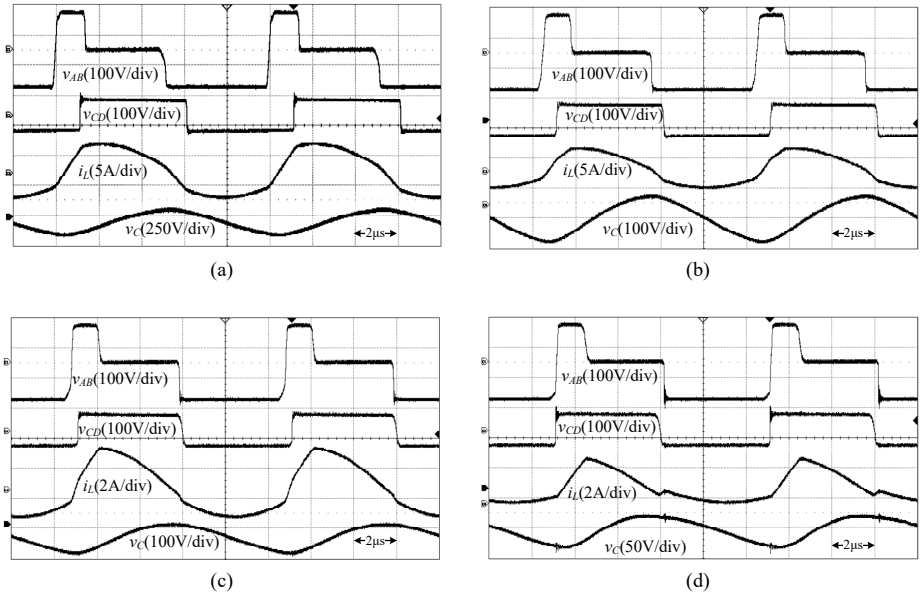


Figure 15. Experimental waveforms of different power levels when $M = 0.6$: (**a**) $P_o = 200$ W, (**b**) $P_o = 150$ W, (**c**) $P_o = 100$ W, (**d**) $P_o = 50$ W.

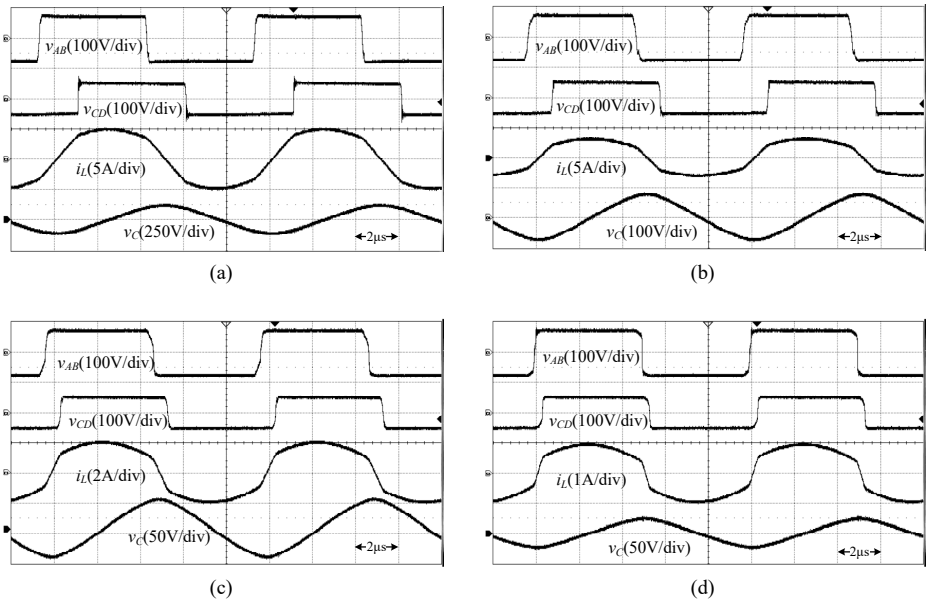


Figure 16. Experimental waveforms of different power levels when $M = 1$: (**a**) $P_o = 200$ W, (**b**) $P_o = 150$ W, (**c**) $P_o = 100$ W, (**d**) $P_o = 50$ W.

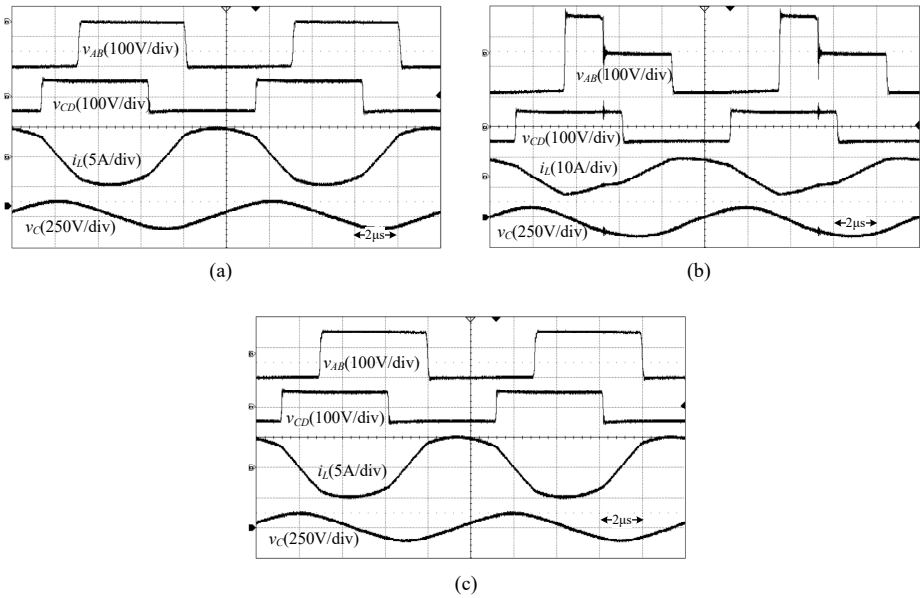


Figure 17. Experimental waveforms of different M when $P_o = -200$ W: (**a**) $M = 0.5$, (**b**) $M = 0.6$, (**c**) $M = 1$.

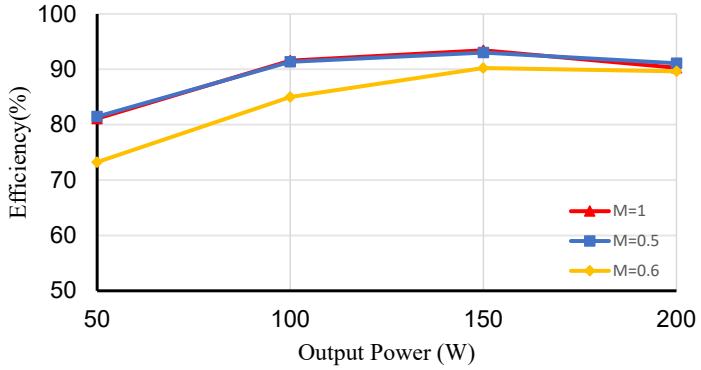


Figure 18. Measured efficiency at different load levels with different M in forward mode.

5. Conclusions

In this paper, a H-DBRC with VMM strategy is proposed for wide voltage range applications. The converter can operate in full-bridge state and half-bridge state to realize wide input voltage operation without adding any auxiliary circuit. As a result, it has significant advantages: (1) Low cost and simple control of a simple circuit. (2) The converter can always keep voltage match, and the voltage gain M expands from 1 to 0.5 with high performance. (3) At $M = 0.5$ and $M = 1$, optimum ZVS operation and minimal circulating current are realized. (4) The bidirectional power flow could be achieved with similar effects and the steady-state solution for both forward and backward modes could be obtained uniformly. The operation principle, soft-switching characteristics, and component design are analyzed in detail in this paper. A 200 W prototype is designed to validate the proposed converter and modulation scheme. The converter operates at 100 kHz with a varying input voltage from 75 V to 150 V and an output voltage of 100 V. A maximum efficiency of 93.43% is obtained when $M = 1$. Due to the wide voltage range operation, the efficiency decreases at light load with high conduction loss. Therefore, the selection of power devices and the design of the magnetic components are very important, which require further investigation in the future.

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