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Processing–Structure–Performance Relationship in Organic Transistors: Experiments and Model

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Abstract: In this paper, organic thin film transistors with different configurations are fabricated, and the effect on their performance when tailoring the semiconductor/insulator and semiconductor/contact interfaces through suitable treatments is analyzed. It is shown that the admittance spectroscopy used together with a properly developed electrical model turns out to be a particularly appropriate technique for correlating the performance of devices based on new materials in the manufacturing methods. The model proposed here to describe the equivalent metal–insulator–semiconductor (MIS) capacitor enables the extraction of a wide range of parameters and the study of the physical phenomena occurring in the transistors: diffusion of mobile ions through the insulator, charge trapping at the interfaces, dispersive transport in the semiconductor, and charge injection at the metal contacts. This is necessary to improve performance and stability in the case, like this one, of a novel organic semiconductor being employed. Atomic force microscopy images are also exploited to support the relationship between the semiconductor morphology and the electrical parameters.

Keywords: admittance; interfaces; modeling; OTFT; performance; processing; spectroscopy

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1. Introduction

Organic materials have gained wide interest in many emerging industrial applications, being particularly suitable where low-cost production, flexibility, and wearable devices are required [1,2]. Great strides have been made in the synthesis of new materials, thanks to the possibility of modifying the electrical properties through their microstructure [3–5]. However, organic devices, such as organic thin film transistors (OTFTs), require an in-depth study of the physical phenomena responsible for their electrical behavior [6,7]. The models developed for inorganic materials do not always adapt to organic technology, and therefore, numerical simulations and suitable analytical models are needed to understand and predict the device behavior, especially when new architectures or newly synthesized materials are used [8–10].

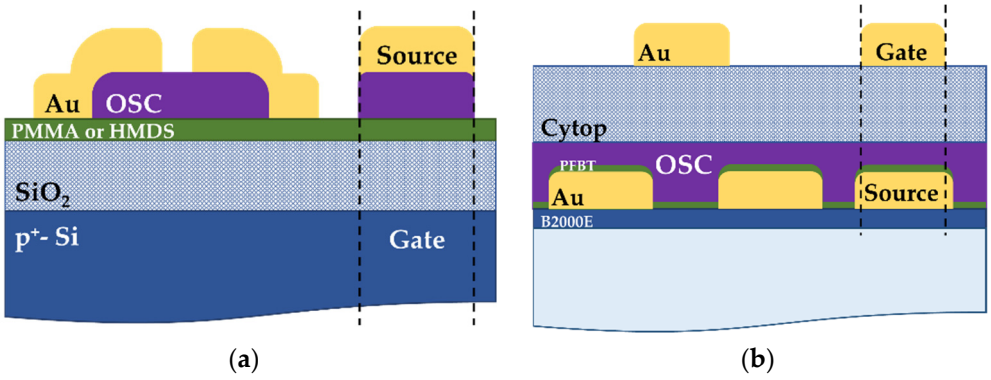
Device stability and performance strongly depend on the materials chosen, on the interfaces formed between the various active layers, on the processes used for deposition, and on the additional treatments. In this work, OTFTs based on a novel organic semiconductor were fabricated using different configurations and interface treatments and were electrically characterized. In order to investigate the relationship between the manufacturing parameters, the film morphology observed by atomic force microscopy (AFM), and the electrical characteristics, the admittance spectroscopy technique was employed. This consists of measuring the complex admittance of the equivalent metal–insulator–semiconductor (MIS) capacitor, which constitutes the OTFT core structure, by varying the bias in order to observe the various operating regimes and the frequency of the AC small signal in order to change the occupancy of the energy levels and investigate the response of slow

and fast species to the electric field [11]. A suitable model is needed to correctly interpret the measurements. In the literature, various models based on an equivalent circuit with different numbers of elements have been used to describe organic devices for various applications [12–17]. The model proposed in this paper accurately describes the experimental data, distinguishing the bulk and interface properties and providing a wide range of OTFT electrical and physical parameters, allowing for optimizing the fabrication process. The model was previously found to be effective in extracting the electrical parameters in transistors based on pentacene, which is a widely used organic semiconductor, and on various gate insulators, both inorganic and organic, in order to highlight the characteristics of the insulator–semiconductor interface [18,19]. In this paper, it is used to investigate a newly synthesized semiconductor and justify the results obtained with DC characterization [20].

2. Materials and Methods

OTFTs were built in two architectures: bottom-gate/top-contact (BG/TC) and top-gate/bottom-contact (TG/BC). The semiconductor, processed by thermal evaporation, was the organic molecule C6-NTTN, where the intermediate π-unit contained thienothiophene, and the terminal π-units contained alkyl-substituted naphthalene [20].

The BG/TC devices (Figure 1a) were built on a p-Si substrate, acting as the bottom gate contact, covered by silicon dioxide (SiO_2) with a thickness of 300 nm, acting as the gate dielectric. In order to analyze the effect of the dielectric surface energy, aside from the bare substrate, other gate insulators were obtained by covering the silicon oxide with a spin-coated thin film (15 nm thick) of poly(methyl methacrylate) (PMMA) or a self-assembled monolayer (SAM) of hexamethyldisilazane (HMDS). The organic semiconductor (OSC) was then evaporated, yielding a 60-nm thick film. In order to analyze the effect of the temperature at which the substrate was maintained during the semiconductor deposition, two high temperatures were employed for the HMDS-treated devices aside from room temperature (RT): 90 °C and 120 °C. On the top, the Au source and drain electrodes were evaporated with a thickness of 50 nm and an aspect ratio of 10 using a shadow mask.



(**a**) (**b**)

Figure 1. Cross-sections of the fabricated OTFTs and, bounded by the dashed lines, the equivalent MIS capacitors in (**a**) BG/TC configuration and (**b**) TG/BC configuration.

The TG/BC devices (Figure 1b) were built on a glass substrate covered by a Polyera ActivInk® B2000E buffer polymer layer. The gold contacts were evaporated with a thickness of 50 nm. In order to study the effect of contact modification, aside from bare gold contacts, the SAM pentafluorobenzenethiol (PFBT) was spin-coated onto the substrate, thus changing both the substrate surface energy (hydrophobicity increased) and the metal work function (from 5.1 eV of gold to 5.35 eV) [21]. Then, the OSC was deposited by thermal evaporation at room temperature, affording a thickness of about 50 nm. The insulator layer was deposited by spin-coating Cytop at 3000 rpm for 60 s and subsequently annealing it at 100 °C, obtaining a thickness of 390 nm. Finally, a gold gate electrode was evaporated.

For each sample, the equivalent metal–insulator–semiconductor (MIS) capacitor was fabricated on the same substrate by depositing a single contact, referred to as the source, superimposed on the gate contact (Figure 1).

All measurements were developed at room temperature in ambient air. OTFT transfer curves were collected at V_{GS} between −60 V and 20 V, and characteristic electrical parameters, such as the field effect mobility μ_{FE}, threshold voltage V_{TH}, and subthreshold swing SS, were estimated by averaging the results of 6 devices for each configuration, using the following channel current equation in the saturation regime:

$$I_{DS} = \frac{W}{2L} C_i \mu_{FE} (V_{GS} - V_{TH})^2, \quad (1)$$

where W and L are the channel width and length, respectively, C_i is the dielectric capacitance, and V_{GS} is the gate source voltage. V_{TH} and μ_{FE} were evaluated as the V_{GS}-axis intersection and from the slope of the tangent to $(I_{DS})^{1/2}$, respectively.

The complex admittance of the MIS capacitors was measured using an Agilent E4980A LCR meter by superimposing a small signal of 10 mV to the DC bias. V_{GS} was swept from −40 V to 20 V, while the small signal frequency was between 200 Hz and 2 MHz. The admittance $Y(\omega)$ was studied according to the parallel model through the capacitance C_P and the loss L_P (the loss is the conductance G_P divided by the angular frequency ω and takes account of the energy dissipated by the device) and is expressed as follows:

$$Y(\omega) = j\omega C_P(\omega) + G_P(\omega) = j\omega[C_P(\omega) - jL_P(\omega)]. \quad (2)$$

The dielectric capacitance was extracted by measuring the equivalent metal–insulator–metal (MIM) device fabricated on each substrate. The bare, PMMA-, and HMDS-treated SiO_2 had capacitances of 11.5, 9.5, and 11.2 nF/cm^2, respectively, whereas the Cytop film's was 4.7 nF/cm^2.

The most meaningful results obtained from the electrical characterizations are discussed in relation to the semiconductor morphology obtained through AFM.

3. Results

The representative transcharacteristics of the seven fabricated OTFTs in the saturation regime are compared in Figure 2. All devices were p-channel transistors with long-term stable characteristics. Observing the results obtained in the BG/TC configuration with an RT deposition, the worst features were detected in the bare SiO_2-based OTFT, with a mobility of about 0.03 cm^2/V·s and an average threshold voltage of −63 V. The insulator surface treatment improved the performance, with an increase in mobility to 0.09 and 0.11 cm^2/V·s on the PMMA and HMDS, respectively, and a shift in V_{TH} to −60 and −35 V, respectively.

Regarding the effect of the substrate temperature, an increase in mobility up to a maximum of 0.16 cm^2/V·s at 90 °C and a worsening at 120 °C, with an average value of 0.1 cm^2/V·s, were observed. The threshold voltage, on the other hand, did not exhibit an evident relationship with the temperature, thus proven to result from the combination of multiple effects. The subthreshold swing showed the same trends of mobility in all the previous cases, demonstrating the existence of a strong relationship between the carrier mobility measured in the channel and the trap density at the interface with the insulator that could be extracted from SS [20].

Finally, regarding the results obtained for the samples in the top-gate configuration, the strongest effect due to PFBT treatment was observed in V_{TH}, which translated from −11 V on bare substrate to about 0 on the treated contacts, while the increase in μ_{FE} from 0.02 to about 0.03 cm^2/V·s was less significant. These variations could be attributed to the modification of both the metal work function and the substrate surface energy.

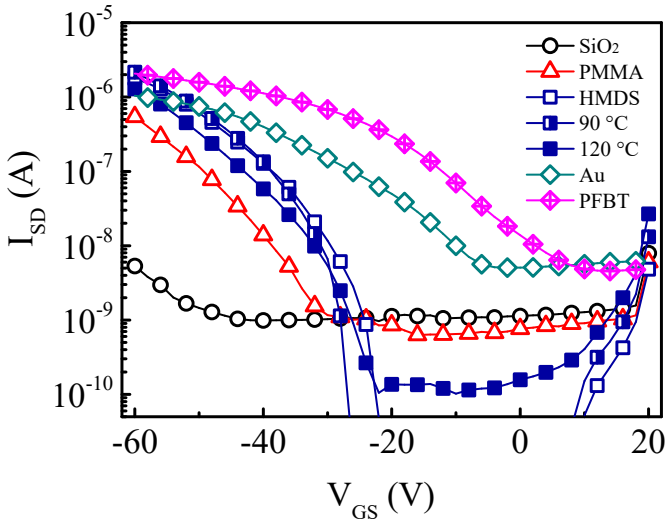


Figure 2. Typical transcharacteristics of the fabricated OTFTs at V_{SD} = 60 V. For the BG devices, open, half-solid, and solid symbols denote the semiconductor deposition at RT, 90 °C, and 120 °C, respectively, while the different colors indicate the various insulator interfaces (SiO_2, PMMA, and HMDS). TG devices are denoted by diamond symbols, of which the cross-centered one indicates the Au contact functionalization (PFBT).

The admittance curves (reported in the discussion section) show some common features. First of all, the maximum value of the capacitance at a low frequency was measured in accumulation and was close to the insulator capacitor C_i. Moving toward the depletion regime, as the voltage varied, the overall capacitance decreased, since it corresponded to the series sum of C_i and the depletion capacitance C_D.

On the other hand, as the frequency increased, three main dispersion events were observed, corresponding to a peak in the loss curve and a simultaneous reduction in capacitance. As can be easily seen from the appearance of the loss peaks, these dispersions had different properties and were representative of distinct phenomena. The first peak observed in the depletion regime at low frequencies moved with the bias but did not change significantly in amplitude, demonstrating the presence of traps in the channel area (i.e., near the semiconductor/insulator interface). The second peak shifted slightly in frequency while significantly decreasing in amplitude with bias, showing a correlation with the semiconductor bulk characterized by a dispersive transport. Finally, a third peak appeared at a high frequency and, being approximately constant both in frequency and in amplitude, it could be associated with a series resistance of the metal contact. Due to the overlap in frequency of these phenomena and their complex interaction, it is necessary to develop an appropriate model for correct data interpretation and the complete extraction of the device parameters.

4. Model

The model proposed for the data interpretation is an electrical circuit (Figure 3) whose elements describe the physical processes occurring in the various layers and at the different interfaces of the organic MIS device [18,19].

The gate insulator layer is defined by the parallel connection of the capacitor $C_i = \varepsilon_i / t_i$, where ε_i and t_i are its permittivity and thickness, respectively, and the constant phase element (CPE). The latter is expressed as:

$$Y_\delta = A_{diff}(j\omega)^{1-\delta}. \quad (3)$$

It describes the anomalous diffusion of slow ions through the insulator [22], presumably water molecules, responsible for the forth weak dispersion occurring at very low

frequency. A_{diff} depends on the diffusing particle density, and $0 < \delta < 0.5$ defines the continuous time random walk ($\delta = 0.5$ corresponds to normal diffusion).

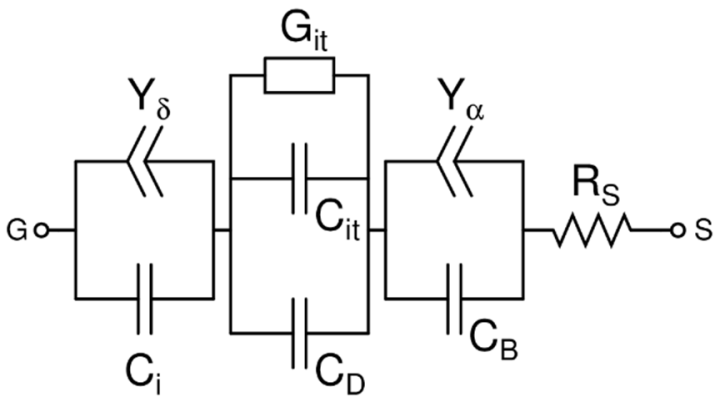


Figure 3. Organic MIS capacitor equivalent circuit.

The semiconductor film, which is divided into a depleted layer and a bulk region whose widths vary with the bias, is described by the series combination of the depletion capacitor $C_D = \varepsilon_{osc}/w_D$, where ε_{osc} and w_D are the OSC permittivity and depletion width, respectively, and the bulk capacitor $C_B = \varepsilon_{osc}/(t_{osc} - w_D)$, where t_{osc} is the OSC thickness.

The effect of trapping at the semiconductor/insulator interface, generating the first main loss peak at a low frequency, is represented by the combination of the capacitor C_{it} and the conductance G_{it} in parallel to C_D, giving the following expression for the depletion layer admittance [23]:

$$Y_D = j\omega\left[C_D + \frac{qD_{it}}{\omega\tau_{it}}tan^{-1}(\omega\tau_{it})\right] + \frac{qD_{it}}{2\tau_{it}}ln\left[1 + (\omega\tau_{it})^2\right], \quad (4)$$

where the presence of a continuous distribution of states with density D_{it} and relaxation time constant τ_{it} is assumed. The structural disorder of the OSC bulk, the cause of the dispersive transport, is described by a CPE in the form $Y_\alpha = G_B(j\omega\tau_B)^\alpha$, placed in parallel with C_B to provide the following bulk admittance according to the Cole–Cole theory [24]:

$$Y_B = j\omega C_B\left[1 + (j\omega\tau_B)^{\alpha-1}\right], \quad (5)$$

where $0 < \alpha < 1$ is the dispersion parameter and τ_B is the OSC relaxation time. It imposes an upper limit on the frequency up to which the injected holes are able to follow the applied AC signal and therefore is responsible for the second main loss peak.

The back contact is, finally, represented by the series resistance R_S, which describes the quality of the semiconductor/metal interface and is responsible for the loss peak at a high frequency.

The model equations were simulated for the seven devices in order to reproduce the experimental data of the complex admittance. While the capacitances of the insulator and OSC layers, in addition to all the known physical and geometrical parameters, were kept constant, all the other parameters were extracted by fitting the simulated curves with the experimental data. A good fit with an average R^2 value of 0.999 was obtained.

Fundamental information, such as the onset voltage V_{ON}, the semiconductor doping density N_A, and the surface potential φ_S, were obtained from the dependence of the depletion layer width w_D, extracted from C_D, on the bias using the following equations:

$$w_D = \frac{\varepsilon_{osc}}{C_i}\left[\sqrt{1 + \frac{2C_i^2}{qN_A\varepsilon_{osc}}(V_{GS} - V_{ON})} - 1\right], \quad (6)$$

$$\varphi_S = E_T - E_F = \frac{qN_A w_D^2}{2\varepsilon_{osc}}, \quad (7)$$

where E_T is the interface trap level accessible at a band bending φ_S and E_F is the bulk Fermi level.

5. Discussion

The results obtained by admittance spectroscopy are reported and discussed below, with the aim of correlating the process parameters with the electrical performance. In particular, the effects on the electrical characteristics of the treatment of the insulator surface, of the substrate temperature during semiconductor deposition, and of the metal contact modification are discussed. In addition, the differences between the two device architectures are analyzed. AFM images are reported to support discussion when significant differences have been detected.

5.1. Effect of Insulator Surface Treatment

The admittance curves of the devices deposited at RT on different insulators are reported in Figure 4, and the extracted parameters are in Table 1. In the comparison between the bare and treated silicon oxide, a significant parameter was A_{diff}. While δ was equal to about 0.2 for all insulating films, indicating an anomalous diffusion, A_{diff} had lower values in the presence of PMMA and HMDS, showing their effectiveness in counteracting the absorption of water and the diffusion of mobile ions through the insulator by forming a barrier. The methyl methacryl groups of PMMA and the methyl groups of HMDS formed a hydrophobic surface, which on the one hand improved the growth of the OSC film, as shown by the increased mobility in the channel, and on the other hand blocked the charge injection from the channel, as shown by the reduction in OTFT leakage currents.

In addition, the doping density N_A, lower for the PMMA and even more for the HMDS, demonstrated an improvement in the OSC morphology which, as reported in Figure 5, became more homogeneous and interconnected thanks to the more hydrophobic substrate.

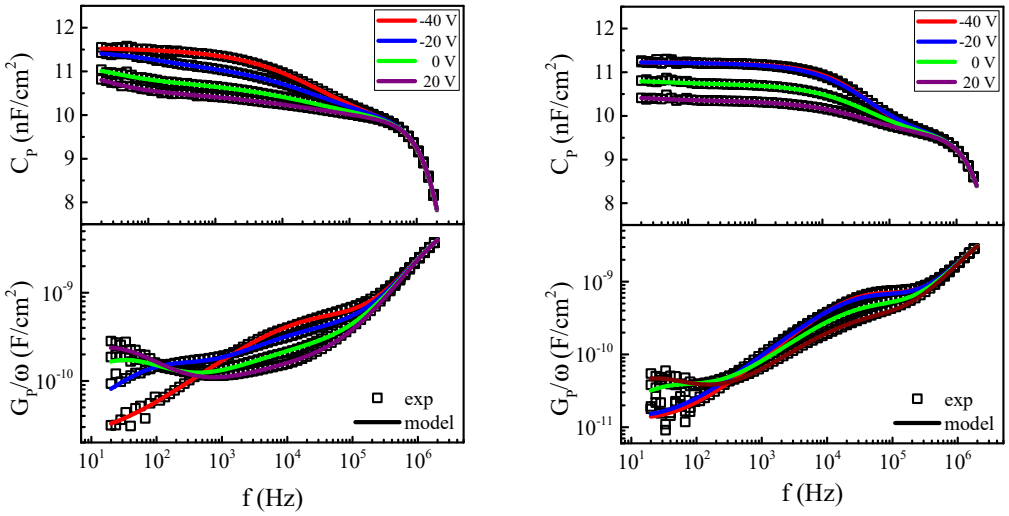
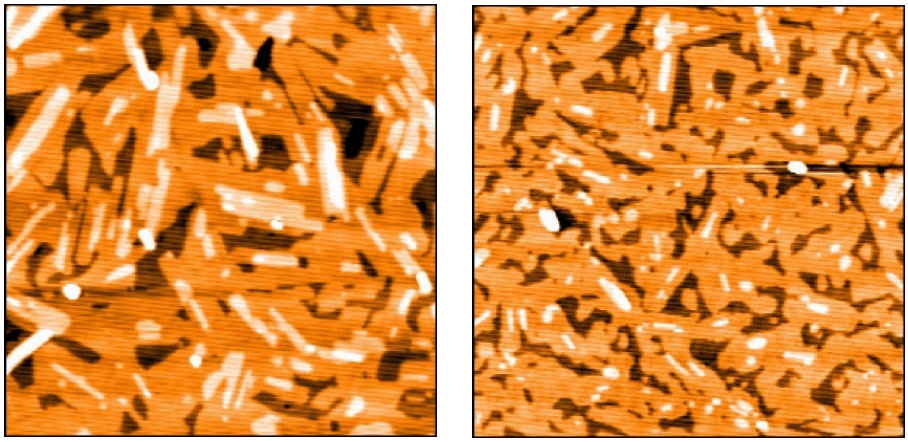


Figure 4. Admittance curves of MIS devices with semiconductor deposited at RT on (**a**) SiO_2 and (**b**) SiO_2/HMDS. Model curves (solid lines) are superimposed on the experimental data (squared symbols).

The lower values of ρ_{OSC} and α for the treated substrates show that the properties of the bulk semiconductor were improved, while the values of D_{it} demonstrate a reduction of the traps which, located at the interface with the insulator, limited the charge transport. An inverse proportionality between D_{it} and μ_{FET} was observed.

Table 1. Model parameters extracted for OTFTs in BG configuration on different insulator layers.

Insulator	μ_{FET} (cm^2/Vs)	A_{diff} ($F(rad/s)^{\delta}$)	V_{ON} (V)	N_A (cm^{-3})	D_{it}^{max} ($cm^{-2}eV^{-1}$)	ρ_{osc}^{min} ($M\Omega \cdot cm$)	α^{av}	R_S ($\Omega \cdot cm^2$)
SiO_2	0.03	1.1×10^{-10}	−37	1.2×10^{18}	1.1×10^{13}	9.6	0.54	4.5
SiO_2/PMMA	0.09	9×10^{-11}	−25	1.1×10^{18}	7×10^{12}	8.1	0.43	3.5
SiO_2/HMDS	0.11	8×10^{-11}	−14	8.3×10^{17}	3.7×10^{12}	7.1	0.3	4

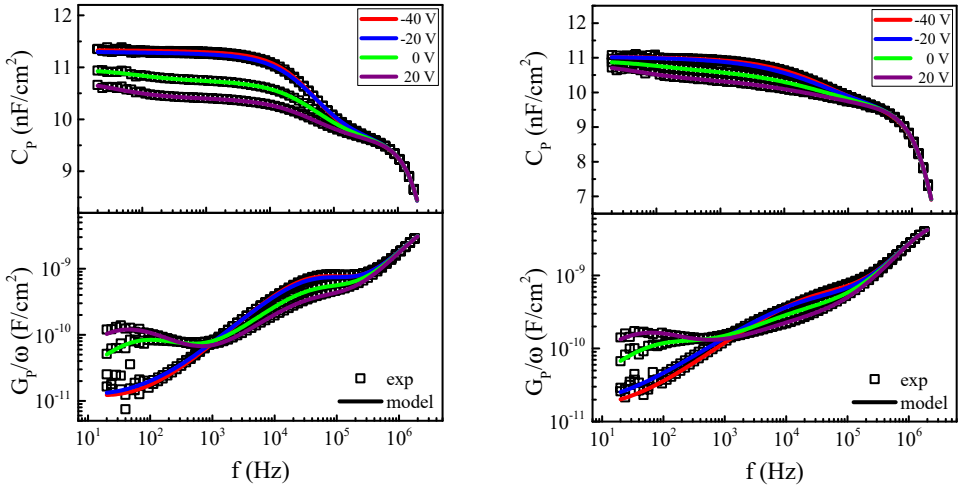


(**a**) (**b**)

Figure 5. AFM images (5 μm × 5 μm) of OSC film deposited at RT (**a**) on SiO_2 and (**b**) on SiO_2/HMDS.

5.2. Effect of the Substate Temperature

The admittance curves of the devices with semiconductors deposited on HMDS at higher temperatures are reported in Figure 6. The parameters extracted through the model (Table 2) show that the main effect of the increase in substrate temperature during deposition was improvement of the OSC conductivity, with a reduction in both the interface traps and bulk dispersion, while an excessive increase in temperature led to a deterioration in performance.



(**a**) (**b**)

Figure 6. Admittance curves of MIS devices with semiconductor deposited on SiO_2/HMDS at (**a**) 90 °C and (**b**) 120 °C. Model curves (solid lines) are superimposed on the experimental data (squared symbols).

Table 2. Model parameters extracted for OTFTs in BG configuration on SiO_2/HMDS insulator for different substrate temperatures during OSC deposition.

Temperature	μ_{FET} (cm^2/Vs)	A_{diff} ($F(rad/s)^{\delta}$)	V_{ON} (V)	N_A (cm^{-3})	D_{it}^{max} ($cm^{-2}\,eV^{-1}$)	ρ_{osc}^{min} (MΩ·cm)	α^{av}	R_S (Ω·cm^2)
RT	0.11	8×10^{-11}	−14	8.3×10^{17}	3.7×10^{12}	7.1	0.3	4
90 °C	0.16	8×10^{-11}	−20	9.2×10^{17}	2.7×10^{12}	6.8	0.22	4.2
120 °C	0.1	8×10^{-11}	−16	1.3×10^{18}	4.9×10^{12}	7.7	0.45	5

The AFM images of the semiconductor film collected on HMDS show that the increase of the substrate temperature induced the creation of wider grains (Figure 7) thanks to the enhanced molecular diffusion on the substrate surface allowing a layer-by-layer film growth [25]. This phenomenon justifies the mobility improvement and confirms the reduction in the trap density at 90 °C. However, the temperature increase made the growing aggregates less interconnected. Indeed, for the semiconductor deposited at 120 °C, wide gaps separated the polycrystalline domains, according to the higher trap density responsible for the reduction in mobility μ_{FE}.

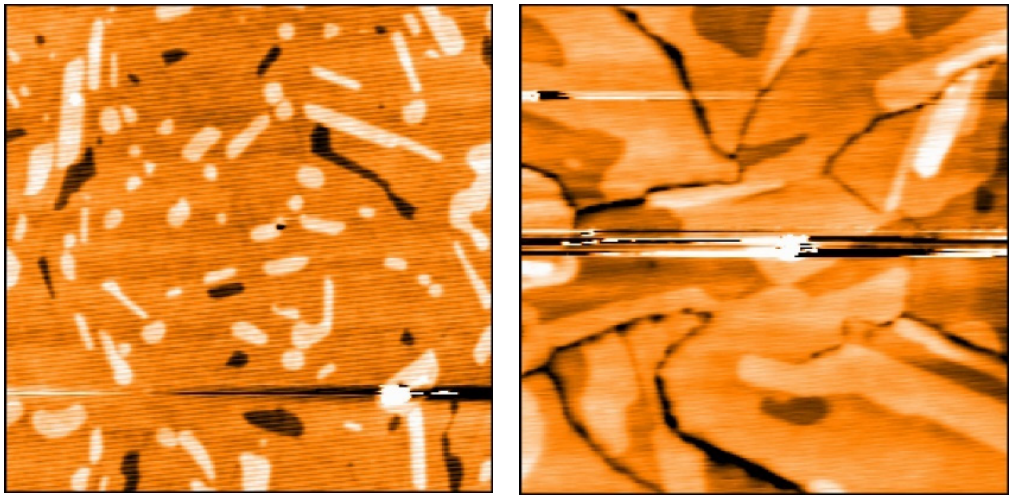


Figure 7. AFM images (5 µm × 5 µm) of OSC film deposited SiO_2/HMDS at (**a**) 90 °C and (**b**) 120 °C.

5.3. Effect of Contact Modification

Admittance experimental data and model curves comparing devices in the TG/BC configuration with bare and treated contacts are shown in Figure 8. The model parameters, reported in Table 3, demonstrate that the improvement in the OTFT threshold voltage, which was a fitting parameter derived from the MOSFET theory valid for the operation with channel inversion, could actually be explained as the translation of the onset voltage, which was instead associated with the flat band condition and directly depended on the channel area and contact properties. In this case, when comparing the V_{ON} and R_S values, it is evident that the reduction in the onset voltage was due to a significant decrease in the contact resistance. The AFM images showed no significant difference in the semiconductor morphology, confirming that the PFBT treatment mainly modified the contacts. Due to the increase in the Au function, a flow of electrons coming from the semiconductor was established toward the metal and up to its Fermi level pinning, causing p-type OSC doping at the metal interface [26] and onset voltage shift to the right [27].

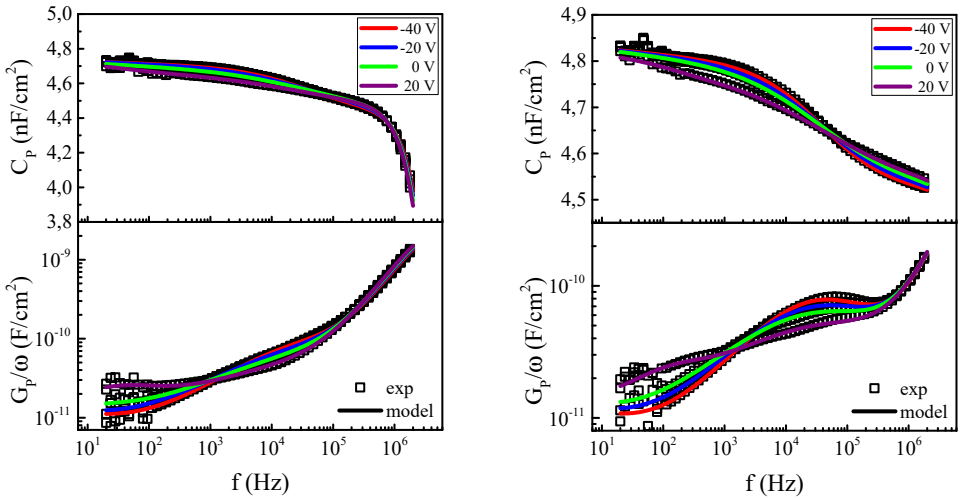


Figure 8. Admittance curves of MIS devices with (**a**) bare Au contacts and (**b**) PFBT-treated contacts. Model curves (solid lines) are superimposed on the experimental data (squared symbols).

Table 3. Model parameters extracted for OTFTs in TG configuration with different contacts.

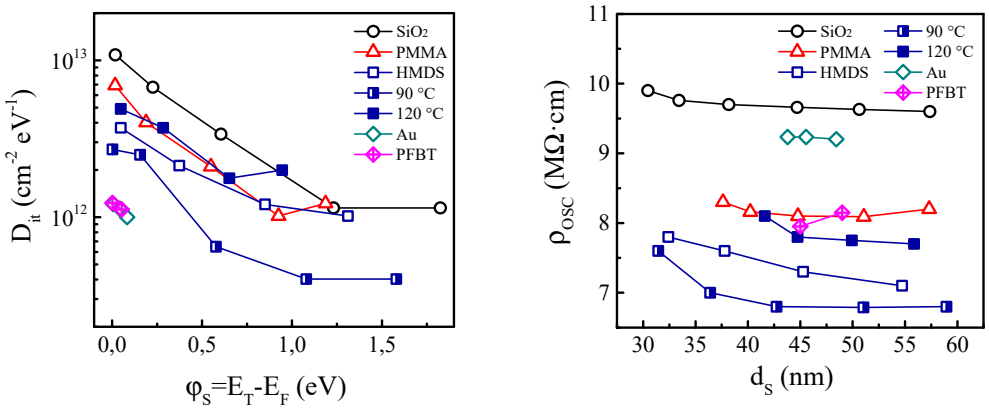
Contacts	μ_{FET} (cm^2/Vs)	A_{diff} ($F(rad/s)^{\delta}$)	V_{ON} (V)	N_A (cm^{-3})	D_{it}^{max} ($cm^{-2}\,eV^{-1}$)	ρ_{osc}^{min} (MΩ·cm)	α^{av}	R_S (Ω·cm^2)
Au	0.02	7×10^{-11}	−3	1.1×10^{18}	1.2×10^{11}	9.2	0.52	6
Au/PFBT	0.03	7×10^{-11}	7	10^{18}	1.3×10^{11}	7.9	0.49	0.6

5.4. Effect of the Device Architecture

The BG/TC device configuration had the advantage of allowing access to the surface of the gate insulator in order to perform treatments before the semiconductor deposition and directly improve the channel area, while the TG/BC geometry also allowed electrode modification before the OSC deposition and was appreciable for the superior position of the dielectric, which also acted as a barrier to the environment.

A fundamental parameter of comparison between the two architectures is the interface trap density. The values of D_{it}, which were extracted from C_{it} and G_{it} and reported in Figure 9a as a function of the surface potential φ_S, showed the presence of an approximately exponential distribution. Furthermore, from the comparison between the two architectures, it is evident that the interface created between the semiconductor and the Cytop insulator in the TG configuration was better than that formed with bare or treated silicon oxide in the BG configuration. Despite this, the resulting channel mobility and the bulk conductivity (Figure 9b) in the TG/BC devices was lower than the other case, and it was not significantly improved through the treatment of the lower surface (i.e., the metal contact). The latter, in fact, could induce a strong variation only in a solution-deposited film, where the surface roughness reduced, or in the first layers of a thermally evaporated semiconductor [18,28].

The results obtained from the admittance analysis show that various factors contributed to the reduction of the threshold voltage. Among these was the OSC film morphology, due to the molecule nucleation process, which was affected by the substrate surface energy. The model parameters, and in particular the dispersion parameter values of the organic semiconductor in both configurations, demonstrate that a hydrophobic substrate was preferable because, as observed in the BG devices with PMMA and HMDS treatments and in the TG devices with PFBT treatment, it reduced the structural defects [29].



(**a**) (**b**)

Figure 9. (**a**) Interface density of states as a function of surface potential and (**b**) average resistivity of the OSC bulk of thickness d_s next to source contact. For BG devices, open, half-solid, and solid symbols denote the semiconductor deposition at RT, 90 °C, and 120 °C, respectively, while the different colors indicate the various insulator interfaces (SiO_2, PMMA, and HMDS). TG devices are denoted by diamond symbols, of which the cross-centered one indicates the Au contact functionalization (PFBT).

The further improvement in V_{TH} observed in the TG/BC devices could be attributed to two other elements. One is the stability of Cytop, as demonstrated by its reduced diffusion factor A_{diff}. Cytop is indeed an insulator rich in fluorine and free of hydroxyl groups, aspects that make it water-repellent and an effective barrier to the environment [30] with a consequent reduction in interface trapping, as confirmed by the lower trap density revealed in the TG devices. The other one is the increase in the work function of gold for the effect of the thiol. Admittance spectroscopy showed that the contact resistance reduced thanks to the metal modification.

6. Conclusions

An electrical model was proposed to extract the significant parameters of OTFTs, characterized through admittance spectroscopy, with the aim of understanding the physical phenomena underlying the device operation and the relationship between the fabrication processes and the electrical performance. This is particularly useful in the case of devices based on novel materials and for the comparison of different treatments.

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