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A 60GS/s Two-Stage Sampler with a Linearity Calibration Loop for PAM-8 Receivers

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Abstract: In this article, we show a 60 GS/s two-stage 8 × 8 time-interleaved sampling circuit, where the second-stage nonlinearity can be controlled by using the voltage that optimizes the static distortions of the sampler. A calibration algorithm can extract the nonlinear contributions of the stages and compensate for them by setting the optimal bias voltage. This can also be used to cancel the front-end nonlinear effects. The sampler was verified by implementing it in TSMC 5 nm FinFET, and a calibration system in a Pulse Amplitude Modulation transceiver, detecting and minimizing the nonlinearities, is presented. The optimum voltage biasing of the sampler was obtained by co-simulating the circuit with the linearity calibration loop implemented in Verilog-A. The histogram of the sampled signal at the slicer input is shown before and after the calibration to show the improvement in the sampled eye opening. Moreover, the resulting bias is equal to the one that maximizes the total harmonic distortion in transient simulations with a 1 GHz input signal, obtaining a minimum of 48.5 dB of total harmonic distortion across different PVT conditions.

Keywords: PAM-8; SerDes receivers; track-and-hold; time-interleaved; linearity

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1. Introduction

Over the last decade, data traffic has increased due to the increasing demand for streaming services, video calling, etc., implying the necessity for high-speed transceivers for either backplane or optic fiber communications in data centers. Pulse Amplitude Modulation with four levels (PAM-4) [1–3] is the main modulation used in wire-line transceivers, in which there are four symbols, each one representing two bits. To further improve the data rate, we can either boost the symbol rate, with the heavy constraint imposed by the channel bandwidth, or increase the order of the modulation. Some solutions can be the PAM-8 [4–6] or another modulation using more than four symbols [7]. In particular, while sending the same number of symbols per second, the PAM-8 improves the bit rate of the receiver by 1.5 times. However, the smaller eye aperture of PAM-8 compared to PAM-4 or Non-Return-to-Zero (NRZ) makes this modulation format very sensitive to noise, distortions, and residual inter-symbol interference (ISI). These effects increase the bit error rate of the system. The ISI and the noise can be reduced with higher current consumption (less noisy analog components and a feed forward equalizer with a higher number of taps). On the other hand, the distortions are not easy to minimize. With the reduction in the supply voltage in advanced technology nodes, the circuits increment their compressing behavior on the signal (lower total harmonic distortion (THD)) for the same dynamic range, needed to maintain a valid signal-to-noise Ratio (SNR). In Figure 1, (a) the symbol error rate (SER) and (b) the mean square error (MSE) are plotted to the varying SNR for various analog front-end (AFE) THD obtained through a MATLAB model of a PAM-8 receiver, as in [8]. The THD represents the static nonlinearities modeled with a Taylor approximation of the components' input–output characteristics. While this model has some limitations, it shows how linearity affects the system performance in some scenarios. The plots show an improvement in the MSE and SER for higher THD values and performance

approaching the ideal case for 50 dB, meaning this value should be a target for the analog circuit design.

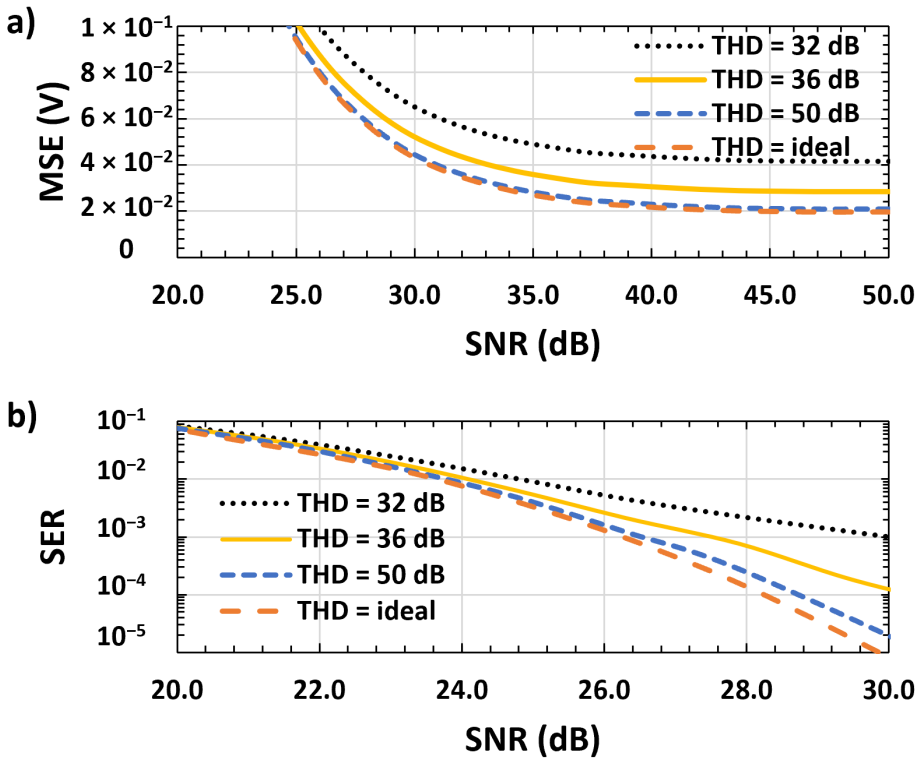

Figure 1. (**a**) MSE and (**b**) SER with the varying of SNR for various THD [8].

To maximize the system performance, the THD, especially of critical blocks such as the track and hold (TH) of time-interleaved (TI) receivers, needs to be optimized through calibration as a consequence of the low circuit linearity across PVT in scaled technology nodes. This solution is normally adopted in the reduction in distortions derived from the interleaved channels mismatches [9,10]. In the literature, the calibration of static distortion is rare [11,12], and no co-simulation nor indepth modeling of AFE components is introduced in the system simulation. The scope of this paper is to find a TI-TH circuit capable of achieving through calibration a receiver THD of the order of 50dB across different PVT conditions to maximize the performance of a PAM-8 receiver (RX). Here, we show the TI sampler presented in [8] using an improved and simpler calibration loop compared to the cited one, where the complexity scales with the number of nonnegligible residual ISI pre- and post-cursors, and a gain error can introduce a component that does not let the system set to the desired value. The proposed loop uses an algorithm that eliminates the errors given by the gain and residual ISI while having a fixed complexity. Furthermore, this improved calibration was implemented in cadence virtuoso with a Verilog-A model, and its performance was verified via co-simulation with the analog circuit, while in [8] MATLAB, modeling of the analog was used.

This work is divided into three major sections. First, in Section 2, the implemented track-and-hold circuit is described, and its linear behavior with the control voltage is shown. Then, the calibration feedback loop is propose,d and its analytical functioning is described in Section 3. Lastly, Virtuoso co-simulation of the transistor-level TH circuit and Verilog-A receiver model were performed, and the simulation results are presented in Section 4.

2. Track-And-Hold Circuit

The diagram in Figure 2 depicts the architecture used for implementing the 64 TI sampler, sampling at 60 GS/s. The interleaving factor was obtained by using a cascade of two TI stages (8 × 8) working at 7.5 GS/s and 937.5 MS/s, respectively.

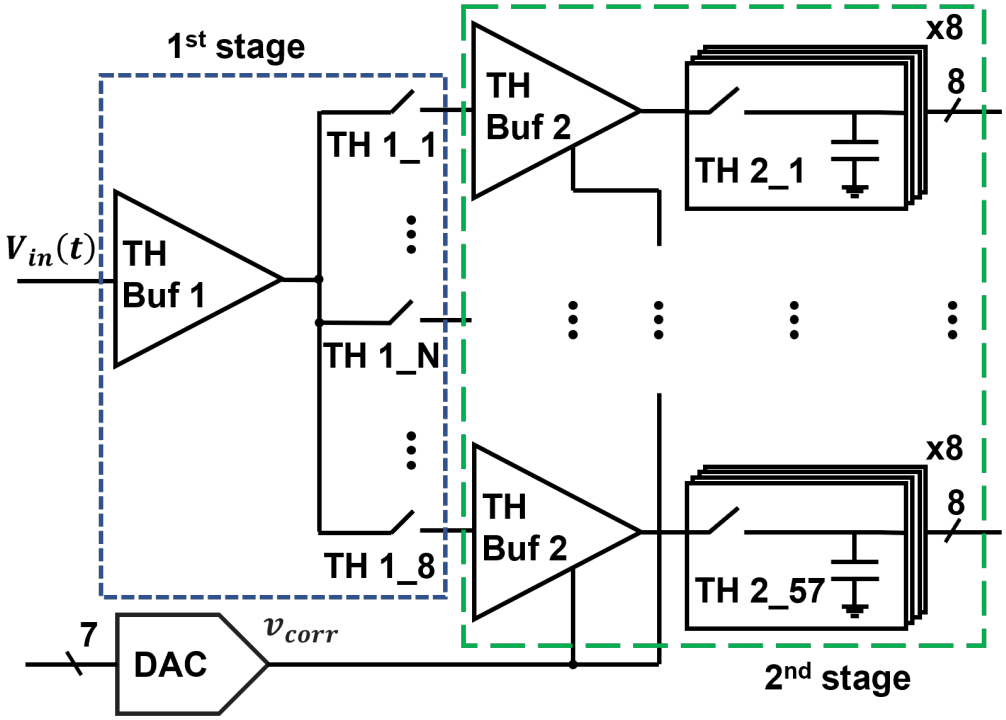

Figure 2. Block diagram of a 64 TI-TH circuit with in blue the first stage sampler and in green the second state , using a DAC for the second-stage buffer bias voltage control [8].

2.1. Circuit Implementation

The circuit described in [13], which implements the first sampling stage (TH buf1), samples the signal on one of eight capacitances at a time. One input signal sample is taken every 16.7 ps. A buffer (TH buf2) is then connected to each sampling capacitance. To implement the second stage interleaving operation, eight parallel switches are connected to the output of the second buffer. The switches are operated to sample the signal on one of the eight sampling capacitances at a time. The buffers composing the second stage sampler can be implemented with the circuits in [14,15], composed of an inverter followed by another one closed in a diode configuration. These circuits show good linearity because while the inverter decompresses the signal, the second one has an opposite behavior, compensating for each other's distortions. This approach has some limitations across process corners and temperatures stemming from the different variations of the linearity of the two blocks. To deal with this problem, we use the buffer topology depicted in Figure 3. The simple gm–gm topology is improved by varying the diode nonlinearity through the voltage v_{corr}, as in [8]. An optimal value of the gate voltage can be chosen to minimize the distortions of the front end.

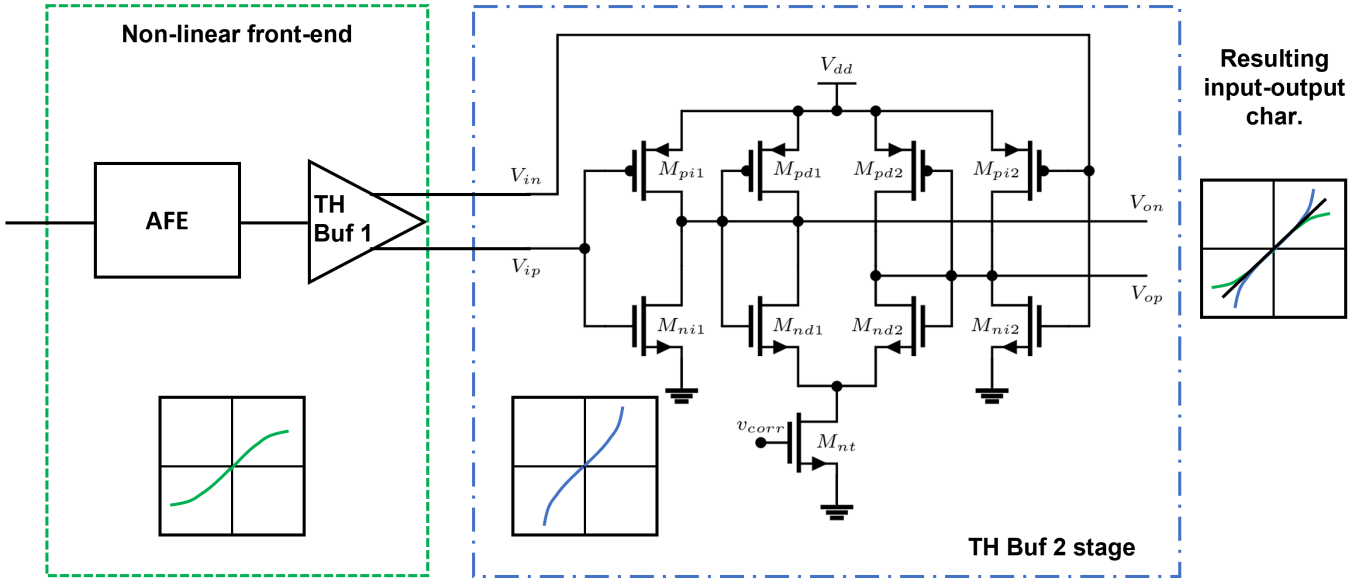

Figure 3. Second-stage TH buffer in blue with its distortion contribution compensating for the previous stages non-linear block in green [8].

2.2. Buffer Distortion Control

An easy way to understand how the distortion of the buffer varies for various values of v_{corr} is to plot, as shown in Figure 4, the relative error (ϵ_r) between the small signal gain for high-DC differential input V_S and the one for zero-DC differential input in different bias conditions:

$$\varepsilon_r = \frac{V_{outd}(V_S) - G_{AC}V_{ind}(V_S = 0)}{G_{AC}V_{ind}(V_S = 0)} \quad (1)$$

with G_{AC} being the small-signal DC gain, V_{outd} the differential small signal output, and V_{ind} the input one. By tuning v_{corr}, the input–output characteristic of the buffer can compensate not just for the buffer distortion but also for the static nonlinearities of the previous stages and AFE as well. This is represented in Figure 3, where the input–output characteristic of the AFE plus the first-stage sampler is schematized with the typical compressing behavior, and where the second-stage buffer with behavior that compensates for this compression is introduced. Unfortunately, the optimal v_{corr} for different PVT conditions may have considerable variations, thus a calibration that tracks the nonlinearities of the circuit becomes mandatory.

A further benefit of the calibration approach is that it may be able to identify the distortions of all the AFE and TH and maximize the THD performance of the system.

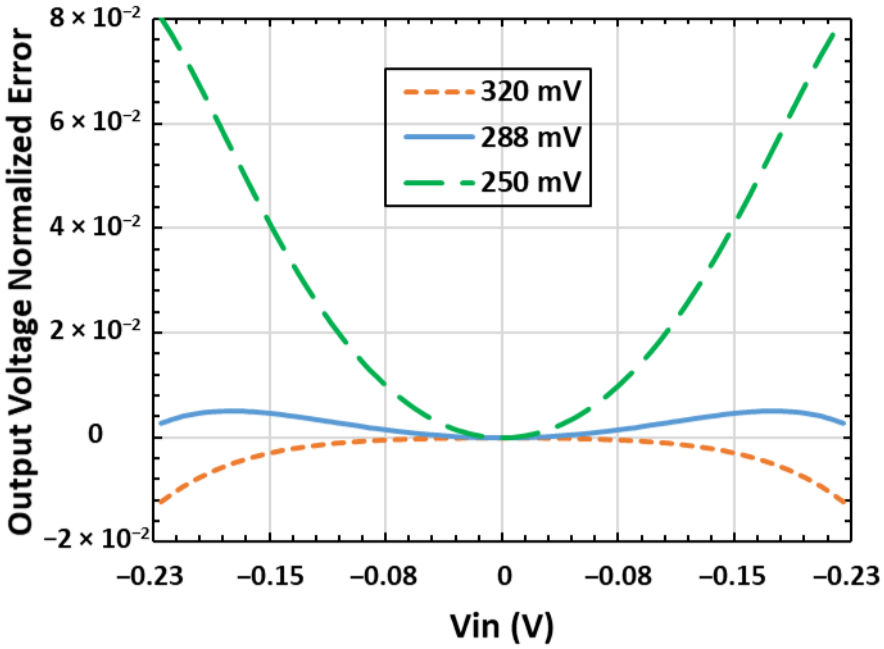

Figure 4. The ϵ_r with the varying of the large-signal differential input for various bias voltages v_{corr} [8].

3. Linearity Calibration Feedback Loop

In this section, we present a calibration loop that is suitable for a PAM-8 receiver. The PAM-8 receiver model used is represented in Figure 5. The transmitter, the channel (IEEE '802.3ck Ch2M - lim_3ck_01_ 0319_c2m_Channel6' with 30 dB loss at 30GHz), and the AFE transfer functions were modeled with the channel symbol. Their combined s parameters matrix (s_{ch}) filters the transmitted symbols and then feeds them to the two stages TH. In the analytical discussion of the model, the input–output characteristics that reflect the buffers' static distortions were modeled using a Taylor polynomial [8,11,12], which depended on v_{corr} in the second stage. For validation, the actual circuit was used.

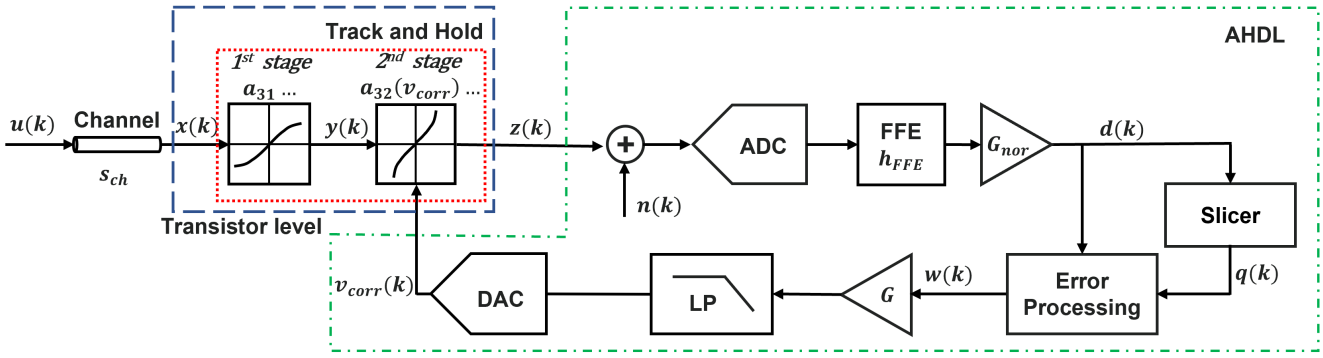

Figure 5. PAM-8 RX using the calibration loop with the transistor level components in blue and the Verilog-A model in green.

Before the signal was sampled by the ADC, the thermal noise was inserted. Then, the ISI introduced by the channel was reduced using a Feed-Forward Equalizer (FFE). The slicer converted soft decisions into hard decisions, and by proper digital processing of this information, the optimum value of v_{corr} was obtained. We used an ideal model to implement the DAC and ADC. The typical analog-to-digital converter can have a spurious free dynamic range (SFDR) of the order of 56 dB [16], which is negligible compared to

the THD of the TI-TH circuit. The digital-to-analog converter only requires a monotone input–output characteristic due to the loop's high gain capable of absorbing the small error derived from its nonlinearities. To better explain the mathematical operations, we take for granted that the circuit samples the signal on the optimum phase; hence, we assume the system works in a discrete time domain, and the channel was modeled with its impulsive response.

The signal sent by the transmitter $u(k)$ was convoluted with the channel impulse response obtaining $x(k) = G_{ch}u(k) \otimes h_{ch}(k)$, where h_{ch} is the equivalent impulse response of s_{ch}, and G_{ch} is the equivalent channel gain. After the distortion introduced by the TH circuit, we have:

$$z(k) = x(k) + a_3x^3(k) + a_5x^5(k) + a_7x^7(k) \tag{2}$$

with a_i being the Taylor coefficients of the overall analog front end, assuming the nonlinearities can be described with a Taylor expansion of the input–output characteristics. If we assume the FFE is optimal and we neglect the residual ISI, $d(k)$ can be written as:

$$d(k) = u(k) + G_{nor}[a_3x^3(k) + a_5x^5(k) + a_7x^7(k) + n(k)] \otimes h_{FFE}(k) \tag{3}$$

with $n(k)$ being the equivalent analog circuit noise with zero mean value and with $G_{nor} = \frac{1}{G_{ch}}$ being the digital gain, which normalizes the signal. The error at the slicer input $d(k) - q(k)$ can be multiplied by the hard decision $q(k)$, and assuming the slicer takes the correct decision $q(k) = u(k)$, (with the MATLAB model of the system in [8], it was verified this can be considered true for SER lower than around 15×10^{-3}) we can write:

$$w(k) = u(k)[d(k) - u(k)] = u(k)G_{nor}\{a_3x^3(k) + a_5x^5(k) + a_7x^7(k) + n(k)\} \otimes h_{FFE}(k). \tag{4}$$

$w(k)$ then multiplies the loop gain G, which is of the order of 10^6, and the result is filtered by a digital low-pass filter (it could also be implemented with an RC filter) and sent to a DAC with seven bits generating $v_{corr}(k) = E\{Gw(k)\}$. By removing the zero mean value terms, which are filtered, we can express in first approximation the voltage $v_{corr}(k)$ as:

$$v_{corr}(k) \approx G\frac{[a_3C_3G_{ch}^2 + a_5C_5G_{ch}^4 + a_7C_7G_{ch}^6]}{2} \approx G\frac{[a_3C_3G_{ch}^2]}{2} \tag{5}$$

where $C_3, \ldots C_7$ are coefficients dependent on the impulse response of the channel and filter and are equal to:

$$0.5G_{ch}^iC_i \approx E\{[x(k)^i \otimes h_{FFE}(k)]u(k)\}, \tag{6}$$

By solving this equation, we can find terms with an even exponent that have a mean value different than zero, meaning there are nonfiltered positive terms that multiply the distortion coefficient. Moreover, the terms of the fifth and seventh order can be in first approximation neglected because they are multiplied for a higher order gain, which is smaller than one $G_{ch} \approx 0.3$. For example, in the particular case of an ideal channel and thus no FFE, there is a third-order coefficient equal to:

$$\begin{aligned} E\{[x(k)^3 \otimes h_{FFE}(k)]u(k)\} =& E\{[(G_{ch}u(k) \otimes h_{ch}(k))^3 \otimes h_{FFE}(k)]u(k)\} = \\ & E\{[(G_{ch}u(k)h_{ch}(0))^3 \otimes h_{FFE}(k)]u(k)\} = \\ & E\{[G_{ch}^3u(k)^3h_{FFE}(0)]u(k)\} = G_{ch}^3E\{[u(k)^4\} \approx 0.5G_{ch}^3. \end{aligned} \tag{7}$$

After sensing the value of a_3, the loop minimizes it, using v_{corr}, thus reducing the third-order harmonic $H3$:

$$H3 \propto 0.8a_3G_{ch}^2 + a_5G_{ch}^4 + 1.02a_7G_{ch}^6 \approx 0.8a_3G_{ch}^2. \tag{8}$$

To obtain the value of the third harmonic, the Fourier transform of a sinusoid $G_{ch}sin(2\pi f_{in}t)$ distorted by the TH circuit can be calculated:

$$\begin{aligned} S(f) = &- \frac{1}{128}((64G_{ch} + 48a_3G_{ch}^3 + 40a_5G_{ch}^5 + 35a_7G_{ch}^7)\delta(f - f_{in}) \\ &+ (16a_3G_{ch}^3 + 20a_5G_{ch}^5 + 21a_7G_{ch}^7)\delta(f - 3f_{in}) + ...). \end{aligned} \tag{9}$$

Then, the third harmonic component $(16a_3G_{ch}^3 + 20a_5G_{ch}^5 + 21a_7G_{ch}^7)\delta(f - 3f_{in})$ can be normalized resulting in (8). Normally, the FFE is not capable of eliminating all the ISI major components, meaning the convolution between the channel and the FFE is not equal to a Kronecker delta ($h_e = h_{ch} \otimes h_{FFE} \neq \delta$). Knowing that $\sum_i h_e(i) = 1$, this results in $h_e(1) < 1$, where $h_e(1)$ is the component that multiplies the symbol $u(k)$. In this case, if for simplicity we neglect a_5 and a_7, we obtain after the filtering:

$$v_{corr}(k) \approx \frac{G[h_e(1) - 1]}{2} + \frac{GG_{ch}^2a_3C_3}{2}. \tag{10}$$

There is a term that is not canceled by the subtraction of $u(k)$ that makes the system set to a wrong value of v_{corr}. The same problem could arise if the gain control is not accurate enough, leading once again to a residual component proportional to $u(k)$, which is not filtered, and which does not let the system settle to the desired value. To overcome these problems, we introduce the error elaboration block shown in Figure 6, different to the one in [8] allows us to remove not only the residual ISI component but also the gain error. For the simplicity of calculation, we assume a_3 is the only distortion component different from zero, $d(k)$ is then:

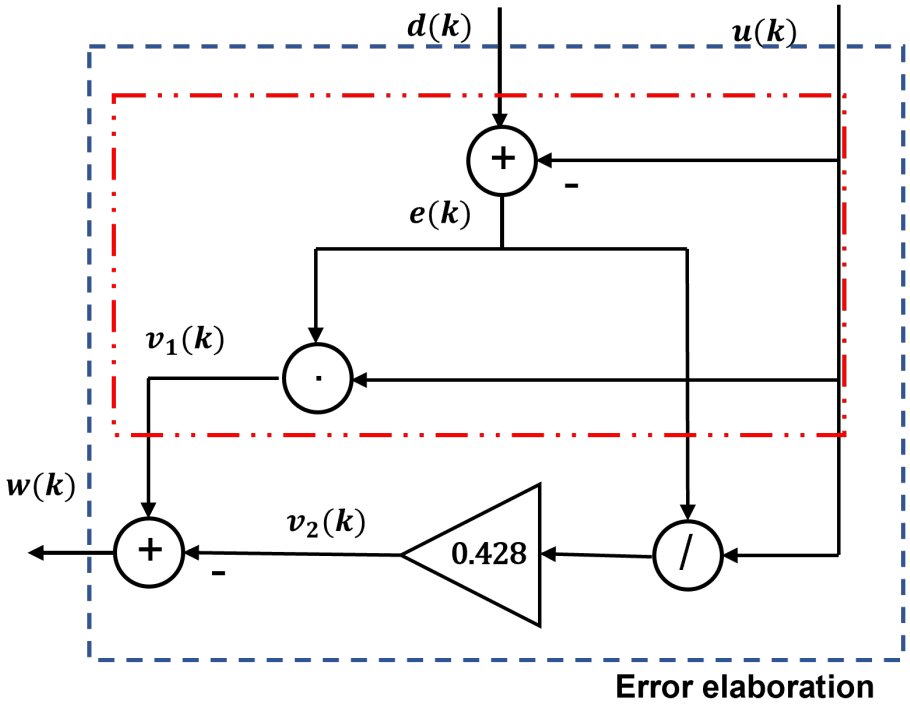

Figure 6. The block that processes the difference between the input and the output of the slicer allowing cancellation of the residual ISI and gain error in blue (in red the non-robust to ISI and gain elaboration block).

$$d(k) = G_r h_e(1)u(k) + G_{nor}[a_3x^3(k) + n(k)] \otimes h_{FFE}(k), \tag{11}$$

where G_r is the residual gain of the system, which is different from 1, in the case when the system can not exactly match the gain of the channel (or the gain variations of the analog

circuit components) $G_{nor} \neq 1/G_{ch}$, and the first order terms given by the residual ISI are neglected because they will be filtered after being multiplied or divided by $u(k)$. Then, by following the calculation shown in the block diagram we have:

$$e(k) = [G_r h_e(1) - 1]u(k) + G_{nor}[a_3 x^3(k) + n(k)] \otimes h_{FFE}(k) \tag{12}$$

$$v_1(k) = [G_r h_e(1) - 1]u^2(k) + u(k)G_{nor}[a_3 x^3(k) + n(k)] \otimes h_{FFE}(k) \tag{13}$$

$$v_2(k) = C_E\{[G_r h_e(1) - 1] + G_{nor}[a_3 x^3(k) + n(k)] \otimes h_{FFE}(k)/u(k)\}. \tag{14}$$

Knowing that $u(k)$ is a random signal, which can assume eight evenly spaced values between -1 and 1, we have $C_E = E\{u^2(k)\} = 0.4286$, and after subtracting $v_1(k) - v_2(k)$ the filtering of the signal $w(k)$, we obtain:

$$v_{corr}(k) \approx 0.14 G a_3 C_3' G_{ch}^2. \tag{15}$$

This allows correct calculation of the system while being independent of the gain and the residual ISI. The error signal must be divided by one of the eight PAM-8 symbols. This means we can easily implement the division with a look-up table (LUT) to obtain the reciprocal of the symbol values followed by a multiplier. This can be performed with ease because the operation is carried on in the calibration path where the loop bandwidths can be small, and latency can be tolerated. Moreover, this elaboration block complexity does not change with the increasing ISI, while the one in [8] requires a number of delays and sums that scale quadratically with the number of nonnegligible ISI components. Therefore, in the presence of a channel difficult to equalize, the system presented in this work does not show criticality.

By operating on samples coming from different interleaving TH buffers and switches, the mismatches impact is averaged out. This means the loop will converge at a v_{corr} that minimizes the overall distortions, but at the cost of a reduction in linearity compared to the ideal matching case.

4. Simulation Results

The validation of the feedback loop was performed by firstly implementing the track-and-hold circuit in TSMC 5 nm technology. During the simulation of the sampler, parasitics were added to the schematics. Principally, they were resistances and capacitances deriving from the post-layout characterization of the technology with the main focus on contact and low metal parasitics, which are critical.

While sampling the signal at 60 GS/s, the TH circuit had an output range of 505 mV_{ppd} generated through a 6 dB gain at Nyquist, and it consumed 18.5 mA from a 0.93 V voltage supply to drive the 64 TI channels capacitive loads equal to 45 fF. The ADC, the digital part of the PAM-8 RX, and the calibration loop were implemented in Verilog-A to enable co-simulation with the actual circuit. TX, AFE, and the channel were modeled using an *s* parameter matrix.

We performed a transient simulation of the receiver using a PRBS PAM-8 signal for three different PVT conditions. As shown in Figure 7a, the system adjusted the value of v_{corr} over time until it settled to the optimal value (around 128×10^3 symbols against the 1.2×10^6 in [12]). By plotting in Figure 8 the histograms of the sampled signals equalized by the FFE at the beginning and the end of the calibration (the three couples of histograms are normalized so that the systems have the same linear gain in both cases), we can easily see an improvement. In particular, the average variance of the eight symbols moved from 34 mV to 27 mV, from 43 mV to 36 mV, and from 27 mV to 19 mV, respectively, for the Typ, SS, and FF corners. Next, the receiver was simulated using an input sinusoid of 252 mV_{ppd} at 1 GHz. Figure 7 b depicts the total harmonic distortion of the track and hold output signal with the varying of the v_{corr}.

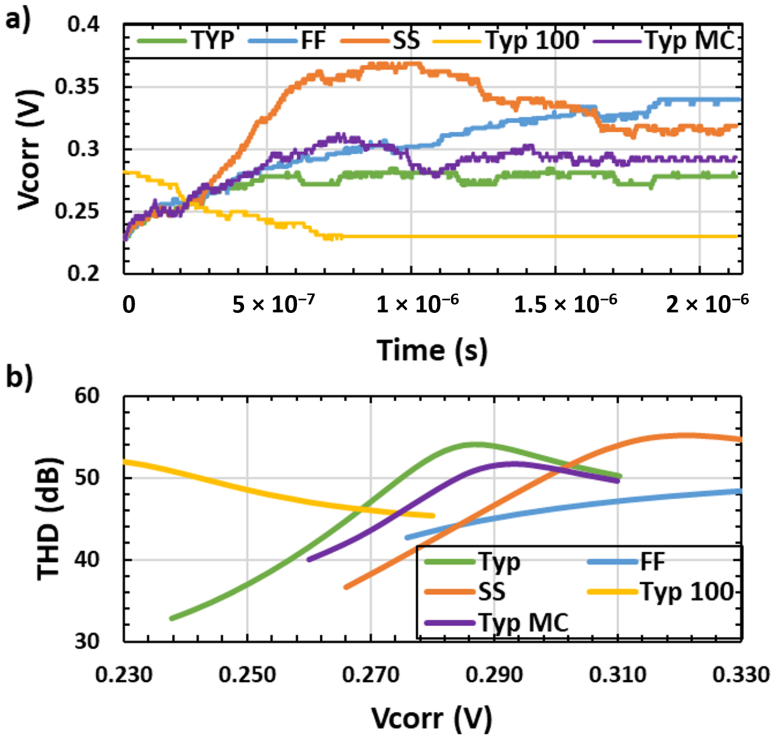

Figure 7. (**a**) Settling of the v_{corr} overtime during the calibration of the system and (**b**) the THD of the TH circuit across different values of v_{corr} for three different PVT conditions, one MC point, and one after a temperature step (the plot stops at v_{corr} = 0.33 V due to the linearity saturation (FF) for higher values).

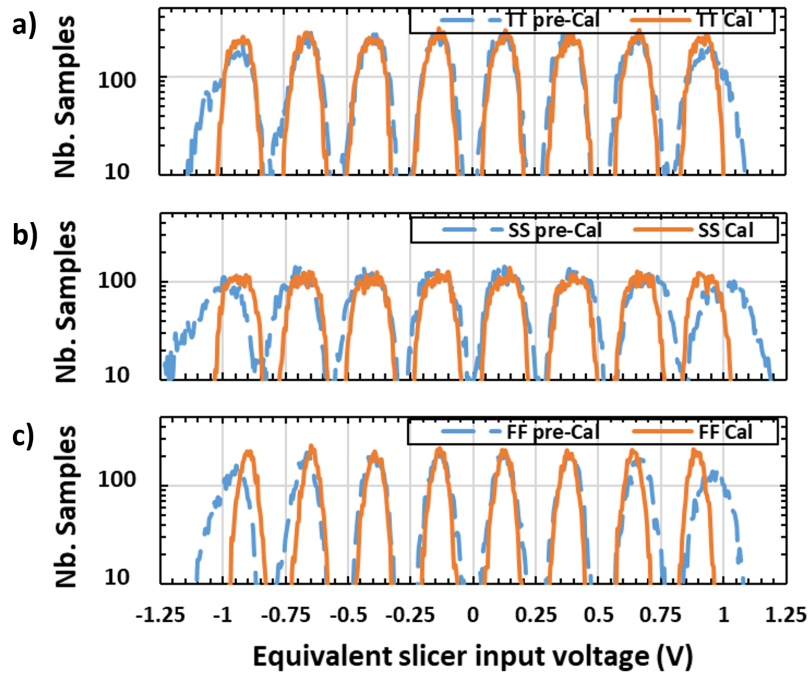

Figure 8. Histograms of the reconstructed signals at the slicer input before and after the linearity calibration for (**a**) Typical, (**b**) SS, and (**c**) FF corner.

The maximum linearity of over 48.5 dB was obtained for values of v_{corr} that matched the ones obtained through the transient calibration simulation, meaning that the system can maximize the static linearity. These simulations were also performed to obtain the

plots in Figure 7 for a single Montecarlo (MC) point and after a temperature step. By looking at the MC results, we can see how the system set to a value that maximized the linearity while having lower linearity compared to the ideal case due to mismatches. The temperature tracking was verified by introducing a positive step (60 °C → 100 °C) after the v_{corr} was settled in the Typical 60 °C condition (green case). The system set to the new value of v_{corr} that maximized the linearity for 100 °C, meaning the system tracked the temperature variations, which were slower in real applications and presented less criticality. The sampled PAC simulation of the system with the varying of v_{corr} was also performed, showing that the frequency response of the system had the same behavior (0.15% bandwidth variation), except for the gain as expected, which showed an 18% variation.

In Table 1, the THD of the circuit proposed in this work is compared with the available literature. A fair comparison is illustrated in [14] where a THD of around 50 dB was obtained for a the same input frequency and output dynamic range for a single PVT condition. On the other hand, in [12], the authors reported a THD of 56.5 dB after the calibration, but, to our knowledge, no throughout characterization of the analog circuit linearity across PVT nor co-simulation with the transistor-level circuit was performed.

Table 1. THD comparison between the literature and this work at three different PVT conditions.

System	[14] Typ	[12]	This Work Typ @ 60 °C	This Work SS @ 125 °C	This Work FF @ −20 °C
Pre-calibration THD	≈50 dB (No calibration was implemented; the THD was extrapolated from the plot)	30.8 dB	31.6 dB	36.4 dB	28.7 dB
Post-calibration THD	-	56.5 dB	54.0 dB	55.2 dB	48.5 dB
Input Frequency	1.01 GHz	5.5 GHz	1 GHz	1 GHz	1 GHz
Transistor-level implementation	Yes	No	Yes	Yes	Yes
Output Dynamic Range	500 mV_{ppd}	-	500 mV_{ppd}	500 mV_{ppd}	500 mV_{ppd}

5. Conclusions

This paper showed a 60 GS/s 8 × 8 TI track and hold in 5 nm FinFET technology with a 6 dB gain at Nyquist, and it proposed a calibration loop applicable to a PAM system, which minimized the distortion of the AFE. The transient co-simulation of the sampler circuit and of the receiver Verilog-A model generated the optimal value of v_{corr}, and the system was able to vary the control voltage to track the temperature change. The histograms at the slicer were evaluated before and after the calibration showing an eye-opening improvement, which resulted in an average reduction in the variances from 34 mV to 27 mV, from 43 mV to 36 mV, and from 27 mV to 19 mV, respectively, for the Typ, SS, and FF corners. Lastly, the obtained v_{corr} was applied to the buffer during a transient simulation with a 1 GHz, 252 mV_{ppd} sinusoidal input, showing a THD of the TH circuit higher than 48.5 dB across different PVT conditions.

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