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A Cost-Effective and Compact All-Digital Dual-Loop Jitter Attenuator for Built-Off-Test Applications

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Abstract: A compact and low-power all-digital CMOS dual-loop jitter attenuator (DJA) for low-cost built-off-test (BOT) applications such as parallel multi-DUT testing is presented. The proposed DJA adopts a new digital phase interpolator (PI)-based clock recovery (CR) loop with an adaptive decimation filter (ADF) function to remove the jitter and phase noise of the input clock, and generate a phase-aligned clean output clock. In addition, by adopting an all-digital multi-phase multiplying delay-locked loop (MDLL), eight low-jitter evenly spaced reference clocks that are required for the PI are generated. In the proposed DJA, both the MDLL and PI-based CR are first-order systems, and so this DJA has the advantage of high system stability. In addition, the proposed DJA has the benefit of a wide operating frequency range, unlike general PLL-based jitter attenuators that have a narrow frequency range and a jitter peaking problem. Implemented in a 40 nm 0.9 V CMOS process, the proposed DJA generates cleaned programmable output clock frequencies from 2.4 to 4.7 GHz. Furthermore, it achieves a peak-to-peak and RMS jitter attenuation of –25.6 dB and –32.6 dB, respectively, at 2.4 GHz. In addition, it occupies an active area of only 0.0257 mm^2 and consumes a power of 7.41 mW at 2.4 GHz.

Keywords: jitter attenuator; jitter cleaner; phase interpolator; MDLL; built-off-test; automatic test

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1. Introduction

With the continuous development of semiconductor scaling technology, the I/O interface operation speed of high-speed DRAMs such as DDR5 (=7.2 Gbps/pin), LPDDR5 (=6.4 Gbps/pin), and GDDR6 (=16 Gbps/pin) has also dramatically increased. Accordingly, the complexity and importance of memory device testing required for performance evaluation and the defect detection of high-speed DRAM and NAND flash memory ICs are increasing. In addition, the test cost accounts for a significant portion of the overall manufacturing cost of high-speed ICs. An essential factor in this increase in test cost is the increase in the price of automatic test equipment (ATE) used to test high-speed memory ICs. In particular, for the at application speed (at-speed) test of the latest high-speed DRAMs, ATE has often needed to be replaced with a faster and more expensive version to support the ever-increasing device-under-test (DUT) speed. This is because it is challenging to maintain the signal integrity characteristics of a multi-channel ATE, which requires the parallel testing (or multisite testing) [1,2] of multiple DUTs using multiple high-speed I/O channels at the same time. In addition, when evaluating the performance of high-speed DUTs, the limited clock frequency and significant clock jitter (or phase noise) characteristics of the existing low-cost ATEs supporting parallel multi-DUT testing may decrease the test accuracy.

Recently, it has been proposed to use a built-off-test (BOT) or built-off-self-test (BOST) module as a cost-effective method for the at-speed testing of high-speed memory ICs [3–5]. As shown in Figure 1, the BOT (or BOST) module is used as a bridge connecting the DUT and the ATE. One of the key technologies in implementing such a parallel multi-DUT test system is a PLL-based clock generator that removes the jitter of the noisy reference

clock provided by the low-cost ATE and multiplies the clock frequency. A common way to perform jitter cleaning and frequency multiplication simultaneously is to use two PLLs connected in series [6,7]. For example, as shown in Figure 1, the first PLL #1 cleans the reference clock jitter, and the second PLL #2 generates a multiplied output clock. As shown in Figure 2a, the conventional PLL #1, which operates as a jitter attenuator (or jitter cleaner), uses an external voltage-controlled crystal oscillator (VCXO) and external loop filters to lower the loop bandwidth, leading to a severe increase in area and power consumption. Since a general PLL-based jitter attenuator has a limited operating frequency range, to make a jitter attenuator supporting a wide frequency range, there is a method using a plurality of PLLs and RF switches, as shown in Figure 2b [8]. However, with this method it is challenging to apply to the BOT-based parallel multi-DUT test system because the size, power consumption, and cost of the jitter attenuator are increased too severely.

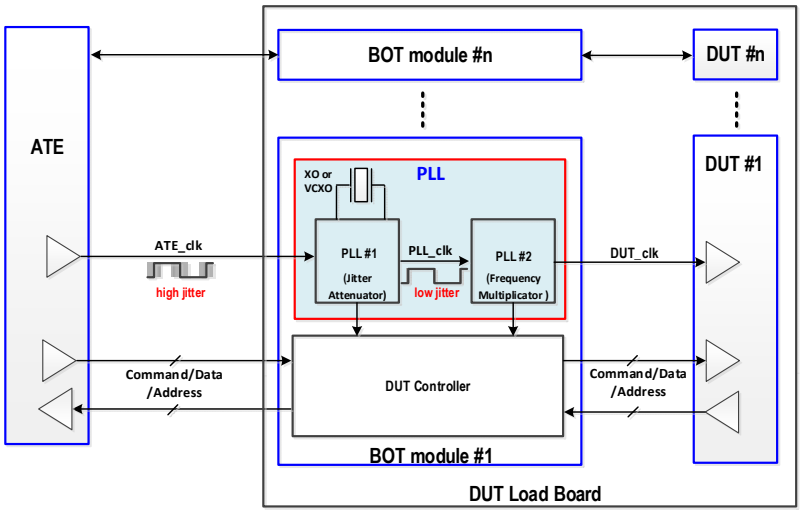
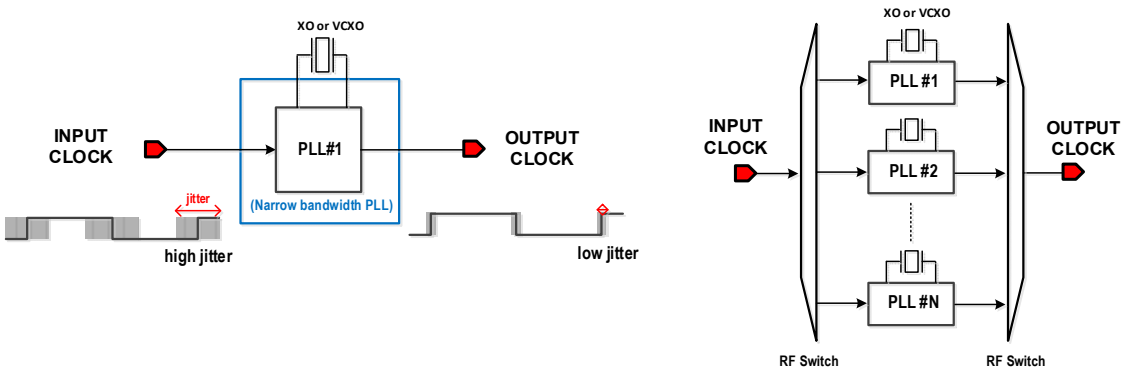


Figure 1. Simplified block diagram of a BOT-based parallel multi-DUT test system.



(**a**) (**b**)

Figure 2. (**a**) Conventional PLL-based clock jitter attenuator. (**b**) Simplified block diagram of a wide-range jitter attenuator architecture using multiple PLLs.

This paper presents a small form factor, low-power CMOS jitter attenuator for a low-cost BOT-based parallel multi-DUT test system. The proposed all-digital dual-loop jitter attenuator (DJA) utilizes a low-jitter multiplying delay-locked loop and a new phase interpolator-based clock recovery loop to operate in the wide frequency range of 2.4~4.7 GHz. The proposed DJA can remove the jitter and phase noise of the input clock and generate an output clock aligned with the average frequency of the input clock. The rest of this paper is organized as follows. Section 2 presents the architecture and operation

of the proposed dual-loop jitter attenuator. Section 3 describes the experimental results. Finally, Section 4 presents the conclusion.

2. Proposed All-Digital Dual-Loop Jitter Attenuator (DJA)

2.1. Proposed DJA Architecture

Figure 3 shows a block diagram of the proposed all-digital dual-loop jitter attenuator (DJA) architecture. The proposed DJA is composed of a dual-loop structure: multiplying the delay-locked loop (MDLL) and the phase interpolator (PI)-based clock recovery (CR) loop. The first digital MDLL loop generates uniformly spaced, low-jitter eight-phase reference clocks (p0~p7) for the PI-based CR loop. The second PI-based CR loop is composed of a digital phase interpolator (PI), a bang-bang phase detector (BBPD), an adaptive decimation filter (ADF), a PI controller, and a 1/4 frequency divider. The ADF consists of a digital loop filter (DLF) and a decimation factor (DF) controller. The proposed DJA can clean the phase noise and jitter from the input clock (CLK_IN) and produce a low-jitter phase-aligned output clock (CLK_OUT). In the jitter attenuator of the proposed dual-loop structure, both the MDLL and PI-based CR are first-order systems, so the proposed DJA has the advantage of increased system stability. In addition, unlike general PLL-based jitter attenuators with a narrow frequency range and jitter peaking problems, the proposed DJA has the advantage of a wide operating frequency range without jitter peaking. The jittery input clock comes in with the phase edge continuously shifting back and forth slightly due to the jitter component. In the proposed DJA, the output signal of the BBPD does not directly drive the digital PI, but the decimation-filtered signal through the ADF is used for driving the PI. After this process, the output clock phase follows the average value of the input clock phase.

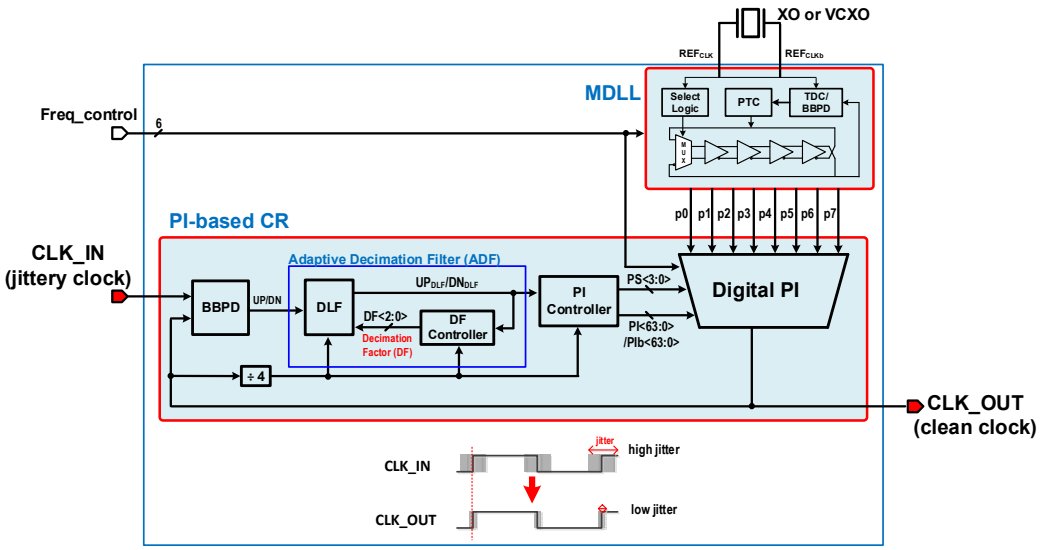


Figure 3. Proposed all-digital dual-loop jitter attenuator (DJA) architecture.

Figure 4 illustrates the dual-loop operation of the proposed DJA. In the proposed DJA, the first MDLL loop is activated at the beginning of the operation. Phase lock and frequency multiplication are performed quickly using the cyclic vernier time-to-digital converter (TDC). Then, using the delta-sigma modulator (DSM) for dithering jitter reduction in sequential tracking mode, N times multiplied low-jitter eight-phase output clocks (p0~p7) are generated. The 6-bit Freq_control signal adjusts the MDLL output frequency. After the MDLL loop is locked, the second PI-based CR loop starts to perform jitter and phase noise attenuating operations. The BBPD compares the jittery input clock (CLK_IN) with the output clock (CLK_OUT) of DJA and generates the UP/DN signal that informs the early or late phase information. The ADF generates the filtered output pulse signal UP_{DLF}/DN_{DLF} according to the coefficients of the decimation factor DF<2:0>. For example,

when DF<2:0> = '001' (DF = 4 in decimal), if the UP (or DN) pulse signal is accumulated four times, the UP_{DLF} (or DN_{DLF}) pulse signal is generated once. The PI controller then uses this UP_{DLF}/DN_{DLF} information to generate the octant selection signal PS<3:0> and the fine resolution signal PI<63:0>/PIb<63:0> needed to control the digital PI.

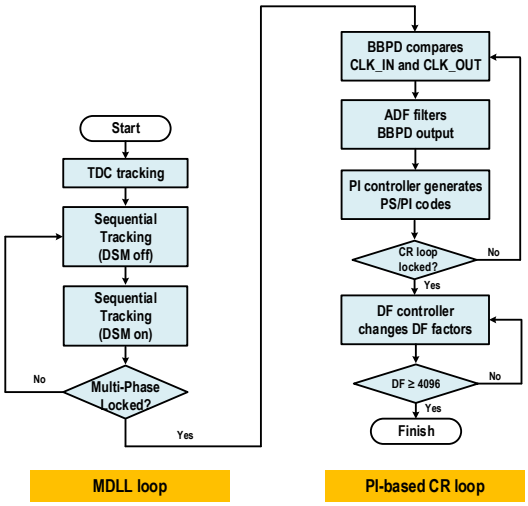


Figure 4. Flowchart illustrating the dual-loop operation of the proposed all-digital DJA.

The proposed PI-based CR loop uses DF<2:0> = '000' (DF = 1 in decimal) at the beginning of the operation to lock the output clock phase to the average frequency of the noisy input clock while maintaining the initial loop bandwidth. Then, decimation filtering [9–11] is performed while increasing the DF code sequentially from '000' to '111' in eight steps to lower the loop bandwidth to 1 K Hz or less. The structure of the proposed PI-based CR is similar to the general PI-based clock and data recovery (CDR). Therefore, Equation (1) below can determine the loop bandwidth of the proposed PI-based CR according to the DF code [12]. Here, $\varnothing_{IN}$ is the amplitude of the input sinusoidal jitter, ΔT is the minimum phase step of PI, DF is the decimation factor, and T_{FSM} is the update period of PI.

$$\text{Loop Bandwidth} \approx \frac{1}{2\pi \cdot \varnothing_{IN}} \cdot \frac{\Delta T}{DF \cdot T_{FSM}} \quad (1)$$

Table 1 shows the decimation factor coefficients in decimal according to the DF<2:0> codes.

Table 1. Decimation factor (DF) coefficients according to DF<2:0> codes.

DF<2:0> Code	Decimation Factor (DF) Coefficients (in Decimal)
000	1
001	4
010	16
011	64
100	256
101	1024
110	2048
111	4096

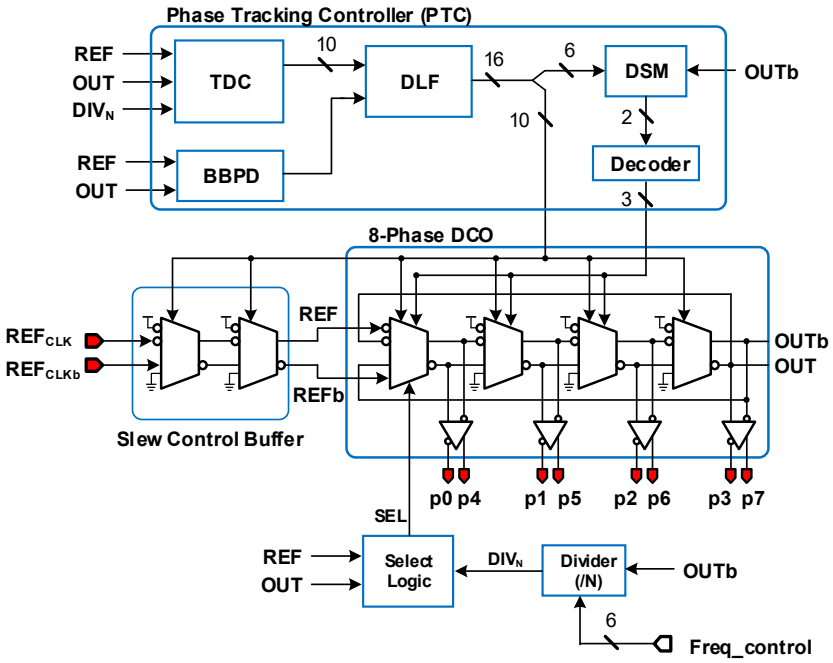
2.2. Proposed Low-Jitter Eight-Phase All-Digital MDLL Frequency Multiplier

Figure 5a shows a block diagram of the proposed low-jitter eight-phase all-digital MDLL [13,14]. It consists of a phase tracking controller (PTC), an eight-phase digitally controlled oscillator (DCO), a slew control buffer, a select logic, and a programmable frequency divider (/N) with a division factor N of 24~47. The proposed MDLL has

two operation modes: TDC tracking and sequential tracking. The PTC consists of a cyclic Vernier TDC, a BBPD, a digital loop filter (DLF), a delta-sigma modulator (DSM), and a binary-to-thermometer decoder. The eight-phase DCO consists of a four-stage delay line to generate eight-phase clocks (p0~p7) with a uniform phase interval of 45 degrees. The delay cell constituting each stage is a mux-based pseudo-differential structure with binary weighted varactors. Figure 5b shows the eight-phase clocks (p0~p7) of the MDLL operating at 2.4 GHz and 4.7 GHz, respectively. The maximum phase errors between the adjacent clocks were less than 1.3 and 1.6 degrees at 2.4 GHz and 4.7 GHz, respectively. Figure 5c shows the jitter simulation results of the proposed MDLL. It achieves a peak-to-peak (p-p) of 4.01 ps and a root mean square (RMS) jitter of 0.394 ps, respectively, at 4.7 GHz.

When the MDLL is turned on, the TDC tracking mode is first performed, and the TDC inside the PTC first measures the initial phase error between the REF and OUT signal using the cyclic Vernier TDC for fast locking operation. The DLF receives the 10-bit phase error information from the TDC and generates a 10-bit signal for controlling the DCO delay. The TDC tracking mode is completed within 100 ns, and the coarse phase lock is completed. After that, the TDC is turned off, and BBPD-based sequential tracking is started. At the beginning of sequential tracking, the DSM is turned off to reduce the residual phase error quickly, and then the DSM is turned on to minimize the dithering of jitter further [14]. The second-order DSM quantizes the 6-bit LSBs of the DLF output, and the binary-to-thermometer decoder generates control codes for adjusting the dithering cells of the delay cell.

The proposed MDLL multiplies the 100 MHz reference clock (REF_{CLK}/REF_{CLKB}) by N times (N = 24~47) to create 2.4~4.7 GHz wide-range eight-phase output clocks. The division factor N can be programmed with the 6-bit Freq_control signal. Since the designed MDLL operates in a wide frequency range from 2.4 GHz to 4.7 GHz, the reference clock's rise time and fall time are finely adjusted using the slew control buffer, effectively reducing jitter. The proposed MDLL achieves a lock time of less than 400 ns.



(**a**)

Figure 5. *Cont.*

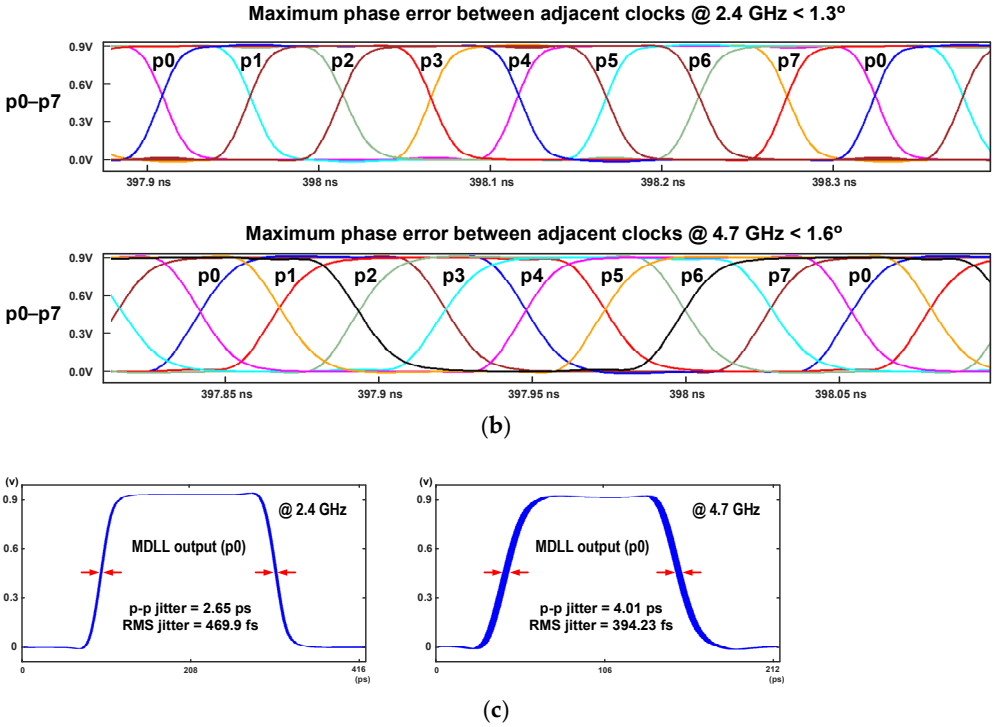


Figure 5. (**a**) Proposed low-jitter eight-phase all-digital MDLL, (**b**) eight-phase output clocks of the MDLL, and (**c**) post-layout-based jitter simulation performance of the proposed all-digital MDLL.

2.3. Proposed Digital PI

Figure 6a shows a block diagram of the proposed digital PI. The PI consists of a phase selector with two 4-to-1 multiplexers (MUX), a slew rate controller with two slew rate control buffers, two compensation capacitor arrays, 64 tri-state inverter-based PIs, an output capacitor array, and an output inverter. According to the PS<3:0> codes, the proposed PI selects two clock signals with a 45° phase difference among the eight-phase reference (p0~p7) inputs. Then, the CLK_OUT signal, whose phase step is controlled with a resolution of about 0.7° (=45°/2^6 = 0.415 ps at 4.7 GHz), is generated according to the PI<63:0> codes.

In the proposed PI, three compensation methods are applied to increase the linearity of the phase interpolation in the wide frequency range: First, a slew rate controller is used that can adjust the rise/fall times of the IN0/IN1 nodes according to the frequency range. When the frequency increases, the M<2:0> code value is changed to increase the driving ability of the slew rate control buffer, and vice versa, when the frequency decreases. Second, a compensation capacitor array (CCA) is used to compensate for the difference between the IN0 and IN1 node capacitance values that vary depending on the PI<63:0> code values. The reason for this compensation is that, referring to the lower right of Figure 6a, the input capacitance of the inverter-based PI may vary depending on the EN/ENb (=PI/PIb code) value controlling the intermediate switch transistors (M1, M2, M5, and M6). As shown on the left of Figure 6b, when there is no CCA, the capacitance of the IN0 node increases as the PI<63:0> code increases, but the capacitance of the IN1 node decreases inversely. Here, the maximum capacitance difference between the IN0 and IN1 nodes is about 8.2 fF. To compensate for the capacitance difference between these two nodes, as shown in the middle of Figure 6b, switched compensation capacitor arrays (CCAs) that can reduce (IN0 node) or increase (IN1 node) the node capacitance value according to the PI<63:0> codes are connected to the IN0 and IN1 nodes, respectively. On the right side of Figure 6b, it can be seen that the maximum difference between IN0 and IN1 node capacitance is significantly reduced from 8.2 fF to 2.8 fF by using the CCA compensation method. Third, an output capacitor array is used to adjust the slew rate of the output node (Ob) according to the

frequency range. When the frequency increases, the M<2:0> code value is reduced to block the connection paths between the Ob node and the output capacitor array. Conversely, if the frequency decreases, the connection path between the Ob node and the output capacitor array increases, thereby increasing the Ob node capacitance.

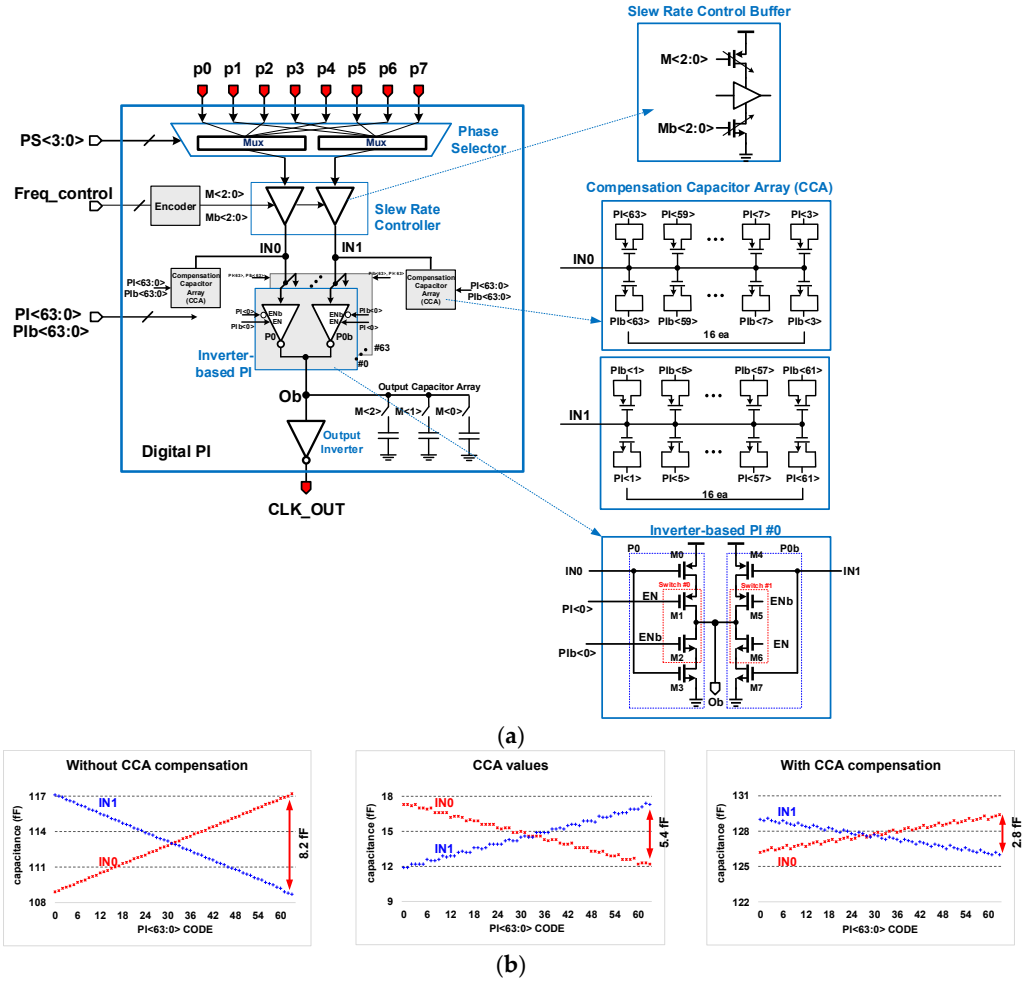


Figure 6. (**a**) Proposed digital PI. (**b**) N0/N1 node capacitance compensation using the compensation capacitor array (CCA).

Figure 7 illustrates the phase interpolation method of the proposed 9-bit PI with 512 (=2^9) steps. The resolution of the proposed digital PI is about 0.7 degrees. Figure 8 illustrates the post-layout simulation results of the proposed digital PI showing the INL and DNL of the PI. It can be seen that INL is significantly reduced from 2.638 LSB to 0.829 LSB using the proposed three compensation methods.

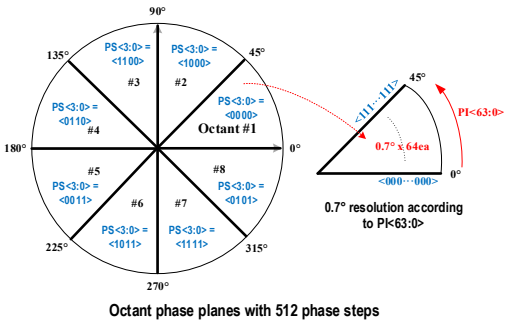


Figure 7. Phase interpolation method of the proposed 9-bit PI with 512 (=2^9) steps.

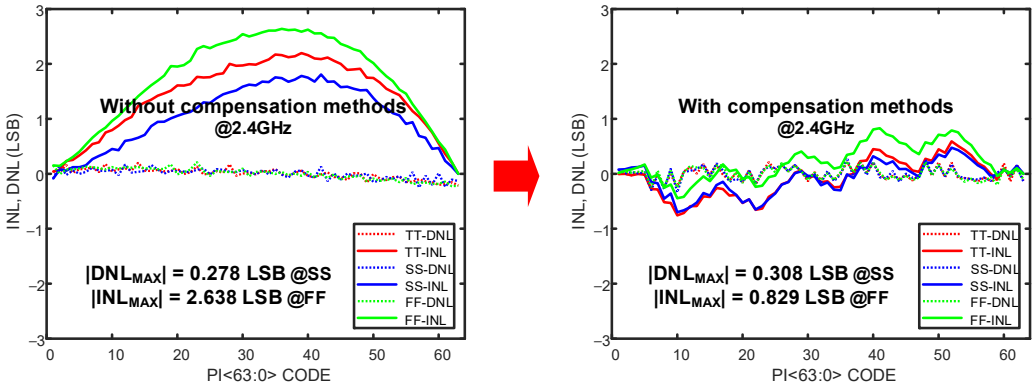


Figure 8. Post-layout corner simulation results of the proposed digital PI showing the INL and DNL of the PI, with and without the proposed compensation methods.

3. Experimental Results

The proposed all-digital DJA was implemented in a 40 nm CMOS process. Figure 9 shows the chip layout of the proposed DJA, where the active core area is only 174 μm × 148 μm = 0.0257 mm^2. The proposed DJA achieves a programmable operating frequency range of 2.4~4.7 GHz. The DJA consumes 11.48 mW at 4.7 GHz. As a result, the proposed DJA effectively removes undesired input clock jitter noise and produces an ultra-low jitter output clock.

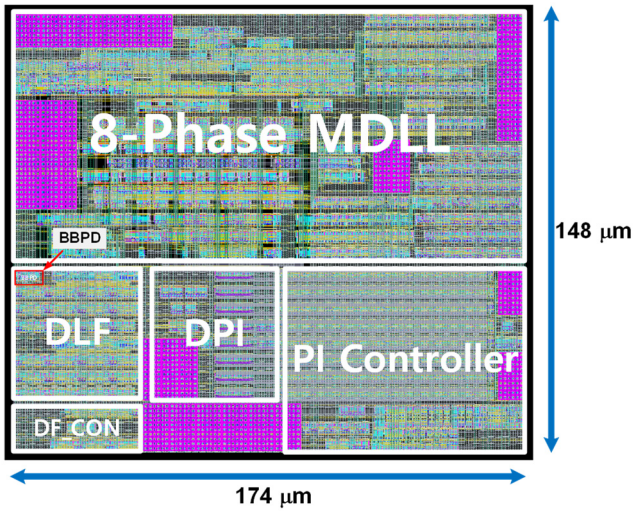


Figure 9. Chip layout of the proposed all-digital DJA.

Figure 10 shows the post-layout simulated locking process of the proposed all-digital DJA at 2.4 GHz. At the beginning of the operation, the MDLL is locked quickly to create eight frequency-multiplied reference clocks. After that, the DJA starts adaptive decimation filtering, and the DF value is sequentially increased up to 4096 whenever the polarity of the DLF output (UP_{DLF}/DN_{DLF}) value changes (DF in decimal: 1→4→256→1024→2048→4096).

Figure 11 shows the jitter transfer simulation results of the proposed DJA. This is the simulation result of DJA modeled using Xmodel, one of the SystemVerilog simulators [15]. When the amplitude of the input sinusoidal jitter is 0.1 UI at the operating frequencies of 2.4 GHz and 4.7 GHz, respectively, it can be seen that the loop bandwidth of the proposed DJA is significantly reduced as the DF value increases. When DF = 4096, the approximate loop bandwidth is as low as 0.77 KHz at 2.4 GHz and 1.53 KHz at 4.7 GHz, respectively.

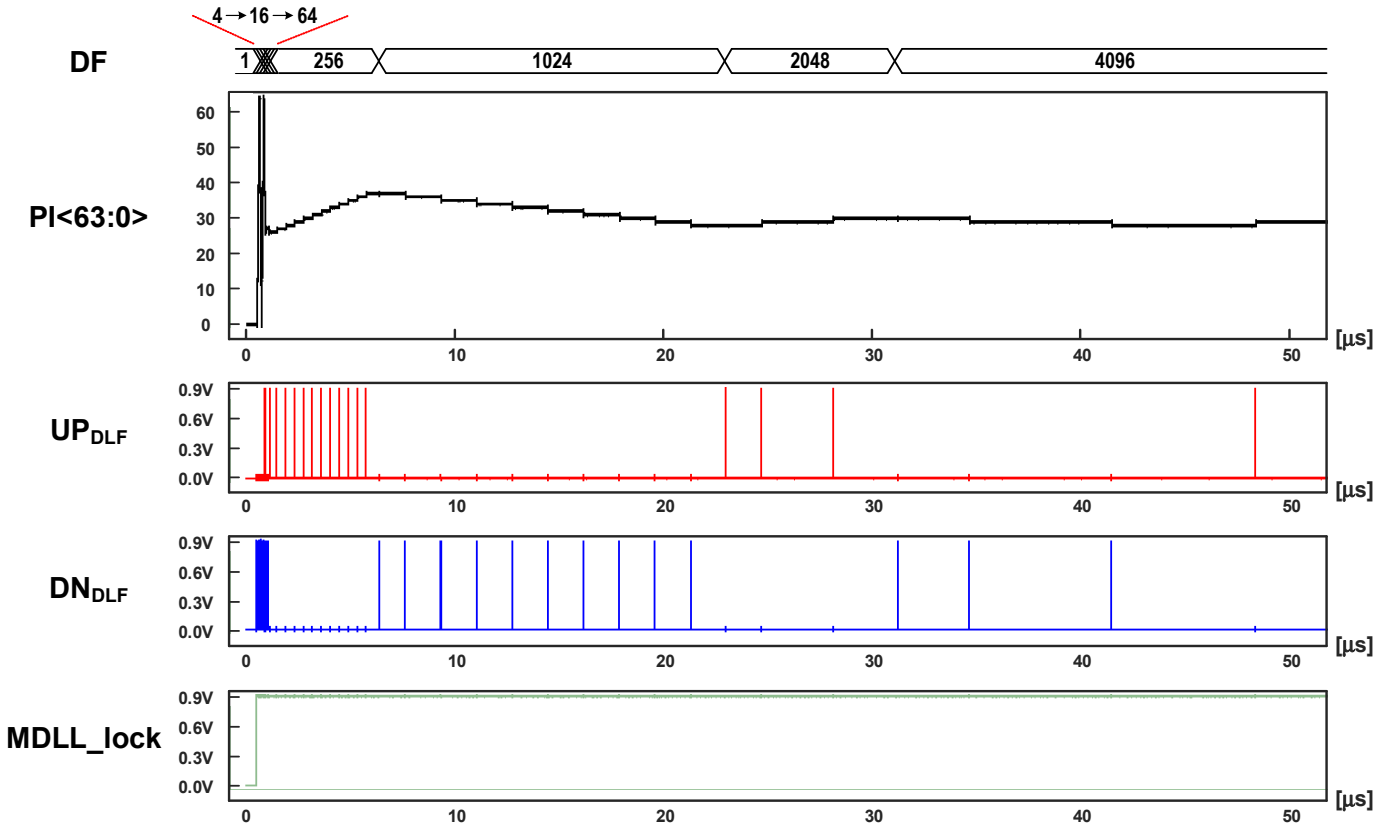


Figure 10. Post-layout simulated locking process of proposed DJA.

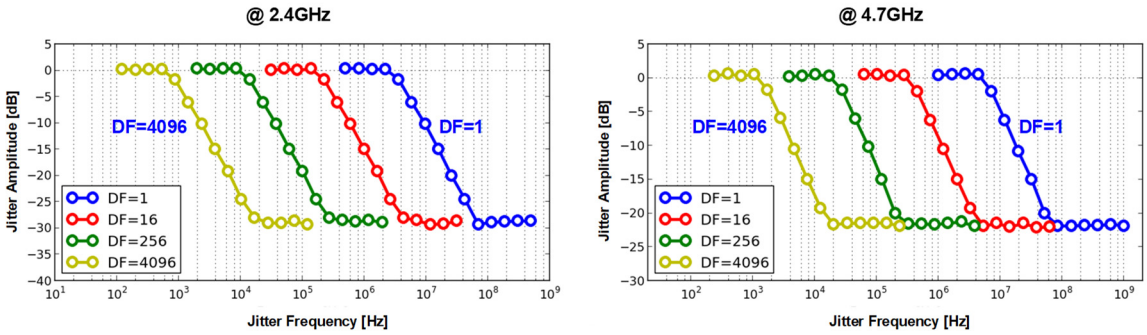


Figure 11. Simulated jitter transfer simulation results at 2.4 GHz and 4.7 GHz.

Figure 12 shows the post-layout simulation results of the proposed DJA operating at 2.4 GHz and 4.7 GHz, respectively. As shown in Figure 12a, when the noisy 2.4 GHz input clock (CLK_IN) has a p-p period jitter of about 97 ps (=0.233 UI) from a 25 KHz sinusoidal input jitter, the proposed DJA generates the clean output clock (CLK_OUT) with a jitter value as small as 5.05 ps (=0.012 UI) at 2.4 GHz. Figure 12b shows that the noisy 4.7 GHz clock with a high p-p period jitter of about 97 ps (=0.242 UI) from a 50 KHz input sinusoidal jitter is filtered and reduced to 5.28 ps (=0.024 UI) after passing through the DJA. Figure 13 shows the post-layout-based phase noise simulation (Synopsys FineSim) plots at 2.4 GHz output frequency. At the output clock frequency of 2.4 GHz, the noisy RMS jitter is reduced from 20.86 ps to 482.6 fs, showing a jitter reduction of about –32.6 dB. At 4.7 GHz, the jitter attenuation performance is about –31.8 dB. Table 2 summarizes the performance of the proposed all-digital DJA. The performance in this design is the post-layout-based FineSim simulation results.

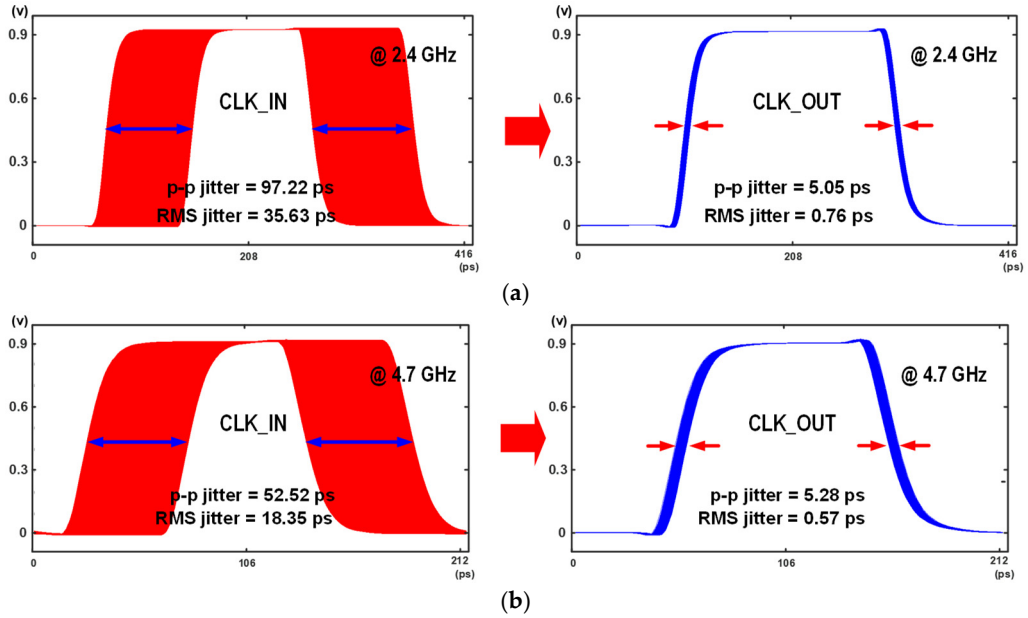


Figure 12. Post-layout simulation results of the proposed DJA showing input and output clock jitter eye diagram at (**a**) 2.4 GHz and (**b**) 4.7 GHz.

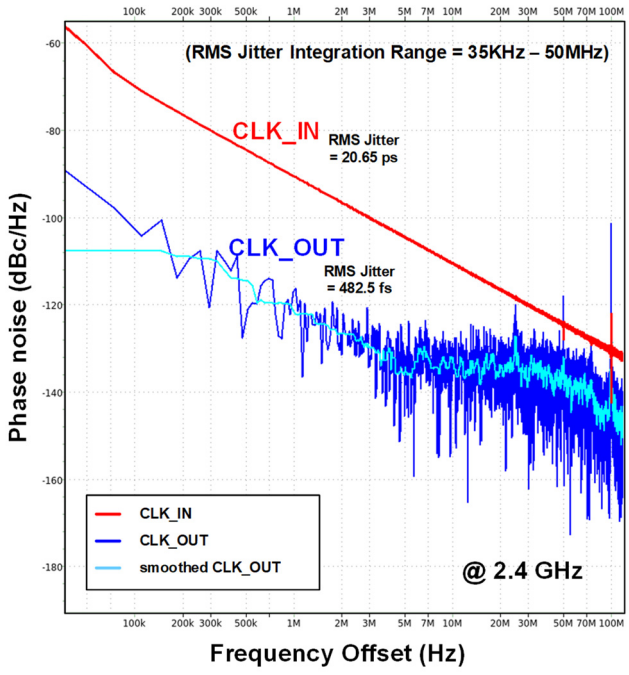


Figure 13. Post-layout-based phase noise simulation plots at 2.4 GHz output frequency.

Table 2. Performance table of the proposed all-digital DJA.

Reference	[6]	[7]	This Work
Technology	NA	NA	40 nm CMOS
Supply voltage (V)	3.3	3.3	0.9
Architecture	Analog PLL-based	Analog PLL-based	All Digital PI-based
Operating frequency (GHz)	3.6–4.0	2.75–3.072	2.4–4.7
Settling time (µs)	NA	NA	<50
Loop bandwidth (Hz)	10–100	10–200	1530 @ 4.7 GHz 770 @ 2.4 GHz
External loop filter capacitor	Required	Required	Not Required
RMS jitter performance (fs)	<200 [1]	111 [1]	330.1 [2] @ 4.7 GHz 482.5 [2] @ 2.4 GHz
Power consumption (mW)	389 [3]	419 [3]	Total: 11.48 @ 4.7 GHz (MDLL: 6.4, PI-based CR: 5.08)
Active core area (mm^2)	NA	NA	0.0257

[1] 12 KHz to 20 MHz RMS jitter integration, [2] 35 KHz to 50 MHz RMS jitter integration, [3] includes LDO and clock driver power.

4. Conclusions

In this paper, a new all-digital jitter attenuator featuring a digital PI-based CR and a multi-phase MDLL for low-cost BOT-based parallel multi-DUT testing is presented. By utilizing a new adaptive decimation filter (ADF) technique, the proposed DJA achieves an RMS jitter attenuation of more than –30 dB in the operating range of 2.4 GHz to 4.7 GHz. The proposed jitter attenuator was implemented in a 40 nm 0.9 V CMOS process, which occupies an active area of only 0.0257 mm^2 and consumes 11.48 mW at 4.7 GHz. The proposed DJA can be a cost-effective and compact solution to replace the conventional PLL-based jitter cleaners in parallel testing systems and high-speed SoC design areas that require jitter and phase noise cleaning of the input clock.

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Conflicts of Interest: The authors declare no conflict of interest.

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