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Dynamic Voltage and Frequency Scaling and Duty-Cycling for Ultra Low-Power Wireless Sensor Nodes

Sabrine Khriji [1,*], Rym Chéour [2] and Olfa Kanoun [1]

[1] Measurement and Sensor Technology, Chemnitz University of Technology, 09126 Chemnitz, Germany
[2] Computer & Embedded Systems Laboratory, National School of Engineers of Sfax, Sfax 3038, Tunisia
* Correspondence: sabrinekhriji@ieee.org

Abstract: Energy efficiency presents a significant challenge to the reliability of Internet of Things (IoT) services. Wireless Sensor Networks (WSNs) present as an elementary technology of IoT, which has limited resources. Appropriate energy management techniques can perform increasing energy efficiency under variable workload conditions. Therefore, this paper aims to experimentally implement a hybrid energy management solution, combining Dynamic Voltage and Frequency Scaling (DVFS) and Duty-Cycling. The DVFS technique is implemented as an effective power management scheme to optimize the operating conditions during data processing. Moreover, the duty-cycling method is applied to reduce the energy consumption of the transceiver. Hardware optimization is performed by selecting the low-power microcontroller, MSP430, using experimental estimation and characterization. Another contribution is evaluating the energy-saving design by defining the normalized power as a metric to measure the consumed power of the proposed model per throughput. Extensive simulations and real-world implementations indicate that normalized power can be significantly reduced while sustaining performance levels in high-data IoT use cases.

Keywords: IoT; wireless sensor networks; WSN; power management; energy saving; DVFS; duty-cycling; communication

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1. Introduction

With the continued advancement of communication technologies, the Internet of things (IoT) is integrated with Wireless Sensor Networks (WSNs) in various applications supporting universal data access with near real-time decision-making [1–3]. Such applications depend strongly on data processing, where batteries and/or energy harvesters supply sensor nodes. However, power sources have restricted energy densities and low charge rates. The energy efficiency in WSNs remains an open research problem. One challenge for WSNs is to achieve low-power features for intelligent sensing systems in a data-driven environment. Exploiting the variable workload characteristics of WSNs is an efficient method to improve energy efficiency. For example, in intelligent irrigation, monitoring air temperature can be performed in hours instead of minutes or seconds. It involves extended periods of inactivity, where there is a potential for energy savings. In other applications, such as landslide monitoring or fire detection, it is essential to make measurements quickly to trigger urgent signals enabling immediate decisions. Thereby, increasing energy efficiency under variable workload conditions can be accomplished through appropriate energy management for data processing [4,5].

1.1. Motivation

In this context, Dynamic Voltage Frequency Scaling (DVFS) presents one of the most energy-efficient management techniques by solving both challenges of on-demand performance and energy reliability. Generally, it is introduced as a framework that enables the change of the frequency and operating voltage of the processor based on system performance requirements at a certain point in time [2].

In this paper, the DVFS is experimentally implemented to optimize the system's power consumption during the operating time. Implementing DVFS in microcontrollers (MCUs) represents a major technological breakthrough in ultra-low power applications, such as for the deployment of wireless sensor nodes or for low-power radio networks, where the power saving should cover the time during the inactive or idle phases. Furthermore, reducing the time spent on the active node through sleep periods helps to minimize the node's energy consumption and thus increases the lifetime of the wireless sensor network [6]. A batch experiment is proposed to make an intelligent duty-cycle selection that will meet the quality of service and energy-saving needs. DVFS and duty-cycling have given rise to our hybrid energy management approach.

In this regard, the total energy consumption of a wireless sensor node is evaluated when it performs specific tasks under very low-power conditions. The aim is to empirically determine the most efficient operating clocking frequency for different specific MCUs operations by measuring and analyzing the normalized power consumed. This evaluation parameter is defined as a measure of power per throughput (mW/MI) in one second. The throughput presents the ratio between the Central Processing Unit (CPU) frequency and the Cycles Per Instruction (CPI). The reason behind measuring the normalized power in active mode is not to focus on the power consumption but on the energy needed to accomplish a unit operation. A high-precision four-wire measuring system is used for all measurements, which involves the guarding and shielding of all interfaces and the measuring cave.

1.2. Contributions

The paper focuses on optimizing the MCU power consumption by considering hardware and software aspects. The main contributions of the work are:

1. Investigation of energy optimization techniques in WSNs;
2. Reducing the overall power consumption of a wireless sensor node through the selection of a low-power MCU and the implementation of a power management-based DVFS technique;
3. Implementing the duty-cycling technique to reduce the energy consumed by the transceiver;
4. Measuring the consumed power during Bluetooth communication;
5. Defining the normalized power as an evaluation metric to measure the energy saving of the implemented solution with high accuracy.

1.3. Paper Organization

The rest of the paper is organized as follows: Section 2 surveys energy reduction techniques in WSNs. In Section 3, the application of DVFS technique is described in detail. Section 4 presents real measurement results obtained from the MSP430f5529LP launchpad. Section 4.2 describes the potential values of the proposed method and possible future works. Section 5 concludes the paper with the main results achieved.

2. Related Works

Many efforts have been performed to minimize the energy consumption of WSNs and extend their lifetime at different levels [7–9]. Multiple factors contribute to power consumption, making it a cross-layer problem, from the hardware architecture to the application layer.

As shown in Figure 1, power consumption can be reduced in three ways: energy-efficient communication protocols, hardware optimization, and energy management.

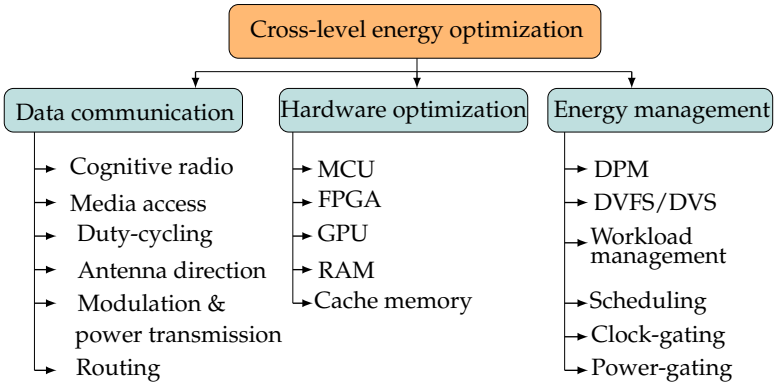


Figure 1. Cross-level energy optimization taxonomy.

2.1. Energy-Efficient Data Communication

Since wireless communication is a significant driver of power consumption, developing energy-efficient communication protocols to predetermine the parameters of the transceiver to be optimized is essential. Various technologies significantly contribute to controlling the power consumed during communication. In particular, this can be achieved by setting up self-organization protocols [10], cognitive radio techniques [11], media access [12], duty-cycling [6,13,14], optimal antenna direction [15], modulation and power transmission [16], and routing protocols [8].

There are some spectra, which are highly used, and others that are highly underused in frequency, time, or space. Therefore, opportunistic spectrum access methods are highly needed, where the cognitive user can dynamically detect licensed spectrum and access it when it is not in use. Cognitive radio is considered an efficient solution to improve wireless communication systems' spectral and energy efficiency by sharing the spectrum efficiently instead of using it in idle licensed channels. The Medium Access Control (MAC) protocol avoids collisions by preventing two interfering nodes from transmitting simultaneously. It applies the variation of the active/sleep mode. In this regard, the Sensor Media Access Control (S-MAC), Timeout Media Access Control (T-MAC), and BoostMAC [14] protocols are designed to provide a trade-off between network quality of service and energy savings. The Hybrid MAC (H-MAC) protocol lowers the equivalent energy consumption while providing a good network quality of service [17].

Another technique to save energy is to reduce the power consumption generated from idle listening by putting the node in sleep mode and awakening it periodically, at planned times only [18]. One of the most energy-efficient operations is directional antennas, which reduces the re-transmission of data and signal interference associated with omni-directional antennas [19]. Once a node transmits data in a particular direction, a nearby node can transfer data simultaneously without interference, significantly improving energy consumption.

Modulation optimization methods are used to determine the optimal radio optimization parameters at minimum energy consumption [20]. The circuit's power consumption is higher than that consumed for transmission at short distances and vice versa for long distances. Therefore, choosing the proper modulation parameters to trade off transmission signal strength and distance between nodes is critical. The appropriate setting of the transmission power of nodes is very crucial for the reduction of the network energy consumption. In the Transmission Power Control (TPC) method, the Link Quality Indicator (LQI), Packet Receive Rate (PRR), and Radio Signal Strength Indicator (RSSI) are the three standard parameters used to estimate the link quality.

The cluster-based routing protocol is introduced as one of the most energy-efficient techniques by minimizing the number of transmitted packets and the distances between nodes [17]. The network is divided into sub-regions, called clusters. In each cluster, one node is selected as a Cluster Head (CH), aggregating data packets from its cluster members and transmitting them to the sink node or to the base station using single-hop or multi-

hop communication schemes. In [21], a method for low-latency, energy-balanced data transmission over a WSN small world has been developed. It uses network characteristics and sensor node properties to define the probabilistic model for introducing small-world features (SWC). Then, to transmit data between the sink and nodes, a routing technique is developed based on the energy cost of links between nodes and applying Dijkstra's algorithm. In [22], authors developed a fuzzy-based energy-aware unequal clustering protocol to balance the energy consumption of the nodes and extend the network lifetime. The network is divided into circular partitioning with unequal cluster radii. CHs are selected based on three parameters: node residual energy, node centrality, and node density.

The authors in [23] proposed a multi-hop data routing method over a low-power wide-area network (LPWAN) [24] for IoT applications. They used the Q-learning approach toward data transfer to improve energy efficiency and quality of service.

2.2. Energy-Efficient Hardware Optimization

Building energy-efficient hardware has yet to raise a high-level interest from the research community, which is more concerned with the communication protocol [25]. However, energy efficiency significantly impacts choosing the right MCU/CPU for a particular task. Selecting the proper hardware, such as the microcontroller and field-programmable gate array (FPGA), significantly impacts the system power consumption [26]. Each microcontroller has a specific architecture. With the advent of multi-core architectures, many programmers use modern processors to maximize code performance by executing independent instructions in separate processors. This solution is called parallelism. Different cores run in parallel, and several special-purpose accelerators are used to support the large computing cores. Every microcontroller is composed of some controllers like clock controllers. By enabling mandatory clocks and disabling unnecessary ones, the overall system clocks are reduced, decreasing the energy consumption of the processing unit and increasing the processing time. Therefore, it is critical to balance energy use and clocking frequency. Another critical factor in reducing energy consumption is to ensure the use of low-power sensors and transceivers.

Authors in [27] investigated the energy impact while executing a set of arithmetic operations and functions on a set of sample MCUs with a Microwatt Meter. Measurements help smart programming decisions and configurations. Indeed, extensive benchmarking using real measurements was performed in [28], where the MSP430 was introduced as one of the most performing microcontrollers providing the best trade-off between performance and power. In addition, it is possible to save significant energy by disabling unnecessary elements using energy-efficient algorithms with numerous hardware elements.

2.3. Energy-Efficient Energy Management

The power management unit controls the processor's clock and hardware peripherals in a wireless sensor node. It sets an appropriate state according to the hardware and software requirements of the running application while always remaining ON to power the MCU, the conditioning circuit, and the wireless front end, even in standby mode. Since some components must remain in standby mode to detect an event, such as timers, external trigger input stages, measurements, and variations, it results in a system energy dissipation that still needs to be negligible. Standby mode accounts for a large part of the total energy dissipation of the sensors. A zero-current standby is proposed to handle this energy overload, with vibrations acting as a trigger for sensor activation and data transmission via Wi-Fi [29].

The third method is to determine the network's most energy-intensive and inefficient workloads through various algorithms such as DVFS, clock-gating, dynamic power management (DPM), and power-gating techniques. Such algorithms can help to reduce the non-optimal configurations in both hardware and software components [30]. DVFS has been gradually incorporated into most smart handheld devices and has been widely adopted by computers, server processors, and mobile devices to conserve energy. In addition, the

DVFS is used for the following components, including the processor, Graphical Processing Unit (GPU), Read Only Memory (RAM), cache memory, and radio transceiver [31]. Authors in [32] exploited the integration of GPU voltage and frequency settings on current NVIDIA boards to calibrate the core voltage/frequency and the memory frequency of the GPU. The GPU DVFS induced a 20% decrease in power consumption with a 4% loss in the GPU's performance. Testing a set of real GPU platforms with 37 GPU reference applications shows that the effect of the DVFS GPU is highly dependent on the characteristics of the application.

Table 1. Comparative study of existing works related to energy saving techniques in WSNs.

Energy Saving Level	Energy Saving Technique	Reference	Paper Contribution
Data communication	Cognitive radio	[33]	A mode switching strategy to harvest energy based on their current energy level and CH selection algorithm based on current energy levels and the average of past energy levels of sensor nodes
	Antenna direction	[34]	A reconfigurable cyclic antenna receiver based on a cyclic initiated and MAC receiver with switched antennas and integrated energy efficient scanning process
	Routing	[21]	Low-latency, energy-balanced data transmission over a WSN small world, a data routing method by optimizing energy cost of the links
		[17]	Fuzzy-based energy aware unequal clustering protocol
		[23]	Multi-hop data routing over a LPWAN using Q-Learning method
	Modulation and power transmission	[20]	Minimum-shift keying (MSK) modulation with Convolutional based on Bit Error Rate (BER), power consumption, wide bandwidth, easy demodulation and with a constant envelope
	Duty cycling	[6]	Improved duty cycling algorithm with 2 residual energy thresholds: for the network and for the residual energy threshold for the path
		[14]	BoostMAC protocol by adjusting the channel poling time and using machine learning classifier to configure the preamble length
Hardware optimization	Low-power devices	[28]	Benchmarking based on real measurements to select the energy-efficient MCU
	Multi-core architectures	[27]	Executing a set of arithmetic operations on a set of sample MCUs
	Co-processor	[35]	GPU-based parallel computing of energy and discrete event simulation in a multi-agent environment
Energy management	Zero-current standby	[29]	Vibrations to overcome overload for sensor activation and data transmission via Wi-Fi
	Workload management	[36]	A communication model that distributes the workload as an integer (0–1) linear programming problem for master and slave nodes based on energy for symmetric and asymmetric cluster-based networks
	Scheduling	[37]	A content-based adaptive and dynamic scheduling
	DPM	[38]	Centric reinforcement learning-based DPM model
	DVFS	[39]	Combination of DVFS and EDF to ensure an energy consumption gain considering time constraints

Authors in [39] provide a workload management system. It categorizes workloads of running applications according to similar events to estimate the processor workload efficiently at runtime and manages DVFS levels of cores based on it. They exploit thread-to-core mapping to achieve energy savings. In [40], an accurate macro-model is presented. It considers the energy and delays for DVFS transitions of the DC-DC modern converter based on the datasheet component values. They divide this overhead delay into phase-locked loop (PLL) and under-locking-related delay. The same applies to the power overhead, which is the sum of the power induced by both the converter and microprocessor. A power-aware model based on the combination of DVFS and global Earliest Deadline First, scheduler (EDF) [30] is implemented to ensure an energy consumption gain that considers time constraints.

2.4. Discussion

Table 1 presents a deep comparison of energy management techniques in WSNs.

As a result of these related works' investigation, the presented work focuses on optimizing the energy of a wireless sensor node in three aspects, i.e., energy-aware hardware selection, DVFS power management, and duty-cycling. Therefore, hardware optimization is performed by selecting the low-power microcontroller, MSP430, using experimental estimation and characterization. Then, the DVFS is implemented as an effective power management scheme to optimize the operating conditions. Behind DVFS is minimal involvement of software and operating systems or through enabling software. The software approach has many advantages but depends on extensive programming and reliable tools to control the high energy costs of large code. The duty-cycling technique is applied to reduce the energy consumption of the transceiver.

3. Dynamic Voltage and Frequency Scaling, and Duty-Cycling

Figure 2 describes the proposed hybrid energy management system combining the three aspects, including energy-efficient communication protocol, hardware optimization, and energy management. It meets the needs of quality of service (QoS) requirements in terms of delay and data throughput. The focus is to test the performance of the proposed solution in terms of energy consumption and execution time under different frequencies and voltages. By satisfying the QoS constraints at the application, network, and data link layers, the expected Quality of Experience (QoE) results are performed.

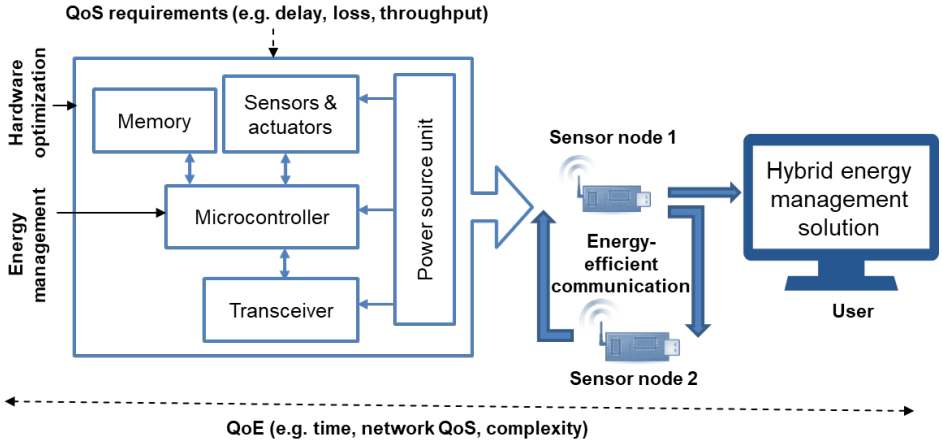


Figure 2. Proposed hybrid energy management system for ultra-low power wireless sensor node towards QoS and QoE. (Blue arrow: Connection between sensor node components, Blue filled arrow: Energy-efficient communication between sensor nodes, Black arrow: Energy-efficient techniques applied at the sensor node level, Dotted line: QoE parameter from the QoS requirements to the user satisfaction).

The architecture of a microcontroller has a significant impact on its energy consumption. Based on the deep study provided in [28], the MSP430 microcontroller outperforms

other microcontrollers in terms of power consumption by having a well-balanced CPU, ALU, and peripheral architecture. For this reason, it is selected to be used in this work.

3.1. DVFS Algorithm Overview

Modern processor architectures deliver high computing performance with a high-power consumption, averaging around 100 Watts. The energy-saving policies applied to the CPU are based on the state change, either in a standby state or a given speed state. In this work, the developed methodology proposes to change the voltage and frequency couple following the Equation (1) principle. Generally, the power consumption of a microprocessor can be divided into three parts [41]:

$$\begin{aligned} P_{cmos} &= P_{static} + P_{dynamic} + P_{short\,circuit} \\ &= V_{DD} I_{leakage} + P_{dynamic} + T_{sc} V_{DD} I_{peak} \end{aligned} \tag{1}$$

where V_{DD} defines the input voltage, $I_{leakage}$ presents total leakage current, T_{sc} is rising time of the input signal and I_{peak} denotes the peak current According to the structure of the Complementary Metal–Oxide–Semiconductor (CMOS) circuit, P_{static} is generated due to reverse-biased diodes. It refers to the dissipated power when the CMOS circuit is inactive or dormant. The leakage current presents the primary factor of P_{static}, which occurs mainly due to the short-channel effects, such as the sub-threshold leakage current and the gate leakage current [41]. The sub-threshold leakage current is the small current across the source and drain terminals during the off-state of the transistor due to the weak inversion layer at the oxide–substrate interface. This takes place when the gate voltage is lower than the threshold voltage. The sub-threshold leakage current increases exponentially as the size of the features continues to decrease. The reduction in transistor geometry is accompanied by a reduction in the thickness of the gate oxide, resulting in improved performance. However, this thinning of the oxide layer results in a leakage current between the substrate and the gate through the oxide. It is important to optimize the leakage power in WSNs.

$P_{dynamic}$ is determined by charging and discharging capacitors. $P_{short\,circuit}$ is caused by switching from the supply voltage to the ground. The energy consumed during the data processing can be divided into switching and leakage energies. When running a program, the switching energy is determined by the software level's supply voltage and the total switched capacitance. The highest power consumption is $P_{dynamic}$, which can be determined in Equation (2):

$$P_{dynamic} = \alpha C V^2 f \tag{2}$$

where α stands for the switching factor, a constant value presenting the probability of switching on any particular clock period. V is the supply voltage, and C is a constant, presenting the capacitance currently switched. f is the clock frequency. According to Equation (2), reducing the frequency decreases the power. This is called Dynamic Frequency Scaling (DFS). This technique adjusts the frequency to reduce the power consumption at the cost of the time necessary to complete instruction within the task deadline. The dynamic power and static power are proportional to V^2 and V, respectively. Thus, reducing the supply voltage of some blocks of a System on a Chip (SoC) to a level near their minimal operating voltage directly affects the total dissipated power.

The DFS technique can be extended by adjusting both frequency and voltage. This method is known as DVFS, which reduces power consumption by driving the device with the minimum core voltage and operating frequency subject to the task deadline. The higher the microcontroller operating frequency is, the higher the core voltage needed to drive the microcontroller. However, a higher core voltage than that needed to execute operating instructions can lead to significant power losses. The power management module (PMM) can adjust the core voltage so that the microcontroller operation runs at the given frequency with minimal power losses. Once the microcontroller is powered on, the PMM gains

control of the system initialization. The DVFS technique is used to reduce both leakage and dynamic power consumption.

The DVFS technique is widely adopted in energy efficiency approaches while meeting the QoS requirements of micro-architectural components, such as GPUs [42], data servers [43], MCUs [26], multi-core [44], memory [45], Network on Chip (NOCs) [46], in the cloud computing [47], in the network packet processing [48], in solving task execution scheduling problems [30], and in solving the problems of the IT industry. The approaches mentioned in Table 2 consider battery-powered devices combined with scarce external power sources while allowing performance penalties to increase the lifetime of the sensor nodes. In addition, they provide a glimpse into the premise of DVFS use in energy harvesting devices. Some works even violate voltage limits risking performance degradation as well. However, in our work, we try to respect the performance and reliability metric by increasing the amount of work achieved when the sensor node is active. We provide a real-world implementation of such a technique and a comprehensive evaluation that pinpoints the benefits of using DVFS.

The implementation of DVFS in a networked sensor system leads to reducing the overall power consumption in soft real-time WSN applications. To meet the deadline with our approach, a system's clock commonly sustains its accuracy by using a synchronization mechanism, such as the Network Time Protocol (NTP), Timing-sync Protocol for Sensor Networks (TPSN), and the Flooding Time Synchronization Protocol (FTSP) [49].

3.2. DVFS Implementation

Using the internal clock source, the methodology followed to perform the DVFS algorithm at the microcontroller is depicted in Figure 3.

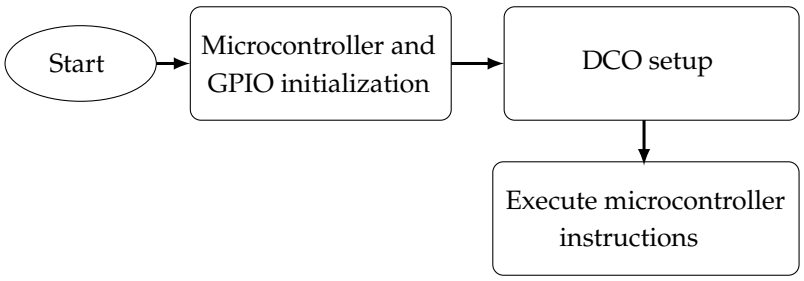


Figure 3. Clocking MSP430F5529LP using the internal clock source.

The board and inputs/outputs initialization step includes two operations. The first one is stopping the Watchdog Timer (WDT). It is crucial since the tested operations run continuously while the measured data acquisition occurs. The watchdog timer's default behavior is resetting the microcontroller if the firmware appears stuck in a loop. This default feature has to be disabled to prevent an infinite boot loop. The second operation is setting up a general purpose Input/Output (GPIO) array. This step is necessary to set up directions for available pins on the board. The second step, called a Digitally Controlled Oscillator (DCO) setup, targets performing the PMM core level setting, clock initialization, and frequency-locked loop setting.

The power management module sets the core power level according to the PMM frequency and core voltage relation. The selected PMM core level must be sufficient to drive the microcontroller application. Accounting for the desired microcontroller frequency, the PMM sets the voltage thresholds of the Supply Voltage Supervisor (SVS) and Supply Voltage Monitor (SVM). The PMM circuit used for the threshold setting is described in Figure 4.

Table 2. WSN-DVFS based techniques' comparison.

Techniques	References	Year	Paper Contributions
DVFS+workload	[39]	2017	- Inter-cluster exploitation: thread-to-core mapping - Adaptation process to select proactively an appropriate V-F pair for a predicted workload - Memory Reads Per Instruction (MRPI) workload classification
EA-DVFS	[50]	2008	- Delays task execution if sufficient energy is not available - Runs at high speed if not
GPU+DVFS	[42]	2013	- GPU Watch to simulate DVFS of the GPU core at the cycle level, based on the Fermi GTX48 GPU according to the 45 nm prediction technology model - DVFS simulation slow off-chip and fast on-chip
DVFS HESS	[51]	2020	- Energy-harvesting based on solar energy - DVFS based low-power microprocessor - Low-power lazy task scheduling policy
DVFS+DPM	[52]	2013	- Two frequencies of voltage/frequency - Turning off a part circuit or running it in low-power modes when no workload
Workload management	[40]	2013	- Transition overhead-aware with modern DC–DC converters for high-end, embedded and ultra low-power applications
DPM+GEDF	[53]	2022	- Time-out DPM in idle mode - Intertask DVFS in active mode - Global Earliest Deadline First, (GEDF) with modified scheduling assumption
Multi-cores+run time management	[44]	2019	- Performance prediction model when making run-time decisions - Application state and workload monitoring for previous DVFS parameters and mappings between threads and kernels
Multicore+task mapping	[54]	2018	- Mapping of imprecise computation tasks on multicore DVFS platforms based on QoS - A low complexity optimal DVFS task mapping based on Benders decomposition
Run time+energy harvesting	[55]	2020	- Capturing the capacitor voltage by a voltage detectors and undervoltaging it with a voltage regulator. - A software modification of the frequency
Our solution		2022	- Ultra low power Microcontrollers - Duty-cycle aware in the transceiver level - DVFS - Workload management

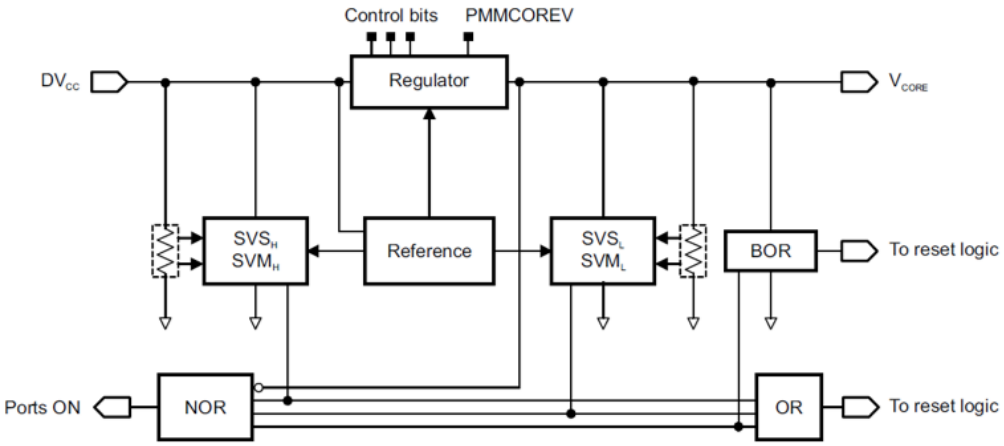


Figure 4. Power management module block diagram following [56].

When the application requires a higher operating frequency to increase the performance, the user can programmatically increase the threshold of High-SVM and High-SVS values, which detects external power voltage to ensure that the power supply is sufficient to drive the core voltage. The Low-SVM is then updated to a higher level, and an SVS/SVM delay mask is activated to enter in a Power-On-Reset (POR) state until the SVS and SVM circuits have settled.

After that, the PMM increases the core voltage to a higher level and waits for the voltage to reach this increased level. Finally, the system sets Low-SVS to a higher level, and the core starts to run. Whenever the core voltage level is modified, the PMM resets the core. The flowchart of the PMM core level mechanism is described in Figure 5.

The microcontroller clock is initialized by setting a user-defined clock to a specified clock source oscillator. For the presented tests, the REFOCLK is used as the source for configuring the internal Frequency Locked Loop (FLL) with no clock divider.

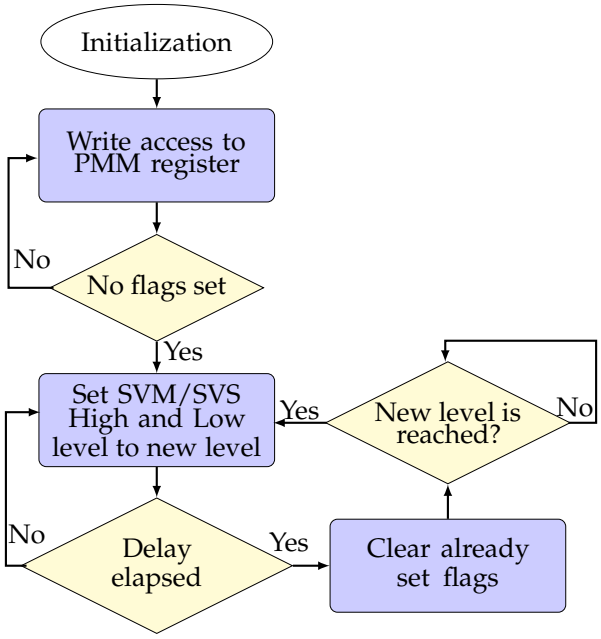


Figure 5. Setting PMM core level (Purple color: Action, yellow color: Condition).

In this stage, the FLL is calibrated to use the MCLK as its oscillator source. The DCO is also configured using the MCLK and FLL reference clock sources. Once the DCO has been configured to operate the microcontroller at a defined frequency, the desired operation

under test is specified within an infinite loop. The microcontroller operations used for our evaluations are nop and add.

4. Experimental Performance Evaluation

To evaluate the power consumption of the MSP430F5529LP development board, clocking the used board via an internal clock source is performed. Thus, the consumed power of the board for different frequencies and voltages is measured, and the obtained results are analyzed.

Measurements are carried out by interfacing the device under test (DUT) with the measurement mainframe E5270A 8-channel Precision IV Analyzer (Keysight Technologies GmbH, Böblingen, Germany) [28] as shown in Figure 6. This device provides power, controls the output voltage, and measures the drained current. It consists of the four wires' measurement techniques. The Source Measure Unit (SMU) applies a voltage to the force connection and measures it over the DUT with a sensing interface. The controller adjusts the supply voltage automatically to meet the voltage drop due to the parasitic resistances of the force wires. The current profile has been measured using the built-in ammeter in series with the force connector. The resulting voltage drop is removed by the feedback-controlled four-wire configuration.

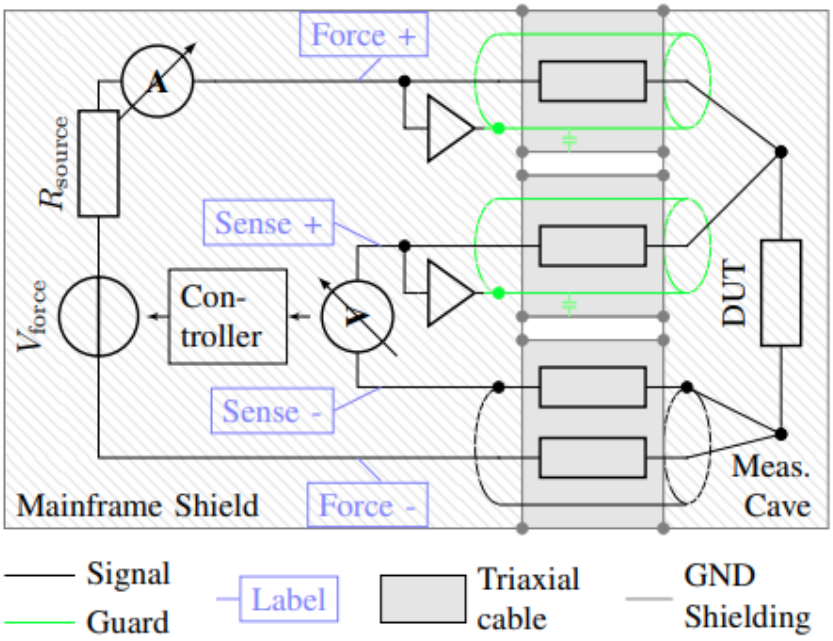


Figure 6. Four-wire measurement configuration involving a Keysight Technologies E5270 8-channel precision mainframe.

An appropriate PMM power level is settled for each measured frequency according to Figure 7. The numbers within the fields denote the supported PMMCOREVx (core voltage level) settings. '0', '1', '2' and '3' correspond to '00', '01', '10' and '11'. The minimum voltage, in this case, is 1.8 V.

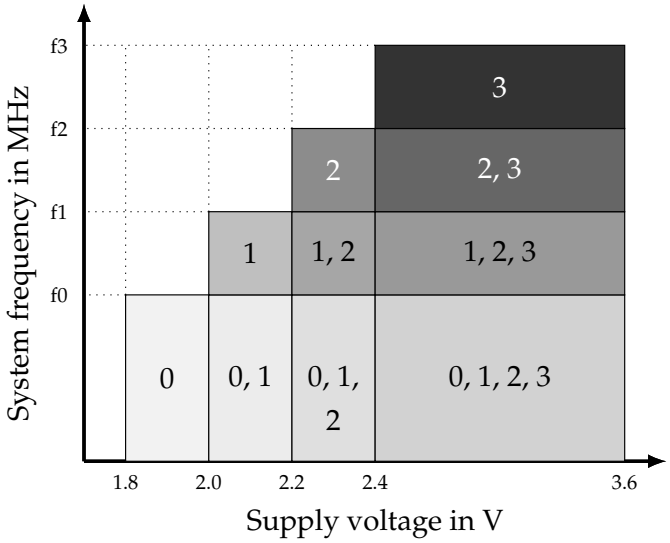


Figure 7. PMM core levels and related frequencies and threshold voltages.

The reduction of the frequency via DVFS increases the execution time. To realize a trade-off between the execution time and the power consumption, we introduce normalized power as an evaluation metric. This metric considers the number of instructions executed in one second, which allows energy consumption profiling. Otherwise, reducing the power only would lead to a significant drop in performance. The benefit of using normalized power is that it accounts for the influence of CPU throughput:

$$Normalized\ Power = \frac{Average\ Power}{Throughput \times 1\ \mu s} \tag{3}$$

$$Throughput = \frac{CPU\ Frequency}{Cycles\ per\ Instruction} \tag{4}$$

Firstly, the frequency is set to 6 MHz and the supply voltage, Vs, varies from 1.8 V to 3.6 V. As seen in Figure 8, the most significant voltage, 3.6 V, matched initially to the greatest normalized power, even though this value drops with time. As depicted in Figure 8a,b, for a voltage equal to 3.6 V, the normalized power increases by 32% once switching from 6 MHz to 20 MHz. When it comes to whole-system performance, the higher the value of the normalized power measured, the faster the processor. Therefore, the processor can provide higher throughput with the same algorithm and the same voltages.

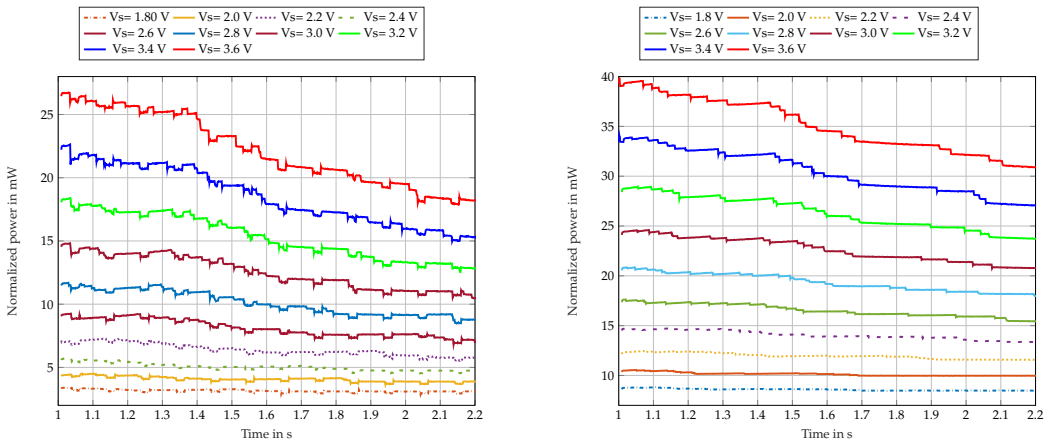


Figure 8. Normalized power during the time for different supply voltages at (**a**) 6 MHz; (**b**) 20 MHz.

4.1. Impacts of DVFS Implementation on Active Operation

The power consumed during active mode is often identified and characterized as a multiplication of the supply voltage and average current of the microcontroller's active mode. This argument is correct when the microcontroller operates in active mode indefinitely. This can be inaccurate, however, when a microcontroller operates in a duty cycle since the total active power is affected by the microcontroller's performance. As seen in Figure 9, every load can be presented by one or multiple resistor–capacitor (RC) circuits. When the CPU requires current, the voltage waveform across the capacitor would produce RC waveforms with small exponential effects. The reason for measuring normalized power in active mode is that the focus will be not on power consumption but on the power required to accomplish a unit operation. Therefore, the normalized power is defined as a measure of power per throughput in 1 s.

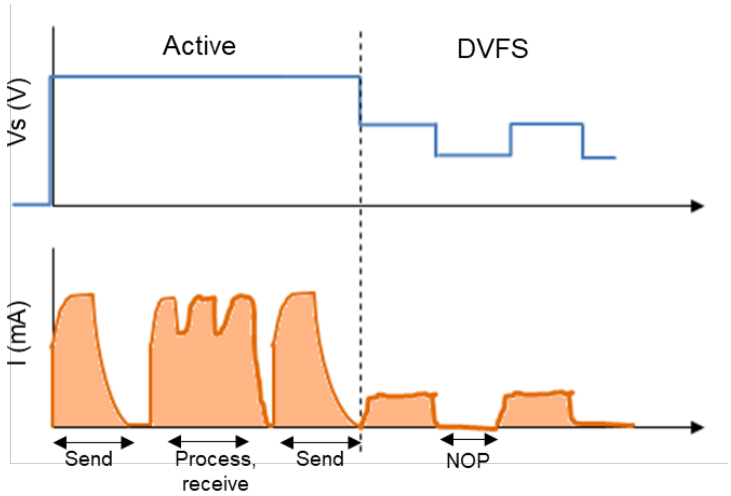
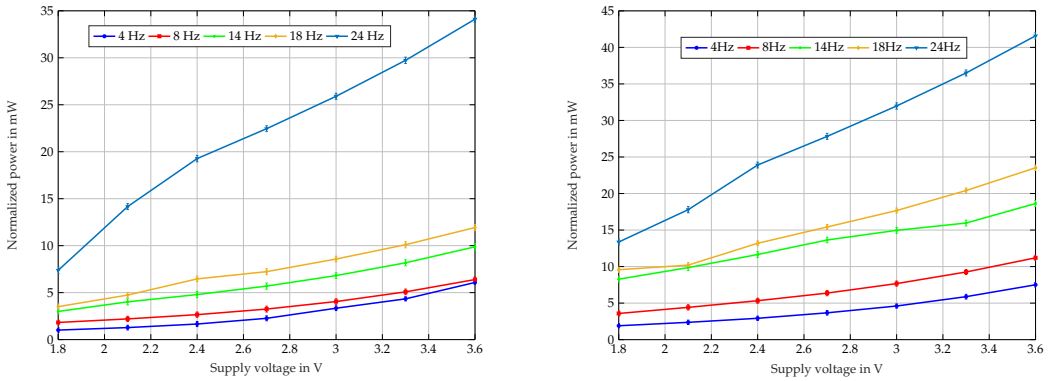


Figure 9. Drained current of the microcontroller during active mode (The dotted line defines the end of the active mode. The orange color presents the consumed current for each mode).

To this end, a set of experiments are realized. Both "nop" and "add" operating instructions are flashed unto the microcontroller alongside clocking instructions.

As depicted in Figure 10a,b, the consumed normalized power is proportional to the supply voltage for a given frequency and given operation. This can be explained by the relationship between the dynamic power consumption and the core voltage of the MCU. This power dissipation is due to the toggling activity of the logic gates. As seen in Equation (2), the consumed power increases as a factor of the square of the core voltage. As shown in Figure 10a, for the frequency equal to 24 MHz, we notice that, when the voltage is gradually increased from 1.8 V to 3.6 V, the normalized power goes from 8 MIPS/W to 34 MIPS/W, resulting in an increase of 76%.

Since one of the most consuming parts of a wireless sensor node is communication, an evaluation of the DVFS implementation is carried out using Bluetooth as a communication module. The Bluetooth pairing is settled to test the power consumption of MSP430F5529LP. The transmitter is configured to continuously send the character "a" during the test duration. As seen in Figure 11, the MSP430F5529LP-based transmitter is connected to the E5270B analyzer. The power supply is tested at 3.6 V supply voltage, as the minimum supply voltage necessary to power the HC-06 Bluetooth module.



(**a**) (**b**)

Figure 10. Normalized power vs. supply voltage at various frequencies for (**a**) "nop" operation; (**b**) "add" operation.

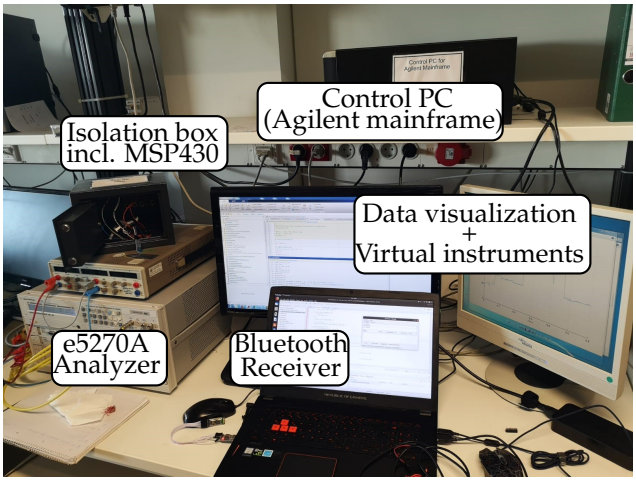


Figure 11. Experimental setup for Bluetooth communication.

In Figure 12, the peak power consumption period occurs during the time slot, $t \approx 0.42$ s, which corresponds to the packet transmission time. Firstly, the MCU is active, and the radio is in sleep mode, consuming about 35 mW. Then, the radio was activated to listen to the channel, leading to increased consumed power. After that, by receiving a packet, the radio consumes about 135 mW. The radio switches to the transmission mode and consumes about 195 mW, corresponding to about 54 mA as drained current.

4.2. Impact of the Duty Cycle on the Power Gain

It can be noticed that the selection of a high operating frequency can generate more efficient normalized power consumption due to the effect of the operating frequency on the duty cycle. For a given voltage, an instruction, such as add, consumes a certain amount of energy during the active phase. However, the power is still consumed by the device during the idle phase of the duty cycle, as seen in Figure 13. In the case of low operating frequency, the average consumed power P_2 may be lower due to the lower power-consuming idle phase of each cycle. However, a large portion of the power is consumed during the idle phase cycle. In the case of high operating frequency, the resulting duty cycle is higher. Hence, there is less power dissipated during the idle phase while no operation occurs despite higher average power consumption P_1.

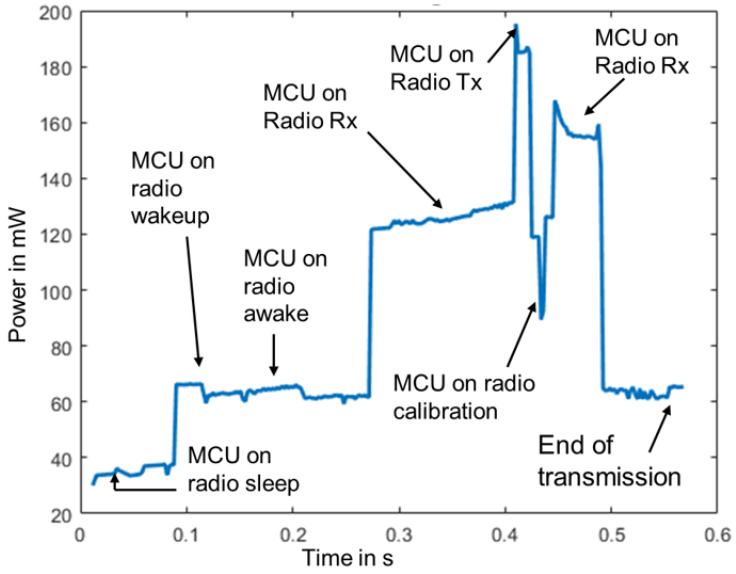


Figure 12. Bluetooth power consumption.

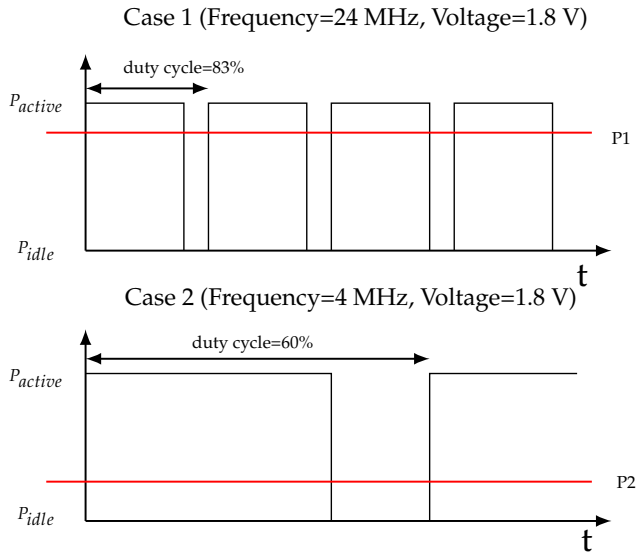


Figure 13. Operating frequency versus power efficiency (P1 and P2 are the average consumed power for high frequency and low frequency, respectively).

DVFS can adjust the system to optimize its performance. The duty cycle value corresponding to the maximum frequency of 24 MHz is equal to 83% and drops to 60% when the frequency is reduced to 4 MHz only proportionally to the normalized power. However, the frequency change is not instantaneous, and switching from one frequency to another requires a time delay. As a result, close frequency changes will significantly slow down the execution of the application, resulting in over consumption. As a result, when the variation reaches 4 MHz from 4 to 8 MHz or from 14 to 18 MHz, the normalized power gain is equal to 5 mW/MIPS. However, when this variation goes to 6 MHz (8–14 or 18–24 MHz), this gain becomes 2 mW/MIPS at the same supply voltage (1.8 V).

Figure 14 summarizes the average power gain for different frequencies with different core voltages. The x-axis presents the core voltage deviation, which means switching from one voltage to another considering the values defined in Figure 7. As an example, to have a deviation of 1.2 V in the core voltage, for 4 MHz, we can move from 2.4 V to 3.6 V or from 2.1 V to 3.3 V or from 1.8 V to 3 V. The average power gain, in this case, is equal to 72.75%. The average power gain increases with the increase of the core voltage deviation.

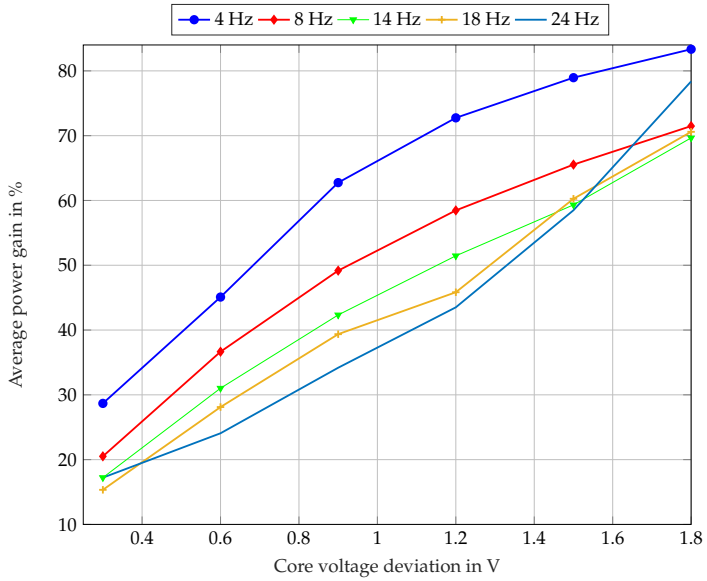


Figure 14. Power gain.

Frequent changes in the DVFS are not the only challenge, as the right frequency must still be used. A misallocated frequency can lead the program to consume more energy, and small frequencies may not be the most energy efficient. If an application runs for a certain time at a given frequency, lowering the execution frequency may extend the execution time of the application to such an extent that the energy consumed will ultimately be greater. Changing frequency is time-consuming, in the range of ten microseconds. Consequently, too frequent changes in frequency will have a negative impact on the system performance, obviously leading to the worst-case execution time (WCET) of the application, and consequently to inefficient energy consumption.

The proposed hybrid energy management system can be implemented for ultra-low-power wireless sensor network applications to ensure the trade-off between energy efficiency and system performance. Generally, the wireless sensor nodes have single-core processors. They are unable to satisfy the increasing demands of data-intensive applications, such as wireless multimedia sensor networks. Therefore, multi-core integrated sensor nodes with advanced communication and computational capacities. Our solution can be integrated into multi-core architectures leading to significant energy reductions compared to the basic methods, where there is no DVFS.

Currently, the developed hybrid energy management solution is implemented to reduce the power consumption of a wireless sensor node in a unique IoT application. However, recently, advanced IoT architectures have been established such as the multiple IoT (MIoT) architecture [57,58]. Generally, an MIoT can be considered as a set of things interconnected by relationships of various types and simultaneously. It involves the concept of instance of a thing in an IoT architecture. An instance presents the virtual view of the corresponding thing. Each IoT node represents instances of the objects participating in it. Therefore, a thing can have multiple instances, one for each IoT it takes part in. In future work, we will implement the proposed solution in a MIoT-based architecture, including several IoT connected to each other through cross nodes and cross edges.

5. Conclusions

This paper focuses on the reduction of the overall power consumption of a wireless sensor node through the selection of a low-power microcontroller, as well as the implementation of the power management-based DVFS technique. In fact, extensive benchmarking based on real-world measurements promoted the MSP430 as the most optimal microcontroller to ensure the best compromise between performance and energy. Therefore, both clocking and power consumption analysis of MSP430f5529LP launchpad is performed to

profile mainly nop and add instructions using DVFS as a power reduction technique. Obtained results prove that high power efficiency is maintained at high operating frequencies for defined instructions. In fact, for a voltage equal to 3.6 V, the normalized power increases by 32% once switching from 6 MHz to 20 MHz. Moreover, it is demonstrated that, when the variation between two frequencies reaches 4 MHz, i.e., from 4 to 8 MHz or from 14 to 18 MHz, the normalized power gain is equal to 5 mW/MIPS at a supply voltage equal to 1.8 V.

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