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A 1.25 MHz, 108 dB Chopped Sampling-Mixer-Based Impedance Spectroscopy SoC in 0.18-µm CMOS

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Abstract: This paper presents an electrochemical impedance spectroscopy (EIS) system-on-chip in 0.18-µm CMOS, achieving a wide scan frequency range of 1.25 MHz. An on-chip direct digital frequency synthesizer generates a digital sine wave as well as in-phase and quadrature-phase clocks that are synchronized to the sinewave. A chopped sampling mixer realizes lock-in detection without requiring quadrature sinewaves while suppressing low-frequency noise and offset. The receive utilizes a 12-bit pipelined SAR ADC operating in 5 MS/s in combination with a digital averaging filter to maximize the dynamic range. The measured performance shows that the prototype EIS chip achieves the highest frequency scan range with a comparable dynamic range of 108 dB and power consumption of 14 mW when compared with the previous state-of-the-art prototypes.

Keywords: electrochemical impedance spectroscopy (EIS); direct digital frequency synthesizer (DDFS); impedance analyzer; pipelined successive approximation register (SAR); analog-to-digital converter (ADC)

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1. Introduction

Electrochemical impedance spectroscopy (EIS) is used in various sensor applications that require impedance measurement of a specific target [1–7]. Notable examples include gas concentration measurement [1], battery condition measurement, [2] human body composition analysis [3], impedance cardiography [4], and lung ventilation monitor [5]. It is also applied to systems that detect molecular substances ranging from intracellular action potential [6], DNA [7], and RNA [8] detection. In these applications, it is commonly required to accurately measure the impedance over a wide frequency range. For instance, DNA and RNA are typically measured between 100 Hz and 10 kHz, whereas some DNA detections are measured up to MHz frequencies [9]. Therefore, it would be ideal if the EIS system could cover a wide frequency range with a fine frequency resolution.

Traditionally, the EIS system has been implemented using a lock-in amplifier followed by a low-pass filter and an A/D converter [10,11]. However, it is challenging to design a general-purpose EIS system covering a wide frequency range. Specifically, a lock-in-based EIS system requires a quadrature analog multiplier with a variable clock frequency generator. Hence, this system must deal with various analog design issues, such as mismatches between in-phase and quadrature-phase (I/Q) signals. A full-digital lock-in system that did not suffer from the quadrature mismatch was demonstrated in [12], but it requires complex digital signal processing that includes high-speed digital multiplication, not to mention the necessity of a high-resolution and high-performance A/D converter (ADC). A recently presented FFT-based impedance analysis has the advantage of calculating impedance at multiple frequencies with a single A/D conversion followed by an FFT analysis, but this system requires a very high-resolution ADC such as 16-bit or 24-bit [1], which is challenging to design, especially when the required ADC clock frequency is over MHz ranges.

In this paper, we present a wide-frequency EIS system-on-chip (SoC) in 0.18-µ*m* CMOS by utilizing the concept of a sampling mixer. The proposed EIS architecture offers a new

way of measuring the impedance over a wide frequency range without using an analog multiplier or a complex FFT engine. Our prototype EIS system is designed as a system-on-chip, which includes a 10-bit direct digital frequency synthesizer (DDFS) with an embedded I/Q generator, a quadrature chopped sampling-mixer front-end, and a 5 MS/s, 2-stage, 12-bit pipelined successive approximation-register ADC for impedance detection. The measured performance confirms the validity of the operation by demonstrating a dynamic range of 108 dB with up to 1.25 MHz impedance frequency scan range. The measured performance is comparable to a state-of-the-art EIS system in terms of frequency and dynamic ranges.

The paper is organized as follows. Section 2 begins with a review of the lock-in impedance detection, followed by introducing a concept of the sampling-mixer-based impedance detection technique. Section 3 shows the architecture of our EIS SoC and describes details of the key circuits that include both the transmitter and the receiver. Section 4 presents the experimental results with a brief discussion. Section 5 concludes the paper.

2. Sampling-Mixer-Based Impedance Spectroscopy

This section begins with a review of lock-in detection, which is the underlying theory of impedance spectroscopy, followed by the concept of the proposed sampling-mixer-based impedance detection technique.

2.1. Review of Lock-In Detection Theory

Measuring the complex impedance of a target can be accomplished by measuring the magnitude and phase response of the target. Therefore, in many sensor applications, the transmitter generates a sinewave that passes through the target to be sensed, and the receiver measures the response, which is then post-processed to calculate the impedance. By iterating this process over a large number of discrete frequencies, one can find the overall impedance characteristic versus frequency, which is often called electrochemical impedance spectroscopy (EIS). Lock-in detection is the most traditional and popular technique in EIS when detecting a very small signal with a magnitude of nV-level under the presence of broadband noise.

To explain the difficulty, consider the cases shown in Figure 1. It is assumed that the amplifier has a DC gain of 1000 $[V/V]$ with a pole frequency of 100 kHz and an input-referred noise level is $\overline{V_n} = 5nV/\sqrt{Hz}$. It is also assumed that the input signal has an amplitude of 10 nV with a frequency of 10 kHz.

Figure 1a illustrates the case when no filtering is used. In this case, the total integrated RMS noise voltage ($\overline{V_{n,out}}$) at the output is calculated as

$$\overline{V_{n,out}} = \frac{5nV}{\sqrt{Hz}} \times 1000 \times \sqrt{\frac{\pi}{2} \times 100kHz} = 2\ mV_{rms}\ , \tag{1}$$

Because the output signal amplitude after the amplifier is only 10 μV, the output SNR is -49 dB, and it is impossible to detect such a signal. Figure 1b illustrates the case that utilizes a sharp band-pass filter with a quality factor (Q) of 100. In this case, the integrated noise power after the filtering can be calculated as

$$\overline{V_{n,out}} = \frac{5nV}{\sqrt{Hz}} \times 1000 \times \sqrt{100Hz} = 50\mu V_{rms}\ , \tag{2}$$

leading to an output SNR of -17 dB, which is still not acceptable. To alleviate this difficulty, the lock-in amplifier shown in Figure 1c down-converts the signal by quadrature multiplication. Since the signal is located at DC after the down-conversion, a low-pass filter with an extremely low bandwidth can be used to filter out the noise. For instance, if the filter bandwidth is 0.01 Hz, $\overline{V_{n,out}}$ is given by

$$\overline{V_{n,out}} = \frac{5nV}{\sqrt{Hz}} \times 1000 \times \sqrt{0.01Hz} = 500nV_{rms}\ , \tag{3}$$

which results in acceptable SNR of 23 dB (Mathematical derivation of the lock-in detection is included in the Appendix A).

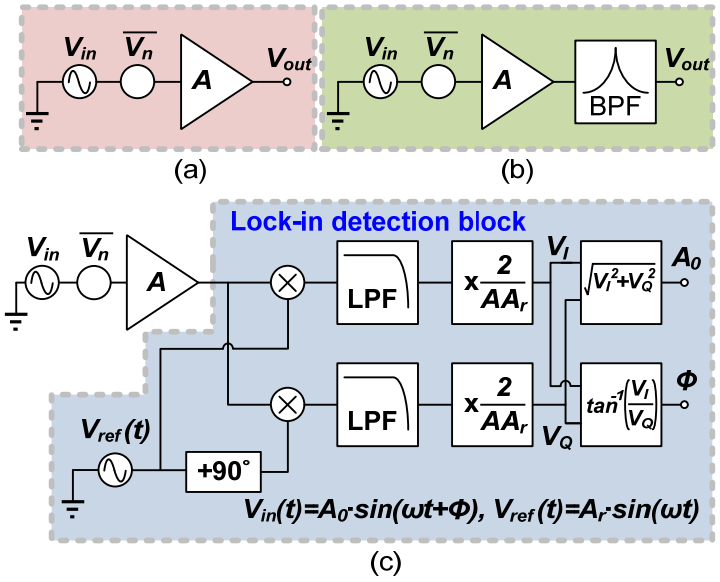

Figure 1. Simple measurement system of V_{in} with (**a**) only an amplifier, (**b**) an amplifier with a bandpass filter, and (**c**) an amplifier and lock-in detection block.

2.2. Sampling-Mixer-Based Impedance Measurement

A key challenge in using lock-in detection for an integrated EIS SoC design is the necessity of a high-linearity analog quadrature multiplier. Moreover, generating a quadrature sinewave over a wide frequency range is not trivial. In this work, we propose to use an alternative technique based on a sampling mixer [13], which is used in wireless RF receiver designs. The central idea is that when the received signal after the target is sampled by quadrature clocks having the exact same frequency as the signal, both the magnitude and phase response of the target can be recovered. Specifically, suppose that the received signals after the quadrature sampling are given by

$$V_{I,\,RX} = A_0 \cdot \sin(2\pi f_s \cdot t_1 + \phi), \tag{4}$$

$$V_{Q,\,RX} = A_0 \cdot \sin\left(2\pi f_s \cdot \left(t_1 + \frac{1}{4} \cdot \frac{1}{f_s}\right) + \phi\right) = A_0 \cdot \cos(2\pi f_s \cdot t_1 + \phi), \tag{5}$$

where A_0 is the amplitude of the received sinewave that reflects the magnitude of the impedance. From these two values, one can easily calculate the magnitude as

$$A_0 = \sqrt{V_{I,RX}^2 + V_{Q,RX}^2}, \tag{6}$$

$$\phi = \tan^{-1}\left(\frac{V_{I,RX}}{V_{Q,RX}}\right). \tag{7}$$

Note the sampling-mixer-based impedance measurement does not require a quadrature sinewave, which is difficult to realize in CMOS circuits. Instead, it requires a quadrature clock and a sampler that are more compatible with CMOS design. There are several key circuit blocks when one wants to implement the sampling-mixed-based impedance measurement. They include: (1) A programmable sinewave and quadrature clock generator, (2) A sampling mixer front-end, and (3) A high-resolution A/D converter. In the following section, we will describe the architecture of our EIS SoC and present details of the circuit implementation.

3. EIS Architecture and Implementation

3.1. EIS Architecture Overview

Figure 2 illustrates the architecture of our sampling-mixer-based EIS SoC. The transmitter generates a programmable sinewave, which drives target impedance. The resulting current from the target is converted to voltage via an off-chip trans-impedance amplifier (TIA), which then drives the sampling-mixer-based on-chip receiver.

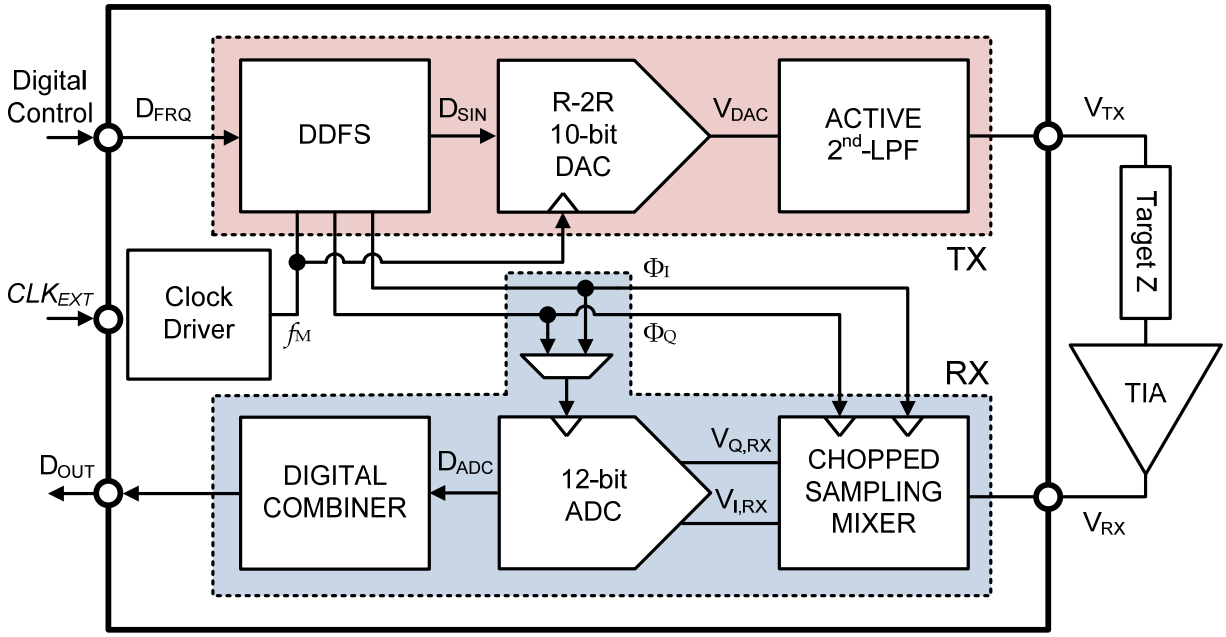

Figure 2. The block diagram of our EIS SoC.

As mentioned above, the transmitter stage must generate a reference sinusoidal signal of a known and programmable frequency. To meet this need, a direct-digital frequency synthesis (DDFS) engine is implemented to generate a 10-bit digital sinewave. The DDFS runs at CLK_{EXT} with f_M = 50 MHz, and the frequency can be finely tunable with a 10-bit resolution. Since the digital sinewave is generated using CLK_{EXT}, the highest frequency of the sinewave is less than f_M. In our implementation, the DDFS can generate possible frequencies from f_{min} = 50 MHz/1024 to f_{max} = 25 MHz. Note that if we want to measure the target impedance at a lower frequency than f_{min}, we can lower the f_M because the sinewave frequency is automatically scalable with the clock frequency. The DDFS is followed by a 10-bit DAC and a 2nd-order active low-pass filter that convert a digital sinewave into an analog one. The DAC adopts an R-2R DAC structure to reduce the number of resistor strings, thereby minimizing the area.

At the receiver side, the signal converted back to voltage through the TIA undergoes the sampling in the CMOS sampling mixer, where chopping is adopted to remove low-frequency noise such as flicker noise. In the sampling process, Φ_I and Φ_Q from the DDFS are used as the in-phase and the quadrature-phase sampling clock, respectively. Since these clocks are synchronized with the input signal, a quadrature sampling with the exact same frequency as the signal is realized. Moreover, to reduce the silicon area, a clock multiplexer is adopted so that either Φ_I or Φ_Q is routed to the sampling clock. By sequentially measuring the received signal at in-phase and quadrature-phase, it is possible to make all required measurements with a single ADC, which greatly saves the area. In addition, using the same ADC for sequential measurements fundamentally removes problems, such as offset and gain mismatches, that may occur when multiple ADCs are used. The ADC in the receiver is a wide-bandwidth pipeline Successive-Approximation-Register (SAR) ADC, the use of which makes extending both resolution and sampling

speed much easier, compared to a conventional SAR ADC. In our design, the ADC operates at 5MS/s with a 12-bit resolution, both of which are necessary for wide-bandwidth and high-dynamic range measurement. The obtained 12-bit resolution output D_{ADC} is then further processed in an off-chip digital averaging filter with a window size of 4096 to enhance the dynamic range of the output.

3.2. DDFS Implementation

Figure 3 illustrates the block diagram of the DDFS in the transmitter. In the transmitter, it is necessary to generate both the sinewave signal with a wide frequency range and the quadrature reference clock of the same frequency. A 10-bit DDFS is designed in this work, where the resolution is chosen to match with the following 10-bit D/A converter. The DDFS includes a digital phase accumulator that adds a fixed amount of phase for a sinewave at every DDFS clock cycle, a sine look-up table that stores the digital sinewave, and an I/Q clock generator that generates the in-phase and the clocks synchronized with the digital sinewave. When the DDFS clock frequency is f_M, and the phase accumulator input is k, which is a programmable 10-bit digital accumulation step for the phase accumulator, the output frequency of the DDFS is given by

$$f_{DDFS} = \frac{k}{2^{10}} \cdot f_M. \tag{8}$$

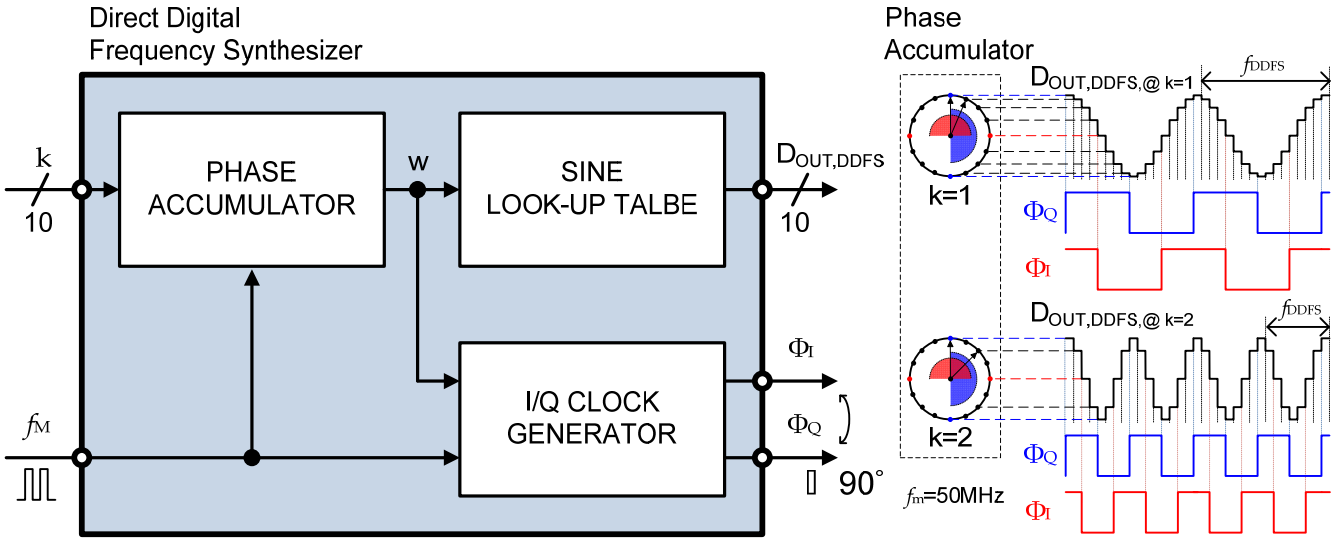

Figure 3. The DDFS block diagram with a principle of DDFS operation.

This is accomplished by defining the look-up table to store the digital sinewave with a 10-bit phase resolution at intervals of $2\pi/1024$. To generate the in-phase and quadrature-phase clock, the overall phase space is divided into four states on the phase boundaries at $\pi/2$, π, $3\pi/2$, and 2π. By decoding these states, the DDFS generates two 90-degree shifted clocks. For example, the in-phase clock Φ_I is a digital high when the DDFS phase is from 0 to π, and the quadrature-phase clock Φ_Q is a digital high when the DDFS phase is between $\pi/2$ and $3\pi/2$. This simple decoding logic allows us to build accurate quadrature clocks synchronized with signal frequency without using extra hardware.

3.3. EIS Receiver

3.3.1. Chopped Sampling Mixer

Figure 4a shows the configuration of the chopped sampling mixer. As described in Section 2, it is necessary to detect the quadrature and in-phase components of the sine wave signal to calculate the magnitude and phase response. In other words, the receiver should be able to sample the signal quadrature voltage (V_Q) and in-phase voltage (V_I)

with a phase difference of $\pi/2$. One concern here is that low-frequency noise, such as the flicker-noise of the switch or the input-referred offset of the ADC, can degrade the measurement accuracy because the signal is at DC. To alleviate this issue, a sampling mixer composed of four switches can be conceived, as illustrated in Figure 4. The switch operates in two configurations; when Φ_{SA} is high, the switch S_{1A} and S_{1B} pair are connected to TIA output (denoted as RX_{IN}) and common-mode voltage (V_{CM}) to the differential input of the ADC. On the contrary, when Φ_{SB} is high, the RX_{IN} and V_{CM} are swapped before being connected to the differential ADC input. Since this process needs to be performed twice for V_Q and V_I, respectively, the sampling and ADC operation are performed for a total of four cycles. Assuming that the total input-referred offset voltage (V_{OS}) and low-frequency noise (V_n) are added on the positive side of the ADC input, as shown in Figure 4, the four sampled values can be expressed as

$$V_{I1} = V_{I,sam} + V_{OS} + V_n\,, \tag{9}$$

$$V_{Q1} = V_{Q,sam} + V_{OS} + V_n\,, \tag{10}$$

$$V_{I2} = -V_{I,sam} + V_{OS} + V_n\,, \tag{11}$$

$$V_{Q2} = -V_{Q,sam} + V_{OS} + V_n\,. \tag{12}$$

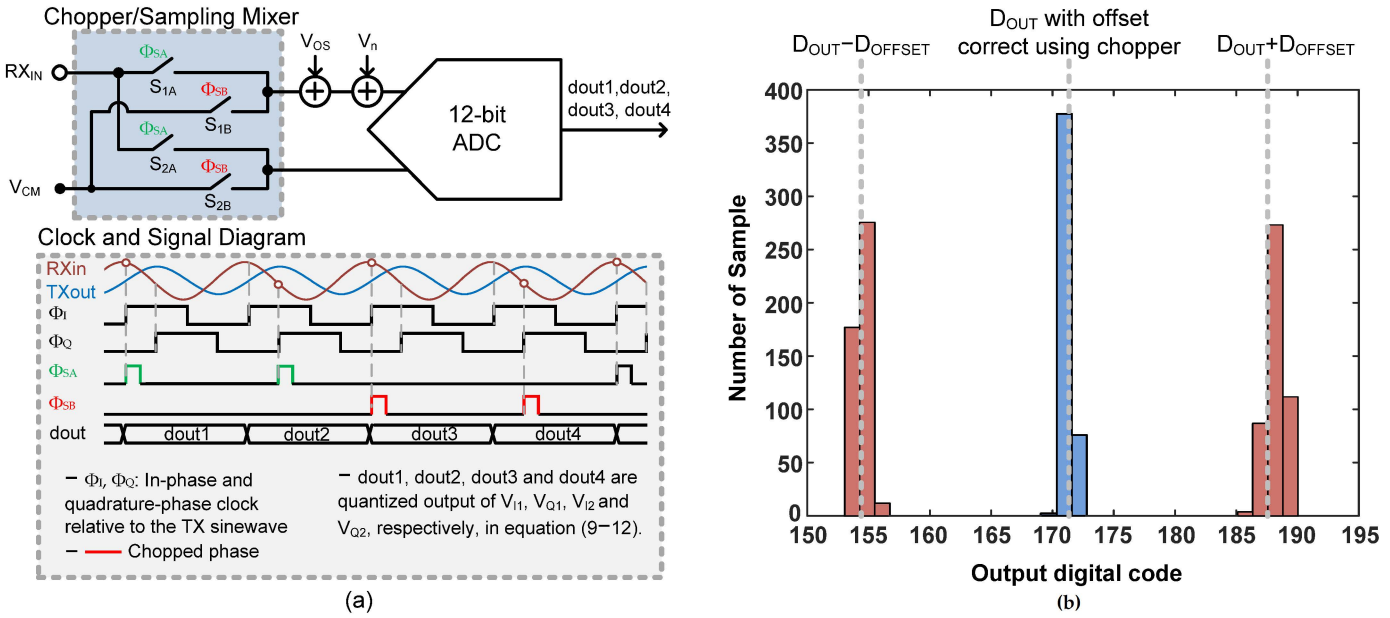

Figure 4. (**a**) The block diagram of a chopped sampling mixer along with key waveforms. (**b**) The simulation result of offset cancellation using a chopping technique.

By combining (9), (10), (11), and (12), one can show that the resulting outputs are given by

$$V_I = \frac{V_{I1} - V_{I2}}{2} = V_{I,sam}, \tag{13}$$

$$V_Q = \frac{V_{Q1} - V_{Q2}}{2} = V_{Q,sam}. \tag{14}$$

Therefore, it can be shown that the low-frequency noise and offsets are canceled out by the chopped sampler with the help of simple digital averaging.

Figure 4b shows the simulation result of a chopper with 50 mV DC input with sampling noise and 5 mV offset. The quantized D_{OUT} value of 50 mV is 171, assuming a 12-bit ADC with 1.2 V input full scale. It is confirmed that the red bins that do not use the chopping

technique show errors (about 17 in terms of digital output code). In contrast, the blue bins with chopping are centered around 171, where offset-included errors are removed.

3.3.2. A 12-Bit 2-Stage Pipelined SAR ADC

The sampled voltage from the chopped sampling mixer needs to be converted to digital values for further post-processing. In this work, it is necessary to design an ADC with wide bandwidth and high resolution. A 12-bit, 2-stage pipelined SAR structure is chosen to satisfy the above design requirements. The overall block diagram and the schematics of the key circuits are shown in Figure 5a. The stage resolutions are 6-bit and 7-bit for the 1st and 2nd stage, respectively, and the inter-stage amplifier gain is chosen to be 16, considering the half-scale reference for the 2nd stage SAR ADC. This arrangement eases the amplifier design with a higher feedback factor while allowing the ADC to tolerate input referred offset of $\pm 1/32$ V_{REF} in the 1st-stage SAR stage without degrading the overall ADC linearity. In addition, linearity errors of the ADC due to capacitor mismatch and parasitic capacitance are addressed by a foreground calibration from which we obtain optimal digital bit weights for the pipelined SAR ADC [14].

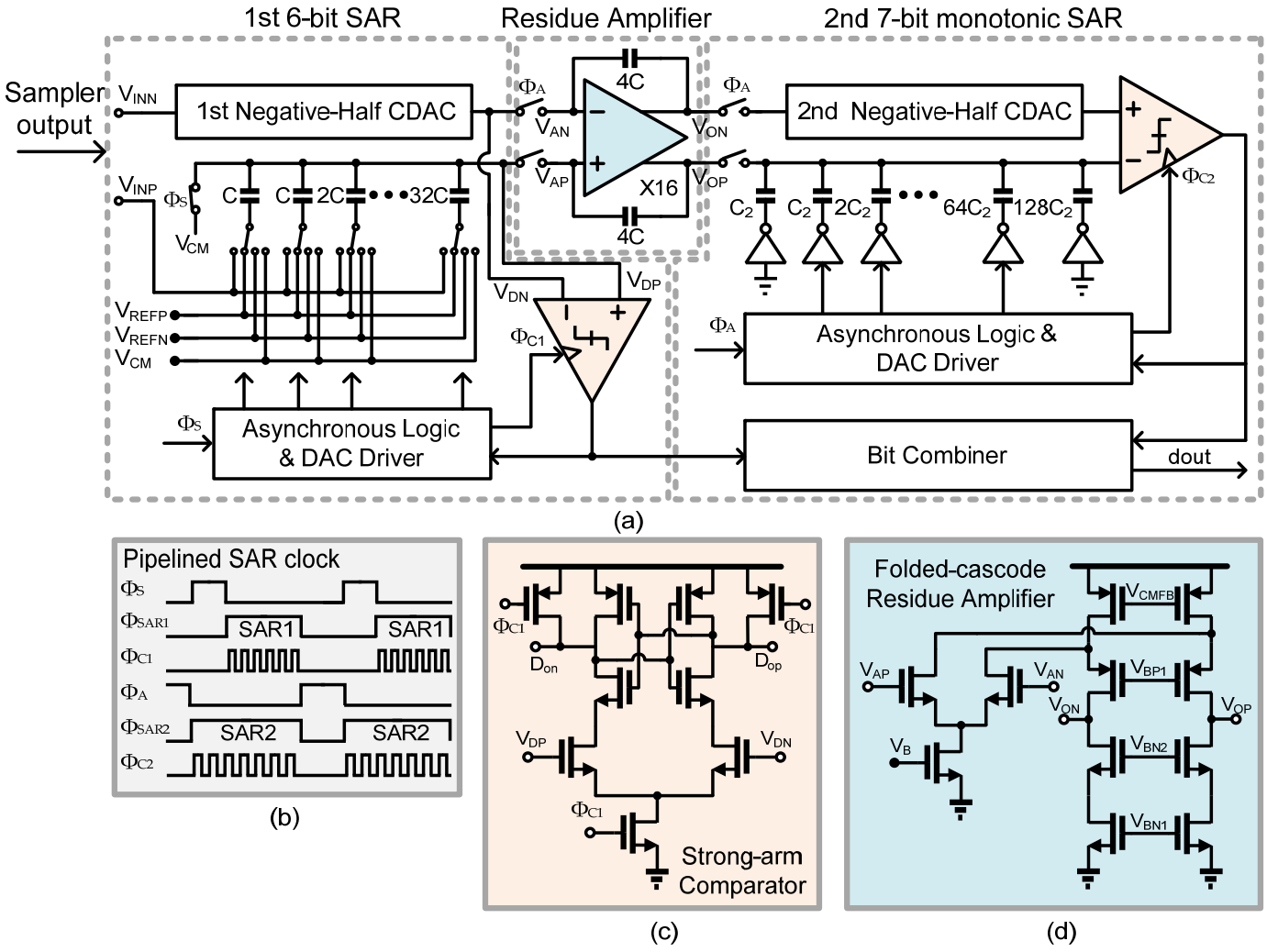

Figure 5. (**a**) The architecture of the 12-bit pipelined SAR ADC. (**b**) The clock diagram of the pipelined SAR ADC. (**c**) The comparator. (**d**) The stage residue amplifier using a folded-cascode structure.

Figure 5b shows the clock diagram of pipelined SAR ADC. The clocking scheme improves ADC throughput by dividing the 12-bit conversions into Φ_{SAR1} and Φ_{SAR2} phases. Compared with a conventional 12-bit SAR ADC that would need 12 comparator

clock cycles, the sampling speed of this ADC is improved by pipelining, which allows placing only six clock cycles for the first stage SAR and seven clock cycles for the second stage SAR, respectively.

The first stage 6-bit CDAC is implemented using a unit capacitance of 28 fF, leading to a total single-ended capacitance of 1.8 pF. A bottom-plate sampling method is adopted for the CDAC implementation, which is immune to the full-scale range reduction of the input stage. The control logic of the SAR ADC adopts asynchronous clocking to increase the power efficiency of the clock generator and is designed to be robust in metastability even in high-speed operation, where the conversion time is relatively fast. The comparator is designed using a strong-arm structure, as shown in Figure 5c.

The second stage 7-bit SAR ADC is designed slightly differently using a top-plate CDAC structure so that the first comparator cycle can be performed immediately after the sampling phase. The CDAC consists of 256 instances of the unit capacitors (C_2), and the unit capacitance is about 4 fF. As mentioned earlier, to secure a 1-bit redundancy, 128 C_2, which is half of the total capacitor, is used as a dummy capacitor so that the half reference is realized [15]. The control logic of the SAR ADC is designed as monotonic switching to minimize the CDAC switching power [16].

As shown in Figure 5d, the inter-stage residue amplifier is designed as a folded-cascode amplifier for a relatively large headroom while having a similar gain compared to the telescopic amplifier. The amplifier designed in 0.18-µm CMOS process achieves a DC gain of 66 dB and unity gain bandwidth of 280 MHz according to SPICE simulations.

Figure 6 shows a simulation result of the 2-stage, 12-bit pipelined SAR ADC. Figure 6a shows the result of the residue transfer function of the inter-stage residue amplifier and the output voltage of the residue amplifier when a 1.2 V input differential voltage is applied. It confirmed that the residue transfer has a gain of 16, as expected. Note that the output of each line segment in the residue transfer must be sufficiently linear for the following-stage resolution, which is 7-bit in our case. The combined linearity has been verified by the time-domain ADC simulation. Figure 6b shows the simulated FFT of this ADC according to the SPICE simulator. The ADC achieves the SNDR of 67.99 dB with random noise enabled.

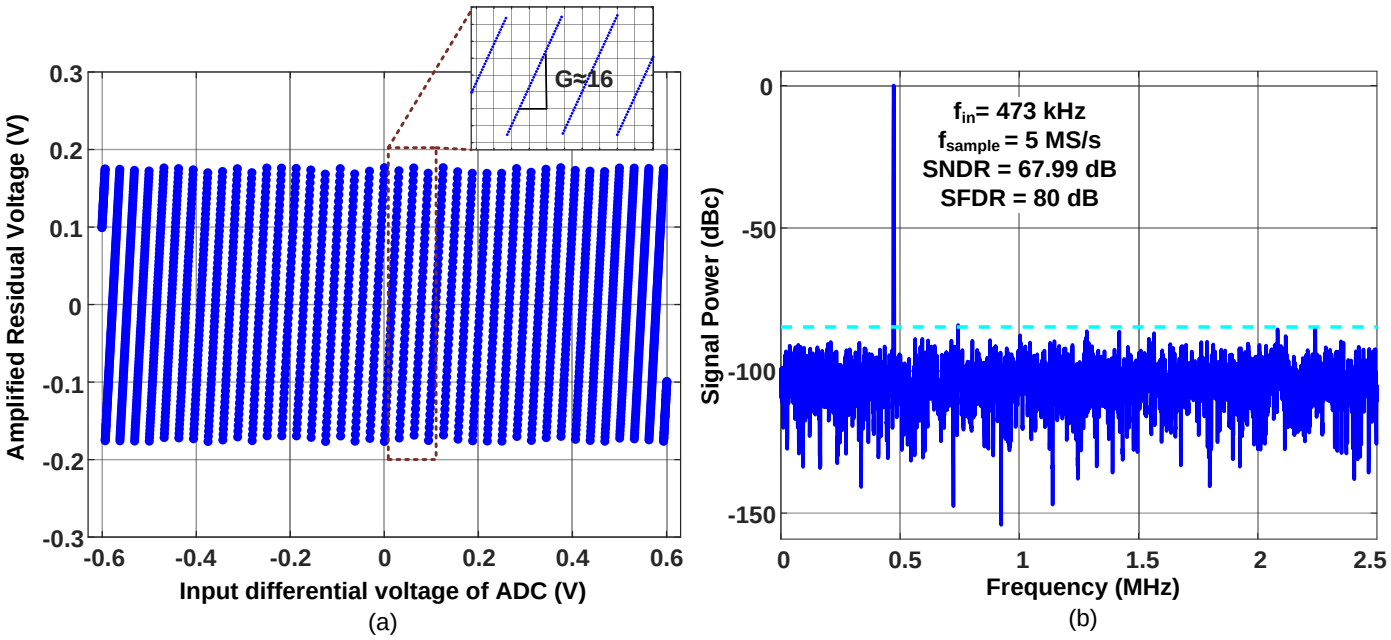

Figure 6. (**a**) The simulated residue transfer function of 2-stage pipelined SAR ADC. (**b**) The simulated ADC spectrum with 473 kHz input when random noise is enabled.

4. Measurement Results

Figure 7 shows the chip microphotograph of the EIS SoC. Fabricated in 0.18-µm CMOS technology, the EIS core, including both the transmitter and the receiver, occupies an area of 0.56 mm^2. The total power consumption is 14 mW when f_M = 50 MHz and the detailed power breakdown is displayed in Figure 8. The EIS measurement setup is shown in Figure 9. The external 50 MHz clock is provided by an off-chip signal generator, and the digital control bits are programmed via an off-chip serial controller. The output of the transmitter drives an off-chip TIA with a feedback resistor, and the TIA output drives back to the input pad of the chip that is directly connected to the EIS receiver, including the chopped sampling mixer and the ADC. The output of the ADC is collected by a logic analyzer, which is further processed in a PC to calculate the impedance as described in Section 2.

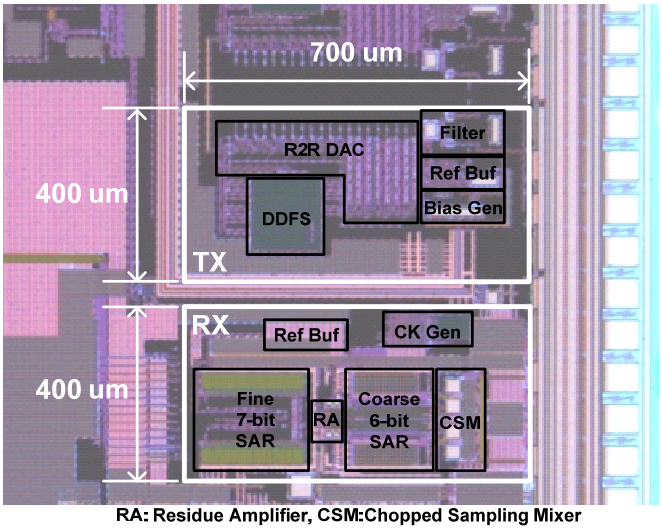

Figure 7. Die photograph of our EIS SoC.

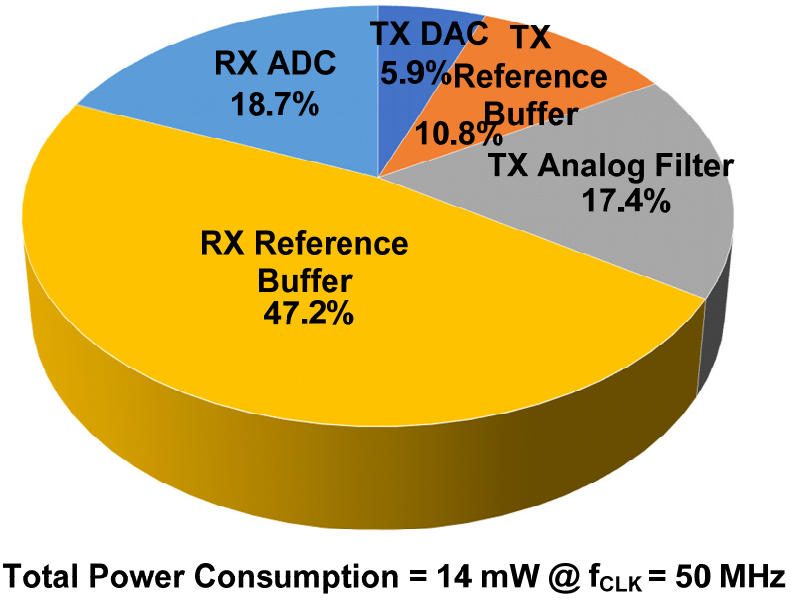

Figure 8. Power breakdown of our EIS SoC at 50 MHz.

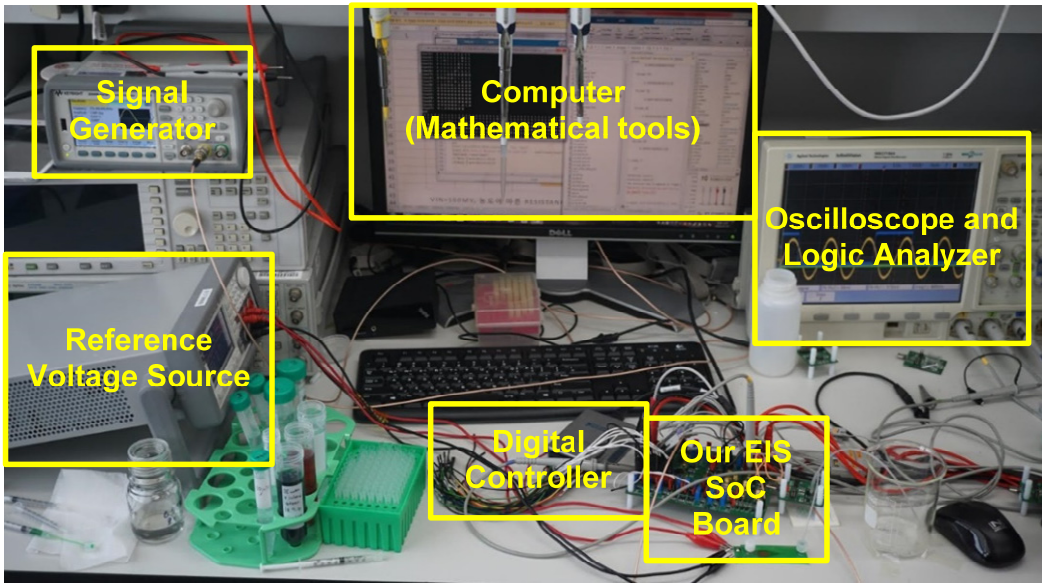

Figure 9. Measurement setup of our EIS system.

The performance of this EIS was measured for a 1 kΩ target reference resistor. Shown in Figure 10a, the measured histogram of the digital output after the digital post-processing reveals that the RMS noise is 6.5 mΩ, which corresponds to a dynamic range of 108 dB. Figure 10b shows the result of measuring the dynamic range (DR) over a wide frequency range from 30 kHz to 1.25 MHz. The graph indicates that the worst-case DR is 97 dB, and the peak DR is 108 dB, as shown above. Figure 11 shows the measurement result of a stand-alone ADC mode via 4096-point FFT. Without the digital averaging, the ADC exhibits SNDR of 62.7 dB and SFDR of 80 dB for f_{in} = 473 kHz and f_{sample} = 5 MHz under 1.8 V supply.

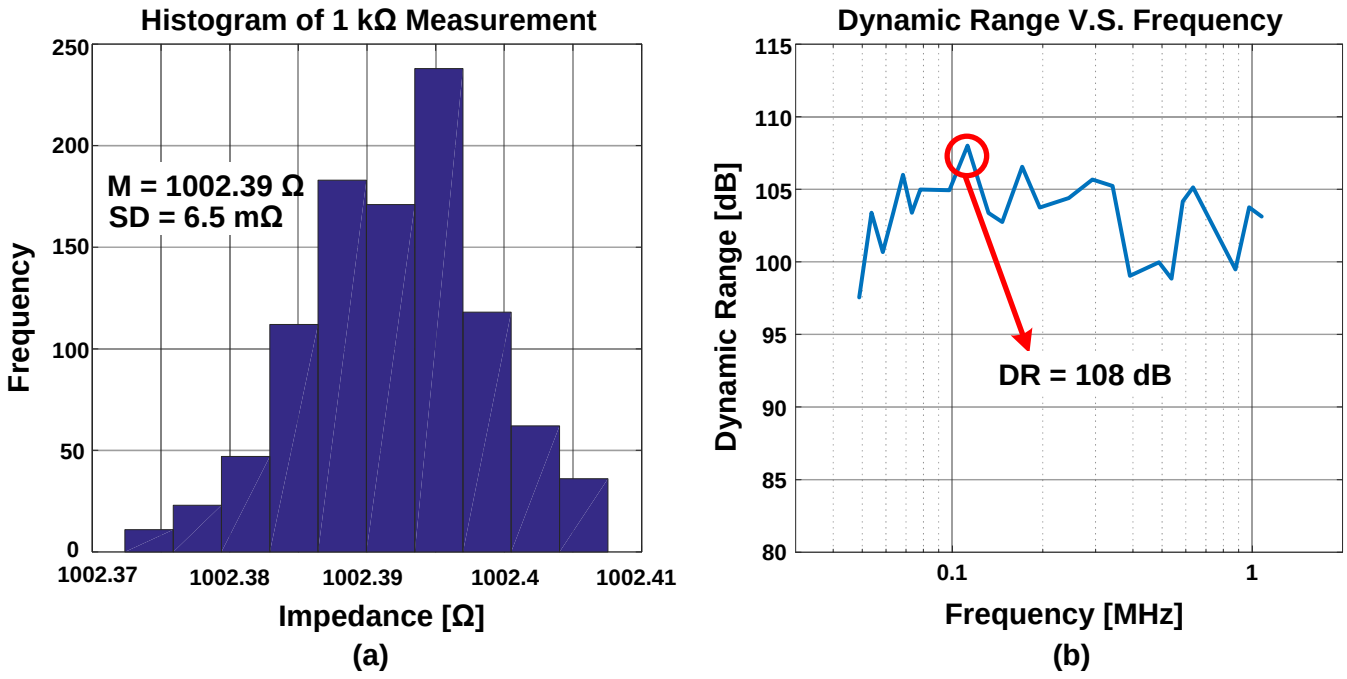

Figure 10. (**a**) Histogram of measured impedance over 1000 measurements. (**b**) Dynamic range measurement from 30 kHz to 1.25 MHz.

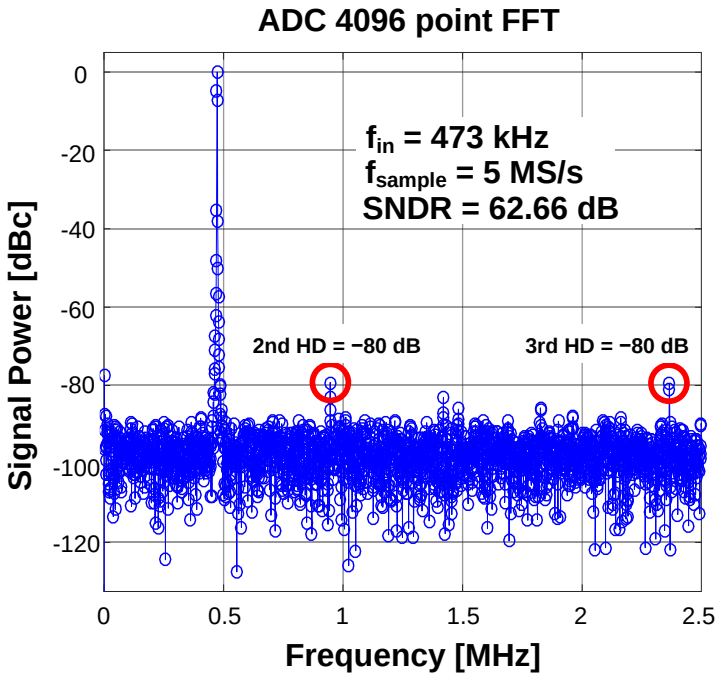

Figure 11. ADC output spectrum with 473 kHz input in stand-alone mode.

Table 1 shows a comparison table that summarizes the performance of our EIS SoC with recently published state-of-the-art EIS papers. Total power dissipation is 14 mW, where the receiver and the transmitter consume 9.2 mW and 4.8 mW, respectively. This level of power consumption is comparable with other state-of-the-art works. In addition, thanks to the sampling-mixed-based topology, our EIS SoC achieves the largest EIS frequency scan range of 1.25 MHz while achieving the highest peak dynamic range of 108 dB.

Table 1. Performance comparison table.

Features	This Work	ISSCC 18 [1]	ISSCC 17 [5]	ISSCC 18 [6]	JSSC 20 [17]
Technology	180 nm	180 nm	65 nm	130 nm	65 nm
Dynamic Range	**108 dB**	105 dB	94 dB	Unknown	76.32 dB
Power	14 mW	20.6 mW	6.69 mW	95 mW	9 mW
Operating Frequency Range	**1.25 MHz**	200 kHz	128 kHz	1 MHz	408 kHz
Frequency Tunability	Tunable	Tunable	Tunable	N/A	Tunable
ADC Structure	12-bit pipelined SAR	16-bit SAR	12-bit SAR	10-bit SAR	Not included

5. Conclusions

This paper presented an electrochemical impedance spectroscopy chip with a measured peak dynamic range of 108 dB. The sampling-mixer-based prototype EIS SoC not only achieves a high dynamic range but also covers a wide frequency scan range from 30 kHz to 1.25 MHz without a need for quadrature sinewaves. The on-chip tunable DDFS provides both in-phase and quadrature-phase clocks with minimal extra digital logic. Thanks to the clever clocking scheme in the sampler, the quadrature measurement is achieved using a single 5 MS/s, 12-bit pipelined SAR ADC. The built-in chopper within the sampling mixer-based receiver reduces possible low-frequency noise in the sampler and input-referred offset of the ADC. With many demonstrated advantages, we believe that the presented EIS architecture can be used universally in various EIS measurements, and this architecture should easily be scalable to a design that demands an EIS frequency scan range over 100 MHz.

Author Contributions: H.K., H.L. and J.K. proposed architecture; H.K. and H.L. designed and simulated the circuit; H.K. performed all measurements; H.K. wrote the draft of the manuscript and J.K. supervised the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Figure 1c shows the simple lock-in detection block diagram where $V_{in}(t)$ and $V_{ref}(t)$ are sinusoidal signals having the same frequency. The $V_{in}(t)$ is a signal whose amplitude (A_0) and phase (φ) are unknown, except for the angular frequency (ω). These two signals can then be expressed as

$$V_{in}(t) = A_0 \cdot \sin(\omega t + \varphi), \tag{A1}$$

$$V_{ref}(t) = A_r \cdot \sin(\omega t). \tag{A2}$$

Suppose that the $V_{in}(t)$ in (A1) passes through the gain of G. To detect the A_0 and φ output, we can multiply $V_{in}(t)$ by both the in-phase and quadrature-phase sinewave of $V_{ref}(t)$, which leads to

$$V_1(t) = \frac{1}{2} G A_0 A_r \{\cos(\varphi) - \cos(2\omega t + \varphi)\}, \tag{A3}$$

$$V_2(t) = \frac{1}{2} G A_0 A_r \{\sin(2\omega t + \varphi) + \sin(\varphi)\}. \tag{A4}$$

By applying low-pass filters to $V_1(t)$ and $V_2(t)$ individually and multiplying a scaling factor of $2/GA_R$, one can easily show that the outputs are given by

$$V_I = A_0 \sin(\varphi) \tag{A5}$$

$$V_Q = A_0 \cos(\varphi) \tag{A6}$$

Finally, by performing simple mathematical operations shown below, both the magnitude and phase of the $V_{in}(t)$ can be obtained, i.e.,

$$A_0 = \sqrt{V_Q^2 + V_I^2}, \tag{A7}$$

$$\varphi = \tan^{-1}\left(\frac{V_I}{V_Q}\right) \tag{A8}$$

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