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Performance Evaluation of SiC-Based Two-Level VSIs with Generalized Carrier-Based PWM Strategies in Motor Drive Applications

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Abstract: Currently, silicon carbide (SiC) MOSFETs are several times higher in cost than the equivalent silicon (Si)-IGBTs; however, the gains in power conversion efficiency, simplification of thermal management, and energy savings in general bring the advantages of lower total cost of ownership. The implementation of discontinuous PWM (DPWM) techniques for controlling the motor drive brings further reductions for the semiconductor switching losses; however, most existing techniques have limited performance on the optimized clamping region, particularly at a low power factor, which is a common operation condition for motor drives employing the widely used V/f control, particularly at partial- or low-load conditions. This paper evaluates the performance of a SiC-based two-level voltage-source inverter (2L-VSI) motor drive operated with generalized carrier-based PWM methods. Theoretical analysis and experimental measurements are conducted in a 2.2 kW heatsink-less 2L-VSI prototype and induction machine, which demonstrates that the minimum switching losses DPWM (MSL-DPWM) is the most favorable solution in practice in terms of the achievable power conversion efficiency and harmonic distortions and also produces the least common-mode current, which is critical in motor drives.

Keywords: silicon carbide (SiC); two-level voltage source inverters (2L-VSIs); carrier-based pulse width modulation; minimum switching losses discontinuous PWM (MSL-DPWM)

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1. Introduction

Three-phase two-level voltage source inverters (2L-VSIs) are undergoing fast development with wide-band-gap semiconductor devices, e.g., silicon carbide (SiC), for outstanding switching performance [1–5]. The remarkable benefits enabled by SiC semiconductors in motor drives include increased power efficiency and higher power density due to faster switching action, simplification in the semiconductor thermal management, and improvements on partial load energy savings when compared to the utilization of silicon (Si) devices, e.g., insulated-gate bipolar transistor (IGBT) and anti-parallel diodes [6,7].

Over the past decade, a growing industrial acceptance of the SiC technology has brought substantial operational metrics improvements; however, today, the cost of SiC MOSFETs can still be up to three- to five-times higher than that of the Si-IGBTs counterparts. Interestingly, the expected power efficiency gains, simplification of thermal management, and energy savings in general can bring marketing competitive advantages because of the achievable lower total cost of ownership (TCO) for the application user [8]. Thus, the SiC semiconductor technology can also be a suitable solution in cost-driven applications.

Several studies are available in the current literature, which presents guidelines for the converter design and the evaluation of the switching performance of SiC-based 2L-VSIs [9–17]. The results have shown that the SiC technology enables a 50–90% reduction in switching losses when compared to the implementation with Si-IGBTs counterparts [9].

A systematic evaluation of the switching performance of a SiC-based inverter for the induction machine drive was investigated in [11].

The power conversion efficiency of SiC MOSFET-based VSIs can be increased to 98.8% by using synchronous rectification [12]. A concise yet accurate second-order model of losses was proposed in [13] while considering the intrinsic parasitic components of the SiC MOSFET, which are meaningful for high-frequency applications. In [14], the design of a 2L-VSI using 1200-V 100-A SiC MOSFET was discussed and compared with Si IGBT-based 2L-VSI. Based on space vector PWM (SVPWM), a variable switching frequency modulation control was proposed in [15] to achieve zero voltage switching (ZVS) for a three-phase grid-connected SiC-based 2L-VSI with a unity power factor. The utilization of discontinuous PWM (DPWM) [18] for the online condition monitoring of SiC MOSFET at a high switching frequency was presented in [16]. The shaft voltage and its corresponding suppression methods were analyzed in [17].

Most of the aforementioned studies focused on the physical characteristics of the SiC devices as well as the performance improvements in terms of semiconductor losses and power density. Less attention has been paid to investigate other performance metrics that are important to both the 2L-VSI and the machine. Particularly, the influence of different PWM techniques to the overall performance of the motor drive system when the SiC semiconductor technology is employed has not been sufficiently researched.

In fact, previous studies on motor drives have concluded that, although the utilization of DPWM methods could achieve a considerable reduction of switching losses in power electronics converters [18–25], the machine harmonic losses mainly due to eddy currents in the stator become larger than those of continuous PWM methods, such as SVPWM. Therefore, there is always a compromise in the choice between the converter losses and current harmonic distortion [18].

However, in some machines, a higher switching frequency operation, enabled by the efficiency improvements with DPWM and/or the implementation of SiC semiconductors, can advantageously reduce eddy current losses [26]. This topic is somewhat less explored in the literature. Most importantly, in motor drive applications, most available publications studied the performance of 2L-VSIs based on Si IGBTs working at low switching-frequency [18,19,21,22], and limited works were found on the performance of SiC-based 2L-VSIs operating at high-frequency with different PWM strategies.

Additionally, the induction-motor-based drive system, which is widely used in industry due to its simplicity and cost savings [27,28], typically operates at partial load and a lower power factor with open-loop V/f control. This increases the 2L-VSI losses due to the higher circulating reactive power and will limit the switching losses reduction achieved by certain DPWM techniques because the optimum clamping region for the machine currents can become difficult to reach.

The contributions of this paper are listed as follows:

1. A new generalized implementation of carrier-based PWM strategy is presented where a modulation signal is generated through a unified form based on the zero-vector distribution. Different from the existing PWM methods in the literature [18,19], the proposed strategy is able to obtain the modulation signals without zero-sequence signal injection.
2. A comprehensive comparison of different performance characteristics in terms of conduction losses, switching losses, harmonic distortion, and common-mode current are investigated via both mathematical analysis and experimental evaluations.
3. The dynamic characteristics of a commercially available PCB surface-mounted SiC MOSFET is achieved through double pulse test (DPT) and the performance of a SiC-based 2L-VSI working at high switching-frequency is evaluated experimentally with an induction machine.
4. The significant issue of common-mode current in SiC-based 2L-VSI is discussed and compared between the continuous and discontinuous PWM methods operating at a high switching frequency.

The rest of the paper is divided as follows. In Section 2, the principles of a generalized carrier-based PWM are described and illustrated in detail. In Section 3, the performance characteristics of the 2L-VSI in terms of conduction and switching losses and harmonic distortion are investigated and compared via analytical models. Finally, in Section 4, a heatsink-less 2.2 kW VSI prototype and induction machine are used to evaluate the performance of the high-frequency SiC-based 2L-VSI with different carrier-based PWM strategies.

2. Generalized Carrier-Based PWM Strategies

A three-phase three-wire 2L-VSI circuit with connection to a three-phase AC motor is shown in Figure 1. Herein, the 2L-VSI is composed of six SiC MOSFETs and two series-connected DC capacitors C_{dc1} and C_{dc2}. In Figure 1, i_a, i_b, and i_c represent the output currents of the inverter, and V_{dc} is the DC-link voltage.

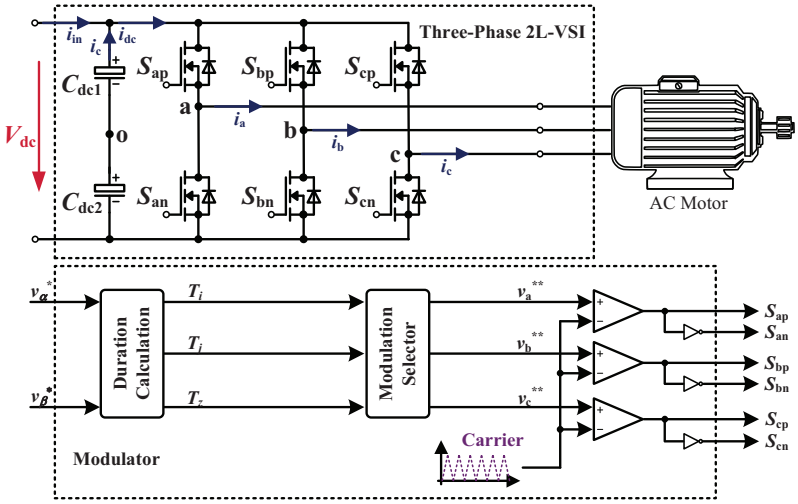

Figure 1. Circuit schematic of the three-phase three-wire 2L-VSI.

2.1. Implementation of Generalized Carrier-Based Modulations in a 2L-VSI

The space-vector technique-based modulation is obtained by suitably managing the inverter output voltage through the eight space vectors of the voltage associated with the eight available switching configurations. As an example in Figure 2, the vector space is divided into twelve sectors, and the space vector V_{ref} of the sampled reference voltage is synthesized by using the two nearest active voltage vectors $\mathbf{V}_1$(100) and $\mathbf{V}_2$ (110) and two zero voltage vectors $\mathbf{V}_0$ and $\mathbf{V}_7$ in one switching period T_s according to the following equations:

$$V_{ref} T_s = \mathbf{V}_1 T_1 + \mathbf{V}_2 T_2 \tag{1}$$

$$T_1 = \frac{\sqrt{3}}{2} m_i \sin(\frac{\pi}{3} - \omega_e t) T_s \tag{2}$$

$$T_2 = \frac{\sqrt{3}}{2} m_i \sin(\omega_e t) T_s \tag{3}$$

$$T_s = T_1 + T_2 + T_0 + T_7 \tag{4}$$

where T_1 and T_2 are the respective times of the applied vectors within the modulation period, and T_0 and T_7 are the times that are related to the application of zero vectors $\mathbf{V}_0$ and $\mathbf{V}_7$, respectively; and $m_i = 2|V_{ref}|/V_{dc}$ is the modulation index. The main difference of various PWM methods is the allocation of zero vectors $\mathbf{V}_0$ and $\mathbf{V}_7$, even if it can use only one of the available zero vectors. Then, as shown in Figure 3, three-phase duty cycles d_a, d_b, and d_c in the sector I are calculated as:

$$\begin{cases} d_{\mathrm{a}} = (T_0 \times 0 + T_1 \times 1 + T_2 \times 1 + T_7 \times 1)/T_s \\ d_{\mathrm{b}} = (T_0 \times 0 + T_1 \times 0 + T_2 \times 1 + T_7 \times 1)/T_s \\ d_{\mathrm{c}} = (T_0 \times 0 + T_1 \times 0 + T_2 \times 0 + T_7 \times 1)/T_s \end{cases} \tag{5}$$

The modulation waveforms v_{a}^{**}, v_{b}^{**}, and v_{c}^{**} that are set to be compared to the PWM carriers are obtained as:

$$\begin{cases} v_{\mathrm{a}}^{**} = 2d_{\mathrm{a}} - 1 \\ v_{\mathrm{b}}^{**} = 2d_{\mathrm{b}} - 1 \\ v_{\mathrm{c}}^{**} = 2d_{\mathrm{c}} - 1 \end{cases} \tag{6}$$

Generally, for each reference voltage V_{ref}, the selected sector and two nearest active voltage vectors $\mathbf{V}_i$ and $\mathbf{V}_j$, whose correspondingly switching states are (S_a^i, S_b^i, S_c^i) and (S_a^j, S_b^j, S_c^j), respectively, $(j > i, i = 12 \rightarrow j = 1)$ can be uniquely defined. A generalized representation for the duration of the two nearest active voltage vectors T_i and T_j in the nth sector of the hexagon in Figure 2 can be written as:

$$T_i = \frac{\sqrt{3}}{2} m_i \sin(l\frac{\pi}{3} - \omega_e t) T_s \tag{7}$$

$$T_j = \frac{\sqrt{3}}{2} m_i \sin[\omega_e t - (l-1)\frac{\pi}{3}] T_s \tag{8}$$

$$T_z = T_s - T_i - T_j \tag{9}$$

where $l = (n + |\sin\frac{n\pi}{2}|)/2$ is the coefficient in T_i and T_j.

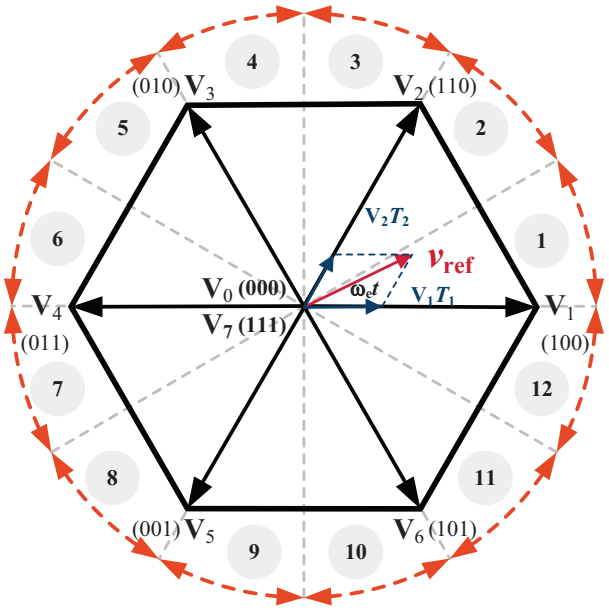

Figure 2. Voltage space vectors of the three-phase two-level VSI.

Different distributions of T_0 and T_7 will yield different PWM modulators, and the distribution of T_0 and T_7 is:

$$T_7 = kT_z \tag{10}$$

$$T_0 = T_z - T_7 \tag{11}$$

where T_z is the total duration of the action zero vectors, and $0 \leq k \leq 1$ is the allocation factor of the zero vectors. Thereafter, the modulation waveforms v_{a}^{**}, v_{b}^{**}, and v_{c}^{**} can be derived as:

$$\begin{bmatrix} v_{\mathrm{a}}^{**} \\ v_{\mathrm{b}}^{**} \\ v_{\mathrm{c}}^{**} \end{bmatrix} = \frac{2}{T_s} \begin{bmatrix} S_a^i & S_a^j & 1 \\ S_b^i & S_b^j & 1 \\ S_c^i & S_c^j & 1 \end{bmatrix} \begin{bmatrix} T_i \\ T_j \\ T_7 \end{bmatrix} - \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{12}$$

In (10), $k = 0.5$ yields the SVPWM with the maximum modulation index, $m_i = 1.15$ in the linear modulation range, where the distribution of T_7 and T_0 is equal. For all of the DPWM strategies, the value of k is varied between 0 and 1 based on the sector definition in Figure 4, where the sectors filled in gray are designated as $k = 1$, and in the remainder, are $k = 0$.

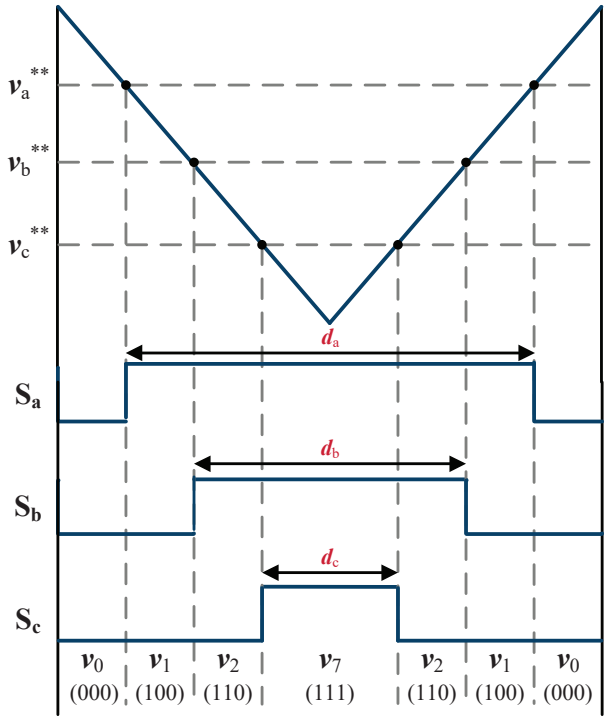

Figure 3. Three-phase duty cycles and vector duration in the sector I.

2.2. DPWMMAX and DPWMMIN

For DPWMMAX and DPWMMIN [19], each of the three legs of the inverter is held at high state or low state for 120° of the fundamental period. k for DPWMMAX in all twelve space-vector sectors is set as 1; while k for DPWMMIN in all twelve space-vector sectors is 0. The sector definitions and modulation waveforms of DPWMMAX and DPWMMIN are shown in Figure 4a and Figure 4b, respectively.

2.3. DPWM0, DPWM1, and DPWM2

DPWMx ($x \in \{0, 1, 2\}$) consists of clamping alternatively the upper switch and the lower switch, respectively, for 60° within a fundamental period [18]. DPWM1 has clamping at the voltage reference peaks; DPWM2 has the clamping phase-shifted by $-30°$ with respect to DPWM1; and DPWM0 has the clamping phase-shifted by $+30°$ with respect to DPWM1. The sector definitions and modulation waveforms of DPWMx are shown in Figure 4c, Figure 4d, and Figure 4e, respectively.

2.4. DPWM3

DPWM3 consists of four intervals of 30° clamping regions of each phase within a fundamental period [18]. The sector definitions and modulation waveforms are shown in Figure 4f.

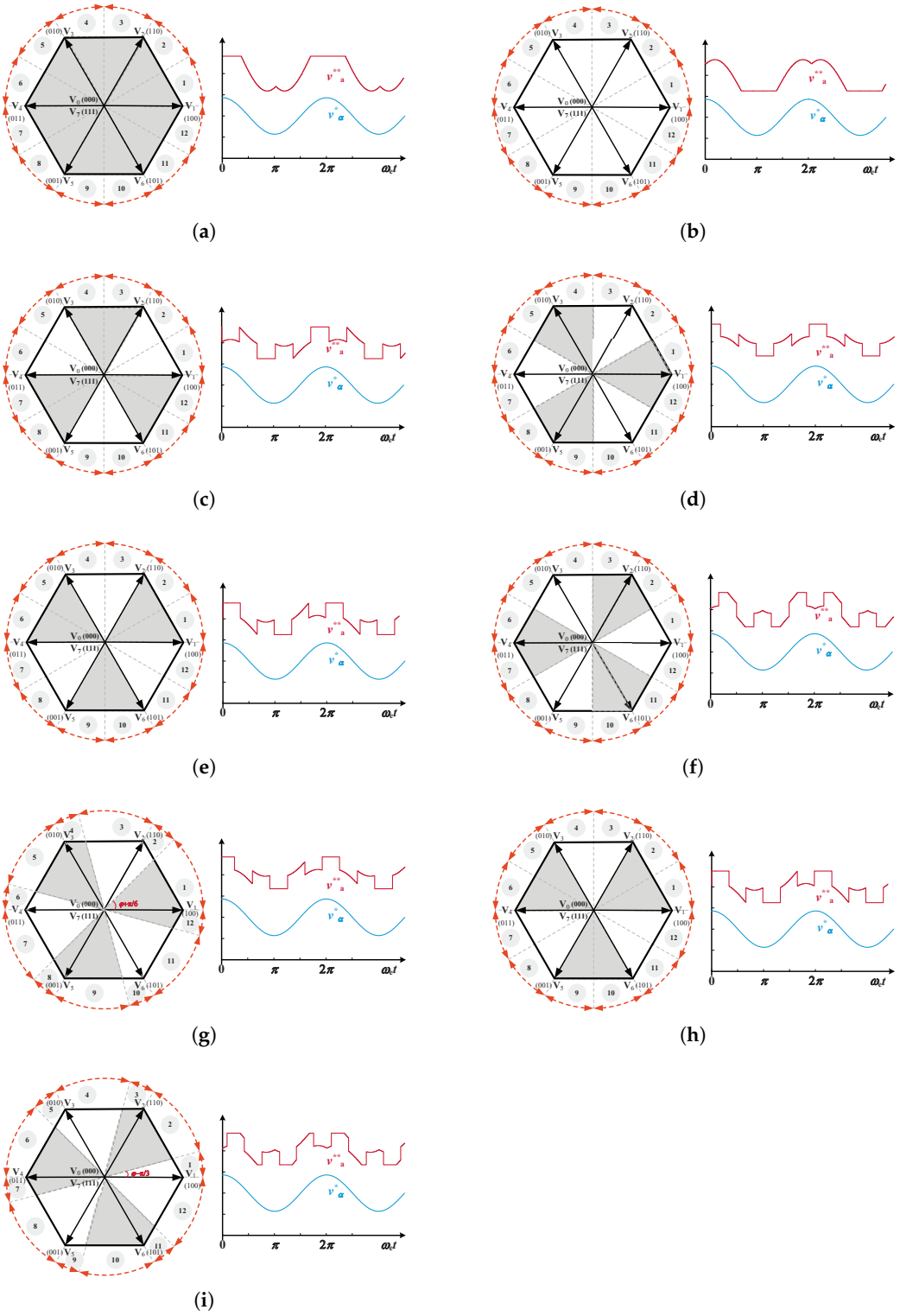

Figure 4. Modulation waveform of discontinuous carrier-based PWM (**a**) DPWMMAX, (**b**) DPWMMIN, (**c**) DPWM0, (**d**) DPWM1, (**e**) DPWM2, (**f**) DPWM3, (**g**) MSL-DPWM when $0 \leq \varphi \leq 30°$, (**h**) MSL-DPWM when $30° \leq \varphi \leq 60°$, and (**i**) MSL-DPWM when $60° \leq \varphi \leq 90°$. Note that the sectors filled in gray are designated as $k = 1$, while, in the remaining sectors, $k = 0$.

2.5. Minimum Switching Losses DPWM (MSL-DPWM)

This strategy implements the optimal DPWM strategies in terms of minimum switching losses based on the power factor angle φ (phase-shift of the phase voltage relative to

the phase current) to define the clamping phase in a fundamental period [20,22]. The sector definitions and modulation waveforms of MSL-DPWM in three different cases (only the main operating condition $0 \leq \varphi \leq 90^\circ$ is presented), are shown in Figure 4g–i. The power factor angle φ can be calculated with:

$$\varphi = \arccos\left(\frac{v_\alpha i_\alpha + v_\beta i_\beta}{\sqrt{v_\alpha^2 + v_\beta^2} \cdot \sqrt{i_\alpha^2 + i_\beta^2}}\right) \tag{13}$$

where v_α, v_β and i_α, i_β are the phase voltage and current in the $\alpha - \beta$ frame obtained through coordinate transformation. The generalized DPWM (GDPWM) studied in [18] can be regarded as the composition of MSL-DPWM when $0 \leq |\varphi| \leq 60^\circ$, DPWM0/2 when $60^\circ < |\varphi| \leq 75^\circ$, and DPWM3 when $75^\circ < |\varphi| \leq 90^\circ$. The DC-bus voltage utilization of the MSL-DPWM is the same as the SVPWM and other DPWM methods, i.e., $0 \leq m_i \leq 1.15$, because the active vectors applied in every sector are exactly the same.

3. Theoretical Analysis and Comparison

3.1. Conduction Losses

The power losses in the SiC MOSFET can be analytically calculated based on the assumption that the switching frequency f_s is much greater than the output fundamental frequency f_o in the machine. According to this assumption, the modulation waveforms can be regarded as a constant during one switching period.

The conduction losses in the SiC MOSFET with the function of the drain-source on-state resistance R_{mos} and the RMS value of the current flowing through its channel $I_{rms,m}$ is:

$$P_{con} = R_{mos} I_{rms,m}^2. \tag{14}$$

Assuming that the channel of the SiC MOSFET is used for reverse conduction and that the conduction of the MOSFET body-diode during the relatively small dead-time is neglected, the conduction losses can be analytically calculated as:

$$I_{rms,m} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_x^2(\omega_e t) d_x(\omega_e t) \mathrm{d}(\omega_e t)} = I_m/2 \qquad x \in \{a, b, c\} \tag{15}$$

where $d_x(\omega_e t)$ is the phase x duty cycle and I_m is the peak or maximum value of the corresponding phase current. Since the value of R_{mos} is temperature-dependent and I_m is in dependency with the load, different PWM methods have negligible effects on the conduction losses.

3.2. Switching Losses

For the theoretical calculation of the switching losses, a linear dependence of the switching energy losses on the amplitude of the fundamental phase current is assumed. The average switching power loss per device over a fundamental period can be defined as [19]:

$$P_{\mathrm{sw}} = \frac{V_{\mathrm{dc}}}{2\pi V_{\mathrm{b}}} f_s E_{\mathrm{on,off,rr}} \int_0^{2\pi} |i(\omega_e t)| \mathrm{d}\omega_e t \tag{16}$$

where $E_{\mathrm{on,off,rr}}$ represents a lumped switching losses per commutation for a specified DC voltage and output current; V_{b} is the DC reference voltage, which was used for measuring $E_{\mathrm{on,off,rr}}$; f_s represents the constant switching frequency of the devices; $i(\omega_e t)$ equals zero in the intervals where no switching occurs and is equal to the phase current otherwise. The switching loss function (SLF) of the traditional DPWM methods normalized to P_{sw} for SVPWM ($2V_{\mathrm{dc}} f_s I_m E_{\mathrm{on,off,rr}} / \pi V_{\mathrm{b}}$) can be found in [18,19] and, for the MSL-DPWM associated with φ, is derived as:

$$SLF_{\mathrm{MSL-DPWM}} = \begin{cases} \frac{1}{2} & 0 \le |\varphi| \le \frac{\pi}{6} \\ \frac{2+\sin(|\varphi|-\frac{2\pi}{3})}{2} & \frac{\pi}{6} < |\varphi| \le \frac{\pi}{3} \\ \frac{2-\sqrt{3}+\sin|\varphi|}{2} & \frac{\pi}{3} < |\varphi| \le \frac{\pi}{2}. \end{cases} \tag{17}$$

SLF for different DPWM methods are compared in Figure 5. We concluded that the MSL-DPWM method indeed achieves the minimum switching losses action over the entire φ range.

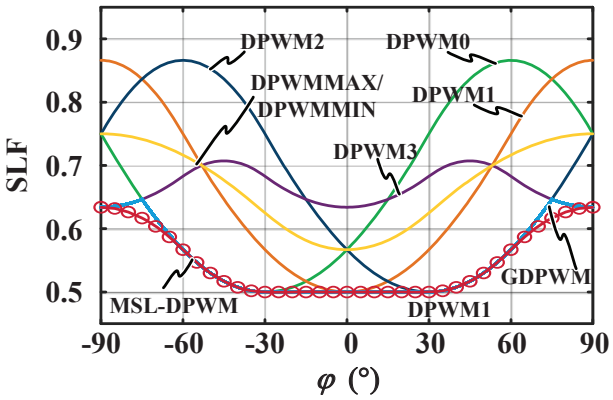

Figure 5. Switching loss functions of various DPWM methods.

3.3. Harmonic Distortion

The output current harmonic content of the VSI is proportional to the integral of its generated output voltage harmonics; hence, the performance of the output current can be investigated theoretically through harmonic flux trajectories [19]. The normalized harmonic flux vector λ_{hn} investigated in terms of the time integral of the harmonic voltage vector in a PWM cycle is shown in (18), where $\mathbf{V}_x$ is the applied voltage vector.

$$\lambda_{\mathrm{hn}}(m_i) = \frac{\pi}{V_{\mathrm{dc}} T_{\mathrm{s}}} \int_0^{T_{\mathrm{s}}} (\mathbf{V}_x - V_{\mathrm{ref}}) \mathrm{d}t \qquad x \in \{0, 1, 2 \cdots 7\} \tag{18}$$

Due to different constructions of V_{ref} in every switching period, the harmonic flux trajectories of the different PWM modulators are various. The RMS harmonic flux $\lambda_{\mathrm{hn-rms}}$ over a PWM cycle and harmonic distortion factor (HDF) [18,19] are given as follows:

$$\lambda_{\mathrm{hn-rms}}(m_i) = \sqrt{\int_0^1 \lambda_{\mathrm{hn}}^2 \mathrm{d}d} \tag{19}$$

$$\mathrm{HDF} = f(m_i) = k_{\mathrm{f}}^2 \times \frac{288}{2\pi^3} \int_0^{2\pi} \lambda_{\mathrm{hn-rms}}^2 \mathrm{d}\omega_e t \tag{20}$$

The square-rms harmonic flux is scaled with k_{f}^2, where k_{f} is the f_s coefficient. k_{f} for SVPWM is 1 and, for the DPWM methods, is decided by the ratio of the f_s of SVPWM to that of DPWM, which depends on the pre-conditions of the comparison. If DPWM methods are compared with SVPWM under the same f_s, k_{f} should be set to 1; if DPWM methods are compared with SVPWM under the same switching losses, k_{f} should be set as the value of SLF as determined in Figure 5. The HDF polynomial functions of the traditional DPWM methods can be found in [18], and the one of the MSL-DPWM method as a function of φ and m_i can be derived as follows:

$$\mathrm{HDF} = \begin{cases} k_f^2 \times \mathrm{HDF}_1 & 0 \le |\varphi| < \frac{\pi}{6} \\ k_f^2 \times \mathrm{HDF}_1 \,|\varphi = \frac{\pi}{6} & \frac{\pi}{6} \le |\varphi| < \frac{\pi}{3} \\ k_f^2 \times \mathrm{HDF}_2 & \frac{\pi}{3} \le |\varphi| \le \frac{\pi}{2} \end{cases} \tag{21}$$

$$\mathrm{HDF}_1 = (\frac{27}{8} - \frac{81\sqrt{3}}{32\pi} + \frac{81\sqrt{3}\cos^2\varphi}{8\pi} - \frac{27\sqrt{3}\cos^4\varphi}{4\pi})m_i^4 - (\frac{4\sqrt{3}}{\pi} + \frac{81\cos\varphi}{2\pi} - \frac{18\cos^3\varphi}{\pi})m_i^3 + 6m_i^2 \tag{22}$$

$$\mathrm{HDF}_2 = (\frac{27}{8} - \frac{27\sqrt{3}}{16\pi} - \frac{27\sqrt{3}\cos^2\varphi}{8\pi} + \frac{27\sqrt{3}\cos^4\varphi}{4\pi})m_i^4 - (\frac{31\sqrt{3}}{\pi} - \frac{45\sin|\varphi|}{2\pi} - \frac{18\cos^2\varphi\sin|\varphi|}{\pi})m_i^3 + 6m_i^2 \tag{23}$$

With the help of the HDF function, the characteristic of the MSL-DPWM at $k_f = 1$ is plotted in Figure 6, and different PWM methods are compared in Figure 7. In Figure 7a, $k_f = 1$ for each DPWM method, i.e., comparison under the same f_s, while $k_f = SLF_{\max}$ (the worse switching losses performance) in Figure 7b. In Figure 7, the values of HDF for MSL-DPWM with different φ are all contained within the red area. A small HDF will lead to a lower ripple with the same filter size or a smaller output filter size for the same current ripple value.

The HDF characteristic of the SVPWM is better than that for all of the other DPWM methods at $k_f = 1$, and its advantage will be decreased in the high m_i range. Moreover, in Figure 7b, under equivalent switching losses, the HDF of the DPWM methods is superior to the one of the SVPWM in the high m_i range, and it is shown that the MSL-DPWM achieves a better harmonic distortion compared with the other DPWM methods. Therefore, the MSL-DPWM method is promising, particularly at high m_i ranges.

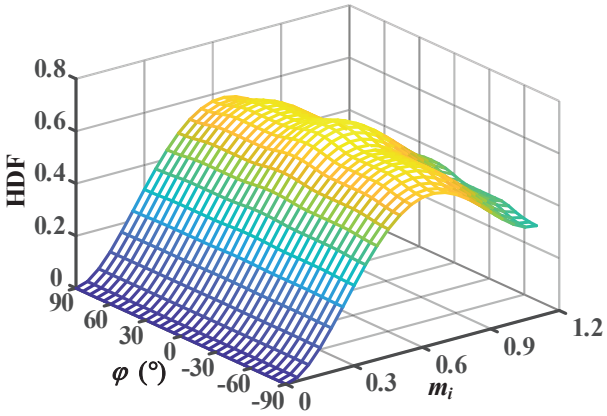

Figure 6. The harmonic distortion factor, HDF, characteristic of the MSL-DPWM at $k_f = 1$.

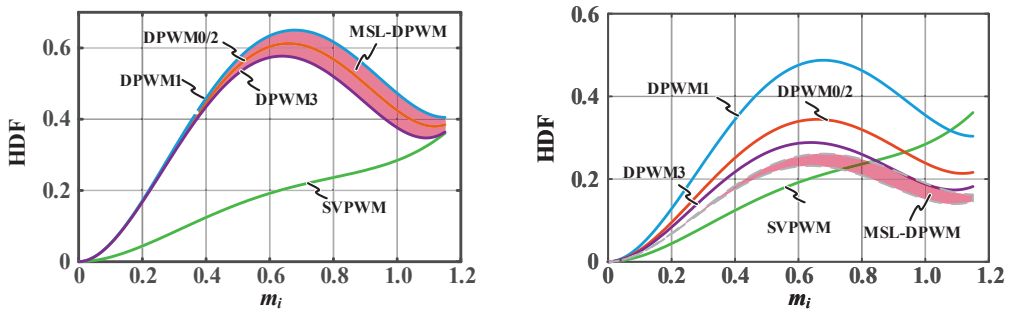

Figure 7. Comparison of the harmonic distortion factor, HDF, with different PWM methods (**a**) at $k_f = 1$ and (**b**) at $k_f = SLF_{max}$.

4. Experimental Evaluation and Discussion

Based on the mathematical model in Section 3, It can be seen that the MSL-DPWM strategy has the ability to achieve the minimum switching losses while displaying a better overall performance than other DPWM methods in terms of the harmonic distortion. Therefore, in Section 4, only the MSL-DPWM is considered to represent the DPWM methods and to be compared with SVPWM.

For experimental evaluation, the implemented SiC-based two-level VSI setup is shown in Figure 8. The generalized carrier-based PWM strategies were operated on a Texas Instruments digital signal processor (DSP) TMS320F28379D. The 900V voltage class PCB surface-mounted SiC MOSFET from Wolfspeed C3M0120090J [29] was selected for the VSI, and a 2.2 kW, 380 V, four-pole, 1400 r/min induction machine was selected as the load for the SiC-based 2L-VSI.

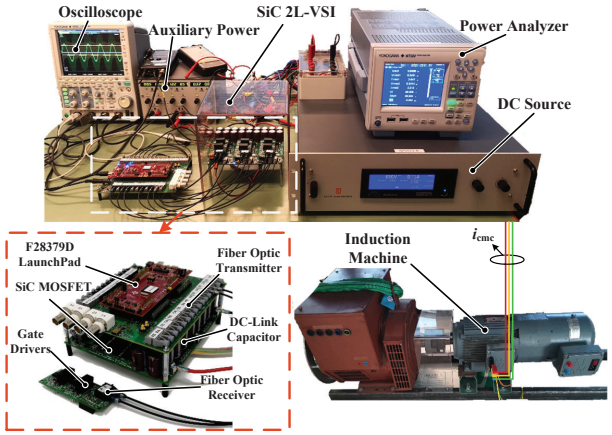

Figure 8. The experimental setup.

4.1. Double Pulse Test

To evaluate the switching characteristics of the selected SiC MOSFET and to obtain a better understanding of the losses on the SiC MOSFET, a double pulse test (DPT) was conducted in a phase-leg of the VSI. An inductor with 720 µH was used as the inductive load; the current was measured by a YOKOGAWA current probe 701933 (30 A, 50 MHz). The experimental testing waveforms at i_{ds} = 15 A, v_{ds} = 600 V, and gate resistor R_g = 10 Ω.

The overlap regions between the voltage and current during the turn-on and turn-off periods can be calculated as the energy power loss of the SiC MOSFET E_{off}, E_{on}, and E_{rr}. The switching energy losses corresponding to the selected C3M0120090J SiC MOSFET device were measured experimentally and compared with the values derived from the manufacturer data-sheet, which is scaled to the same v_{ds} and R_g values [29] as shown in Figure 9. Although there exist differences in E_{on}, E_{off}, and E_{rr} between the measured results

and datasheet values due to the differences in the hardware circuit, e.g., the gate driver and PCB layout (e.g., the parasitic inductance within the commutation loop), the total measured and data-sheet derived energy curves, E_{total}, are equivalent.

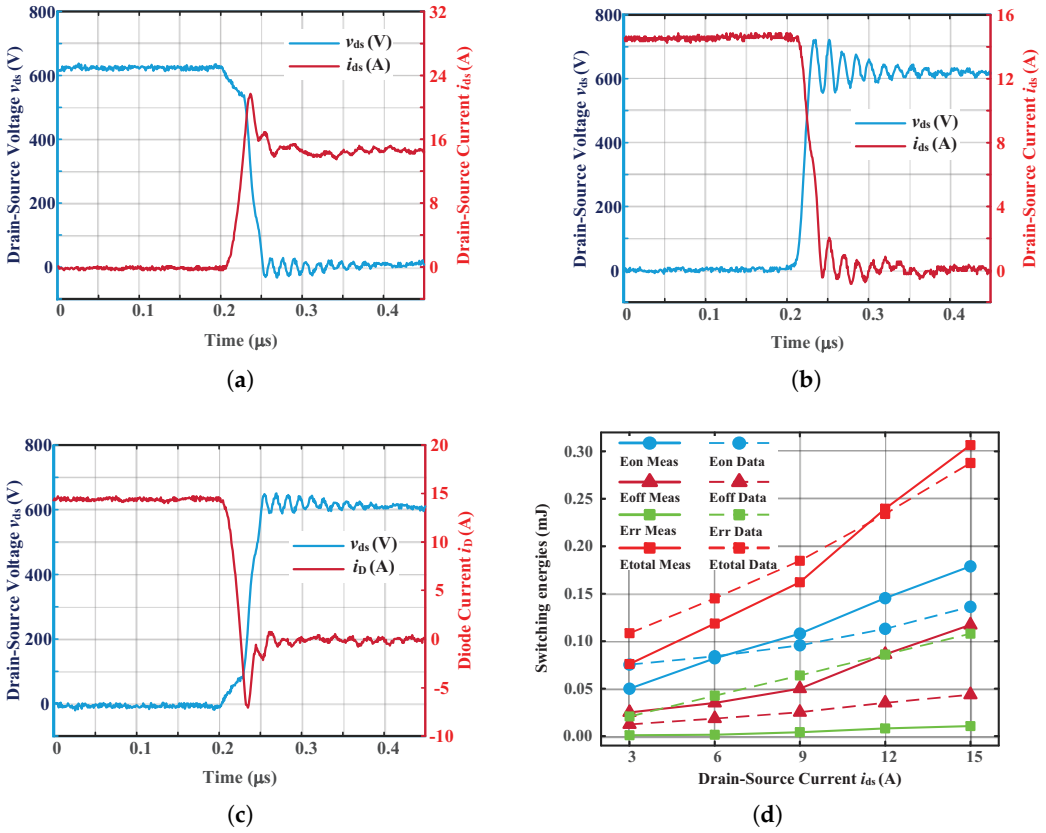

Figure 9. Switching characteristics of a phase-leg at $v_{\text{ds}} = 600$ V and $R_{\text{g}} = 10\ \Omega$ (**a**) turn-on transient, (**b**) turn-off transient, (**c**) anti-parallel diode reverse recovery transient, and (**d**) relationship between the switching energy and load current.

4.2. Steady-State Output Waveforms

The steady-state experimental waveforms of the gate signal S_{a}, phase output current i_{a}, common-mode current (CMC) i_{cmc} and the modulation waveform of the phase voltage v_a^{**} with SVPWM and MSL-DPWM methods at different load conditions are shown in Figure 10. The CMC and output current were tested with a Pearson current sensor 110 with a 20 MHz bandwidth. The open-loop V/f control method is employed. The DC voltage is fixed at 650 V, and the switching frequency f_s is 10 kHz. The detailed operation points are presented in Table 1, where two modulation indices m_i are selected with three different loads. It can be seen that all operating points of the machine are working at a high power factor angle ($\varphi > 60°$), which means that the DPWM methods studied in [18] cannot achieve the minimum switching losses.

The modulation waveforms of the MSL-DPWM are adjusted based on the power factor angle φ, which can be calculated from (13), and the switching signal is clamped during a third of the fundamental waveform. As shown in Figure 10, the phase currents are always sinusoidal, and the PWM current ripple is small and comparable in both methods. Therefore, it can be concluded that, due to the high f_s and large inductance in the machine, the influence of different PWM methods on the harmonic distortion is limited.

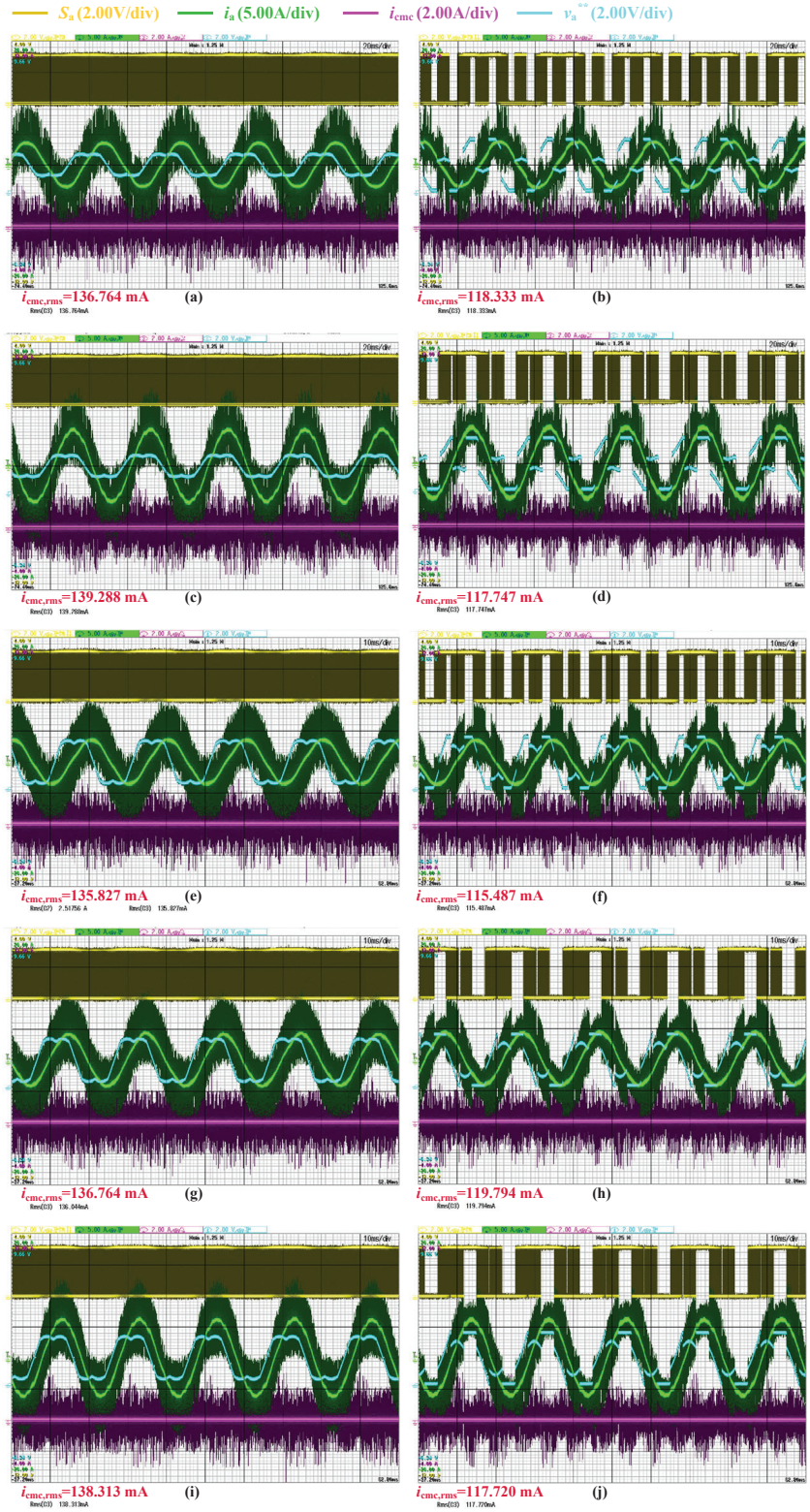

Figure 10. Steady−state output waveforms with SVPWM and MSL-DPWM methods at f_s = 10 kHz with different operating conditions: (**a**) SVPWM at f_o = 25 Hz and no load, (**b**) MSL-DPWM at f_o = 25 Hz and no load, (**c**) SVPWM at f_o = 25 Hz and half load, (**d**) MSL-DPWM at f_o = 25 Hz and half load, (**e**) SVPWM at f_o = 50 Hz and no load, (**f**) MSL-DPWM at f_o = 50 Hz and no load, (**g**) SVPWM at f_o = 50 Hz and half load, (**h**) MSL-DPWM at f_o = 50 Hz and half load, (**i**) SVPWM at f_o = 50 Hz and full load, and (**j**) MSL-DPWM at f_o = 50 Hz and full load.

Table 1. Operation conditions.

V/f	Load	Modulation Index (m_i)	Phase Angle (φ)
190 V/25 Hz	No	0.48	85°
	Half	0.48	70°
380 V/50 Hz	Half	0.95	69°
	Full	0.95	61°

4.3. Current THD

The comparisons of the current total harmonic distortion (THD) are presented in Figure 11a,b. The results were calculated with the software MATLAB 2020a with the data collected from the oscilloscope (YOKOGAWA DLM2034), where harmonic components up to 1 MHz were considered. We found that, with the increment of f_s, the current THD of both PWM methods reduced as expected. Moreover, at higher output frequency and high output load, i.e., high m_i, the difference in the current THD between SVPWM and MSL-DPWM was smaller—as predicted in Figure 7a.

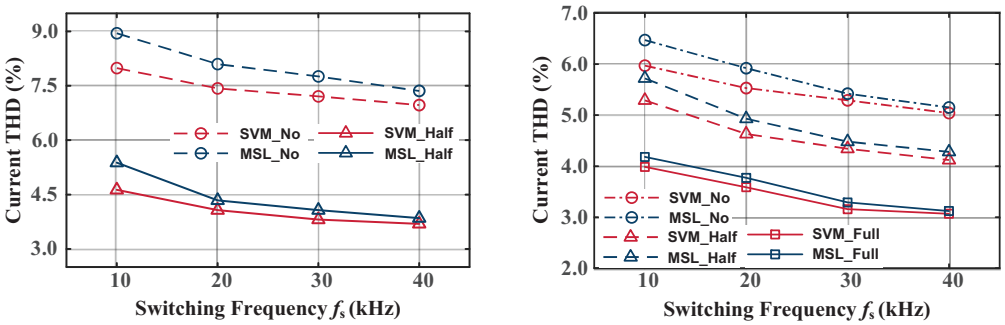

Figure 11. Comparison of current THD: (**a**) current THD at f_o = 25 Hz with no and half load and (**b**) current THD at f_o = 50 Hz with no, half, and full load, respectively.

4.4. Power Losses and Efficiency

Based on the dynamic characterization of the selected SiC MOSFET, the second-order curve fitting expressions for the calculation of switching energies for E_{off}, E_{on}, and E_{rr} can be found in (24)–(26) (in mJ). The comparisons of the calculated losses with two different PWM methods are shown in Figure 12. It can be seen that there is only a slight difference in the conduction losses, which is mainly due to the different current harmonics. The switching losses of the MSL-DPWM are lower than those of the SVPWM, and follows a linear dependency with f_s. With the increase in f_s, there is no substantial difference in the semiconductor conduction losses, nor in the losses of the DC-link capacitors (the equivalent series resistance (ESR) of the selected electrolytic capacitors is constant to current harmonics above 10 kHz); however, the advantage of the MSL-DPWM in switching losses was distinct.

$$E_{\text{off}} = \frac{V_{\text{dc}}}{600}\left(-4.3\times10^{-5}i_{\text{ds}}^2 + 8.4\times10^{-3}i_{\text{ds}}\right)(\text{mJ}) \tag{24}$$

$$E_{\text{on}} = \frac{V_{\text{dc}}}{600}\left(-3.9\times10^{-4}i_{\text{ds}}^2 + 1.78\times10^{-2}i_{\text{ds}}\right)(\text{mJ}) \tag{25}$$

$$E_{\text{rr}} = \frac{V_{\text{dc}}}{600}\left(3.11\times10^{-5}i_{\text{ds}}^2 + 2.4\times10^{-4}i_{\text{ds}}\right)(\text{mJ}) \tag{26}$$

The comparison of the efficiency as measured by the power analyzer YOKOGAWA WT500 is shown in Figure 13, where, for each operating point, the efficiency attained with the MSL-DPWM is higher than that for SVPWM, and the difference in efficiency becomes larger as the switching frequency increases. Therefore, from the perspective of

efficiency, MSL-DPWM is more favorable than SVPWM for a 2L-VSI operating with a high switching frequency.

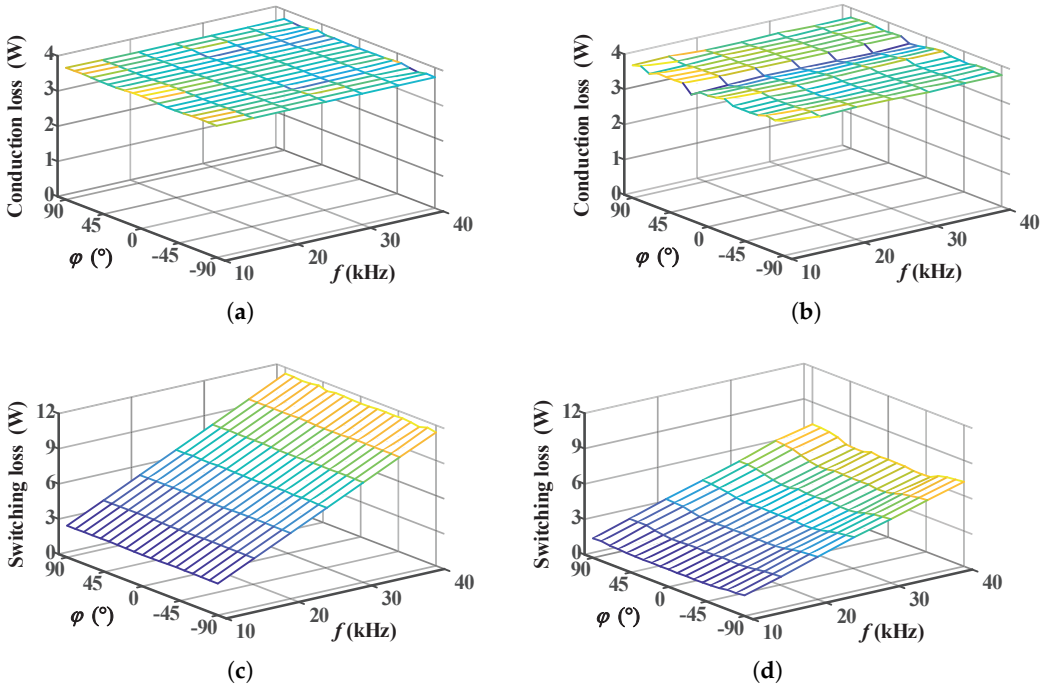

Figure 12. The calculated losses benchmark, (**a**) conduction losses for SVPWM, (**b**) conduction losses for MSL-DPWM, (**c**) switching losses for SVPWM, and (**d**) switching losses for MSL-DPWM.

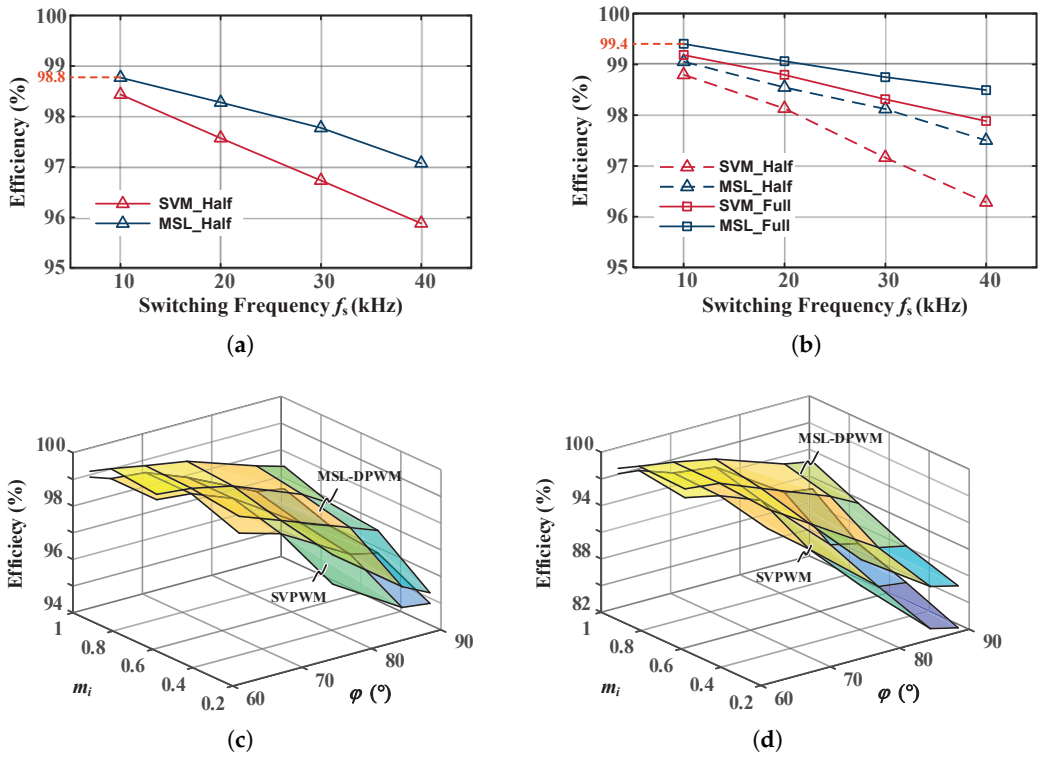

Figure 13. Comparison of the measured efficiency: (**a**) at f_o = 25 Hz with half load, (**b**) at f_o = 50 Hz with half and full load, (**c**) a 3D plot of the efficiency with various modulation indices and the power factor at f_s = 10 kHz, and (**d**) a 3D plot of the efficiency with various modulation indices and the power factor at f_s = 40 kHz.

The 3D plots of efficiency comparisons at various modulation indices and the power factor angle at f_s = 10 kHz and f_s = 40 kHz are presented in Figure 13a and Figure 13b, respectively, where $m_i = 0.22, 0.48, 0.72, 0.95$ are considered with different load conditions, i.e., the V/f controller is operating at 95 V/12.5 Hz, 190 V/25 Hz, 285 V/37.5 Hz, and 380 V/50 Hz. The efficiency of both SVPWM and MSL-DPWM are increased with the operations with a higher modulation index and power factor because both less circulating reactive power (smaller I_m) and a lower current THD will exist.

4.5. Common-Mode Current

The main experimental waveforms at 40 kHz are shown in Figure 14. It can be seen that the CMC and the noise on the output phase current at 40 kHz are higher than those at 10 kHz as shown in Figure 10.

The comparison of CMC at different operating points is given in Figure 15. It can be seen that, in the motor drive, the modulation methods and f_s have a large effect on CMC, while the operating conditions of the machine have little influence. The CMC noise contains current spikes closely associated with the dv/dt of the common-mode voltage [30], which can be expressed as:

$$v_{\mathrm{cmv}} = \frac{v_{\mathrm{ao}} + v_{\mathrm{bo}} + v_{\mathrm{co}}}{3} \tag{27}$$

where $v_{\mathrm{ao}}, v_{\mathrm{bo}}, v_{\mathrm{co}}$ represent the output phase to DC neutral point voltages and take values of $\pm V_{\mathrm{dc}}/2$. With SVPWM, the peak-to-peak value of the common-mode voltage is V_{dc} in every switching period, while, for the MSL-DWPM, the peak-to-peak value of the common-mode voltage is $2V_{\mathrm{dc}}/3$ in every switching period so that the dv/dt of the common-mode voltage can be decreased [31]. Therefore, the CMC noise in the time domain of the MSL-DPWM is lower when compared to the SVPWM case.

The FFT analysis of the CMC from 5 kHz to 20 MHz is provided in Figure 16. The results were calculated using MATLAB 2020a with the data collected from an oscilloscope with a 250 MHz sampling rate. For each f_o, the harmonic component of the SVPWM at f_s = 40 kHz was the highest, and that of the MSL-DPWM at f_s = 10 kHz was the lowest, and these results also verify the conclusion obtained in Figure 15a,b.

4.6. Discussion

Based on the experimental results, with the SiC MOSFET applied, the f_s can be considerably increased without overly compromising the system power efficiency. The issue of current harmonic distortion of SiC-based high-frequency 2L-VSIs is not as significant as in low f_s applications. However, the common-mode current will be more severe at high f_s, and a suitable common-mode filter may needed to be employed in the SiC-based high-frequency 2L-VSIs to overcome the possible degradation of the machine insulation, which may shorten this component's lifetime.

Furthermore, the study demonstrated that the MSL-DPWM strategy implemented in this paper is advantageous in relation to the widely employed SVPWM. The use of MSL-DPWM leads to higher power efficiency and, above all, smaller circulating CMC. The later is particularly critical for the machine's lifetime since the high frequency CMC may degrade stator winding insulation and accelerate the wear of bearings. This occurs because the CMC generated by the VSI generated common-mode voltage will cause bearing currents to flow through the motor parasitic capacitors to the rotor iron, i.e, from the bearings to the grounded stator cases [32]. This will increase the thermal stresses on the stator winding and the bearing, thereby, reducing the insulation lifetime [33].

Therefore, with a high switching frequency applied, different PWM methods on SiC-based 2L-VSI have lesser impacts on the harmonics distortions, and greater attention should be paid to the issues caused by circulating CMC. MSL-DPWM is more favorable for SiC-based 2L-VSIs in practice for the improved power efficiency and lower CMC.

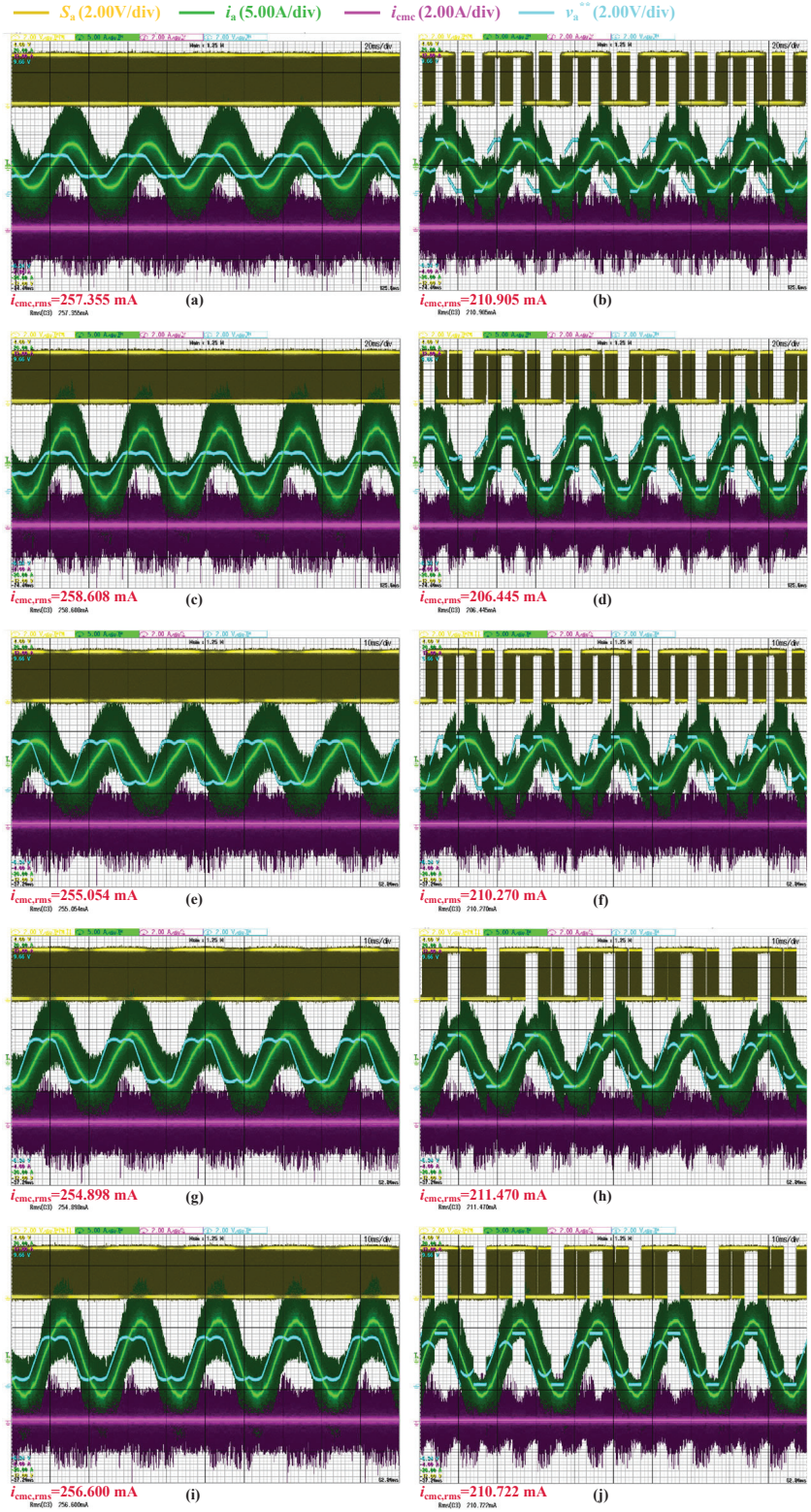

Figure 14. Output waveforms at f_s = 40 kHz: (**a**) SVPWM at f_o = 25 Hz and no load, (**b**) MSL-DPWM at f_o = 25 Hz and no load, (**c**) SVPWM at f_o = 25 Hz and half load, (**d**) MSL-DPWM at f_o = 25 Hz and half load, (**e**) SVPWM at f_o = 50 Hz and no load, (**f**) MSL-DPWM at f_o = 50 Hz and no load, (**g**) SVPWM at f_o = 50 Hz and half load, (**h**) MSL-DPWM at f_o = 50 Hz and half load, (**i**) SVPWM at f_o = 50 Hz and full load, and (**j**) MSL-DPWM at f_o = 50 Hz and full load.

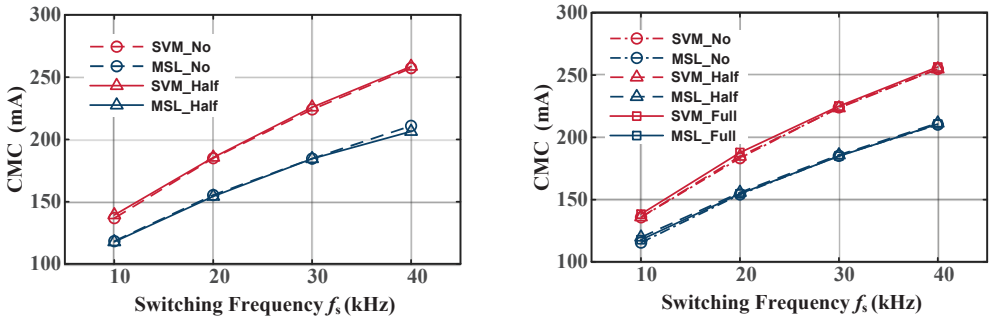

Figure 15. Comparison of the current THD: (**a**) current THD at f_o = 25 Hz with no and half load and (**b**) current THD at f_o = 50 Hz with no, half, and full load, respectively.

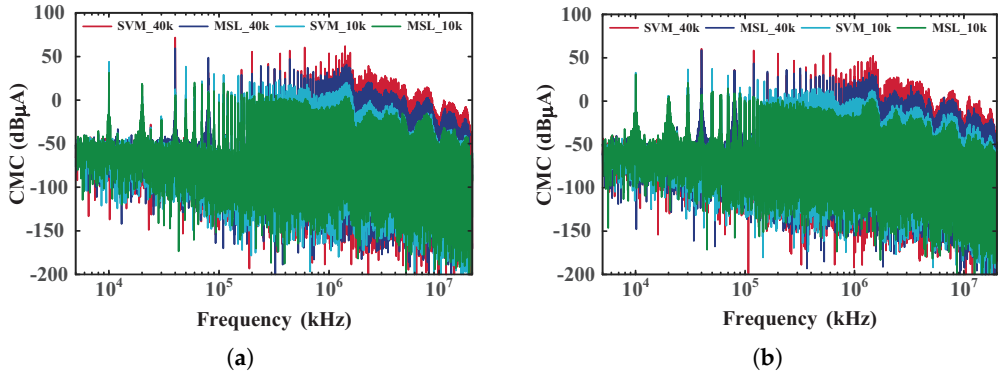

Figure 16. FFT analysis (**a**) at f_o = 25 Hz with half load and (**b**) at f_o = 50 Hz with full load.

5. Conclusions

This paper evaluated the performance of a SiC-based 2L-VSI operating at a high switching frequency with a new generalized carrier-based PWM method. First, The carrier-based PWM methods were described and illustrated through a generalized approach and model. Thereafter, the characteristics of the different PWM methods were investigated and compared through mathematical analysis. Finally, detailed experiments were performed in a heatsink-less 2.2 kW VSI prototype and induction machine. We found that the MSL-DPWM strategy was more favorable for SiC-based 2L-VSIs in practice in motor-drive applications because it was able to achieve higher efficiency, acceptable current distortion, and smaller CMC when compared to the commonly employed SVPWM method.

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