electronics

MDPI

Article

Analog Frontend for Reliable Human Body Temperature Measurement for IoT Devices

Paweł Narczyk * and Witold Adam Pleskacz

Institute of Microelectronics & Optoelectronics, Warsaw University of Technology, ul. Nowowiejska 15/19, 00-665 Warsaw, Poland; witold.pleskacz@pw.edu.pl
* Correspondence: p.narczyk@imio.pw.edu.pl

Abstract: In this paper an analog frontend for a reliable measurement of the human body temperature is presented. A new and novel temperature calibration technique using an on-chip resistor was developed specifically for the analog frontend. The discussed analog frontend consists of a bandgap current reference, a precision current source, a programmable gain amplifier, a voltage source proportional to absolute temperature and an on-chip calibration resistor. The developed calibration technique enables very high accuracy, even 0.1 °C, to be obtained in a very wide temperature range. This calibration method was elaborated for integrated circuits operating in temperatures from −40 °C to +125 °C. The presented analog frontend consumes no more than 185 µA and was designed and manufactured with United Microelectronics Corporation (UMC) CMOS 130 nm technology. The data presented in the paper were obtained from process corner and Monte Carlo simulations as well as from measurements. The measurements were taken using a manual wafer prober with climate-controlled microchamber, at temperatures ranging from −40 °C to +125 °C.

Keywords: biomedical circuits and systems; human body temperature measurement; analog frontend; temperature calibration; physical sensors; sensor interface; sensing systems; IoT

Citation: Narczyk, P.; Pleskacz, W.A. Analog Frontend for Reliable Human Body Temperature Measurement for IoT Devices. *Electronics* **2022**, *11*, 434. https://doi.org/10.3390/electronics11030434

Academic Editor: Yunho Jung

Received: 14 December 2021
Accepted: 29 January 2022
Published: 31 January 2022

1. Introduction

Currently, we are observing an increasing demand for health monitoring mobile devices. This demand is driven by many different factors such as ageing societies, the need for monitoring people working in extremely difficult conditions or in remote and inaccessible locations, monitoring people responsible for other people's lives (e.g., pilots, drivers, firefighters, police officers and soldiers) or just the increased popularity of healthy lifestyles. The ability to remotely monitor various vital signs, including human body temperature, makes it possible to determine the current psychophysical state. Therefore, any necessary medical assistance can be provided on time, which could save lives in extreme cases [1,2].

This work presents an entire analog frontend (AFE) for reliable measurement of human body temperature. The developed temperature calibration technique uses an on-chip resistor and enables very high accuracy to be achieved in a very wide temperature range. This calibration method was elaborated for integrated circuits (ICs) operating at temperatures varying from −40 °C to +125 °C. This unique feature makes the AFE operational in any possible weather conditions and suitable for integration with powerful microprocessors in SoC (system on chip) structures. Currently, processors can generate huge amounts of heat and therefore heat up a silicon body. The data presented in this paper were obtained from process corner and Monte Carlo simulations as well as from measurements. Measurements were taken using a manual wafer prober with climate control microchamber, at temperatures ranging from −40 °C to +125 °C.

In this paper, a summary of two research projects is presented. The results were obtained from designing, manufacturing and characterizing two highly integrated systems-on-chip for dynamic acquisition and processing the most important human physiological

parameters: BioChip [1] and BioSoC [2]. Some of the research results (methodology, simulation results and preliminary measurement results) were previously presented at the scientific conferences DDECS and MIXDES and were published as conference proceedings papers [3–5], respectively. This work, in addition to the consolidated, comprehensive, and entire study, has been extended with additional measurement results of manufactured integrated circuits (from additional wafers of another production lot).

Section 2 gives a brief overview of the method to measure human body temperature and explains why it was necessary to develop a new approach to temperature calibration. Having reviewed the key aspects of the measurement of human body temperature, Section 3 presents the entire analog frontend. Section 4 describes the developed temperature calibration technique in more detail and presents process corner and Monte Carlo simulations of human body temperature measurement with and without this technique. Section 5 provides measurement results of all the designed analog blocks. Final conclusions are presented in Section 6.

2. Thermistor Sensor

In dynamic conditions (when a person is in constant movement), or in the case of people who require continuous temperature monitoring, one of the best ways to measure human body temperature is to use a thermistor sensor. The resistance of a thermistor changes noticeably with ambient temperature. The sensor is attached to human skin and the measurement is performed with the assumption that the temperatures of the thermistor and skin are the same. An external thermistor is connected to an IC through wiring imprinted into the fabric and then through a special connector on PCB. The whole chip is integrated with textronic clothes. A sample curve of a negative temperature coefficient (NTC) thermistor is presented in Figure 1.

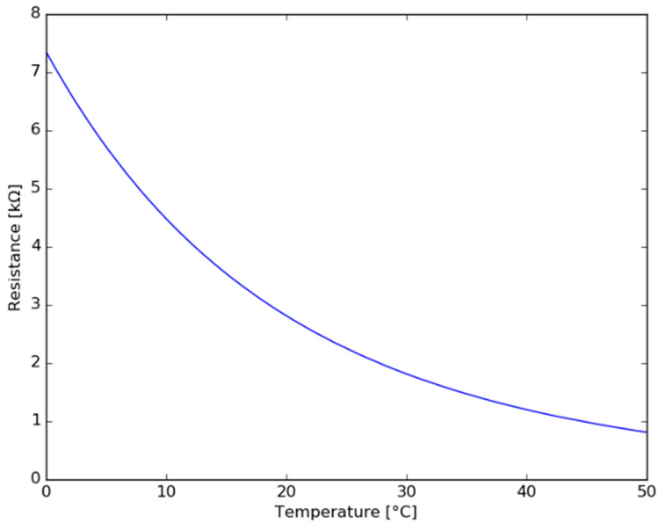

Figure 1. A sample thermistor curve.

Human body temperature will be measured in the range between +25 °C and +45 °C. The resistance of the thermistor changes from about 980 Ω to about 2250 Ω. Table 1 presents detailed, worst-case information about the discussed thermistor. This information is crucial because it determines the accuracy of the whole analog frontend.

Table 1. Detailed thermistor values.

Temperature [°C]	Resistance R [Ω]	Difference between Current and Previous R [Ω]	Difference between Current and Previous R [%]
39.6	1219	-	-
39.7	1215	4	0.33
39.8	1210	5	0.41
40.0	1190	-	-
40.1	1186	4	0.34
40.2	1181	5	0.42

The data shown in Table 1 demonstrate clearly that the measurement of human body temperature with 0.1 °C precision requires the voltage across the thermistor to be measured with very high accuracy (better than 0.5% in the worst case). This accuracy is defined by the values presented in the fourth column of Table 1. The sum of all potential measurement errors resulting from the temperature and supply voltage instability, reference current and gain mismatch or noise has to be lower than the presented values. While process corners and mismatches can be easily calibrated, the temperature drift cannot. The presented data highlight the importance of the low temperature coefficient of the whole AFE. Assuming that the whole measurement error is caused by the current reference only, and the rest of the AFE is ideal, the bandgap current reference temperature coefficient has to be better than 35 ppm/°C.

As shown in Table 2, a number of previous studies have demonstrated that it is almost impossible to design a bandgap current reference with such a small temperature coefficient in such a wide temperature range. Only the last result is better than the required one, but in a narrower temperature range and in BiCMOS technology. In today's CMOS technologies, there is a growing problem with the temperature stability of integrated circuit parameters, especially in the case of a very wide range of operation temperatures. In the high temperature range, the leakage current increases rapidly. On the other hand, in the low temperature range the threshold voltage increases quickly with decreasing temperature. Bandgap reference is not always the answer to these problems. In some cases, temperature calibration performed in the digital domain is a better solution.

Table 2. Bandgap current reference temperature coefficients.

Reference	CMOS Technology [µm]	Temperature Range [°C]	Temperature Coefficient [ppm/°C]
[6]	-	0 ÷ 75	226
[7]	0.5	0 ÷ 80	130
[8]	0.5	−20 ÷ 120	158
[9]	0.35	0 ÷ 80	44
[10]	0.25	−40 ÷ 150	368
[11]	0.25	0 ÷ 120	60
[12]	0.18	0 ÷ 110	50
[13]	0.18	−30 ÷ 135	57
[14]	0.18	0 ÷ 100	185
[15]	0.35 BiCMOS	−30 ÷ 100	28

The standard temperature calibration technique is based on measuring IC's temperature and then applying appropriate correction taken from a special look-up table. In CMOS technology the substrate PNP bipolar junction transistor (BJT) is very often used as a temperature sensor. The principle of the sensor's operation is that the forward voltage of the base-emitter junction of a BJT is temperature-dependent. Sensing this voltage makes it possible to calculate the temperature of the IC and then a necessary correction is done based on the previous temperature characterization and special look-up tables; see [16,17].

This calibration technique has many different variants because an IC's temperature can be monitored in many different ways. Another calibration method is to use an inverter-based ring oscillator, the frequency of which varies with temperature. An appropriate counter records the number of cycles and provides feedback information. If the number from the counter is higher than the stored one, it means that the temperature has changed. Comparing the calculated frequency with the one measured previously at room temperature enables the necessary corrections to be made [18].

The so-called adaptive body bias (ABB) is a completely different temperature calibration technique. Process and temperature variations cause the nominal parameters of modern-day digital circuits to vary significantly from the intended values. The ABB technique provides a post-silicon tuning capability to counter lot-to-lot, wafer-to-wafer, die-to-die and within-die variations. The ABB technique can be performed both in the digital and analog domain. In both solutions, IC temperature monitoring is essential. In the digital domain a body bias generator is generating separate voltages for NMOS and PMOS transistors based on a look-up table with pre-computed values. The appropriate value is selected based on the IC's temperature. In the analog domain, a body bias generator is controlled directly by the temperature sensor. ABB has been widely used for digital circuits ([19,20]) and recently was also proposed for relatively simple analog circuits containing a small number of transistors, such as a low noise amplifier or power amplifier. The adaptive body biasing technique uses a current source to sense the circuit temperature [21] and then to generate the relevant voltage to adjust the threshold voltage of a MOS transistor. Adaptive gate bias (AGB) is a very similar technique that can be used for temperature calibration. A bias voltage is generated based on the IC's temperature to counter the degradation of circuit performance with increasing temperature [22]. ABB or AGB could be suitable for certain types of circuits but applying these techniques to more complex and more sophisticated analog circuits could be very challenging, since it is very probable that different transistors will have to be biased with different voltages.

The one thing all the methods described above have in common is that they require additional analog blocks that occupy extra die area and consume additional power. Moreover, these methods are affected by IC aging caused by mobility and threshold voltage degradation, especially if they are based on a comparison with earlier characterization. Therefore, there is a need for a simple and effective method of temperature calibration. This paper attempts to provide a solution to this problem.

3. Analog Frontend

The presented analog frontend was designed and manufactured in UMC CMOS 130 nm technology. The AFE is supplied from 1.2 V and consumes no more than 185 µA, but it should be remembered that the external thermistor is fed with a 100 µA current. The AFE consists of a bandgap current reference (BGR), a precision current source (PCS), a programmable gain amplifier (PGA), a voltage source proportional to absolute temperature (PTAT voltage source) and an on-chip calibration resistor. A simplified block diagram of the AFE is presented in Figure 2.

The discussed AFE has four different operating modes. The first or primary mode is used to measure the human body temperature. The three additional modes are used for temperature calibration. In the first mode, the external thermistor is connected to the AFE's inputs. The thermistor is driven from the PCS and the voltage generated across its resistance is fed to the PGA and finally to the analog-to-digital converter (ADC was not part of this work). The second mode operates in the same way, but the PGA's input is coupled with the internal on-chip calibration resistor. The third mode is used to measure the output voltage of the PTAT voltage source. The last mode is used to determine the PGA offset voltage by shorting its inputs.

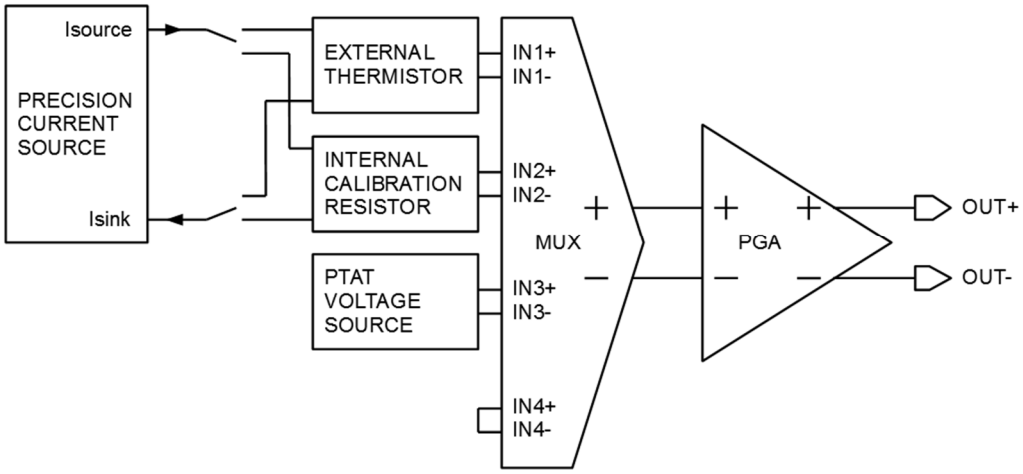

Figure 2. A simplified block diagram of the analog frontend.

3.1. Precision Current Source

A simplified schematic diagram of the PCS is presented in Figure 3, [23]. The source was integrated with a BGR. The BGR was based on a resistorless voltage reference with low sensitivity to process, supply voltage and temperature variations [24]. Simplified transistor symbols were used for the clarity of the schematic diagrams. Unless indicated otherwise, the bodies of all NMOS/PMOS transistors are biased with Vss/Vdd, respectively.

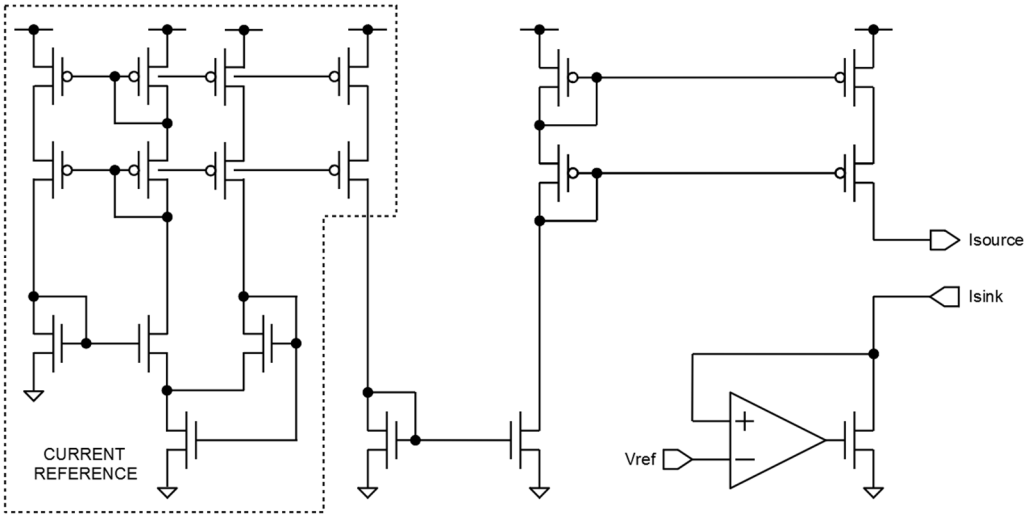

Figure 3. A simplified schematic diagram of the precision current source.

The nominal measurement current was set to 100 µA. The current is a trade-off between the noise level and the self-heating effect of the thermistor. Higher current results in lower noise level but also higher self-heating effect. If the measured resistance range and selected current value are considered, then the voltage across the thermistor changes approximately from 90 mV to 230 mV. Additionally, there is a possibility to force the required offset voltage at the output pin of the PCS (Vref signal in the Figure 3), which is also the reference terminal for the thermistor and the PGA. This feature makes it possible to adjust the thermistor voltage drop to the dynamic ranges of both the PGA and the ADC.

The PCS output current characteristics against temperature across all process corner and Monte Carlo simulations are shown in Figures 4 and 5, respectively. Process corners represent the extremes of fabrication parameter variations (TT: typical-typical, FF: fast-fast, SS: slow-slow, SNFP: slow NMOS-fast PMOS, FNSP: fast NMOS-slow PMOS). The calculated temperature coefficients are given in Table 3.

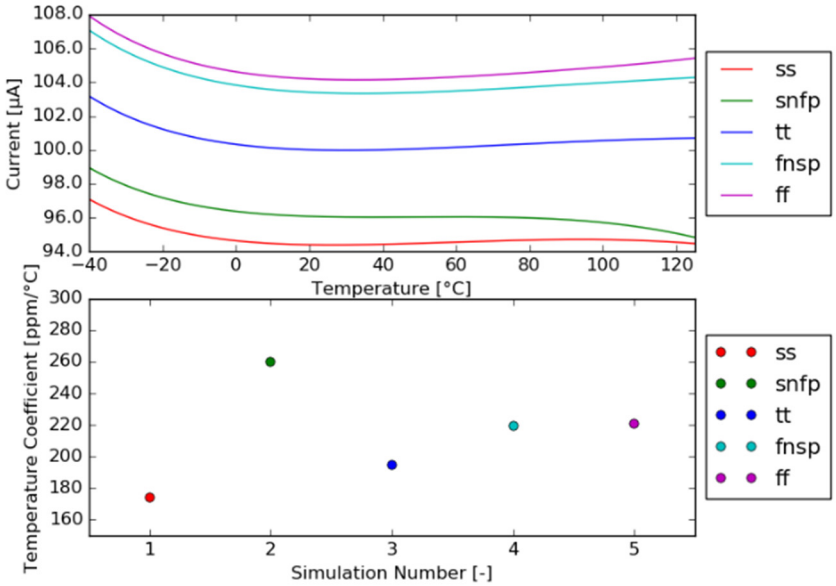

Figure 4. Process corner simulations of PCS output current.

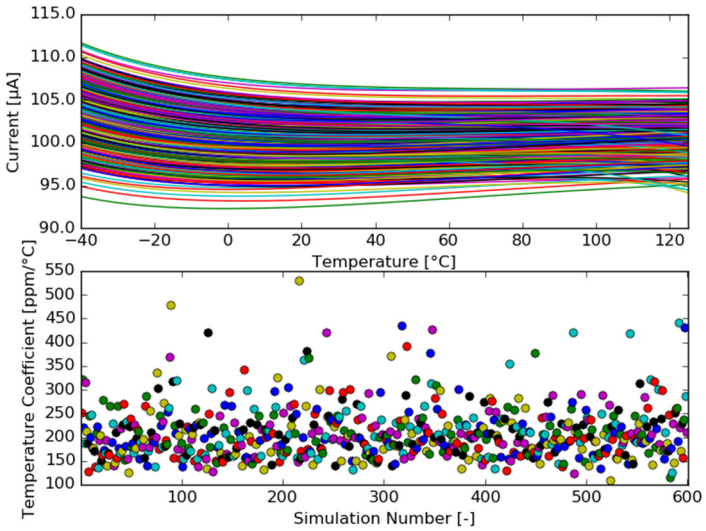

Figure 5. Monte Carlo simulations of PCS output current.

Table 3. Simulation-based temperature coefficients of PCS.

Simulation	SS	SNFP	TT	FNSP	FF	MC worst	MC best
Temperature coefficient [ppm/°C]	174	260	194	220	221	529	108

3.2. Programmable Gain Amplifier

A simplified diagram of the PGA is presented in Figure 6 [23]. This architecture was chosen to achieve a very low gain temperature coefficient. The total gain of the amplifier, assuming high transimpedance amplifier gain, is given by:

$$G_{TOT} = \frac{gm_{OTA1}}{gm_{OTA2}} \quad (1)$$

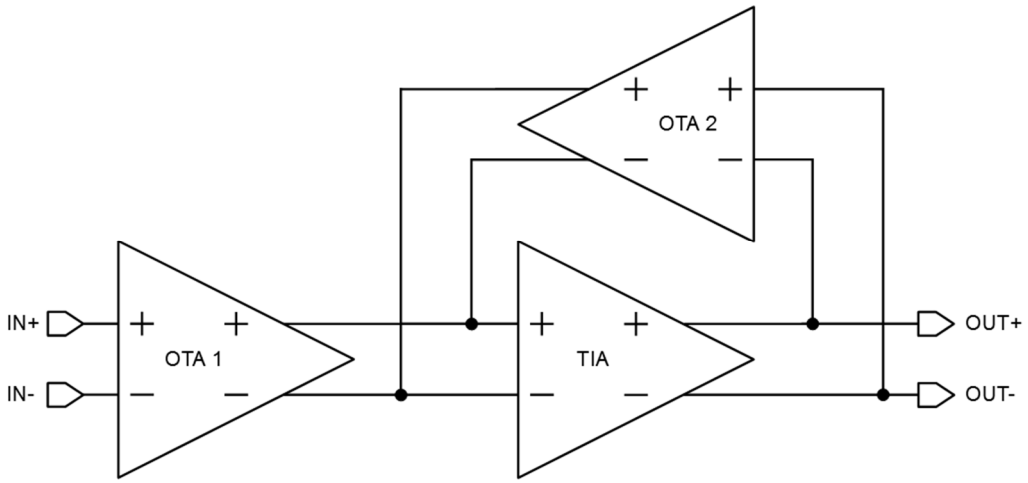

Figure 6. A simplified schematic diagram of the programmable gain amplifier.

The key aspect of the selected architecture is that both operational transconductance amplifiers (OTA 1 and OTA 2) share the same structure, which is presented in Figure 7. The transconductance temperature coefficients of both OTAs are almost the same (the only differences may result from the local process variations). Therefore, the transconductance ratio of the OTAs is almost constant in a very wide temperature range. A very stable transconductance ratio of Equation (1) results in almost constant PGA gain across a wide temperature range. The gain of the transimpedance amplifier (TIA) is high, therefore its influence on the PGA gain is insignificant (Figure 8). The primary function of the TIA is to ensure the appropriate current drive for the input impedance of the ADC. The gain of the PGA can be controlled by changing the gain of OTA 1 without a significant impact on the gain temperature coefficient of the whole PGA. The default gain was set to 6 dB.

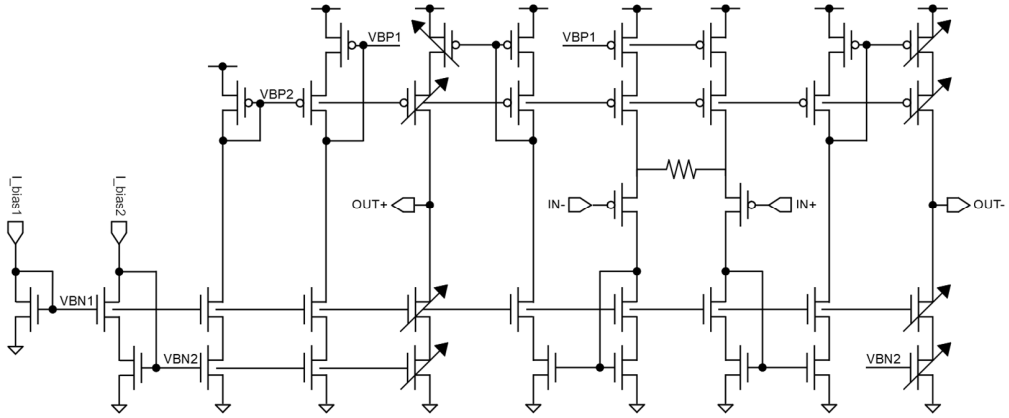

Figure 7. A simplified schematic diagram of the transconductance amplifier.

The PGA gain characteristics against temperature across all process corner and Monte Carlo simulations are shown in Figures 9 and 10, respectively. The calculated temperature coefficients are given in Table 4. It is fundamental to achieve as low a temperature coefficient as possible to reach the required measurement accuracy because the proposed calibration technique does not allow the PGA to be calibrated separately.

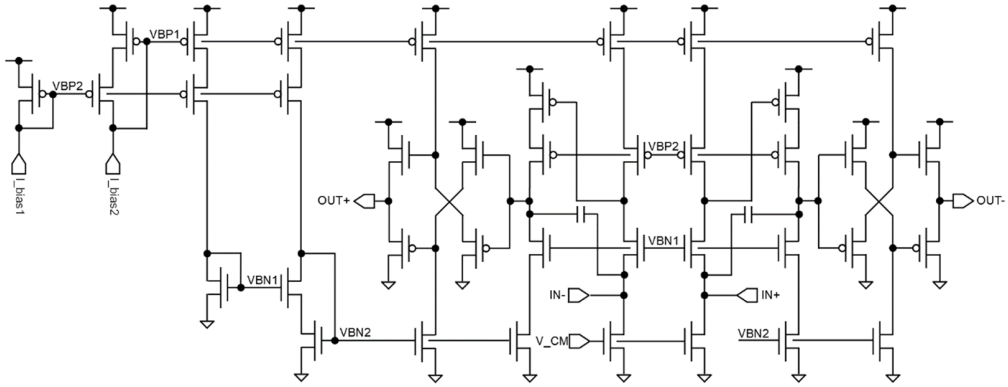

Figure 8. A simplified schematic diagram of the transimpedance amplifier.

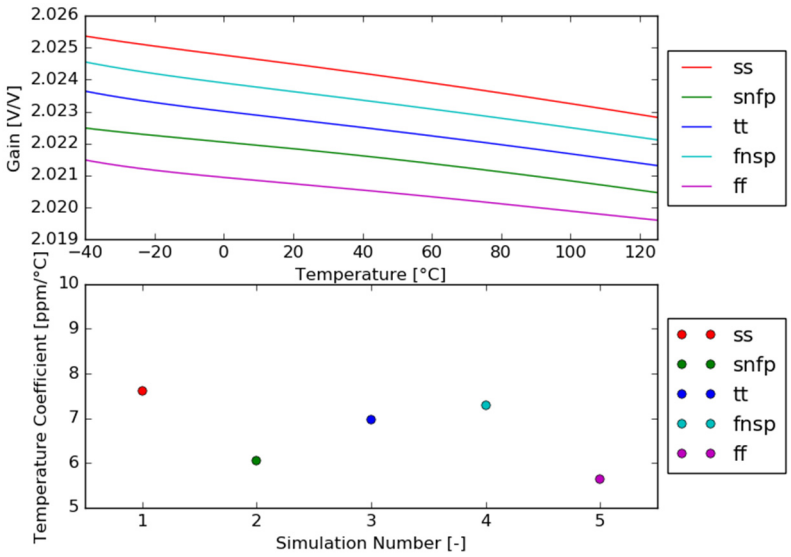

Figure 9. Process corner simulations of PGA voltage gain.

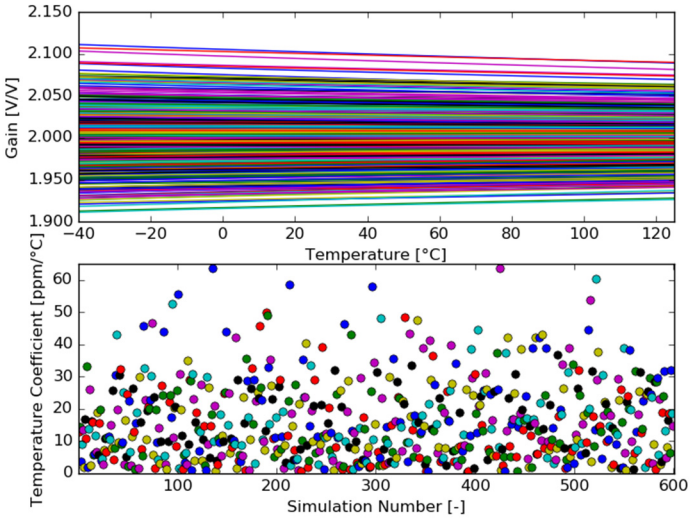

Figure 10. Monte Carlo simulations of PGA voltage gain.

Table 4. Simulation-based temperature coefficients of PGA.

Simulation	SS	SNFP	TT	FNSP	FF	MC Worst	MC Best
Temperature coefficient [ppm/°C]	7.6	6.1	7.0	7.3	5.7	63.6	0.4

3.3. Voltage Source Proportional to Absolute Temperature

Another element of the AFE is the PTAT voltage source. This is a modification of the BGR used in the PCS, but PTAT voltage source can use any architecture (e.g., [25]). Furthermore, the PTAT voltage source has to have a differential output; therefore, an additional voltage divider was added. A simplified diagram of the PTAT voltage source is presented in Figure 11. The PTAT output voltage is shown as a function of temperature in Figure 12 (simulation of all process corners) and Figure 13 (Monte Carlo simulations).

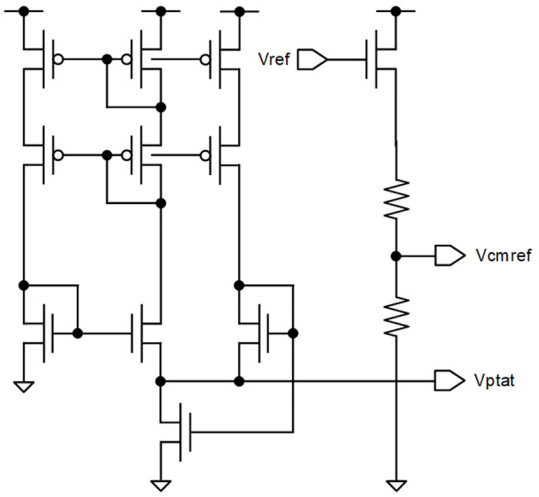

Figure 11. A simplified schematic diagram of the voltage source proportional to absolute temperature.

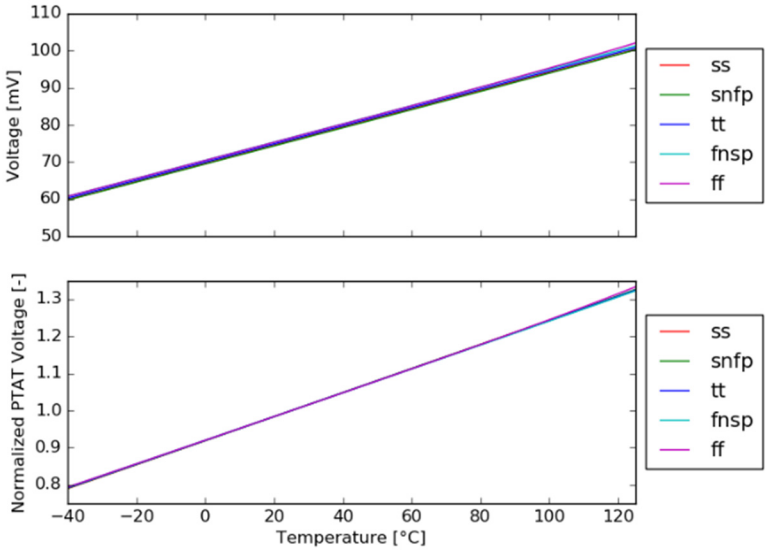

Figure 12. Process corner simulation of PTAT output voltage.

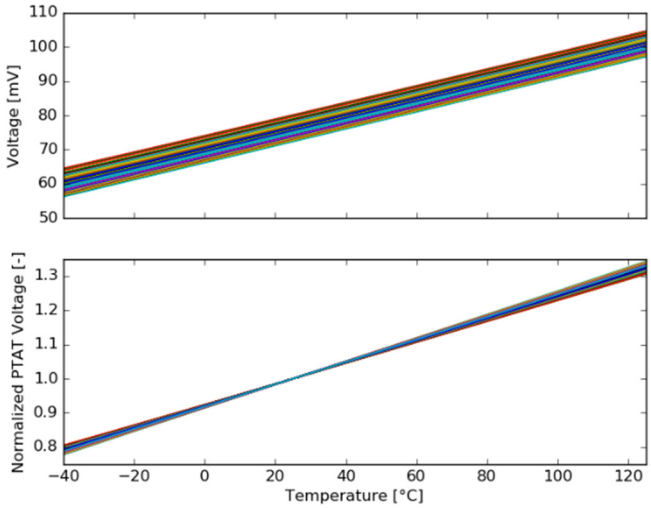

Figure 13. Monte Carlo simulations of PTAT output voltage.

3.4. Calibration Resistor

The last component of the AFE is the on-chip calibration resistor. A diffusion resistor was selected, and the resistance was chosen to be around the middle of the range of the thermistor's resistance. The resistance of the calibration resistor can vary by ±30% from the nominal value. However, the characteristics normalized to the resistance value at a given temperature are the same for any selected temperature (Figures 14 and 15). This feature is crucial because it makes the developed temperature calibration technique immune to process variations. On-chip calibration resistor characteristics were normalized to the resistance at 25 °C.

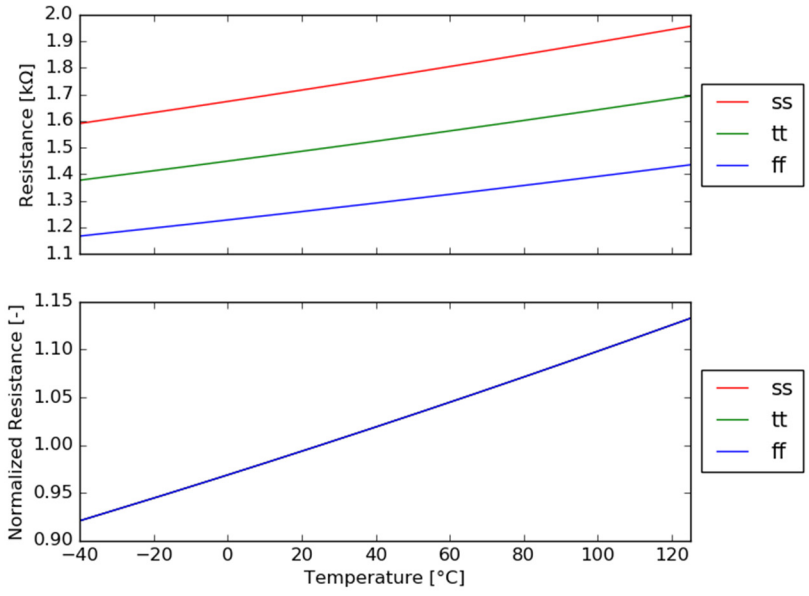

Figure 14. Process corner simulations of the resistance of the on-chip calibration resistor.

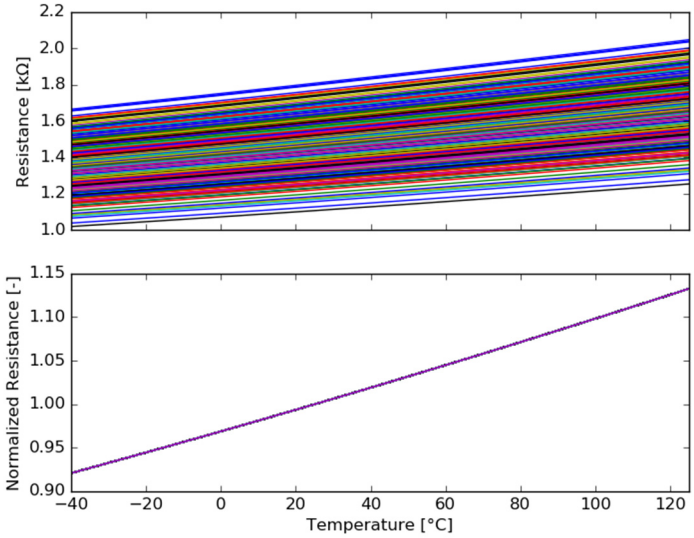

Figure 15. Monte Carlo simulations of the resistance of the on-chip calibration resistor.

4. Temperature Calibration Technique

The proposed original temperature calibration technique [5] is performed in two phases. The first phase is executed only once, at the very beginning of the usage of the chip, preferably during factory tests. The second phase is repeated before the proper human body temperature measurement and should be performed only if the chip's temperature changes significantly, causing too large a measurement error. If the chip temperature is stable, the frequency of the second phase execution can be reduced to reduce power consumption.

The first phase consists of four steps. The very first step is to determine the offset voltage of the PGA. Therefore, the input terminals of the amplifier have to be shorted and the output voltage of the amplifier has to be measured. Subsequently, in the second step, a precise external calibration resistor is connected to the input terminals of the AFE. It is very important to know the exact value of the calibration resistance (R) that may be also calculated from the equation below:

$$R = \frac{U_{meased}}{I_{PCS} \times G_{PGA}} \tag{2}$$

However, due to global and local process variations (I_{PCS_err}, G_{PGA_err}), the values of the PCS output current (I_{PCS}) and PGA gain (G_{PGA}) deviate from the nominal ones (I_{PCS_nom}, G_{PGA_nom}) and true values are not known. Nevertheless, Equation (2) can be transformed into:

$$R = \frac{U_{meased}}{(I_{PCS\_nom} \times I_{PCS\_err}) \times (G_{PGA\_nom} \times G_{PGA\_err})} \tag{3}$$

Finally, the PCS current error and PGA gain error can be combined into the total error of the whole AFE:

$$R = \frac{U_{meased}}{I_{PCS\_nom} \times G_{PGA\_nom}} \times AFE_{err} \tag{4}$$

Thereby measuring the voltage drop across the known external precision calibration resistor (U_{meased}) the total error of the whole AFE may be easily calculated (AFE_{err}). The third step is to connect the internal, on-chip calibration resistor to the AFE. Having computed the previously mentioned error of the whole AFE, it is now possible to calculate the true value of the on-chip calibration resistance. In the last step, the PTAT voltage source is connected to the PGA. Both values, the resistance of the on-chip calibration resistor and the voltage generated by the PTAT voltage source, have to be stored for the second phase of temperature calibration, preferably in embedded flash memory.

The second phase consists of two steps. The first step is to measure the output voltage of the PTAT voltage source. Having measured this voltage and then compared it to the previous result, one may determine the change in the operating temperature of the integrated circuit. This calculation is based on the known temperature characteristics of the PTAT voltage source shown in Figures 11 and 12. Thereby, it is possible to compute the true, theoretical calibration resistance based on the already known temperature characteristics shown in Figures 13 and 14. The second step is to measure the actual calibration resistance. The difference between those two values, the calculated and the measured one, results from the temperature drift of the whole AFE; therefore, the measurement error can be determined. This completes the whole calibration procedure. Only after the whole calibration procedure is performed is it possible to execute the proper measurement of the thermistor. Having the temperature drift error of the whole AFE calculated during the calibration procedure, the true resistance of the thermistor may be determined and therefore the human body temperature may be computed with very high accuracy.

A model implementing the temperature calibration technique, proposed in Section 4, was developed. This model was written in Python. The required input data are stored in look-up tables with a 0.1 °C step. The main goal of the discussed model is to present the simulation results of human body temperature measurement with the proposed temperature calibration technique either neglected or used.

Finally, the data presented in Figures 4, 9, 12 and 14 were fed to the temperature calibration model and 1000 simulations were run. In each simulated process corner, the integrated circuit temperature and human body temperature were drawn. For each set of drawn values, the measurement errors of human body temperature and absolute temperature were calculated with the proposed calibration technique either neglected or used. The results are presented in Figures 16 and 17, respectively. In the first case, the maximum measurement error is higher than 1°C. This is a huge error considering that the human body temperature changes in a relatively narrow range. In the second case, the simulation was made with the temperature calibration technique taken into account and the absolute error does not exceed 0.1 °C. These results may be explained by two facts. First, the PGA gain coefficient is a few times better (i.e., lower) than the minimum required one. Second, the data describing the thermistor characteristics are kept with 0.1 °C resolution. Increasing this resolution should also result in decreasing the error. However, the minimum error is always limited by the gain temperature coefficient of the PGA.

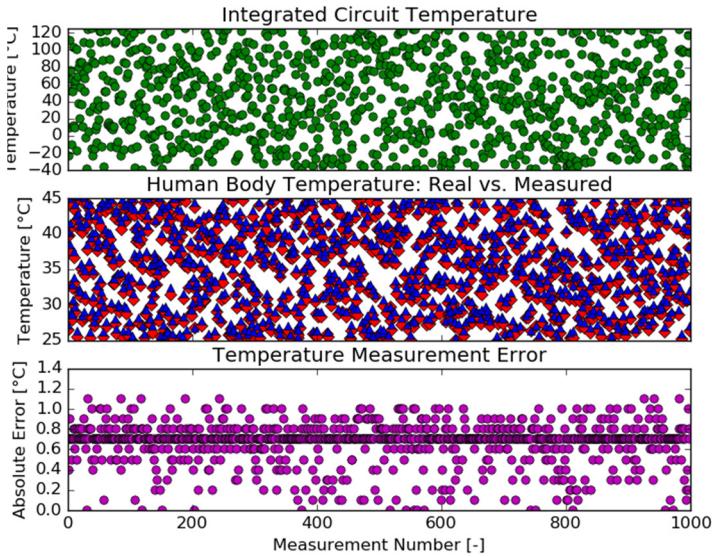

Figure 16. Process corner simulations without temperature calibration technique.

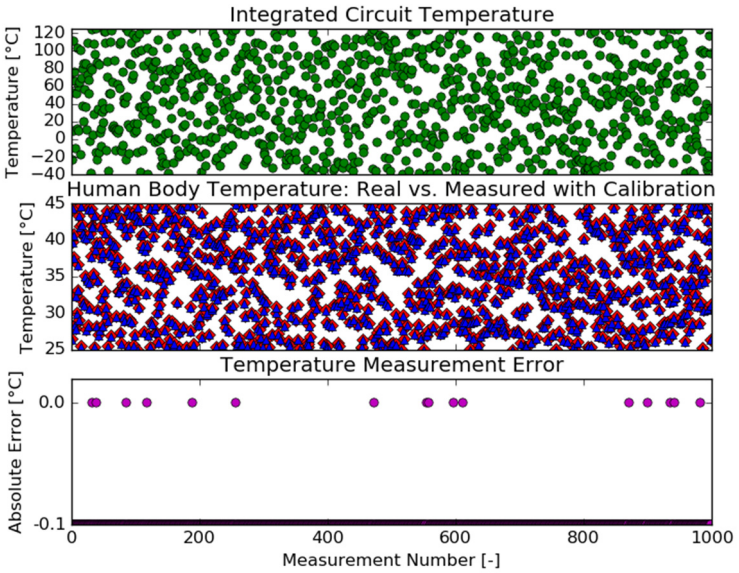

Figure 17. Process corner simulations with temperature calibration technique.

The whole simulation flow discussed in Section 4 was repeated using Monte Carlo simulations. The simulations of the temperature calibration model with the proposed calibration technique either neglected or used are presented in Figures 18 and 19, respectively. The results obtained in Monte Carlo simulations are generally worse than those from process corner simulations. This indicates that the designed analog blocks are more sensitive to local variations than global ones. However, the proposed temperature calibration technique continues to provide very high measurement accuracy.

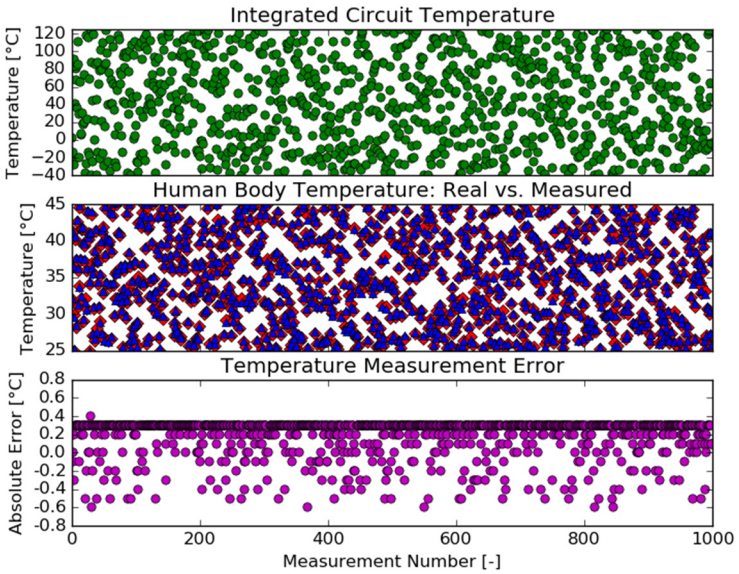

Figure 18. Monte Carlo simulations without temperature calibration technique.

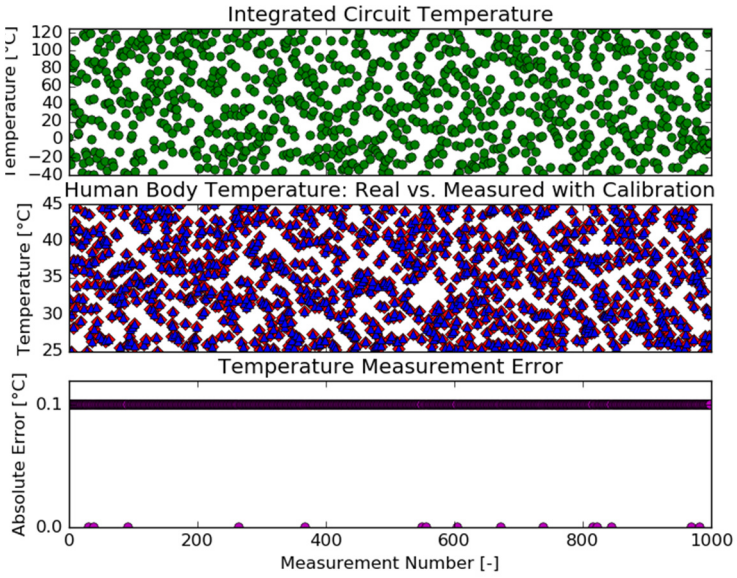

Figure 19. Monte Carlo simulations with temperature calibration technique.

5. Measurements Results

The test chip layout is presented in Figure 20 with the measured devices clearly indicated. The test chip contained all the building blocks, although they were not integrated into one analog frontend. Test chips were manufactured in two different lots. Measurements were taken using a manual wafer prober with a climate-controlled microchamber [4]. The temperature was changed from −40 °C to +125 °C with 5 °C steps. For each temperature, several measurements were performed to ensure that temperature had stabilized and to eliminate random errors. Unfortunately, the resistance between the bonding pad and the probe had some impact on the measurement accuracy. This resistance changed with probe movement along the surface of the bonding pad causing a systematic error for a specific temperature point.

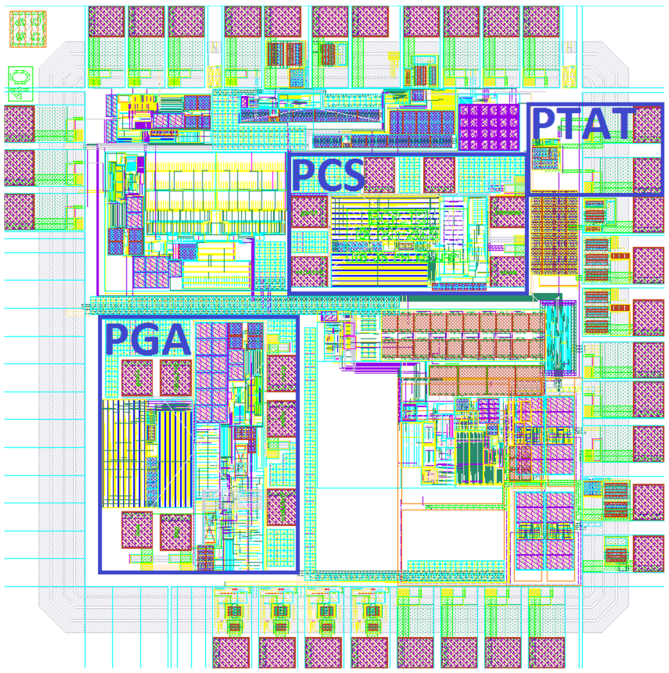

Figure 20. Test chip layout.

The measured output current temperature characteristics of ten different PCS are shown in Figure 21 and the calculated temperature coefficients are given in Table 5. The results of the measurements are comparable to the simulation results.

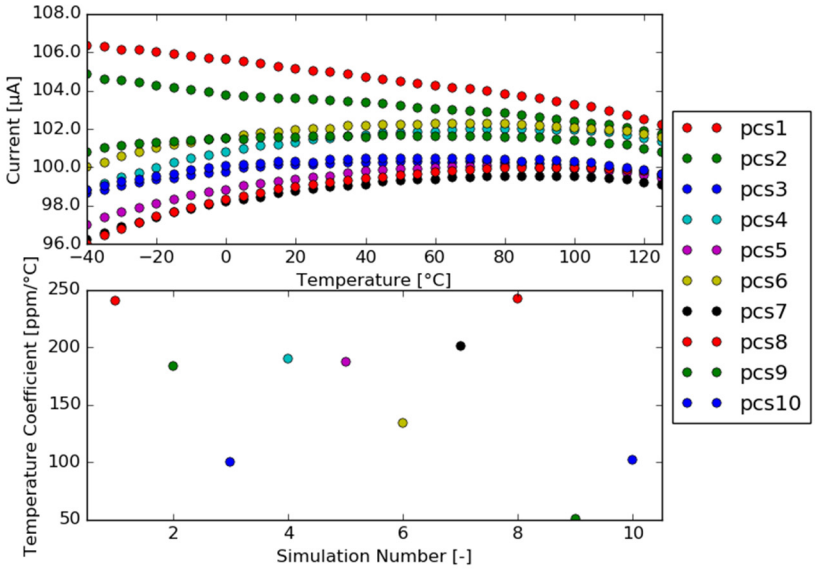

Figure 21. PCS output current against temperature.

Table 5. Experimental temperature coefficients of PCS.

Measurement device	PCS 1	PCS 2	PCS 3	PCS 4	PCS 5	PCS 6	PCS 7	PCS 8	PCS 9	PCS 10
Temperature coefficient [ppm/°C]	241	184	100	190	188	134	202	243	51	102

The measured gain-temperature characteristics of ten different PGAs are presented in Figure 22 and the calculated temperature coefficients are given in Table 6. The experimental results are much worse than the simulation ones. This may be explained by the fact that the gain was measured in a single-ended configuration instead of the fully differential one because the number of the available probe holders were limited. It seems that these gain temperature coefficients are worse because of the common mode voltage temperature instability rather than the gain instability itself. To achieve 0.1 °C measurement accuracy it is crucial that the gain temperature coefficient is not worse than the minimum temperature stability defined in Section 2. This aspect is really important because there is no possibility to calibrate the PGA gain separately.

Table 6. Experimental temperature coefficients of PGA.

Measurement device	PGA 1	PGA 2	PGA 3	PGA 4	PGA 5	PGA 6	PGA 7	PGA 8	PGA 9	PGA 10
Temperature coefficient [ppm/°C]	115	66.6	28.8	100	51.3	134	226	19.8	66.5	119

The measured PTAT output voltage is shown in Figure 23 as a function of temperature. PTAT voltage was measured using both single-ended and differential configurations to compare the obtained results. The linearity of the differential signal is slightly worse due to the temperature drift of the voltage from the voltage divider, but this error is negligible. Ten different PTAT voltage sources were measured.

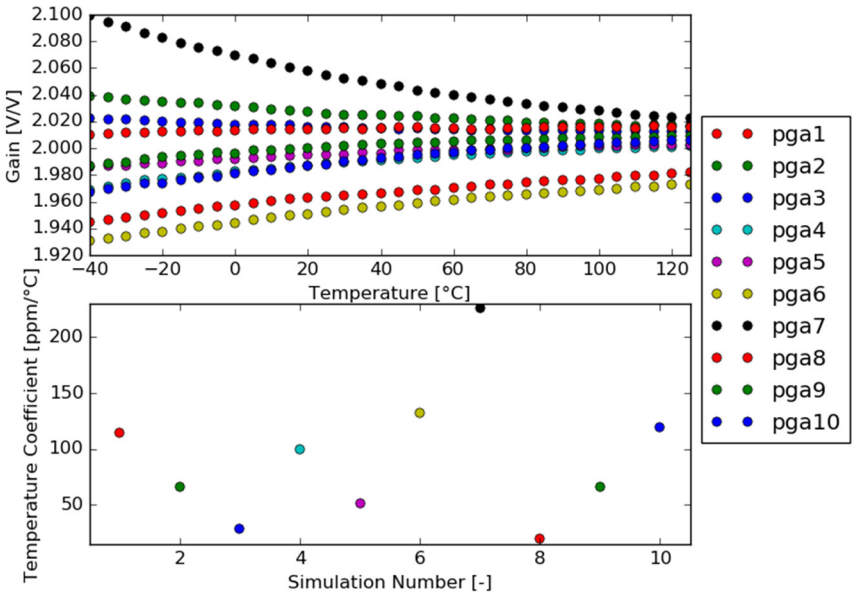

Figure 22. PGA gain against temperature.

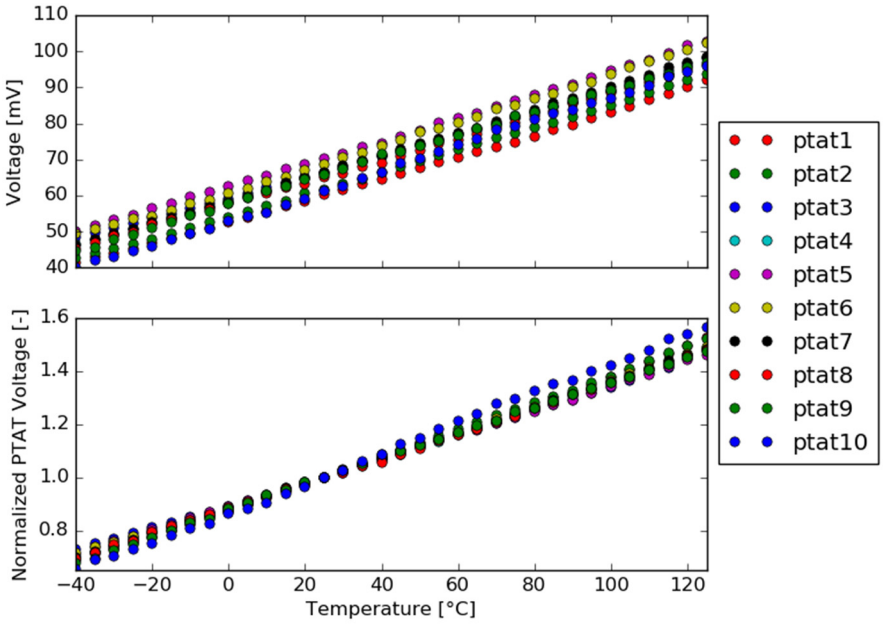

Figure 23. PTAT output voltage versus temperature.

The experimental characteristics of four different calibration resistors are presented in Figure 24. In contrast to previous measurements, the test chips containing calibration resistors came from two different tape-outs, but within one tape-out from the same lot. It is not surprising that these characteristics are very similar.

The measurement results were fed to the AFE model described in Section 4. The model simulation results obtained with the temperature calibration technique either neglected or taken into account are shown in Figures 25 and 26, respectively. In both simulations the human body temperature is fixed and equal to 37 °C. Each figure contains two diagrams. The upper diagram shows the real temperature of the human body (red line) along with its measured value (blue line). The lower diagram represents the absolute measurement error (magenta line). In the first case (no temperature calibration technique), the maximum measurement error is higher than 1 °C. This is a very large error because human body temperature changes in a relatively narrow range. In the second case, the simulation is

made with the temperature calibration technique and has an absolute error up to 0.2 °C, which is worse than the required 0.1 °C. The maximum accuracy is limited by the gain temperature coefficient of the PGA, because this error cannot be calibrated. Resolving the problem with PGA gain measurement will result in improved overall accuracy.

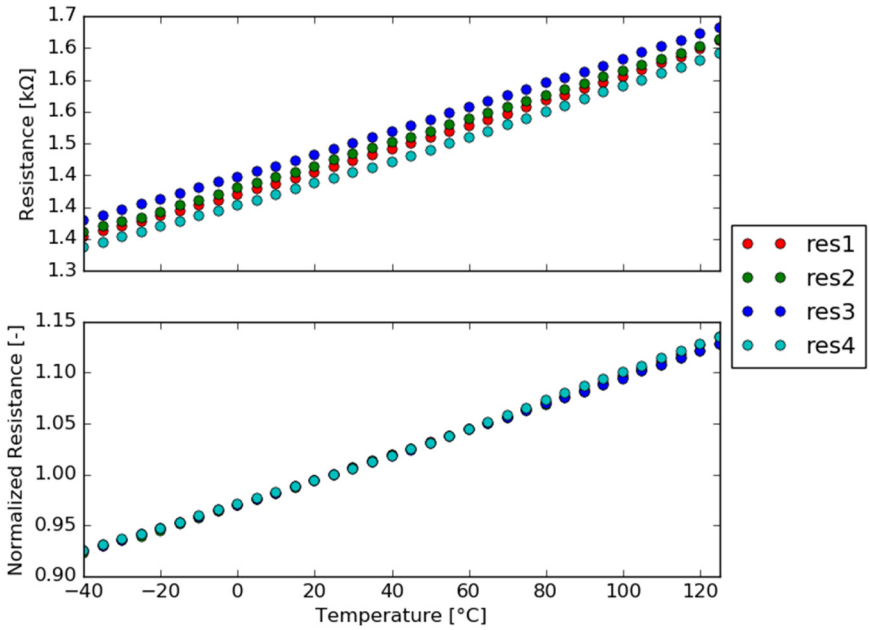

Figure 24. Resistance of the calibration resistor versus temperature.

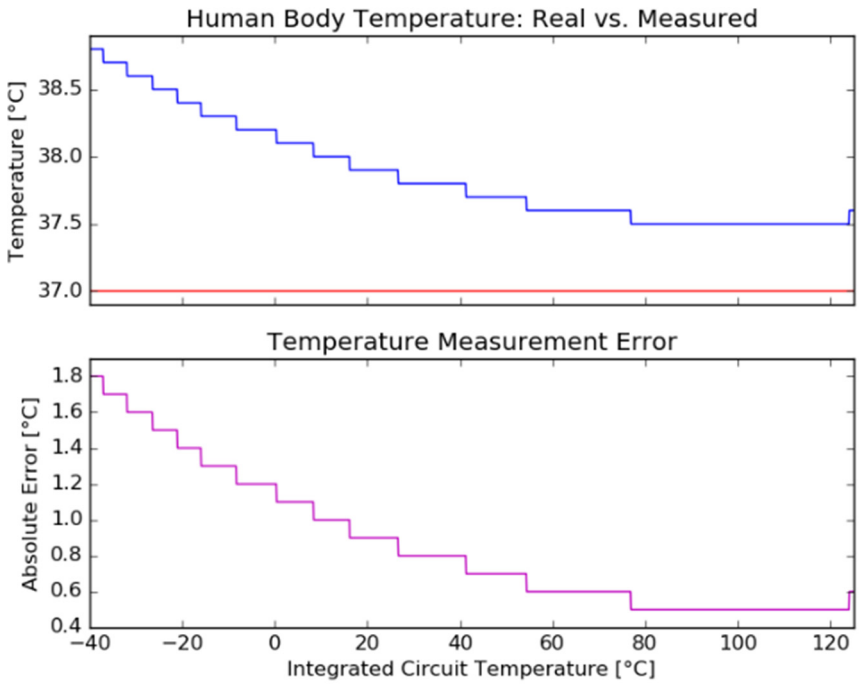

Figure 25. AFE model simulation results without temperature calibration technique.

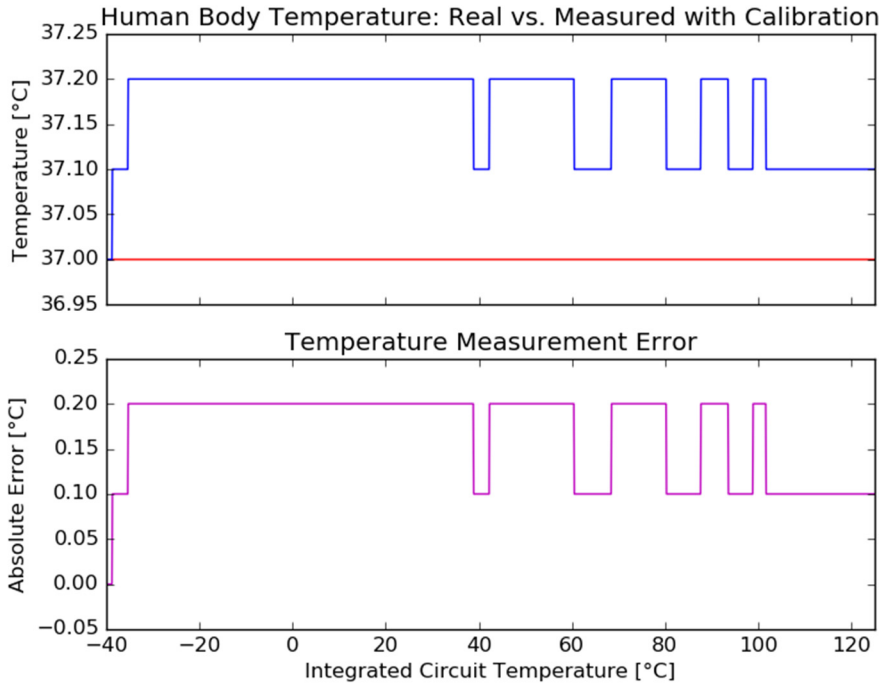

Figure 26. AFE model simulation results with temperature calibration technique.

6. Conclusions

The purpose of this paper was to demonstrate that the proposed new and novel temperature calibration technique provides very high measurement accuracy. The findings of this research (presented in Sections 4 and 5), based not only on simulation results but also on measurements, seem to prove this point. Further efforts and future research will be focused on implementing the described algorithm in an SoC processor and finding out if the proposed technique works in dynamic conditions.

Doe to the novelty of the presented approach, it was very difficult to compare the obtained results with those published previously. Different temperature calibration techniques, described briefly in Section 2, are performed either in the analog domain (body bias) or in the digital domain (look-up tables). However, all these methods are very complex, which means higher power consumption and additional area on a silicon die. Moreover, they require time-consuming characterization and are vulnerable to ageing (especially these based on look-up tables). The IC ageing process, due to mobility degradation, changes the resistance of the calibration resistor. In the proposed temperature calibration technique, the ageing problem may be solved by measuring the on-chip calibration resistor at several different temperatures (three-point calibration). A new resistance regression line in the whole range of the operating temperature of an IC may be calculated based on the calibration resistor linear characteristic against temperature. The proposed calibration technique may be used in any measurements where the temperature stability is a crucial factor. Furthermore, the calibration resistor used in this technique could be replaced with any device with well-defined thermal characteristics. The demonstrated advantages seem to make this temperature calibration technique universal, convenient and reliable.

Author Contributions: The work presented in this paper was a collaboration of all authors. Methodology, investigation, validation, visualization, writing—original draft: P.N.; supervision, writing—review and editing, project administration, funding acquisition: W.A.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded in part by the Polish National Centre for Research and Development under project no. PBS1/B2/13/2012.

Acknowledgments: The authors would like to thank Krzysztof Siwiec and Lidia Łukasiak from Warsaw University of Technology for help and valuable feedback.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Siwiec, K.; Marcinek, K.; Borejko, T.; Jarosz, A.; Kopanski, J.; Kurjata-Pfitzner, E.; Narczyk, P.; Plasota, M.; Wielgus, A.; Pleskacz, W.A.; et al. A CMOS system-on-chip for physiological parameters acquisition, processing and monitoring. In Proceedings of the 2015 22nd International Conference Mixed Design of Integrated Circuits & Systems (MIXDES), Torun, Poland, 25–27 June 2015; pp. 37–42. [CrossRef]
2. Siwiec, K.; Marcinek, K.; Boguszewicz, P.; Borejko, T.; Halauko, A.; Jarosz, A.; Kopanski, J.; Kurjata-Pfitzner, E.; Narczyk, P.; Plasota, M.; et al. BioSoC: Highly integrated System-on-Chip for health monitoring. In Proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Kosice, Slovakia, 20–22 April 2016; pp. 1–6. [CrossRef]
3. Narczyk, P.; Siwiec, K.; Pleskacz, W.A. Precision human body temperature measurement based on thermistor sensor. In Proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Kosice, Slovakia, 20–22 April 2016; pp. 1–5. [CrossRef]
4. Narczyk, P.; Siwiec, K.; Pleskacz, W.A. Analog front-end for precise human body temperature measurement. In Proceedings of the 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Dresden, Germany, 19–21 April 2017; pp. 67–72. [CrossRef]
5. Narczyk, P.; Siwiec, K.; Pleskacz, W.A. Temperature calibration technique based on on-chip resistor. In Proceedings of the 2017 MIXDES-24th International Conference "Mixed Design of Integrated Circuits and Systems, Bydgoszcz, Poland, 22–24 June 2017. [CrossRef]
6. Lee, C.-H.; Park, H.-J. All-CMOS temperature independent current reference. *Electron. Lett.* **1996**, *32*, 1280–1281. [CrossRef]
7. Serrano, G.; Hasler, P. A Precision Low-TC Wide-Range CMOS Current Reference. *IEEE J. Solid-State Circuits* **2008**, *43*, 558–565. [CrossRef]
8. Yi, W.; Lenain, H.; Xiaolang, Y. All CMOS temperature, supply voltage and process independent current reference. In Proceedings of the 2007 7th International Conference on ASIC, Guilin, China, 22–25 October 2007; pp. 600–603. [CrossRef]
9. De Vita, G.; Iannaccone, G. A 109 nW, 44 ppm/°C CMOS Current Reference with Low Sensitivity to Process Variations. In Proceedings of the 2007 IEEE International Symposium on Circuits and Systems, New Orleans, LA, USA, 27–30 May 2007; pp. 3804–3807. [CrossRef]
10. Badillo, D. 1.5V CMOS current reference with extended temperature operating range. In Proceedings of the 2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353), Phoenix-Scottsdale, AZ, USA, 26–29 May 2002. [CrossRef]
11. Yoo, C.; Park, J. CMOS current reference with supply and temperature compensation. *Electron. Lett.* **2007**, *43*, 1422–1424. [CrossRef]
12. Chen, J.; Shi, B. 1 V CMOS current reference with 50 ppm/°C temperature coefficient. *Electron. Lett.* **2003**, *39*, 209–210. [CrossRef]
13. Jahagirdar, V.; Hirur, R. CMOS current reference with temperature compensation. In Proceedings of the 2015 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT), Coimbatore, India, 5–7 March 2015; pp. 1–4. [CrossRef]
14. Bendali, A.; Audet, Y. A 1-V CMOS Current Reference with Temperature and Process Compensation. *IEEE Trans. Circuits Syst. I: Regul. Pap.* **2007**, *54*, 1424–1429. [CrossRef]
15. Fiori, F.; Crovetti, P. A new compact temperature-compensated CMOS current reference. *IEEE Trans. Circuits Syst. II Express Briefs* **2005**, *52*, 724–728. [CrossRef]
16. Lu, J.; Lee, H.J.; Kim, K.K.; Kim, Y.-B. A low power high resolution digital PWM with process and temperature calibrations for digital controlled DC-DC converters. In Proceedings of the 2014 International SoC Design Conference (ISOCC), Jeju, Korea, 3–6 November 2014; pp. 244–245. [CrossRef]
17. Mikulic, J.; Brezovec, I.; Magerl, M.; Schatzberger, G.; Baric, A. Temperature calibration of an on-chip relaxation oscillator. In Proceedings of the 2017 40th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO), Opatija, Croatia, 22–26 May 2017. [CrossRef]
18. Wang, J.; Koh, L.H.; Goh, W.L. A 13.8-MHz RC oscillator with self-calibration for ±0.4% temperature stability from −55 to 125 °C. In Proceedings of the 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, 1–4 June 2015; pp. 423–426. [CrossRef]
19. Kumar, S.V.; Kim, C.H.; Sapatnekar, S.S. Mathematically assisted adaptive body bias (ABB) for temperature compensation in gigascale LSI systems. In Proceedings of the Asia and South Pacific Conference on Design Automation, Yokohama, Japan, 24–27 January 2006. [CrossRef]
20. Sathanur, A.; Pullini, A.; Benini, L.; De Micheli, G.; Macii, E. Physically clustered forward body biasing for variability compensation in nanometer CMOS design. In Proceedings of the 2009 Design, Automation & Test in Europe Conference & Exhibition, Nice, France, 20–24 April 2009; pp. 154–159. [CrossRef]
21. Yuan, J.; Kritchanchai, E. Power amplifier resilient design for process, voltage, and temperature variations. *Microelectron. Reliab.* **2013**, *53*, 856–860. [CrossRef]

22. Chen, S.; Yuan, J.-S. Adaptive Gate Bias for Power Amplifier Temperature Compensation. *IEEE Trans. Device Mater. Reliab.* **2011**, *11*, 442–449. [CrossRef]
23. Baker, R.J. *CMOS: Circuit Design, Layout, and Simulation*; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2010. [CrossRef]
24. Borejko, T.; Pleskacz, W.A. A Resistorless Voltage Reference Source for 90 nm CMOS Technology with Low Sensitivity to Process and Temperature Variations. In Proceedings of the 2008 11th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Bratislava, Slovakia, 16–18 April 2008; pp. 1–6. [CrossRef]
25. Malits, M.; Brouk, I.; Nemirovsky, Y. Study of CMOS-SOI Integrated Temperature Sensing Circuits for On-Chip Temperature Monitoring. *Sensors* **2018**, *18*, 1629. [CrossRef] [PubMed]