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A Non-Isolated Hybrid Zeta Converter with a High Voltage Gain and Reduced Size of Components

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Abstract: In this paper a novel non-coupled inductor-based hybrid Zeta converter with a minimal duty cycle is proposed. The converter's potential benefits include buck and boost operation modes, easy implementation, continuous input current, and high efficiency. The converter provides a higher voltage gain than a conventional Zeta converter and is adapted to EV and LED applications due to the continuous input current. The proposed converter operates in three distinct operation modes via two electronic switches, each operated independently with a different duty ratio. This paper also analyzes the converter's performance based on equivalent circuits, and analytical waveforms in each operating mode and design procedure are shown. The voltage gain and dynamic modelling are computed for both buck and boost operational modes for the hybrid Zeta converter. The efficiency and performance of the converter in both operating modes are validated using MATLAB/Simulink. Hardware in the loop (HIL) testing method on RT-LAB OP-5700 for both operation modes of the converter are performed. The peak efficiency of the proposed converter with an input voltage of 36 V is obtained at 95.2%. The proposed converter offers a wide voltage gain at a small duty cycle with fewer components and high efficiency. Simulations and experiments have been carried out under different conditions and the results proved that the proposed converter is a viable solution.

Keywords: duty ratio control; dynamic modeling; hybrid Zeta converter; non-isolated DC-DC converter; small signal analysis

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1. Introduction

Renewable energy sources are increasing in prominence as non-renewable sources become limited. However, the output voltage level of renewables such as solar, wind, and hydrogen fuel is very low; to solve this issue, a different types of power converters (buck, boost and buck-boost) have been addressed in many research studies. Power converters with voltage boost or buck operations based on the load ratings are essential in renewable energy systems [1–3]. Furthermore, these converters regulate the output voltage more than a wide range of input voltages. The regulated DC power supply influences the converter effective performance and component rating selection. As a result, component selection is a key concern that impacts the converter performance. Most power converter researchers have been interested in converter topologies with limited components that attain large voltage gain with minimal duty cycles, and several non-isolated DC-DC converter topologies have been proposed over the years. Different types of buck-boost converters, are the CUK converter [4], the Zeta converter [5], and the SEPIC converter [6]. The traditional buck-boost converters' voltage gain ratio is $D/(1-D)$, and their duty cycle ranges from 0 to 1, producing a maximum voltage at higher duty cycles and a low output voltage at lower duty cycles. However, high duty cycle cannot be used due to

semiconductor device limitations [7]. Furthermore, due to the simplicity of the design of these converters, the current and voltage stresses on the elements are significantly high, and the voltage gain is also restricted in buck mode.

To overcome the aforementioned concerns, a non-isolated single switch cascaded buck-boost converter was proposed, as described in [8]. This converter has a high voltage gain but a fluctuating output voltage and a step-down voltage gain that is insufficient. In [9], a high voltage gain transformer-less buck-boost converter was proposed. Because semiconductor devices are exposed to a tremendous amount of current and voltage stress, the converter's overall losses are quite significant. In [10], a four buck-boost converter with high voltage gain, using a single power switch and common ground was developed. This converter's limitation is that the duty cycle must be smaller than 0.5. In [11], an alternative buck-boost converter with a single switch and voltage gain twice that of the typical buck-boost converter is described. The primary limitations of the converter described in [11] are fluctuating output voltage and a larger number of components, which diminishes converter efficiency. In [12], a KY converter with rapid transient response, comparable to a buck converter with minimal output voltage ripple and constant output current was presented. Although the controlling for power semiconductor devices is complicated, the KY converter voltage gain is neither to excessive nor too poor to supply the wide output voltage range. A zero-voltage switching hybrid Zeta converter including active clamping was recommended in [13]. To limit the number of components in the converter, the Zeta and flyback converters used an equal number of active switches. Two cascaded Zeta converters were used in [14] to reduce output voltage ripple. In [15], a transformer-less quadratic boost-CUK converter with one active switch was designed. The converter has a high voltage gain and a low voltage stress across the switches, but it has more components. As a consequence, the converter suffers from substantial losses. Similarly, buck-boost converters with a large conversion ratio have also been presented [16–19].

This paper introduced a hybrid non-isolated DC-DC Zeta converter with higher voltage gain and fewer components. The proposed converter offers a wide voltage gain with a small duty cycle as compared to traditional buck-boost, SEPIC, CUK, and Zeta converters. The proposed voltage gain assessment and converter design parameters are also presented. This paper is structured as follows: The proposed converter's operating principle, steady-state analysis, passive component design, and efficiency calculation are illustrated in Section 2. Section 3 discusses the validation of simulation and HIL test results. Finally, in Section 4, the paper conclusions are presented.

2. Materials and Methods

2.1. The Hybrid DC-DC Zeta Converter Operating Principle

The circuit is based on the Zeta topology and comprises of two active power switches (S_1 and S_2), two diodes (D_1 and D_2), two inductors (L_1 and L_2), two capacitors (C_1 and C_0), and a load R_0, as shown in Figure 1. The following assumptions have been made to make the converter analysis easier.

A. All semiconductor devices, such as MOSFETs and diodes, are considered ideal.
B. Two capacitors, C_1 and C_2, are substantial enough to maintain a constant voltage.

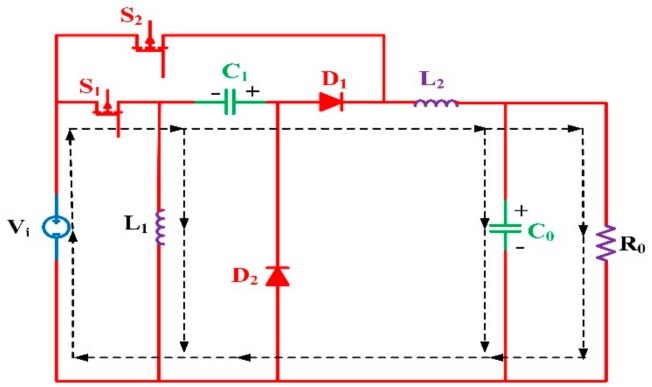


Figure 1. Proposed hybrid Zeta converter.

As shown in Figure 2, the working mode of the converter is controlled in three distinct operation modes based on the state of the switches as they are turned ON and OFF. Figure 3 depicts the equivalent circuits for each working mode.

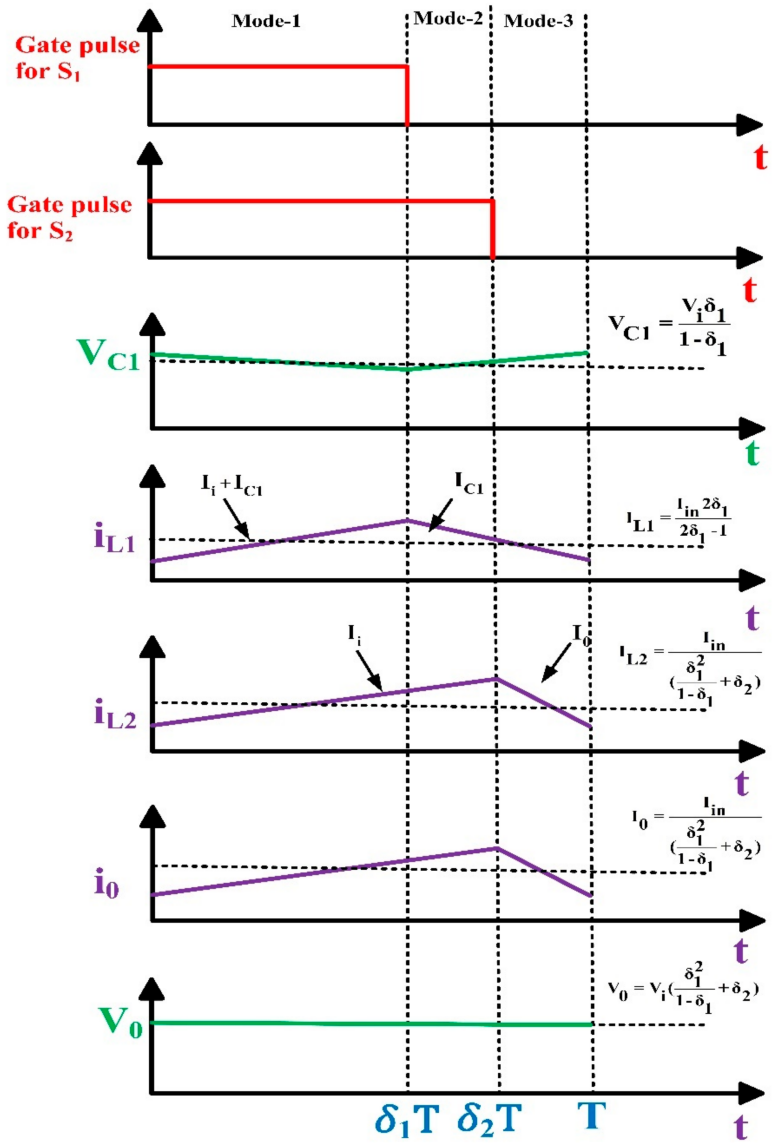


Figure 2. The proposed converter's waveforms for one switching interval.

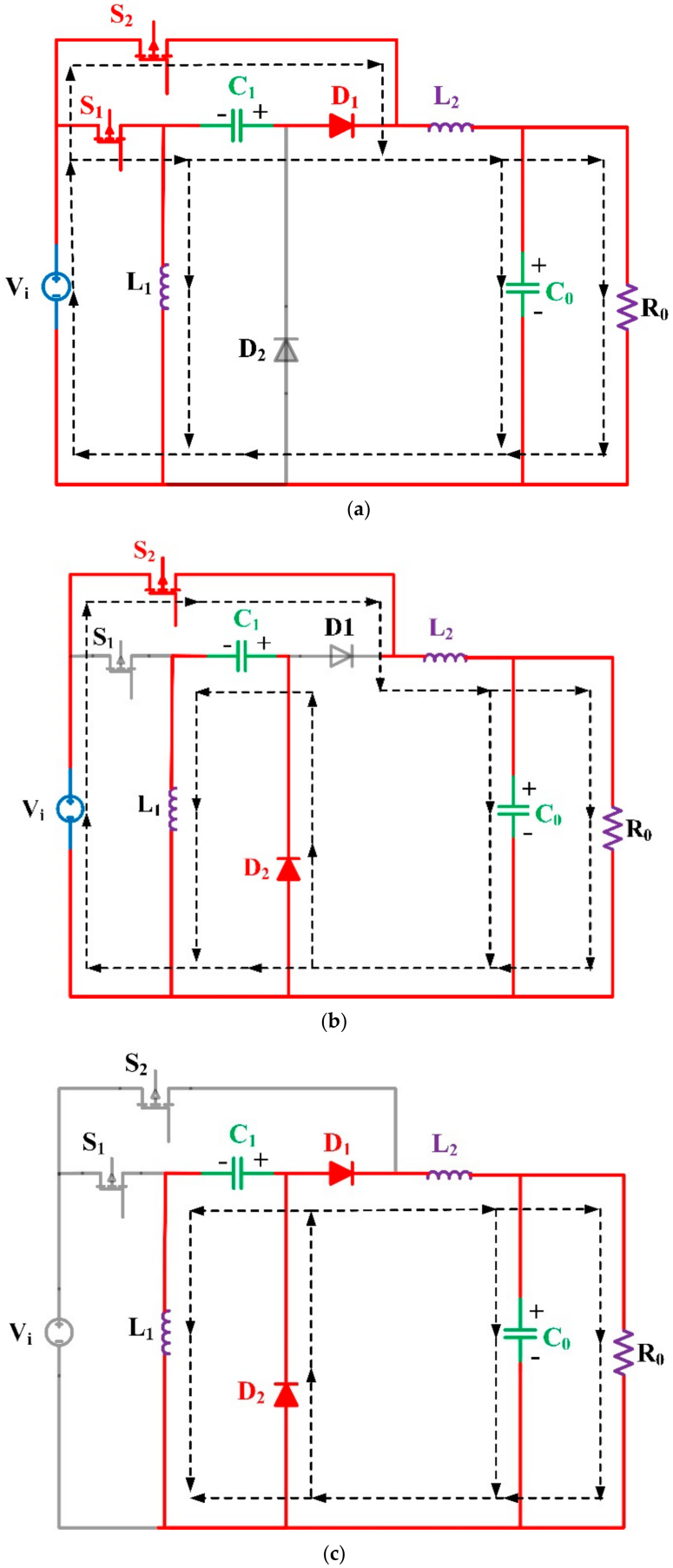


Figure 3. The proposed hybrid Zeta converter equivalent circuits. (**a**) Mode-1 (**b**) Mode-2 (**c**) Mode-3.

I. **Mode-1 ($0 < t < \delta_1 T$):** In this mode Switch S_1 and S_2 are turned ON and V_i is in parallel with inductor L_1, so the voltage across inductor L_1 is equal to the V_i. L_1 is charged through V_i, and L_2 is charged through $V_i + V_{C1}$ and capacitor C_1 is discharged through $L_2 + V_0$, which are illustrated in Figure 3a. As a result, the following equations can be obtained:

$$V_{L1} = V_i \tag{1}$$

$$V_{L2} = V_i + V_{C1} - V_0 \tag{2}$$

II. **Mode 2 ($\delta_1 T < t < \delta_2 T$):** Switch S_1 is turned OFF, while switch S_2 is switched ON in this mode. L_1 is discharged through V_{C1}, L_2 is charged through V_i, and capacitor C_1 is charged through L_1 as illustrated in Figure 3b. The inductor voltages can be computed as

$$V_{L1} = -V_{C1} \tag{3}$$

$$V_{L2} = V_i - V_0 \tag{4}$$

III. **Mode-3 ($\delta_2 T < t < T$):** In this mode, two switches are turned OFF. L_1 is discharged through V_{C1}, and L_2 is discharged through V_0, and capacitor C_1 is charged through L_1 as in Figure 3c. The inductor voltages can be computed as

$$V_{L1} = -V_{C1} \tag{5}$$

$$V_{L2} = -V_0 \tag{6}$$

2.2. Steady-State Analysis of the Converter

2.2.1. Voltage Gain Analysis

Implementing the volt-second balance equation to the inductor L_1 yields the voltage of the capacitor V_{C1}.

$$\frac{1}{T}\left(\int_0^{\delta_1} V_i dt + \int_{\delta_1}^{\delta_2} -V_{C1} dt + \int_{\delta_2}^{T} -V_{C1} dt\right) = 0 \tag{7}$$

After simplifying Equation (7), the average value of V_{C1} can be determined as

$$\frac{\delta_1 V_i}{(1-\delta_1)} = V_{C1} \tag{8}$$

Using a volt-second balance equation on inductor L_2, the following voltage gain can be obtained:

$$\frac{1}{T}\left(\int_0^{\delta_1} (V_i + V_{C1} - V_0) dt + \int_{\delta_1}^{\delta_2} (V_i - V_0) dt + \int_{\delta_2}^{T} (-V_0) dt\right) = 0 \tag{9}$$

After simplifying Equation (9), the voltage gain can be determined as

$$\frac{V_0}{V_i} = \left(\frac{\delta_1^2}{1-\delta_1} + \delta_2\right) \tag{10}$$

2.2.2. Dynamic Modelling

It is important to analyze the converter performance in transient mode, which can be accomplished through dynamic modeling of the converter. This modeling can be used to achieve converter stability around the operating point. As stated in the aforementioned section, the converter works in three different operating modes. For each operating mode, dynamic simulation is derived using a state-space model. The converter state variables are

i_{L1}, i_{L2}, V_{C0}, and V_{C1}. Because the state variables are controlled by two duty cycles δ_1 and δ_2, the state-space average model can be expressed as

$$L_1 \frac{di_{L1}}{dt} = \delta_1 V_i + (1 - \delta_1)(-V_{C1}) \tag{11}$$

$$L_2 \frac{di_{L2}}{dt} = \delta_2 V_i + \delta_1 V_{C1} - V_0 \tag{12}$$

$$C_1 \frac{dV_{C1}}{dt} = (1 - 2\delta_1) i_{L1} + i_{in} 2\delta_1 \tag{13}$$

$$C_0 \frac{dV_{C0}}{dt} = i_{L2} - \frac{V_0}{R_0} \tag{14}$$

According to small-signal modeling, duty cycles and state variables are divided into two parts: steady state values (X, D) and perturbations ($\widetilde{X}$,$\widetilde{d}$) as shown below:

$$x = \widetilde{X} + \widetilde{x},\ d = \widetilde{D} + \widetilde{d} \tag{15}$$

The perturbations are thought to be much smaller than the steady-state values. The converter's small signal model can be formed by substituting Equation (15) into Equations (11)–(14), and is represented in matrix form as:

$$\dot{\widetilde{x}} = A\widetilde{x} + B\widetilde{u} \tag{16}$$

$$\widetilde{y} = C\widetilde{x} + D\widetilde{u} \tag{17}$$

$$A = \begin{bmatrix} 0 & 0 & \frac{1-\hat{\delta_1}}{L_1} & 0 \\ 0 & 0 & \frac{\hat{\delta_1}}{L_2} & \frac{-1}{L_2} \\ \frac{1-2\hat{\delta_1}}{C_1} & 0 & 0 & 0 \\ 0 & \frac{1}{C_0} & 0 & -\frac{1}{R_0 C_0} \end{bmatrix};\ B = \begin{bmatrix} \frac{V_i + V_{C1}}{L_1} & 0 \\ \frac{V_{C1}}{L_2} & \frac{V_i}{L_2} \\ \frac{-i_{L1}}{C_1} & 0 \\ 0 & 0 \end{bmatrix};\ C = \begin{bmatrix} 0 & 1 & 0 & -1 \end{bmatrix};\ D = 0 \tag{18}$$

$$\widetilde{X} = \begin{bmatrix} \widetilde{i}_{L1} \\ \widetilde{i}_{L2} \\ \widetilde{v}_{C1} \\ \widetilde{v}_{C0} \end{bmatrix};\ \widetilde{u} = \begin{bmatrix} \widetilde{\delta}_1 \\ \widetilde{\delta}_2 \end{bmatrix}; \tag{19}$$

where A is the state matrix, B is the input matrix, C is the output matrix, D is the feedforward matrix, $\widetilde{X}$ is the state vector, and $\widetilde{u}$ is the output vector.

The converter stability is provided by the eigenvalue of a matrix 'A'. The matrix 'A' values are calculated based on the maximum range of duty ratios, as shown in Figure 4.

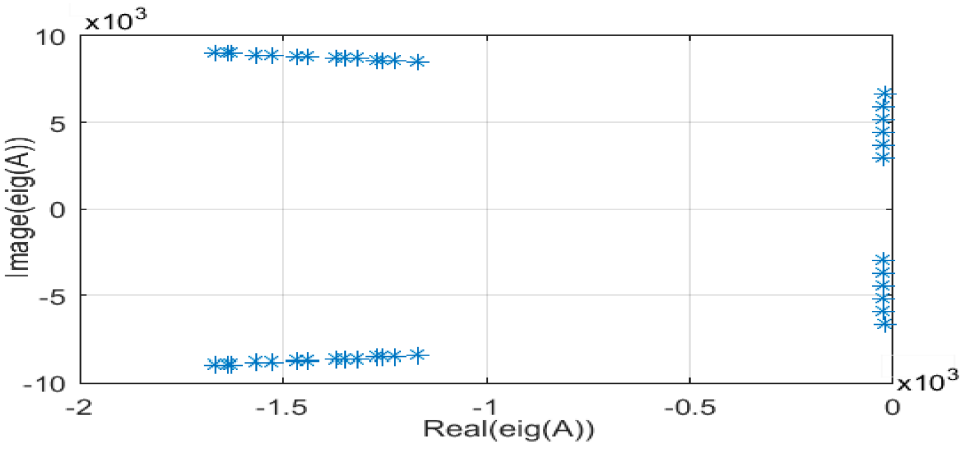


Figure 4. The Eigenvalues of matrix 'A'.

Figure 4 shows that the eigenvalues of a matrix 'A' are negative real and imaginary, so it is implied that the converter is stable for the maximum duty range.

2.3. Passive Component Design and Efficiency Calculation

The components must be carefully chosen to achieve an optimal converter design. Additionally, the discontinuous conduction mode (DCM) converter has several disadvantages, including poor dynamic behavior relying on switching frequency, output power rating, and inductor rating. Therefore, the converter must be built to function in continuous conduction mode (CCM) mode [20]. As a result, the main equations are presented here for the proposed converter under the CCM operation.

2.3.1. Inductor Design

The duty cycle, switching frequency (f_s) and the load resistor (R_0) rating are influence the evaluation of converter inductors. The minimum value of two inductors is computed using the Equations (20) and (21).

$$L_{1min} > \frac{(1-\delta_1)^2 R_0}{2f} \tag{20}$$

$$L_{2min} > \frac{(1-\delta_2) R_0}{2f} \tag{21}$$

2.3.2. Capacitor Design

The capacitor's internal resistance is assumed to be zero. The capacitor's value is reliant on the input voltage (V_i), duty cycle, switching frequency (f_s), voltage ripple voltage ripple (ΔV_c), and can be calculated as

$$C_1 = \frac{\delta_1 V_i}{(1-\delta_1)\Delta V_c f_s} \tag{22}$$

$$C_0 = \frac{\delta_2 V_i}{8\Delta V_c f_s{}^2 L_2} \tag{23}$$

2.3.3. Efficiency Calculations

The proposed converter's efficiency can be estimated from Equation (24):

$$\%\eta = \frac{P_0}{P_0 + P_{losses}} \tag{24}$$

Total power losses and converter efficiency are calculated by calculating the individual power losses of each component in the circuit.

$$P_{losses} = P_{L\_losses} + P_{Ca\_losses} + P_{D\_losses} + P_{Co\_losses} + P_{SW\_losses} \tag{25}$$

The inductor losses (P_{L_losses}), capacitor losses (P_{Ca_losses}), diode losses (P_{D_losses}), conduction losses of the switch (P_{Co_losses}), and switching losses of the switch (P_{SW_losses}) are considered in the losses equation.

The following equation can be used to calculate switching losses:

$$P_{SW\_losses} = (E_{on} + E_{off}) f_s \tag{26}$$

The conduction losses of active power switches are computed in both operating modes using Equation (27).

$$P_{Co\_losses} = V_{CE} I_{C(avg)} + R_c I^2_{c(rms)} \tag{27}$$

where R_c is the conduction resistance of the power switch.

The diode's power losses can be computed as follows:

$$P_{D\_losses} = R_D I^2_{D(rms)} + V_f I_{D(avg)} \quad (28)$$

where R_D and V_f are the forward resistance of the diode and forward voltage, respectively.

The inductor power losses are divided into two parts: copper losses caused by the winding internal resistance (R_L) and core losses caused by hysteresis of the magnetic core, ripple flux density, and eddy currents. The copper losses of two inductors as follows:

$$P_{L\_losses} = R_{L1} I^2_{L1(rms)} + R_{L2} I^2_{L2(rms)} \quad (29)$$

Internal resistance causes power losses in the capacitor (R_{c1}). The following formula can be used to calculate total capacitor losses:

$$P_{Ca\_losses} = R_{C1} I^2_{C1(rms)} + R_{C2} I^2_{C2(rms)} + R_{C3} I^2_{C3(rms)} \quad (30)$$

2.4. Comparison with Other Topologies

The proposed converter is comparable with the classical Zeta, KY, and the converters described in [12,19,21]. Table 1 illustrates the validation of the proposed converter's capabilities in terms of voltage gain and component count. The proposed converter outperforms the converters reported in [12,21], and the conventional Zeta converter in terms of voltage gain. The voltage gain versus duty cycle for several buck-boost converters is illustrated in Figure 5. Furthermore, the proposed converter contains fewer components than the converters described in [18,19]. The proposed converter also provides a constant input current, making it more appropriate for applications of fuel cells and renewable energy sources.

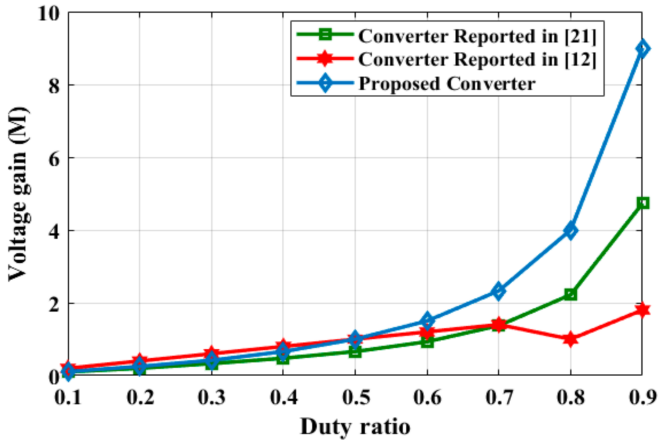


Figure 5. Voltage gain comparison of the proposed converter and similar converters.

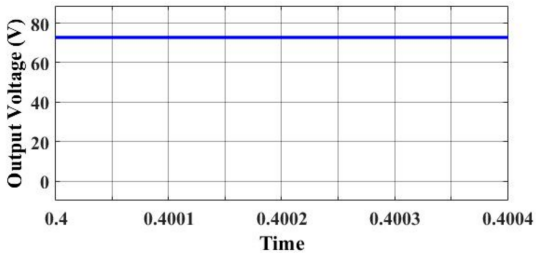
Table 1. An overview of the proposed converter's performance compared to existing converters.

Converter Topology	Proposed Converter	Reported in [12]	Reported in [21]	Reported in [18]	Traditional Zeta Converter
Number of switches	2	2	1	1	1
Number of diodes	2	1	3	3	1
Number of inductors	2	2	2	3	2
Number of capacitors	2	3	2	5	2
Total component count	8	8	8	12	6
Input current	Continuous	Continuous	Continuous	Discontinuous	Continuous
Voltage gain	$(\frac{\delta^2_1}{1-\delta_1} + \delta_2)$	2δ	$\frac{\delta}{1-\delta^2}$	$\frac{-3\delta}{1-\delta}$	$\frac{\delta}{1-\delta}$

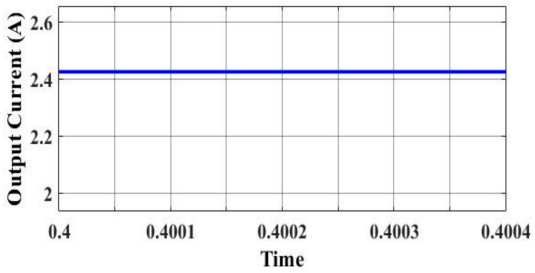
3. Results

The proposed converter was tested using both simulations and experimental methods. The OPAL-RT 5700 HIL set-up was used to assess the analytical results. This section provides the simulation and HIL results of the hybrid zeta converter in step-up and step-down operation modes. To evaluate the capability of the converter, it was first simulated in MATLAB/Simulink software. Table 2 shows the components that were employed in both simulation and HIL mode. The inductor and capacitor values have been selected based on the Equations (20)–(23). The simulation waveforms of the proposed hybrid zeta converter in step-up are displayed in Figure 6. Figure 6a illustrates the simulation output voltage waveform of the converter. It is in step-up mode from 36 V to 72 V with a duty cycle of 65% for switch S_1 and 79% for S_2. The obtained simulated value of 72 V is almost equal to the theoretical value obtained from Equation (10). The theoretical output current of the proposed converter for the load of 30 Ω is 2.5 A, which is obtained from the equation (V_0/R_0). The simulated output current is 2.4 A, and it is illustrated in Figure 6b. During the time interval $\delta_1 T$, the inductor L_1 is associated in parallel to the input source and the current across the inductor increases to the maximum value of 6.4 A, for the remaining time the inductor is connected parallel to the capacitor C_1. The current across the inductor decreases linearly and reaches its minimum value of 3.1 A.

Similarly, during the time interval $\delta_2 T$, inductor L_2 is connected in series to the input source and the current across the inductor increases to a maximum value of 3.1 A for remaining time the inductor is connected to the load while the current across the inductor decreases linearly and reaches its minimum value of 1.8 A. The average inductor current across i_{L1} and i_{L2} are 5.7 A and 2.8 A, respectively. Figure 6c,d demonstrated that the converter works in continuous conduction mode. During the time interval $\delta_1 T$, the capacitor C_1 is connected in parallel to the inductor L_1, so the capacitor discharges its energy and reaches its minimum value and the remaining time, the capacitor charges via inductor L_1 reaching its maximum value of 65 V. Figure 6e, shows the average capacitor value of step-up mode.

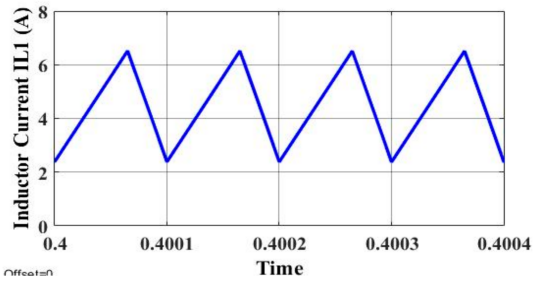


(**a**)

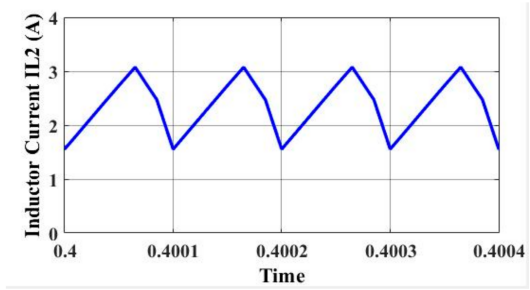


(**b**)

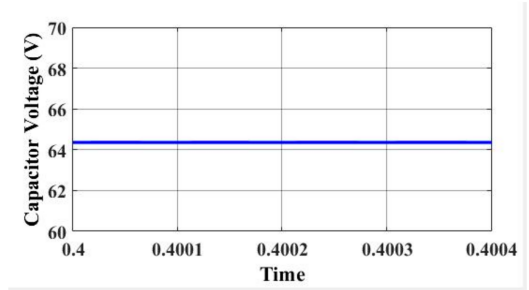
Figure 6. *Cont.*



(**c**)



(**d**)

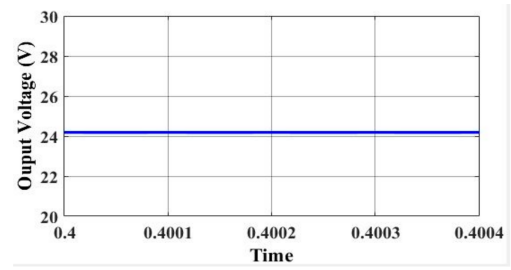


(**e**)

Figure 6. Output wave forms of step-up mode. (**a**) Output voltage, (**b**) output current, (**c**) inductor current (I_{L1}), (**d**) inductor current (I_{L2}), and (**e**) capacitor voltage (V_{C1}).

As for step-up operation mode, Figure 7 displays the simulation results of the proposed hybrid Zeta converter in step-down operation mode. The simulated output voltage of the converter in a step-down mode for the input voltage of 36 V is 22.5 V, as shown in Figure 7a. The theoretical voltage obtained from Equation (10) is 25 V for the duty cycle of 33%. Figure 7b shows the proposed hybrid converter output current with the value of 2 A. During the time interval $\delta_1 T$, the inductor L_1 is linked in parallel with the input source and the current across the inductor increases to the maximum value of 2 A. In the remaining time the inductor is connected in parallel to the capacitor C_1 and the current across the inductor is decreases linearly and reaches its minimum value of 0.5 A.

Similarly, the inductor L_2 is connected in series to the input source at the interval of time δ_2. The current across the inductor increases to the maximum value of 2.2 A, and the remaining time the inductor is associated in series to the load and the current across the inductor decreases linearly and reaches its minimum value of 0.4 A. The average inductor current across the two inductors i_{L1} and i_{L2} is 1.7 A. Figure 7c,d highlight the converter working in continuous conduction mode. During the time interval $\delta_1 T$, the capacitor C_1 is connected in parallel to the inductor L_1. During this time, the capacitor discharges its energy and reaches to minimum value and the capacitor charges via inductor L_1 reaching its maximum value of 18 V. Figure 7e, shows the average capacitor value of step-down operation mode at 17 V.



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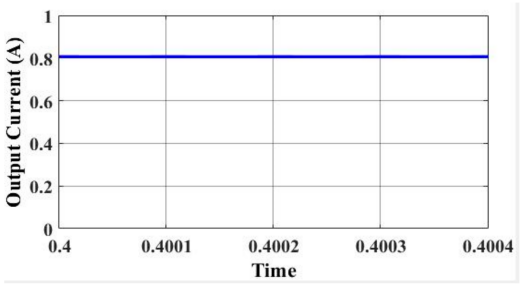

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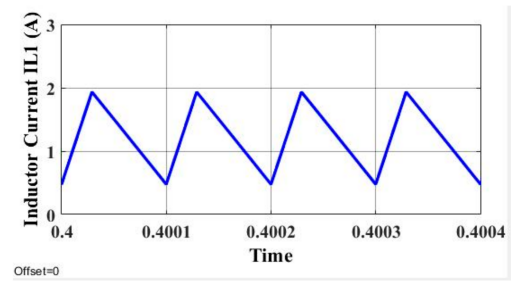

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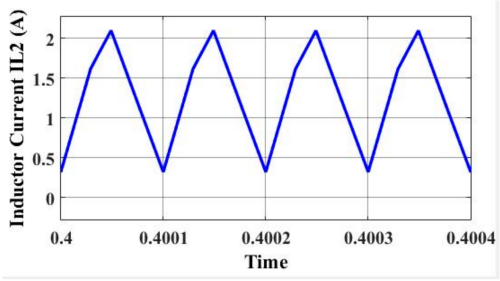

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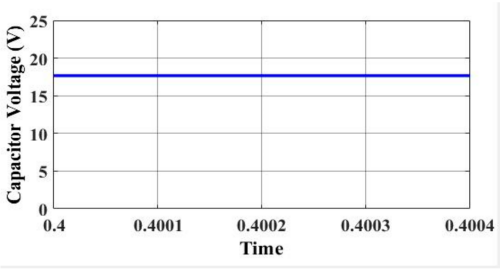


(**e**)

Figure 7. Output wave forms of step-down mode. (**a**) Output voltage, (**b**) output current, (**c**) inductor current (I_{L1}), (**d**) inductor current (I_{L2}), and (**e**) capacitor voltage (V_{C1}).

Table 2. The proposed converter's component specification.

Components	Range
Inductor L_1	1 mH, R_L = 35 m Ω
Inductor L_2	1 mH, R_L = 40 m Ω
Capacitor C_0	10 µH, R_L = 0.051 Ω
Capacitor C_1	100 µH, R_L = 0.02 Ω
V_{in}, f	36 V, 10 KHz

HIL systems are widely used in engineering for real-time simulation pre-prototyping tests. HIL stacks are capable of quickly creating and synchronising prototypes. The machine and controller are installed in OPAL-RT to allow the system to run at the current clock time. The high-speed nano- to microsecond OPAL-RT sample speed makes this a real-time dynamic system. The digital simulator (RTDS) commands for the RT-LAB are controlled by the user PC. The RT-LAB OP-5700 is used to edit, build, load, and execute the prototype. Table 3 addresses the HIL stack specifications as well as the capacity to run real-time systems. With a power rating of 173 W, the proposed hybrid Zeta converter was tested in CCM mode in both operational modes.

The HIL results were tested using the RT-LAB OP5700 HIL simulator, which consists of the programmable control board (PCB-E06-0560), DSO-X 3014A. The PCB can be used to exchange data between the simulation and real controllers via analogue outputs and digital inputs. The real-time results configuration of test bench is shown in the Figure 8.

Table 3. Specifications of the OP-5700 HIL simulator.

Name of the Device	OP5700 Simulator
FPGA	Xilinx®Virtex®7 FPGA on VC707 board Processing speed : 200 ns–20 µ s
I/O Lines	256 lines, routed to eight analog or digital, 16 or 32 channels
High-Speed Communication Ports	16SFP sockets, up to 5 GBps
I/O Connectors	Four-panel of 4 DB37 connectors
Monitoring Connectors	Four-panel of RJ45 connectors
PC Interface	Standard PC connectors
Power Rating	Input: 100-240VAC, 50–60 Hz, 10/5 A Power: 600 W

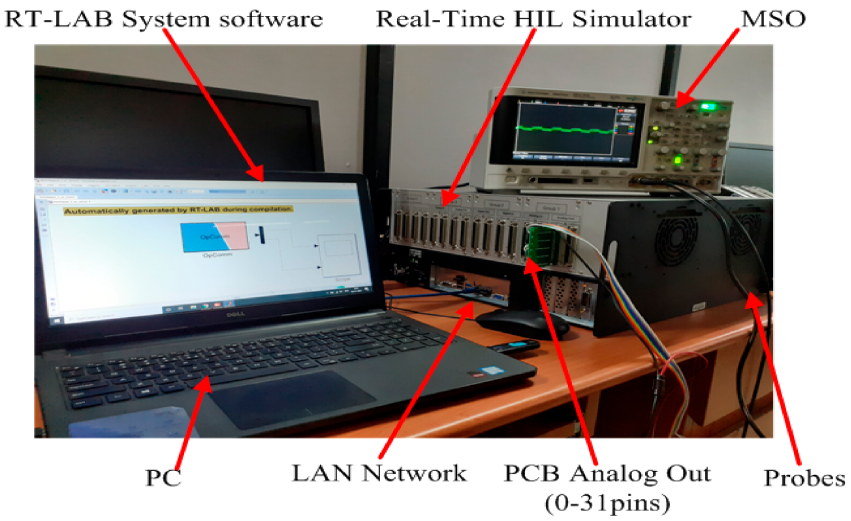
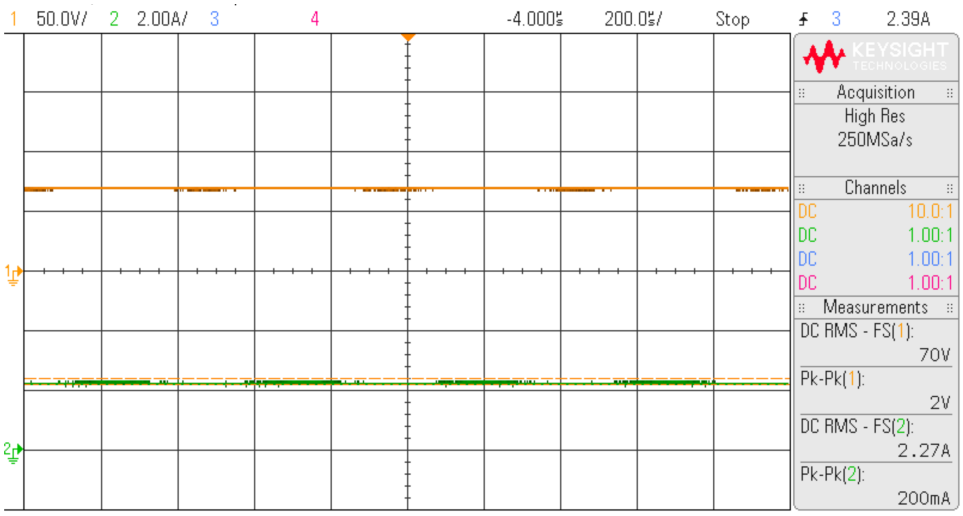
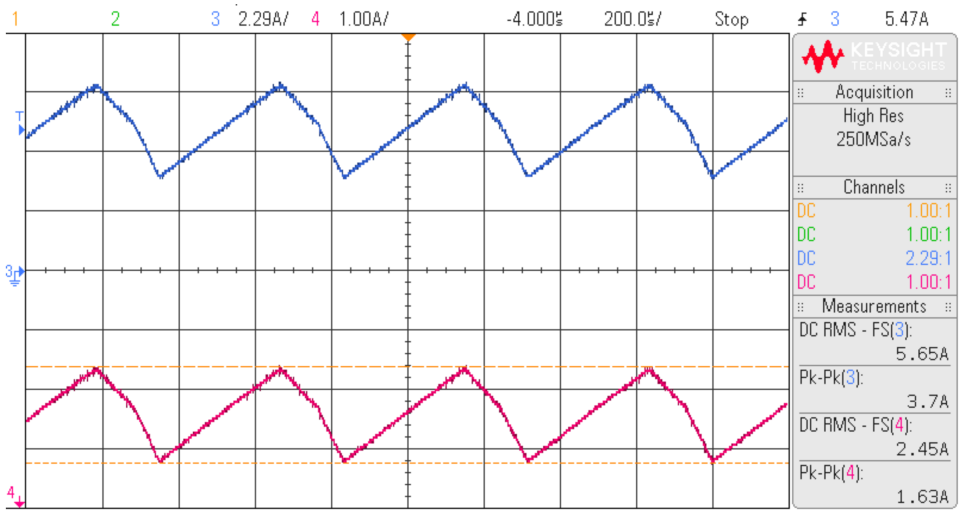


Figure 8. HIL experimental set-up of the proposed Zeta converter.

Figure 9a depicts the HIL test output voltage waveform of the converter, which has a step-up from 36 V to 72 V with a duty cycle of 65% for switch S_1 and 79% for switch S_2. The obtained HIL test voltage value was 70 V, which is nearly identical to the MATLAB/Simulink result value obtained from Equation (10). The proposed converter's theoretical output current for a load of 30 Ω is 2.5 A, as calculated by the equation (V_0/R_0). The HIL test output current was 2.27 A, as shown in Figure 9b. The inductor L_1 was connected in parallel to the input source during the time interval $\delta_1 T$. As a result, the current across the inductor increased to a maximum of 5.65 A, and the inductor was connected in parallel to the capacitor C_1 for the rest of the time. The current across the inductor decreased linearly until it reached its minimum value of 3.7 A. Similarly, inductor L_2 was connected in series to the input source during the time interval $\delta_2 T$. As a result, the current across the inductor rose to a maximum of 2.45 A. The rest of the time the inductor was connected to the load, so the current across the inductor decreased linearly until it reaches its minimum value of 1.63 A. The average inductor currents across i_{L1} and i_{L2} were 4.68 A and 2.04 A, respectively. Figure 9b shows that the converter operates in continuous conduction mode. During the time interval $\delta_1 T$, the capacitor C_1 was connected in parallel to the inductor L_1, causing the capacitor to discharge its energy and reach its minimum value of 64 V, as shown in Figure 9c.

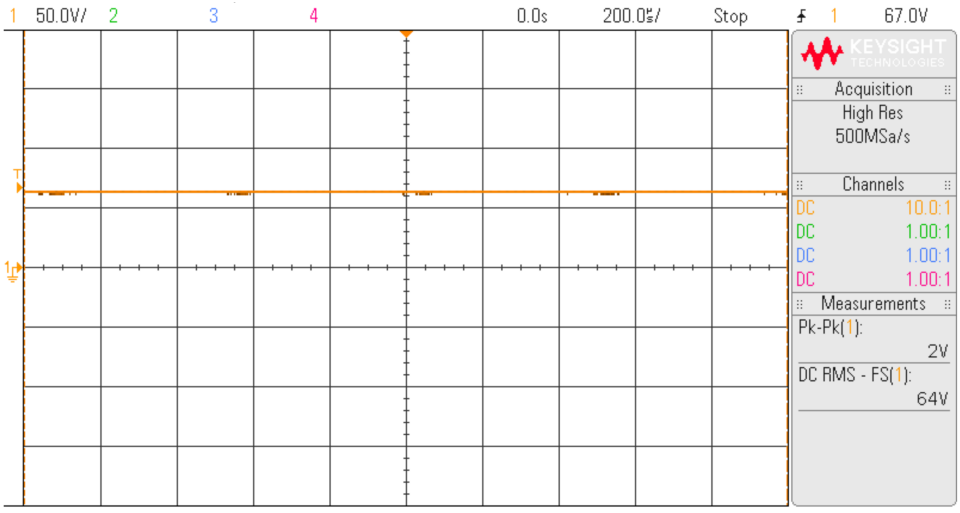


(**a**)



(**b**)

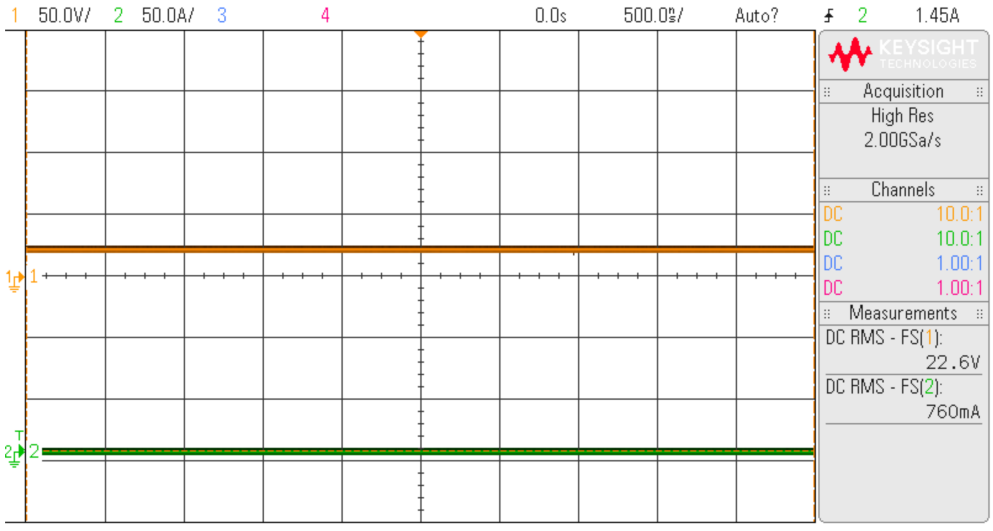
Figure 9. *Cont.*



(**c**)

Figure 9. Output wave forms of step-up mode. (**a**) Output voltage and output current, (**b**) voltage across inductors (I_{L1} and I_{L2}), and (**c**) capacitor voltage (V_{C1}).

Figure 10 shows the HIL results of the proposed hybrid zeta converter in step-down operation mode. As shown in Figure 10a, the experimental output voltage of the converter in step-down mode for a 36 V input voltage was 22.6 V. For a duty cycle of 33%, the theoretical voltage obtained from Equation (10) is 25 V. Figure 10b depicts the proposed hybrid converter output current of 760 mA. The inductor L_1 was connected in parallel with the input source during the time interval $\delta_1 T$. As a result, the current across the inductor reached a maximum of 1.61 A, and the inductor was connected in parallel to the capacitor C_1 for the rest of the time. As a result, the current across the inductor decreased linearly. Similarly, at time interval $\delta_2 T$, the inductor L_2 was connected in series to the input source. The current across the inductor increased to its maximum value of 1.63 A, and the inductor remained connected in series to the load for the rest of the time, so the current across the inductor decreased linearly. The average inductor current across the two inductors i_{L1} and i_{L2} was 1.61 A. Figure 10b confirms that the converter operates in continuous conduction mode. The capacitor C_1 was connected in parallel to the inductor L_1 during the time interval $\delta_1 T$, so the capacitor discharged its energy and reached its minimum value. Figure 10c depicts the average capacitor value in the step-down operation mode at 14 V.



(**a**)

Figure 10. *Cont.*

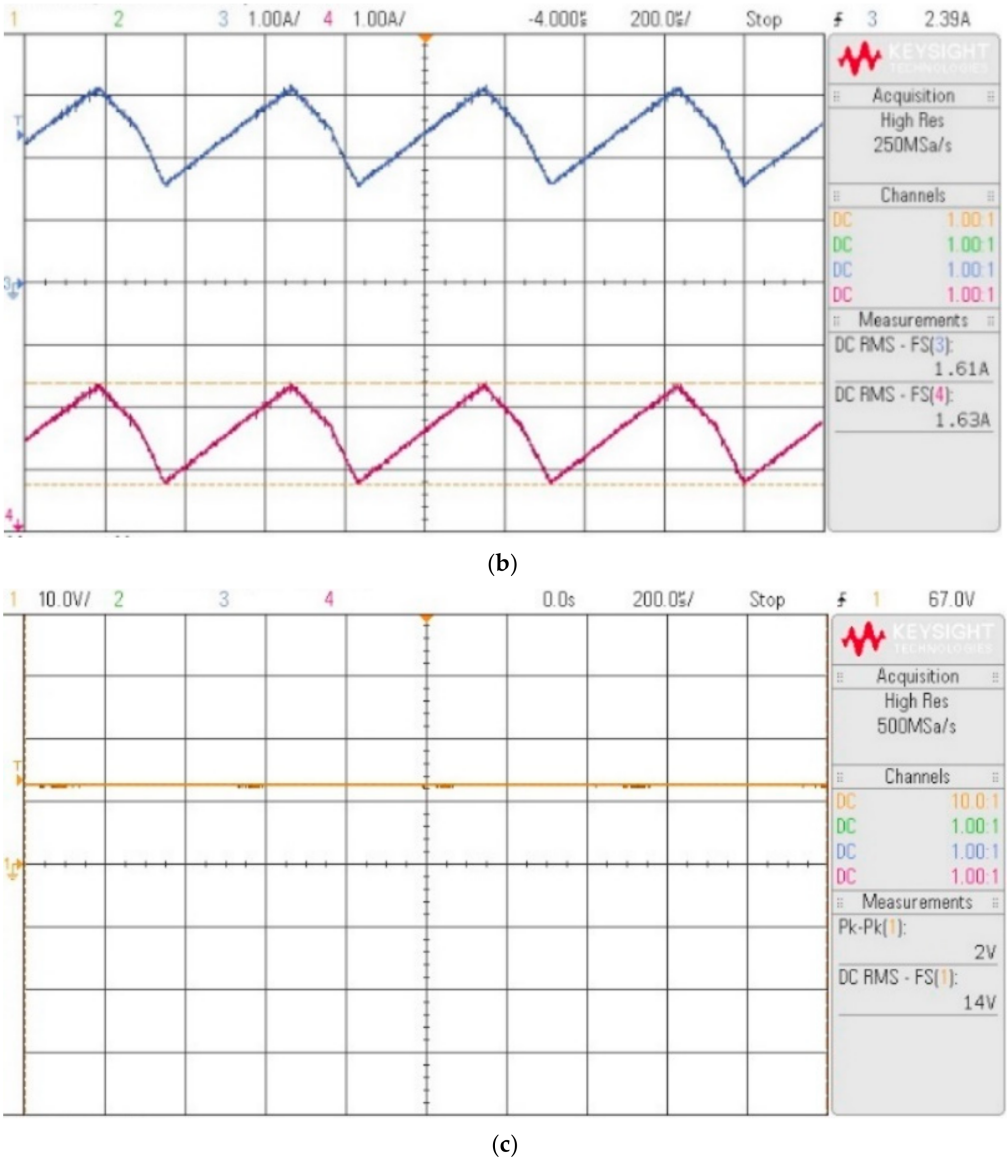


Figure 10. Output waveforms of step-down mode. (**a**) Output voltage and output current, (**b**) inductor voltage (I_{L1} and I_{L2}), and (**c**) capacitor voltage (V_{C1}).

However, the proposed converter also has a few limitations, as shown in Table 4.

Table 4. Limitations of the proposed converter.

Limitations
• All semiconductor devices, such as MOSFETS and diodes are considered ideal. Otherwise, the voltage gain reduces. • The ripple current in the load is more for the proposed zeta converter than for the conventional SEPIC converter. • A buck controller is required to drive the high speed PMOS. Therefore, for implementation of closed loop operation there is more complexity. • High input voltage ripple.

Figure 11 illustrates the converter efficiency curves and loss distribution in the step-up and step-down converters. The step-up converter was more efficient than the step-down converter, as illustrated in Figure 11a. In step-up mode, the proposed converter achieved a maximum efficiency of 95.2%. Furthermore, Figure 11b depicts the power loss distribution

of every element in the proposed converter in both operating modes. From the calculated values, the proposed converter diode losses have a more major influence on converter performance.

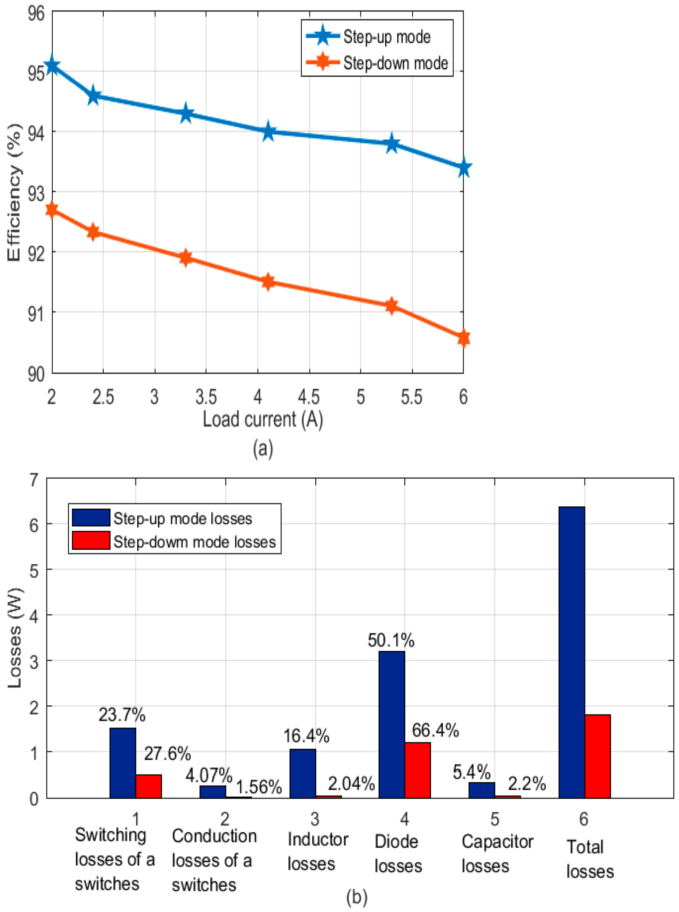


Figure 11. Efficiency and loss distributions. (**a**) Efficiency curve and (**b**) losses distributions under V_0 = 72 v, P_0 = 173 W.

4. Conclusions

A non-isolated hybrid Zeta converter was proposed in this paper. The proposed converter achieves high voltage gain without using a coupled inductor or an isolated transformer. Furthermore, the converter has a compact design and generates a high output voltage with minimal duty cycle for both step-up and step-down operation modes. In the CCM mode, the performance analysis of the converter in both step-up and step-down modes has been explained. The schematic representation, converter analysis, small signal-modelling, and design process were addressed. To determine the performance characteristics of the proposed hybrid Zeta converter, a comparison was made with other non-isolated DC-DC switch-mode converters. The dynamic modeling of the proposed converter was described in detail to determine its stability. In addition, the proposed converter performance was validated using MATLAB/ Simulink software program and HIL testing experimental method.

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