

Article

Broadband Class-J GaN Doherty Power Amplifier

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Abstract: This paper presents a broadband 3–3.7 GHz class-J Doherty power amplifier exploiting second harmonic tuning in the output network. Furthermore, the output impedance inverter is eliminated and its effect is embedded in the main device's output matching network, thus trading off among bandwidth, efficiency, and gain. The proposed amplifier adopts two 10 W packaged GaN transistors, and it achieves in measurement 60–74%, and 46–50% drain efficiency at saturation and 6 dB output back-off, respectively, with a saturated output power of 43–44.2 dBm and a small-signal gain of 10–13 dB. The proposed DPA exhibits a simulated adjacent channel power ratio less than –30 dBc at 36 dBm average output power, when a 16-QAM modulation with 5 MHz bandwidth is applied to the 3.5 GHz carrier.

Keywords: back-off; class-J; Doherty power amplifier; GaN HEMT; high efficiency; linearity



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1. Introduction

Due to the increasingly growing demand for wireless communication systems with high quality and high data rates, the radio frequency (RF) transceiver is being pushed to operate at higher frequencies and wider bandwidths, and with modulation schemes characterized by high Peak-to-Average Power Ratios (PAPRs). The power amplifier (PA) strongly affects the performance of the transmitter [1–3], and thus it should operate as efficiently as possible over wide bandwidths, maintaining a sufficient level of linearity, which is especially challenging for 5G systems, based on Orthogonal Frequency Division Modulation (OFDM). OFDM signals have a varying envelope and high PAPR of the order of 10 dB to 12 dB for aggregated multicarrier signals [4], thus making the design of a PA that operates efficiently over wide dynamic and frequency ranges a critical challenge [5–9]. Crest Factor Reduction or Selected Mapping techniques [10,11] are normally adopted to reduce the PAPR of these signals to the 6 dB to 8 dB range, hence mitigating the negative effects of very high PAPR on the PA efficiency.

Nonetheless, in conventional PA architectures, the efficiency drops significantly when output power decreases with respect to its maximum value, where the efficiency is also maximum. This being a major drawback for non-constant envelope modulations, the efficiency enhancement in back-off has been addressed resorting to various techniques. These belong to two main categories, namely those based on supply modulation, such as envelope elimination restoration [12,13] and envelope tracking [14–16], and those exploiting load modulation [17]. The Doherty architecture [18–20], the Chireix outphasing [21–23], and the Load Modulated Power Amplifier (LMBA) [24,25] belong to the latter category. Among these PA architectures, the Doherty PA (DPA) has had a significant success thanks to its simplicity and ease of implementation in single-RF-input form, with a comparatively good intrinsic linearity [26]. Dual input DPAs have indeed also been explored [27–29],

demonstrating superior performance compared to their single-input counterparts, but their appeal for real-field applications remains questionable due to the higher system complexity and cost.

One of the main challenges in the design of DPAs is achieving very wide bandwidths, which is hindered by several factors [30,31], among which it is worth mentioning the quarter wavelength transmission line that is used as an impedance inverting network (IIN) between the main device and the common node, the reactive parasitic effects of the active devices, and the possible presence of offset lines or narrowband post-matching networks.

Moreover, in order to enhance PA performance, harmonic tuning techniques have been considered so far [32–34], but most of them suffer from bandwidth limitations. The class-J PA shows wide bandwidth compared to other harmonic-tuned PAs [35–37], while its sensitivity to harmonics of the matching network is lower than class F [38,39].

In this paper, a wideband class-J DPA with high efficiency and linearity is designed using the CGH40010F GaN HEMT from Wolfspeed, targeting operation around 3.5 GHz, which is of interest for sub-6 GHz 5G applications.

The novelty of the proposed DPA is twofold: on one hand, the removal of the IIN on the main path and the embedding of the impedance inversion in the output matching network (OMN) improves the bandwidth, and on the other hand, the exploitation of the effect of the second harmonic allows us to keep gain and efficiency high over a 700 MHz bandwidth. The implemented class-J DPA achieves, in continuous wave (CW) measurement conditions, saturated and 6 dB output power back-off (OBO) efficiency of 60–74% and 46–50%, respectively, with an associated saturated output power of 43–44.2 dBm over the 3–3.7 GHz frequency range.

The structure of the paper is the following. In Section 2, the theory underlying the Doherty and class-J operation is discussed, and it is then applied to the proposed PA design in Section 3. Section 4 reports the simulation results, including linearity assessment. The measurement results are shown in Section 5, and finally, conclusions are drawn in Section 6.

2. Theoretical Analysis

This section reviews the theoretical foundations of the Doherty and class-J amplifiers, explaining how these concepts are exploited for the design of the proposed class-J DPA.

2.1. Doherty PA

The block diagram of a conventional class AB-C DPA is shown in Figure 1a, where the transistors are replaced by a simplified model composed of an ideal current generator and an output LC network, representing the reactive parasitic effects in the band of interest. In this work, two CGH40010F packages GaN HEMTs are adopted, whose parasitic elements are considered to be $C_p = 1.27$ pF and $L_p = 0.73$ nH [40].

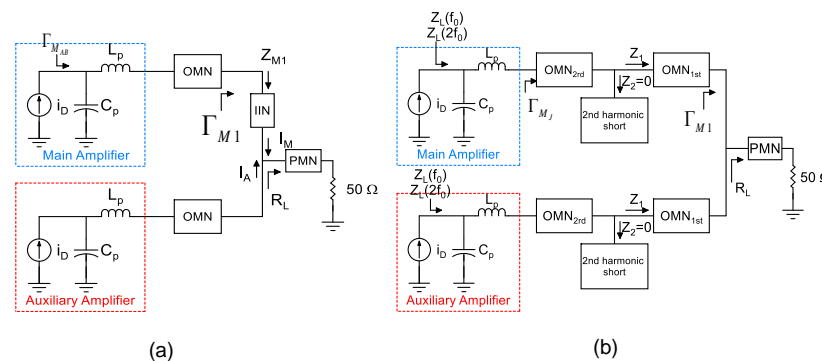


Figure 1. Schematic diagram of the (a) conventional DPA. (b) Proposed Class-J DPA.

The ideal scattering parameters of the cascade of the output parasitics of the device and its output matching network (OMN) are expressed as follows [41]:

$$A = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & e^{j\phi} \\ e^{j\phi} & 0 \end{bmatrix} \tag{1}$$

where ϕ is the phase of S_{21} , and the network is assumed lossless. Therefore, the load reflection coefficients at the intrinsic drain terminal of the main device can be expressed as [41]:

$$\Gamma_{M_{AB}} = S_{11} + \frac{S_{12}S_{21}\Gamma_{M1}}{1 - S_{22}\Gamma_{M1}} = \Gamma_{M1}e^{j2\phi} \tag{2}$$

where Γ_{M1} is the reflection coefficient before the IIN (a quarter wavelength line with characteristic impedance equal to R_{opt}) and it is expressed as:

$$\Gamma_{M1} = \frac{Z_{M1} - R_{opt}}{Z_{M1} + R_{opt}} \tag{3}$$

where R_{opt} represents the intrinsic optimum load of the class-AB main device, and Z_{M1} is derived as follows:

$$Z_{M1} = R_{opt}(2 - x) \tag{4}$$

The parameter x is the ratio between auxiliary and main current ($x = I_A/I_M$), and the common node impedance is assumed to be equal to $R_{opt}/2$. Substituting (3) and (4) into (2) leads to

$$\Gamma_{M_{AB}} = \frac{R_{opt}(2 - x) - R_{opt}}{R_{opt}(2 - x) + R_{opt}}e^{j2\phi} = \frac{1 - x}{3 - x}e^{j2\phi}. \tag{5}$$

As shown in (5), $\Gamma_{M_{AB}}$ is a function of x and θ . The presence of the IIN and the fact that the impedance at the common node of the Doherty combiner changes with frequency, limit the bandwidth of the DPA [42]. A possible solution to mitigate this issue is to remove the $\lambda/4$ line acting as IIN and designing the OMN of the main device so as to perform the impedance inversion required by the Doherty load modulation [32].

Furthermore, a conventional class AB-C DPA only considers the load at the fundamental frequency f_0 , and assumes a short-circuit termination at all higher harmonics. Since properly terminating the higher harmonics can significantly improve performance, in this design the OMNs have been designed to operate the devices in class J.

2.2. Class-J PA

The waveforms of the intrinsic drain current (i_D) and drain-source voltage (v_{DS}) of a class-J amplifier are described by the following equations [38]:

$$i_D(\omega t) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2} \cos(\omega t) + \frac{2I_{max}}{3\pi} \cos(2\omega t) \tag{6}$$

$$v_{DS}(\omega t) = V_{DD} + (V_{DD} - V_K) \cos(\omega t) - \alpha(V_{DD} - V_K) \sin(\omega t) - 0.5\alpha \sin(2\omega t) + \dots \tag{7}$$

where I_{max} is the maximum current of the transistor, V_K is its knee voltage, V_{DD} is its supply voltage, and α is the empirical coefficient representing the reactive component of a class-J load, and it assumes values between -1 and $+1$.

By using Equations (6) and (7), the intrinsic impedance of the main device at saturation, at fundamental and second harmonic, can be derived as:

$$Z_L(f_0) = (1 + j\alpha)R_{opt} \tag{8}$$

$$Z_L(2f_0) = -j\frac{3\pi}{8}\alpha R_{opt}. \tag{9}$$

In back-off, the drain current is expressed as follows [43]:

$$i_{D,OBO}(\omega t) = \frac{1}{\gamma} \left[\frac{I_{max}}{\pi} + \frac{I_{max}}{2} \cos(\omega t) + \frac{2I_{max}}{3\pi} \cos(2\omega t) + \dots \right] \tag{10}$$

where γ is the ratio between output power at saturation and at the selected OBO point ($\gamma = P_{out,sat} / P_{out,OBO}$). Therefore, adopting (7) and (10), the main OBO impedance at the fundamental frequency can be calculated as:

$$Z_{L,OBO}(f_0) = \gamma(1 + j\alpha)R_{opt}. \tag{11}$$

The matching network design considering a variable load at both fundamental and second harmonic would be extremely difficult. Besides, in this case, the second harmonic impedance has a limited variation with power and is therefore assumed to be constant. The constant second harmonic impedance is expressed as follows:

$$Z_L(2f_0) = Z_{L,OBO}(2f_0) = Z_{L,sat}(2f_0) = -j\frac{3\pi}{8}\alpha R_{opt} \tag{12}$$

As shown in Equations (8), (9), (11) and (12), the fundamental impedance should have a resistive and a reactive component, the second harmonic impedance should be purely reactive, and the higher harmonics are assumed to be shorted at the transistor intrinsic drain plane.

3. Class-J DPA Design Strategy

In order to achieve class-J operation for the main and auxiliary devices, their OMNs, which share the same structure, are designed in a modular way: in particular, each OMN is composed of three parts, as shown in Figure 1b. A second harmonic matching network (OMN 2nd), terminated by a second harmonic short (SC 2nd), synthesizes the proper impedance at the second harmonic, then the matching network OMN 1st sets the proper load at the fundamental frequency without affecting the second harmonic. Based on Equations (3) and (8), the intrinsic main reflection coefficient at fundamental for the class-J DPA can be written as:

$$\Gamma_{Mj} = \frac{R_{opt}(2-x)(1+j\alpha) - R_{opt}e^{j2\phi}}{R_{opt}(2-x)(1+j\alpha) + R_{opt}} = \frac{(2-x)(1+j\alpha)}{(2-x)(1+j\alpha)} e^{j2\phi} \tag{13}$$

Based on Equation (13), the obtained class-J reflection coefficient is as a function of x , α , and ϕ , thus gives more degrees of freedom to design the output matching network with respect to the classical class-AB case. Figure 2 shows the impedance of class-J at the fundamental and second harmonics for $R_{opt} = 50 \Omega$. The real part of the fundamental impedance at OBO and saturation is constant, whereas the imaginary part changes from $-kR_{opt}$ to $+kR_{opt}$, where k equals 1 and 2 at saturation and at OBO, respectively.

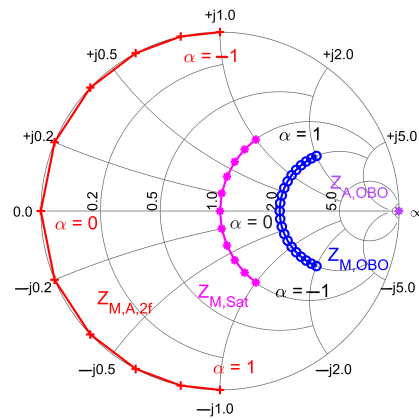


Figure 2. Intrinsic main and auxiliary impedances of the DPA class-J at the fundamental and second harmonics when $R_{opt} = 50 \Omega$.

According to Equations (6) and (7), the output power at fundamental frequency and the drain efficiency of our class-J PA are:

$$P_{outJ} = \frac{(V_{DD} - V_K)}{4} I_{max} \tag{14}$$

$$DE_J = \frac{P_{outJ}}{P_{DC}} = \frac{\frac{(V_{DD}-V_K)}{4} I_{max}}{V_{DD} \frac{I_{max}}{\pi}} = \frac{\pi}{4} \left(1 - \frac{V_K}{V_{DD}} \right) \tag{15}$$

Thus, P_{outJ} and DE_J are independent of α . The dependency of the reflection coefficient Γ_{Mj} on α hence provides a degree of freedom to design the OMN, without compromising power and efficiency. In particular, in this work the value $\alpha = 0.5$, yielding to an optimum load for class-J operation $R_{opt,J} = 1.25R_{opt}$, larger than the load resistance $2R_L$.

Differently from a conventional DPA, which adopts a quarter-wavelength transmission line as IIN, the OMN of the proposed DPA embeds the impedance inversion too, which widens the bandwidth. In this work, a low pass matching network is used, shown in Figure 3. The capacitor C_1 is representative of the parasitic drain capacitance, and the inductance L_4 is exploited as drain bias feed. The Chebyshev theory [44] is used to calculate all elements of the OMN. The optimum bandwidth is achieved when the impedance ratios are:

$$\frac{R_{opt,J}}{R_1} = \frac{R_1}{R_2} = \frac{R_2}{2R_L} \tag{16}$$

where R_1 and R_2 are calculated as:

$$R_1 = \sqrt[3]{2R_{opt,J}^2 R_L} \quad R_2 = \sqrt[3]{4R_L^2 R_{opt,J}} \tag{17}$$

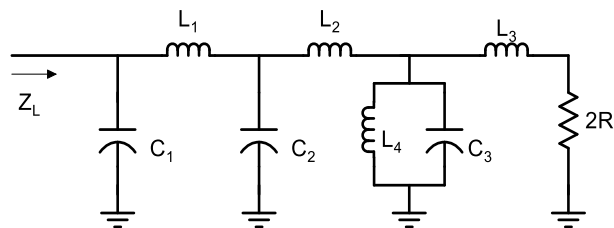


Figure 3. Low pass output matching network.

According to (16), the values of L and C of each of the three ladder networks, are given by:

$$\begin{aligned} L_1 &= \frac{Q_1 R_1}{\omega}, & L_2 &= \frac{Q_2 R_2}{\omega}, & L_3 &= \frac{2Q_3 R_L}{\omega} \\ C_1 &= \frac{Q_1}{R_{\text{opt},J}\omega}, & C_2 &= \frac{Q_2}{R_1\omega}, & C_3 &= \frac{Q_3}{R_2\omega} \end{aligned} \quad (18)$$

where Q_1 , Q_2 , and Q_3 are defined as:

$$Q_1 = \sqrt{\frac{R_{\text{opt},J}}{R_1} - 1}, \quad Q_2 = \sqrt{\frac{R_1}{R_2} - 1}, \quad Q_3 = \sqrt{\frac{R_2}{2R_L} - 1} \quad (19)$$

Since C_1 is related to the parasitic of the transistor and has a constant value, Q_1 and R_{opt} must be selected accordingly. The values of the OMN's elements obtained from Equations (16)–(19) are illustrated in Table 1 for $R_L = 25 \Omega$ and $R_{\text{opt},J} = 62.5 \Omega$.

Table 1. Values of the OMN components.

Elements	L_1	L_2	L_3	C_1	C_2	C_3
Value	0.75 nH	0.7 nH	0.6 nH	0.2 pF	0.22 pF	0.25 pF

Since the implementation of the OMN with lumped capacitors and inductors is not applicable at the frequencies of interest, due to the low-quality factor of the Surface Mount Device (SMD) inductors, the equivalent distributed form, using microstrip lines is extracted. The capacitors are replaced by open-circuited stubs, while inductors are replaced by transmission lines. In this work, a Rogers RO4350B substrate ($\epsilon_r = 3.66$, substrate height and metal thickness of 0.8 mm and 35 μm , respectively) is used. The length of the transmission lines and stubs is calculated as [44]:

$$l_{\text{line}} = \frac{\omega L}{Z_{\infty,1}\beta} \quad (20)$$

$$l_{\text{stub}} = \frac{\arctan(2\omega Z_{\infty,c}C)}{\beta} \quad (21)$$

where Z_1 and Z_c are the characteristic impedance of the line for the inductor and capacitor and β is the propagation constant. The final output matching networks for the main and the auxiliary devices are shown in Figure 4a. Figure 4b shows the simulated internal output impedance of the main and auxiliary transistor, for the fundamental and second harmonic at saturation and at 6 dB OBO. As can be noted, the second harmonic impedance is constant in both cases, while the fundamental impedance is properly modulated by the power level.

The simulated drain current and drain-source voltage waveforms at saturation are demonstrated in Figure 5 at 3.5 GHz, confirming that the designed DPA generates the expected class-J-mode waveforms with quasi-half-sinusoidal current and voltage.

At the input, a parallel resistor–capacitor network ($R = 60 \Omega$, $C = 3.3 \text{ pF}$) is inserted in series to the gate of each transistor for in- and out-of-band stabilization. The wideband input matching network (IMN) minimizes the input mismatch. Finally, an uneven 90° hybrid splitter feeds the input power to the main and auxiliary PAs with splitting ratio of $P_{\text{Aux}}/P_{\text{Main}} = 1.5$.

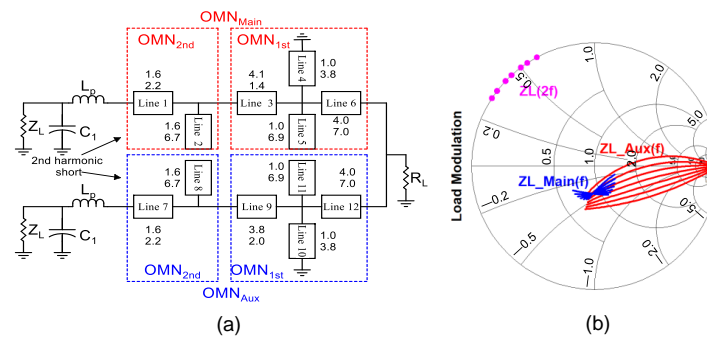


Figure 4. (a) Schematic of the OMNs (dimension length and width are in millimeters), and (b) corresponding simulated fundamental and second harmonics load modulation for the main and auxiliary PAs.

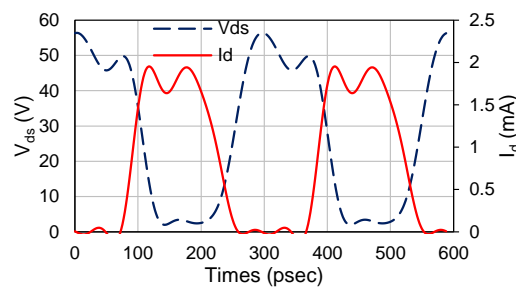


Figure 5. Simulated waveforms of the drain-source voltage and drain current at 3.5 GHz.

4. Simulation Results

The DPA performance is evaluated in simulation in the frequency range 3–3.7 GHz, under the following operating conditions: $V_{GM} = -2.95$ V, $V_{GA} = -6$ V, $V_{DD} = 28$ V, with a quiescent drain current of 112 mA. Figure 6 shows the CW simulation results of the drain efficiency and gain over the operating bandwidth.

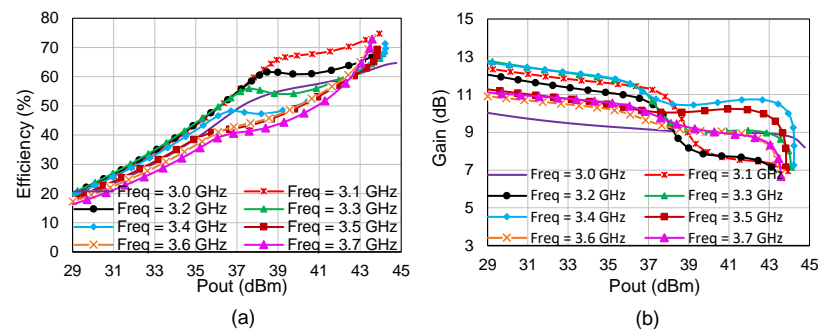


Figure 6. Simulated (a) drain efficiency and (b) gain of the designed DPA versus output power.

A two-tone analysis is also performed at 3.5 GHz to evaluate the linearity of the DPA. The third and fifth order intermodulation distortion (IMD3 and IMD5), shown in Figure 7a versus output power, remain better than -20 dBc and -31 dBc, respectively, for $P_{out} < 43$ dBm. In order to assess the system-level behavior, the DPA is simulated using a 16-QAM modulated signal and 6 dB PAPR. The input and output power spectrum at the center frequency of 3.5 GHz and with 5 MHz bandwidth are shown in Figure 7b. At an average output power of 36 dBm, the simulated ACPR is -30 dBc, and which is comparable to the results shown in [8,45].

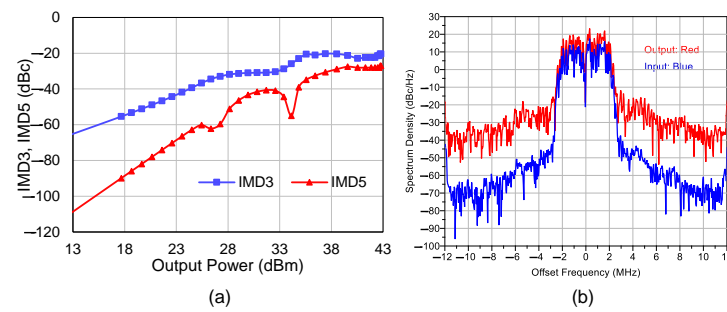


Figure 7. (a) Simulated IMD3 and IMD5 versus output power. (b) Simulated input (blue) and output (red) spectra at 3.5 GHz.

5. Measurement Results

Figure 8 shows the photograph of the proposed class-J Doherty PA. The amplifier has been characterized from 3 GHz to 3.7 GHz, in the following operating condition: $V_{GM} = -2.8\text{ V}$, $V_{GA} = -6\text{ V}$, $V_{DD} = 28\text{ V}$, $I_D = 110\text{ mA}$. The scattering parameters of the DPA are illustrated in Figure 9, showing a flat gain of around 12 dB over the target 700 MHz bandwidth, with S_{11} and S_{22} better than -10 dB , confirming also a good agreement between simulation and measurement.

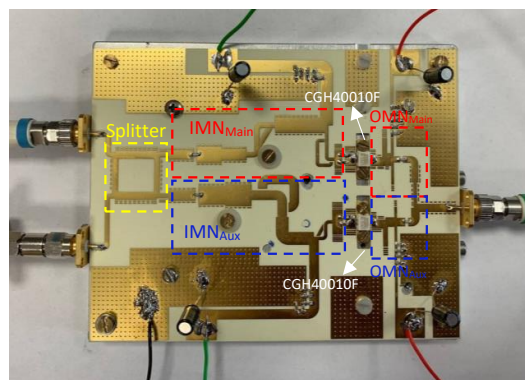


Figure 8. Photograph of the fabricated class-J DPA.

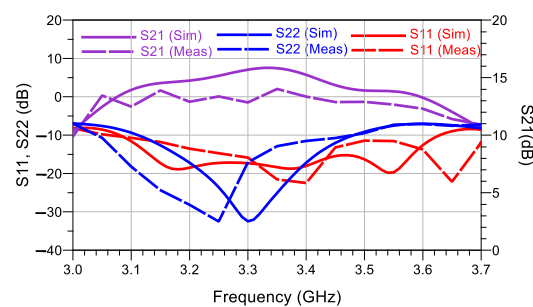


Figure 9. Measured and simulated scattering parameters of the proposed DPA.

The large-signal CW measurement results versus output power are shown in Figure 10. Power gain, drain efficiency, and output power versus frequency at saturation and at 6 dB OBO are illustrated in Figure 11. The drain efficiency is in the 60–74% range at saturation, while at 6 dB OBO, it is between 46% and 50%. The saturated output power is in the 43–44.2 dBm range.

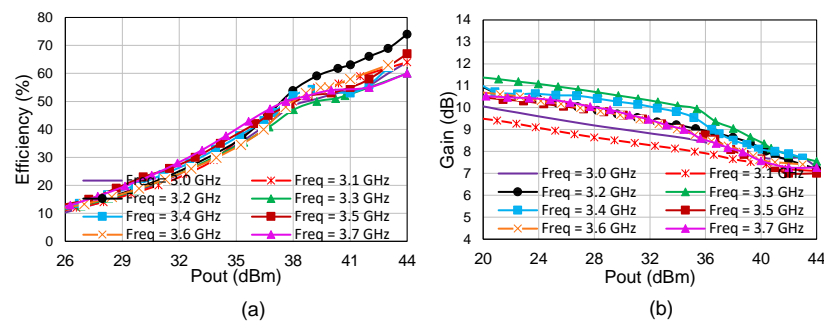


Figure 10. Measured CW performance of the DPA: (a) drain efficiency and (b) gain.

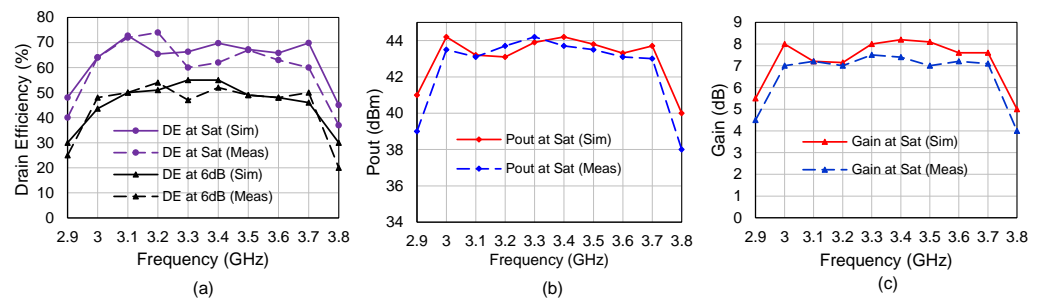


Figure 11. Measured (dashed) and simulated (solid) CW performance of the proposed DPA versus frequency at saturation and at 6 dB OBO: (a) drain efficiency, (b) output power, and (c) gain.

The proposed class-J DPA is compared with other works in Table 2. The performance obtained is well in line with the state of the art in the target frequency range, thus demonstrating that the developed amplifier is suitable for 5G applications in the S-band.

Table 2. Comparison of the proposed class-J DPA with the literature: only designs based on the same CGH40010F device are considered.

Ref.	Freq. (GHz)	Pout (dBm)	DE Sat. (%)	DE OBO (%)	Gain (dB)
[1]	1.45–2.45	42–44	48–64.2	36–52	6–13
[8]	2.9–3.3	43.9	70	40.6–44.2	6–11
[34]	1.4–2.45	41.8–43.5	47.5–64.2	35.5–52	6–13
[45]	2.2–2.6	43–44	60–65	45–53	-
[42]	2.8–3.6	43–44.2	62–76	44–56	8–13
[39]	2.4	42.3	69.3	54	12
[40]	3–3.6	43–44	55–66	38–56	12
This Work	3–3.7	43–44.2	60–74	46–50	11–13

6. Conclusions

In this paper, a wideband 20 W class-J Doherty PA with high efficiency and linearity is proposed for 5G applications, operating in the 3–3.7 GHz frequency range. Unlike conventional DPAs, the quarter-wavelength transmission line has been eliminated, embedding the impedance inversion in the output matching network, which also includes harmonic tuning to enable class-J operation. The saturated output power achieved in measurement is from 43 dBm to 44.2 dBm, while the drain efficiency at saturation and at 6 dB OBO are 46–50% and 60–74%, respectively.

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