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A Simple Virtual-Vector-Based PWM Formulation for Multilevel Three-Phase Neutral-Point-Clamped DC–AC Converters including the Overmodulation Region

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Abstract: Neutral-point-clamped (NPC) power conversion topologies are among the most popular multilevel topologies in current industrial products and in industrial and academic research. The proper operation of multilevel three-phase NPC DC–AC converters requires the use of specific pulse-width modulation (PWM) strategies that maintain the DC-link capacitor voltage balance and concurrently optimize various performance factors such as efficiency and harmonic distortion. Although several such PWM strategies have been proposed in the literature, their formulation is often complex and/or covers only particular cases and operating conditions. This manuscript presents a simple formulation of the original virtual-vector-based PWM, which enables capacitor voltage balance in every switching cycle. The formulation is presented, for the general case, in terms of basic phase voltage modulating signals, with no reference to space vectors, involving any number of levels and for any operating conditions, including the overmodulation region. The equivalence of the presented formulation to the original PWM strategy is demonstrated through simulation under different scenarios and operating conditions. Thus, this manuscript offers in a one-stop source a simple, effective, and comprehensive PWM formulation to operate multilevel three-phase NPC DC–AC converters with any number of levels in any operating condition.

Keywords: neutral-point-clamped; multilevel; virtual vector; power converter; pulse-width modulation; capacitor voltage balance

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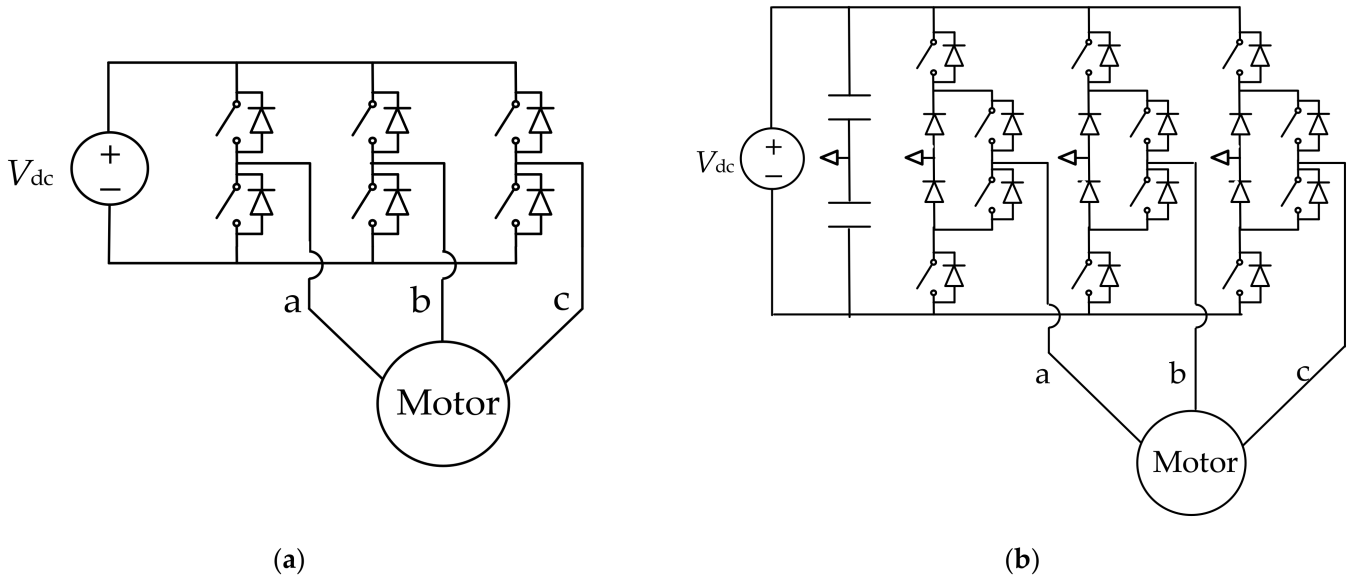
1. Introduction

One of the major application areas of power electronics is electrical motor drives [1,2] due to the substantial amount of systems that use an electric motor, the performance benefits achieved by driving the motor through a power converter, and the vast amount of energy that is processed by these systems.

Three-phase synchronous and asynchronous motors are the most popular, while they are often driven by a conventional two-level three-phase DC–AC voltage source converter, made of three two-level converter legs, as depicted in Figure 1a. However, the motor voltage, current, and corresponding power ratings vary substantially from one application to another, and this requires the use of different suitable power devices to configure the inverter for each case. An alternative solution is to use a multilevel topology to configure the motor drive, such as in the simple three-level example of Figure 1b. In this case, from a given robust power device with optimized performance and low cost, a range of motor drives at different voltage and power ratings can be configured by simply adjusting the number of levels. In addition, the multilevel converter brings additional benefits in terms of efficiency, harmonic distortion, electromagnetic compatibility, etc.



(**a**) (**b**)

Figure 1. Three-phase motor drives. (**a**) Conventional two-level converter; (**b**) three-level diode-clamped NPC converter.

Different multilevel topologies can be considered for the purpose of assembling a motor drive [3–7]. These topologies can be broadly classified in the cascaded H-bridge, flying capacitors, and neutral-point-clamped (NPC) families. Among them, the NPC family is of special interest because it offers the greatest potential to maximize power density [8–15], since the converter legs, functionally equivalent to a single-pole multiple-throw switch, are configured only with a combination of semiconductor devices, without any capacitors, inductors, or transformers, which are otherwise needed in other converter families. Then, a single set of series-connected capacitors forms the common DC-link for all legs. However, the operation of NPC multilevel converters is challenging, as the balancing of the DC-link capacitor voltages is not straightforward. This problem has been widely reported and studied in the literature [16], where it has been demonstrated that traditional multilevel pulse-width modulation (PWM) strategies lack the capacity to balance the DC-link capacitor voltages, and the problem is especially serious at four and more levels for a wide range of operating conditions, since some of the capacitor voltages collapse. Fortunately, several special PWM strategies enable the multilevel NPC DC–AC converter operation for the full modulation range with capacitor voltage balance. These include virtual-vector-based PWMs (VVPWMs) [17–32], the carrier-overlapped PWM (COPWM) [33], and other variants [34].

As long as the sum of all phase currents equals zero and the phase current ripple is relatively small, VVPWMs guarantee the balance in every switching cycle, with the drawback of increasing the number of switching transitions and harmonic distortion as compared to conventional PWM strategies. They are applicable for any number of levels and phases, and they have been extended to the overmodulation region in the three-phase case. Being able to operate in the overmodulation region is important in motor drives to maximize the achievable motor speed for a given DC-link voltage. On the other hand, modulations such as the COPWM also reach capacitor voltage balance in all operating conditions featuring lower switching losses and harmonic distortion as compared to VVPWMs. Nevertheless, the balance is achieved in a line cycle, which calls for a much larger DC-link capacitance, especially in motor drives that should operate at low speeds. Additionally, they have only been defined for a limited number of levels (four levels) and the undermodulation or linear modulation range.

Therefore, this article will focus on multilevel NPC motor drives operated with VVPWMs, which represents a competitive solution already in use in industry, mainly at three

levels. These PWM strategies were originally conceived and defined with the aid of the converter space vector diagram (SVD) [17,18]. Since their direct implementation from the SVD becomes quite complex, several efforts have been devoted to finding a simplified implementation through closed-form expressions defining the duty ratio of connection of each leg to each DC-link point or through the definition of an equivalent carrier-based PWM. This seems to be of major importance to facilitate a wide acceptance of these topologies. A simple PWM strategy implementation mitigates the difficulties associated with their inherent higher complexity, given that they introduce a higher number of switching devices.

In this context, this paper presents a novel and simplified formulation to implement VVPWMs for three-phase NPC DC–AC converters with any number of levels, including the operation in the overmodulation region.

The paper is organized as follows: In Section 2, a review of the basic NPC topologies and their operating principle is presented. In Section 3, the novel simplified VVPWM formulation is presented. In Section 4, the good performance and equivalence of this novel formulation to the original VVPWM strategy definition is proved through simulation. Finally, Section 5 presents the conclusions.

2. Review of NPC Topologies and Their Operating Principle

Pure multilevel NPC converters are built with a combination of converter legs, each functionally equivalent to a single-pole multiple-throw switch, as depicted in Figure 2. At every point in time, the leg AC terminal can be electrically connected to one of the DC-link points: to any of the two outer DC-link points dc_1 and dc_n, or to any of the $n-2$ inner neutral points dc_2 to dc_{n-1}.

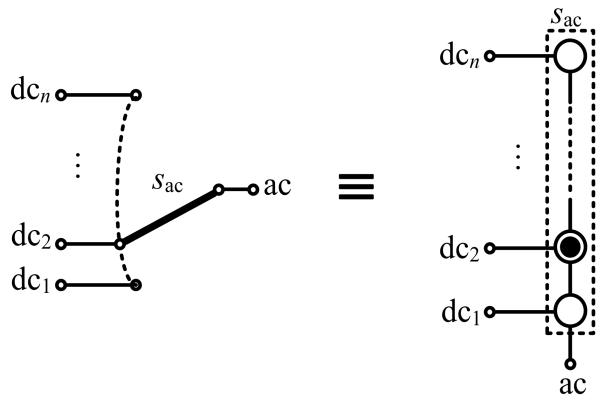


Figure 2. Functional model of an n-level NPC converter leg. The single-pole n-throw switch is represented with two alternative symbols.

Several circuit topologies are possible to build such converter legs. The main topologies are shown in Figure 3 [9]. All of them combine a number of transistors and diodes to perform the single-pole multiple-throw switch function. Figure 3a presents the active or transistor-clamped NPC (ANPC) version of the topology built with a pyramidal connection of a single type of transistor with antiparallel diode, with a voltage rating equal to one elementary voltage level $V_{\mathrm{dc}}/(n-1)$. Removing the inner transistors from the pyramid leads to the passive or diode-clamped NPC (PNPC) version of the topology, as shown in Figure 3b. The topologies in Figure 3a,b require a substantial number of devices, especially as the number of levels increases. In order to reduce the number of devices, some of the devices in Figure 3a,b can be combined into other devices with higher voltage rating, leading to the reduced ANPC and PNPC topologies shown in Figure 3c,d. Other topologies can be found in the literature designated as NPC but are in fact hybrid topologies combining the former topologies with others such as the flying capacitors. In this paper, these hybrid topologies are not considered, although the presented modulation strategy can be also adapted to many of them.

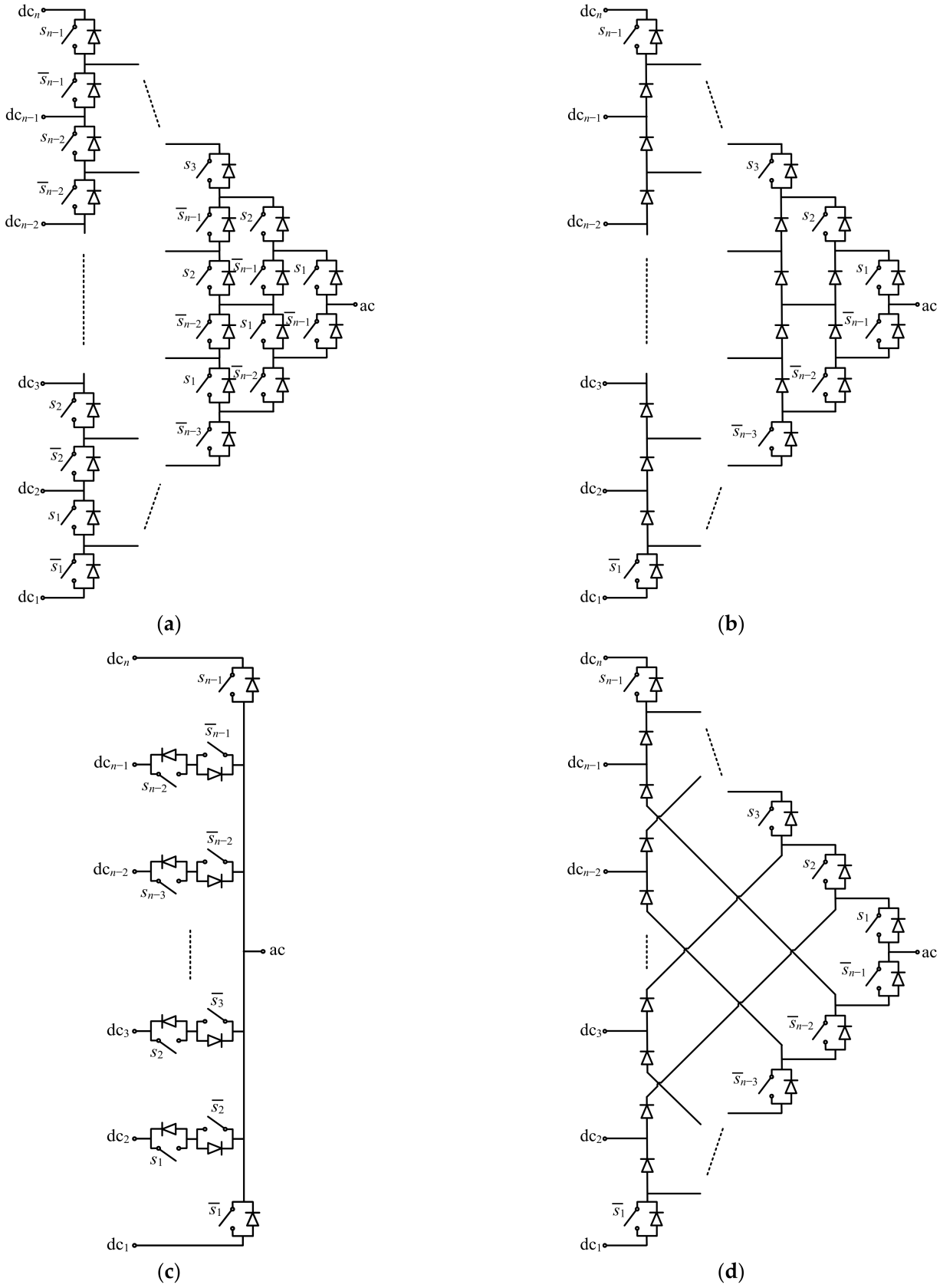


Figure 3. NPC leg topologies [9]. (**a**) Active NPC (ANPC); (**b**) passive NPC (PNPC); (**c**) reduced ANPC; (**d**) reduced PNPC.

Figure 3 also indicates the binary control signal applied to every transistor (s_k). A value equal to 1 indicates that the corresponding switch is ON, while a 0 value indicates that the switch is OFF. It can be seen that the devices from the same diagonal share the same control signal, and that devices from negative diagonals feature the complementary signal of devices from positive diagonals. Overall, the leg presents $n-1$ independent control signals, from s_1 to s_{n-1}. Table 1 defines the fundamental set of leg switching states to connect the leg AC terminal to each of the DC-link terminals [9]. It can be observed that the independent binary control signals follow a thermometric code.

Table 1. NPC leg switching states [9].

s_{ac}	Connection of AC Terminal to	s_1	s_2	s_3	...	s_{k-1}	s_k	...	s_{n-3}	s_{n-2}	s_{n-1}
1	dc_1	0	0	0	...	0	0	...	0	0	0
2	dc_2	1	0	0	...	0	0	...	0	0	0
3	dc_3	1	1	0	...	0	0	...	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
k	dc_k	1	1	1	...	1	0	...	0	0	0
...	...	...	...	...	...	...	...	...	...	...	...
$n-2$	dc_{n-2}	1	1	1	...	1	1	...	1	0	0
$n-1$	dc_{n-1}	1	1	1	...	1	1	...	1	1	0
n	dc_n	1	1	1	...	1	1	...	1	1	1

3. Simplified Virtual-Vector-Based PWM Formulation

In this section, a novel and simple formulation of the original VVPWM [17,18] for multilevel three-phase NPC DC–AC converters, as shown in Figure 4, is presented, with the aim to facilitate its comprehension and implementation and provide additional insight. In Section 3.1, the formulation is initially presented for the undermodulation or linear modulation range. This range is characterized by a value of the modulation index $m \in [0, 1]$, where m is defined as the ratio of the peak value of the fundamental phase-to-load-neutral voltage to its maximum value in the linear modulation range ($m = v_{x,1,pk}/(v_{dc}/\text{sqrt}(3))$, where $x \in \{a, b, c\}$). The formulation is later extended in Section 3.2 to the overmodulation range, covering the full range of $m \in [0, 2{\cdot}\text{sqrt}(3)/\pi = 1.1027]$.

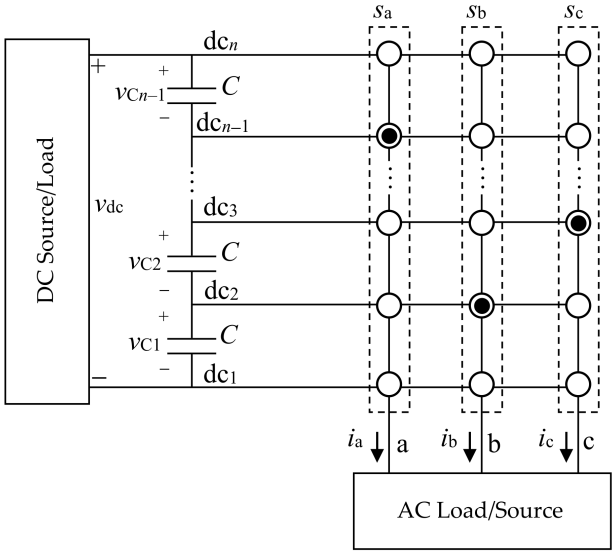


Figure 4. Multilevel three-phase NPC DC–AC conversion system.

3.1. Undermodulation Range

The formulation starts with a set of three-phase modulating signals (d_a, d_b, and d_c), representing a normalized value of the desired set of three-phase AC voltages from phase to load neutral (v_a, v_b, and v_c):

$$\begin{aligned} d_a &= \frac{v_a}{v_{dc}} = \frac{m}{\sqrt{3}} \cdot \cos(\theta) \\ d_b &= \frac{v_b}{v_{dc}} = \frac{m}{\sqrt{3}} \cdot \cos\left(\theta - \frac{2\pi}{3}\right) \\ d_c &= \frac{v_c}{v_{dc}} = \frac{m}{\sqrt{3}} \cdot \cos\left(\theta - \frac{4\pi}{3}\right) \end{aligned} \tag{1}$$

where $\theta = \omega \cdot t$ is the line-cycle angle.

In the second step, at each point in time, the maximum and minimum values of the modulating signals are determined:

$$\begin{aligned} d_{max} &= \max(d_a, d_b, d_c) \\ d_{min} &= \min(d_a, d_b, d_c). \end{aligned} \tag{2}$$

In the third and final step, the duty ratios of connection of each phase $x \in \{a, b, c\}$ to each DC-link point $y \in \{1, 2, \ldots, n\}$, designated as $d_{x,y}$, are calculated as

$$\begin{aligned} d_{x,1} &= d_{max} - d_x \\ d_{x,n} &= d_x - d_{min} \\ d_{x,k} &= \frac{1 - d_{x,1} - d_{x,n}}{n-2} \end{aligned} \tag{3}$$

where $k \in \{2, 3, \ldots, n-1\}$.

This formulation can be easily extended to a case with any odd number of phases $p \geq 3$, with $x \in \{1, 2, \ldots, p\}$, as follows:

$$\begin{aligned} d_x &= \frac{v_x}{v_{dc}} = \frac{m}{2 \cdot \cos\left(\frac{\pi}{2p}\right)} \cdot \cos\left(\theta - (x-1) \cdot \frac{2\pi}{p}\right) \\ d_{max} &= \max(d_1, d_2, \ldots, d_p) \\ d_{min} &= \min(d_1, d_2, \ldots, d_p) \\ d_{x,1} &= d_{max} - d_x \\ d_{x,n} &= d_x - d_{min} \\ d_{x,k} &= \frac{1 - d_{x,1} - d_{x,n}}{n-2} \end{aligned} \tag{4}$$

With the previous values of the phase duty ratios, each converter leg can be then directly controlled, applying the switching states from Table 1, in each switching cycle with period T_s, to produce the sequence of connection to the DC-link points illustrated in Figure 5.

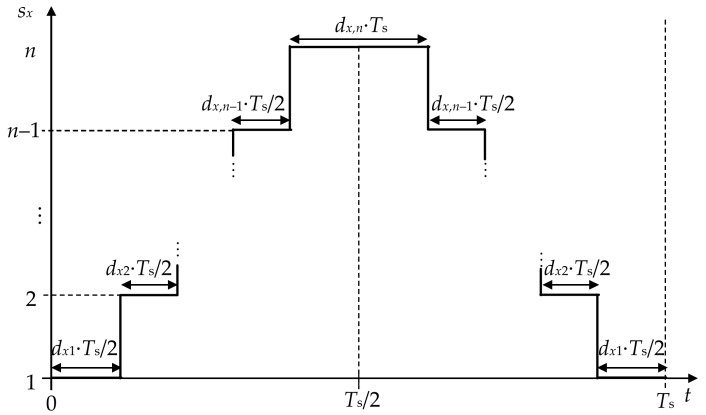


Figure 5. Sequence of connection of each leg to the DC-link points over a switching cycle.

As can be observed from Equation (4), the formulation in the undermodulation range, for any number of phases and levels, becomes extremely simple.

3.2. Full Modulation Range

If the formulation needs to cover the full range of the modulation index for a three-phase DC–AC converter, including both the undermodulation range ($m \in [0, 1]$) and the overmodulation range ($m \in]1, 1.1027]$), then it becomes more complex. However, in the following, a fairly simple formulation is presented covering the aforementioned full modulation range, which represents the main contribution of the article.

The VVPWM strategy applied in the overmodulation range is equivalent to the strategy originally presented in [18]; i.e., it produces the same switch control signals. However, the formulation presented here is simplified. The overmodulation approach presented in [18] is composed of two substrategies or overmodulation modes: overmodulation mode I (OMI), applied for $m \in]1, m_{\text{maxI}} = 3{\cdot}\ln(3)/\pi = 1.0491]$, and overmodulation mode II (OMII), applied for $m \in]m_{\text{maxI}}, m_{\text{maxII}} = 2{*}\text{sqrt}(3)/\pi = 1.1027]$. The value m_{maxII} corresponds to six-step operation. In addition, in [18] a reduction in the maximum modulation index value in the linear modulation range is introduced to guarantee that the duty ratio of connection to the neutral points is always higher than zero, which guarantees capacitor voltage regulation margin in every switching cycle. This reduction is introduced through the so-called hexagonal boundary compression factor $hbc \in [0, 1]$, which indicates the per-unit scaling of the SVD hexagonal boundary. A value close to 1 can be typically selected.

The first proposed formulation for the full modulation range is as follows. Initially, a modified modulation index value, designated as m', is determined, depending on the modulation region, according to the desired modulation index m, as indicated in Algorithm 1.

Algorithm 1

if $m \leq hbc$
  $mode = 1$
  $m' = m$
elseif $hbc < m \leq hbc{\cdot}m_{\text{maxI}}$
  $mode = 1$
  $\theta_c = \frac{\pi}{6} \cdot \left(\frac{m_{\text{maxI}} - m/hbc}{m_{\text{maxI}} - 1} \right)$
  $m' = \frac{hbc}{\sin(\theta_c + \pi/3)}$
elseif $hbc{\cdot}m_{\text{maxI}} < m \leq hbc{\cdot}m_{\text{maxII}}$
  $mode = 2$
  $\theta_h = \frac{\pi}{6} \cdot \left(\frac{m/hbc - m_{\text{maxI}}}{m_{\text{maxII}} - m_{\text{maxI}}} \right)$
  $m' = \frac{hbc}{\sin(\theta_h + \pi/3)}$
end

Subsequently, the phase duty ratios $d_{x,y}$, $x \in \{a, b, c\}$, $y \in \{1, 2, \ldots, n\}$ can be calculated according to Algorithm 2, where med(x,y,z) outputs the medium value among variables x, y, and z; ceil(x) outputs the nearest integer above x; floor(x) outputs the nearest integer below x; and $k \in \{2, 3, \ldots, n-1\}$.

The combination of Algorithms 1 and 2 already provides a general and fairly simple implementation of the VVPWM including the overmodulation region. However, in Algorithm 1, the calculation of m' involves trigonometric functions. In order to avoid the need to evaluate trigonometric functions, Algorithm 1 can be replaced by Algorithm 3.

The simplification in Algorithm 3 is obtained with the disadvantage of introducing some error between the achieved effective modulation index, designated as m_e (i.e., the modulation index calculated from the amplitude of the fundamental component of the resulting phase voltage), and the modulation index command m, in the overmodulation region. This error will be analyzed in the following section.

Algorithm 2

$d_{\mathrm{a}} = \frac{m'}{\sqrt{3}} \cdot \cos(\theta)$
$d_{\mathrm{b}} = \frac{m'}{\sqrt{3}} \cdot \cos\left(\theta - \frac{2\pi}{3}\right)$
$d_{\mathrm{c}} = \frac{m'}{\sqrt{3}} \cdot \cos\left(\theta - \frac{4\pi}{3}\right)$
$d_{\max} = \max(d_{\mathrm{a}}, d_{\mathrm{b}}, d_{\mathrm{c}})$
$d_{\mathrm{med}} = \mathrm{med}(d_{\mathrm{a}}, d_{\mathrm{b}}, d_{\mathrm{c}})$
$d_{\min} = \min(d_{\mathrm{a}}, d_{\mathrm{b}}, d_{\mathrm{c}})$
$d_{\mathrm{pp}} = d_{\max} - d_{\min}$
if $d_{\mathrm{pp}} \leq hbc$
    if $mode = 1$
        $d_{x,1} = d_{\max} - d_x$
        $d_{x,n} = d_x - d_{\min}$
    elseif $mode = 2$
        if $d_{\mathrm{med}} \leq 0$
            $d_{x,1} = hbc \cdot \mathrm{ceil}\left(\frac{d_{\max} - d_x}{d_{\mathrm{pp}}}\right)$
            $d_{x,n} = hbc \cdot \mathrm{floor}\left(\frac{d_x - d_{\min}}{d_{\mathrm{pp}}}\right)$
        elseif $d_{\mathrm{med}} > 0$
            $d_{x,1} = hbc \cdot \mathrm{floor}\left(\frac{d_{\max} - d_x}{d_{\mathrm{pp}}}\right)$
            $d_{x,n} = hbc \cdot \mathrm{ceil}\left(\frac{d_x - d_{\min}}{d_{\mathrm{pp}}}\right)$
        end
    end
elseif $d_{\mathrm{pp}} > hbc$
    $d_{x,1} = hbc \cdot \frac{d_{\max} - d_x}{d_{\mathrm{pp}}}$
    $d_{x,n} = hbc \cdot \frac{d_x - d_{\min}}{d_{\mathrm{pp}}}$
end
$d_{x,k} = \frac{1 - d_{x,1} - d_{x,n}}{n-2}$

Algorithm 3

if $m \leq hbc$
    mode = 1
    $m' = m$
elseif $hbc < m \leq hbc \cdot m_{\mathrm{maxI}}$
    $mode = 1$
    $m' = hbc + (m - hbc) \cdot \left(\frac{2/\sqrt{3} - 1}{m_{\mathrm{maxI}} - 1}\right)$
elseif $hbc \cdot m_{\mathrm{maxI}} < m \leq hbc \cdot m_{\mathrm{maxII}}$
    $mode = 2$
    $m' = \frac{2}{\sqrt{3}} \cdot hbc - (m - hbc \cdot m_{\mathrm{maxI}}) \cdot \left(\frac{2/\sqrt{3} - 1}{m_{\mathrm{maxII}} - m_{\mathrm{maxI}}}\right)$
end

4. Simulation Results

In this section, a set of simulation results are presented to prove the good performance of the proposed formulation under a wide range of operating conditions. The system simulated is the multilevel NPC DC–AC conversion system of Figure 4, with eventually an increase in the number of phases. The DC source is assumed to be a simple DC voltage source and the AC load is assumed to be a wye-connected series resistive–inductive load. Table 2 summarizes the fixed simulation conditions.

Figure 6 illustrates the performance in the undermodulation range of a three-phase system under different modulation index values and numbers of levels. It can be observed that the phase duty ratio pattern matches the one from the original publication describing the PWM strategy [17] and that the capacitor voltages remain balanced on a per switching-cycle basis with a small capacitor voltage ripple despite the small value of the DC-link capacitance.

Table 2. Simulation conditions.

Parameter	Description	Value
V_{dc}	Total DC-link voltage	100 V
C	Capacitance of each DC-link capacitor	100 µF
f_o	Line-cycle fundamental frequency	50 Hz
f_s	Switching frequency	10 kHz
R_L	Per-phase load resistance	10 Ω
L_L	Per-phase load inductance	2 mH

Using Equation (4), Figure 7 extends the application of the VVPWM strategy to a higher number of phases. As observed in Figure 7b,c, the shape of the phase duty ratios varies as the number of phases increases, showing a pattern slightly more complex than that in the three-phase case shown in Figure 7a. However, all capacitor voltages remain balanced in every switching cycle, and a proper overall performance with balanced and sinusoidal phase currents is achieved.

Figure 8 illustrates the operation in the overmodulation range, under two modulation index values corresponding to the two subregions within the overmodulation range: OMI and OMII. It can be seen that the phase duty ratios saturate in some portions of the line cycle. This is characteristic of the overmodulation region and leads to the introduction of low-order harmonics in the line-to-line voltages and phase currents. Again, the DC-link capacitor voltages remain balanced in every switching cycle.

As mentioned in Section 3, the application of the VVPWM in the full modulation range can be achieved by combining Algorithm 2 with either Algorithm 1 or Algorithm 3. Algorithm 3 is attractive since it does not involve the evaluation of trigonometric functions. However, this advantage is achieved with the drawback of worse linearity between the commanded modulation index value (m) and the effective modulation index value (m_e) computed from the fundamental component of the output phase voltage. This is illustrated in Figure 9 under two possible values of the *hbc* parameter. The root mean square error (*RMSE*) between m_e and m is indicated in Figure 9 for each curve. It can be observed that the *RMSE* is higher with Algorithm 3 than with Algorithm 1. However, the difference between m_e and m is typically lower than 2%, which should be acceptable in many applications. With reference to the case of Figures 9a, 10 and 11 explore the differences in line-to-line voltage and phase current harmonic distortion under two operating points where the two algorithms mostly differ: m = 1.025 and m = 1.075, respectively. Some relatively minor harmonic distortion differences can be observed, due to the different effective operating point in each case.

As mentioned in Section 1 and proved in the literature, the VVPWM achieves capacitor voltage balance in every switching cycle for any operating condition with the disadvantage of higher harmonic distortion and higher switching losses than with conventional multilevel PWM strategies. This is illustrated in Figures 12 and 13, as discussed in [17]. Figure 12 compares the line-to-line voltage total harmonic distortion (THD) under the VVPWM and a conventional nearest-three-vector (NTV) PWM under different numbers of levels n. The THD value under the case of a two-level three-phase DC–AC converter is also shown as a reference for comparison. The VVPWM produces a higher THD than the NTV PWM, but the VVPWM does not require large capacitors and/or additional balancing circuitry to keep the capacitor voltages balanced, as is the case of NTV PWM. The THD values are consistently lower than those in the case of a two-level converter. Figure 13 compares the total switching power loss in per unit value of the total switching power loss of a two-level converter. As can be observed, the VVPWM produces more switching power loss than a conventional NTV PWM strategy, but the loss is smaller than that in a two-level converter. In general, conduction power loss should be similar regardless of the selected modulation strategy.

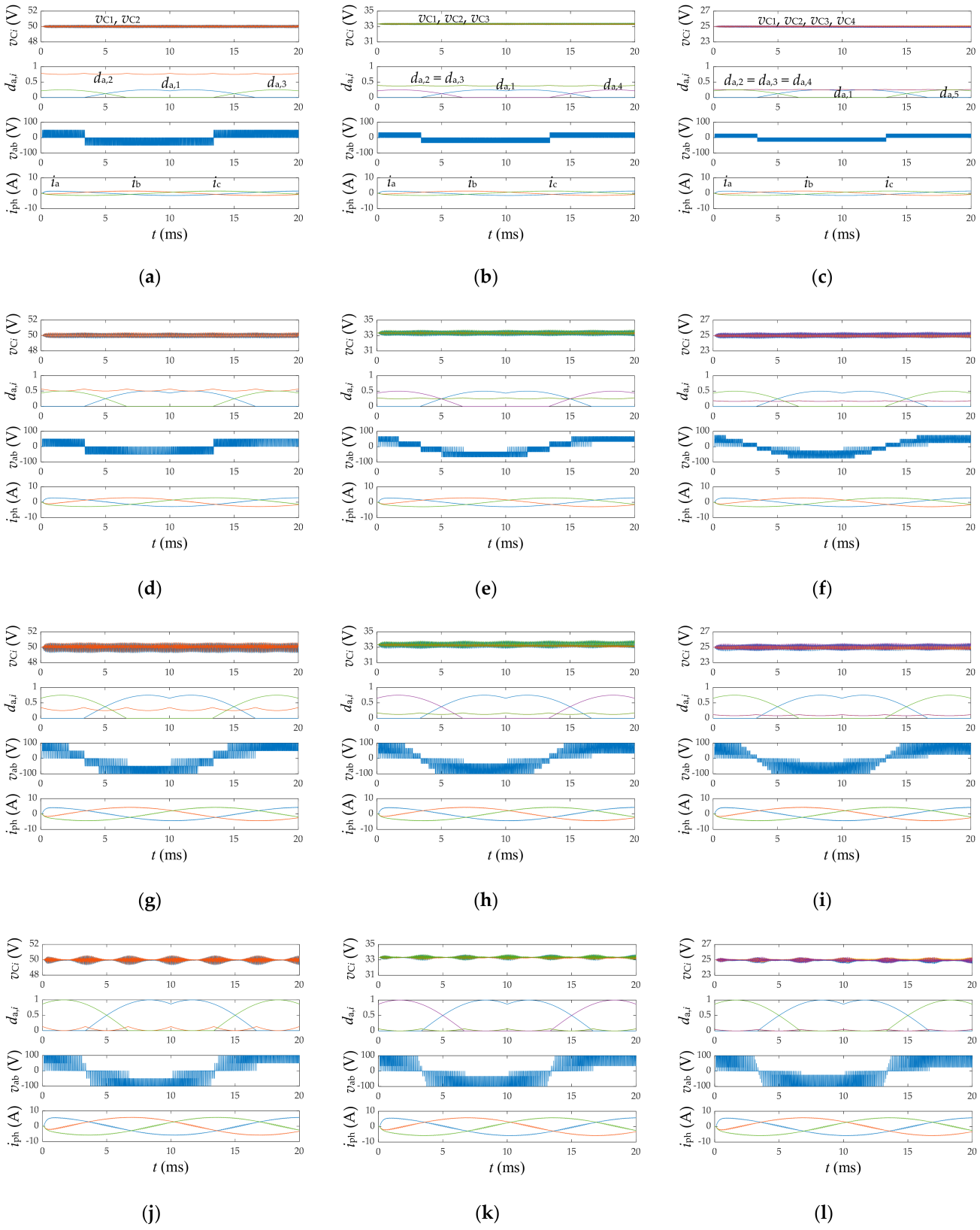


Figure 6. Simulation results for the three-phase NPC DC–AC conversion system of Figure 4, operated with the proposed VVPWM strategy formulation, under different modulation index values m and numbers of levels n in the undermodulation range (hbc = 1). (**a**) m = 0.25, n = 3; (**b**) m = 0.25, n = 4; (**c**) m = 0.25, n = 5; (**d**) m = 0.5, n = 3; (**e**) m = 0.5, n = 4; (**f**) m = 0.5, n = 5; (**g**) m = 0.75, n = 3; (**h**) m = 0.75, n = 4; (**i**) m = 0.75, n = 5; (**j**) m = 1, n = 3; (**k**) m = 1, n = 4; (**l**) m = 1, n = 5.

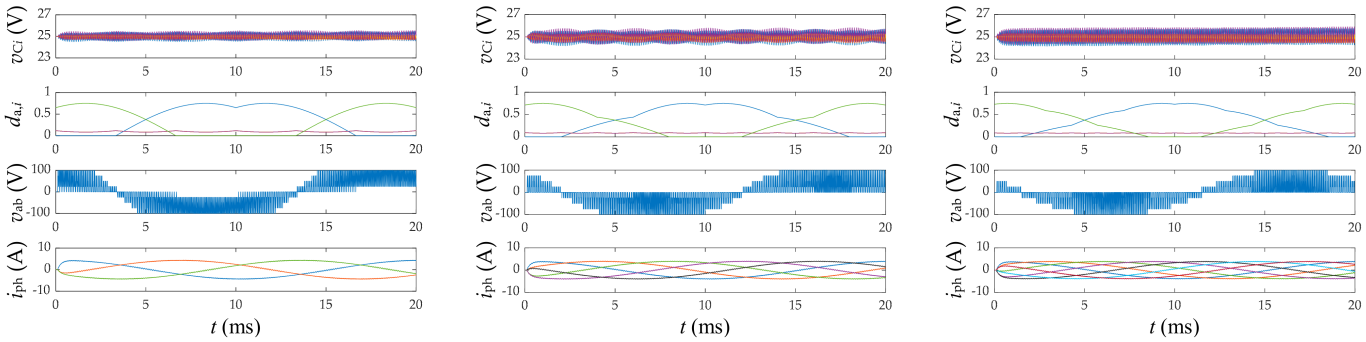


Figure 7. Simulation results for an NPC DC–AC conversion system, operated with the proposed VVPWM strategy formulation, under m = 0.75, n = 5, and different numbers of phases. (**a**) Three phases; (**b**) five phases; (**c**) seven phases.

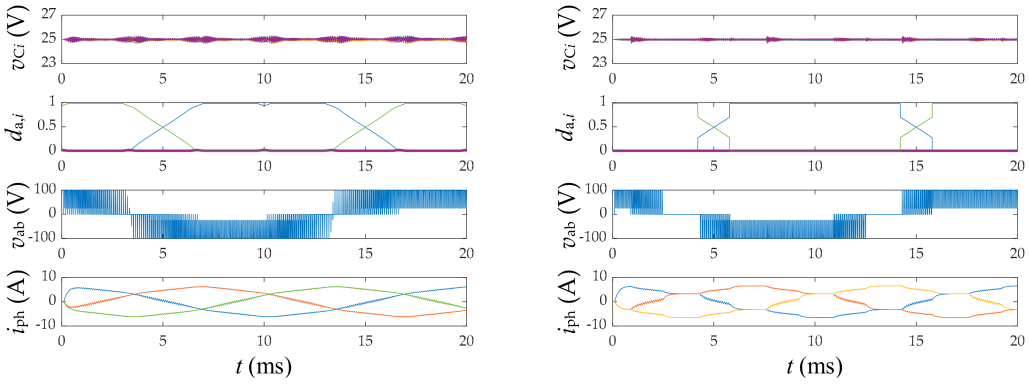


Figure 8. Simulation results for the three-phase NPC DC–AC conversion system of Figure 4, with n = 5, operated with the proposed VVPWM strategy formulation and *hbc* = 0.98, under two different modulation index values m corresponding to the overmodulation region. (**a**) m = 1.01 (OMI); (**b**) m = 1.07 (OMII).

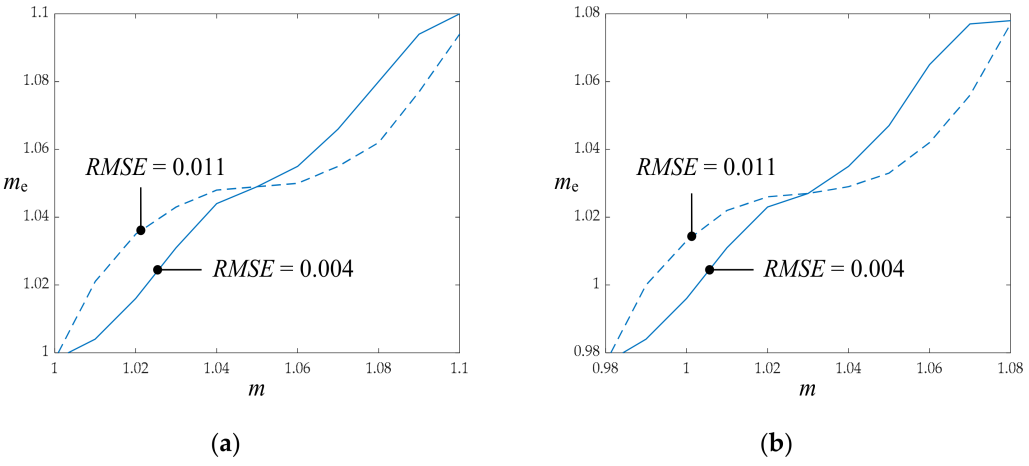


Figure 9. Effective modulation index (m_e) as a function of the commanded modulation index (m) in the overmodulation region for two cases: algorithm implemented with Algorithms 1 and 2 (solid line) and algorithm implemented with Algorithms 2 and 3 (dashed line). (**a**) *hbc* = 1; (**b**) *hbc* = 0.98.

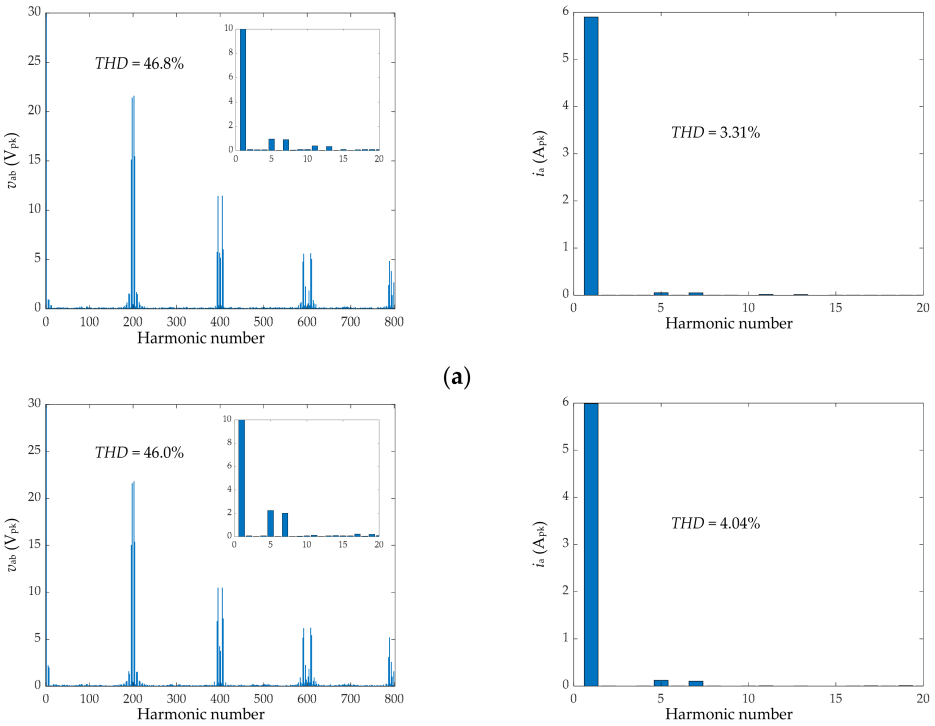


Figure 10. Line-to-line voltage and phase current harmonic distortion under m = 1.025 and hbc = 1. (**a**) Algorithm implemented with Algorithms 1 and 2; (**b**) algorithm implemented with Algorithms 2 and 3.

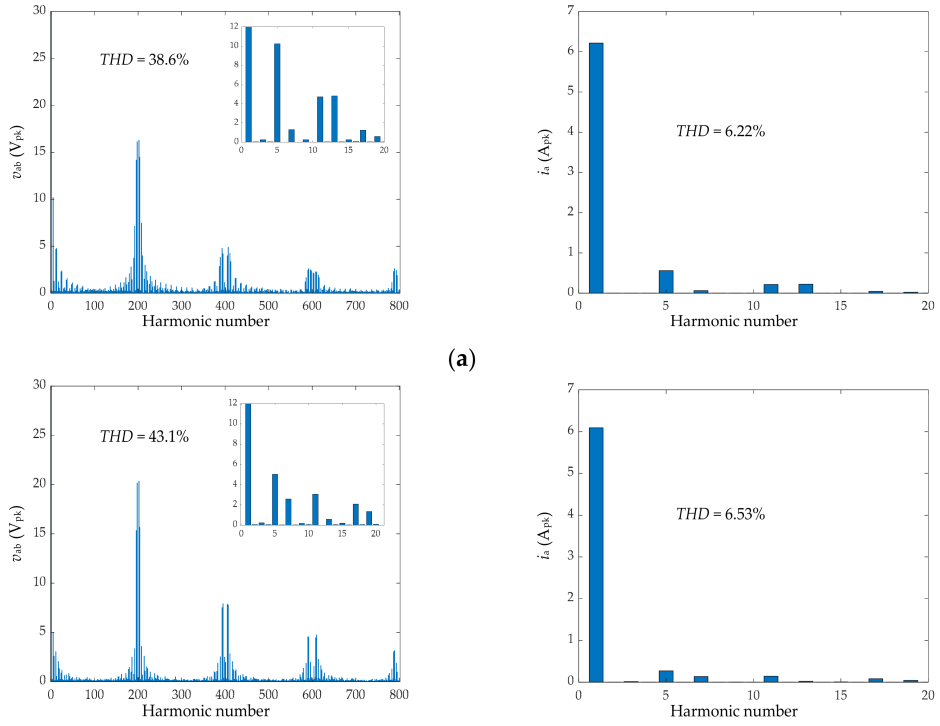


Figure 11. Line-to-line voltage and phase current harmonic distortion under m = 1.075 and hbc = 1. (**a**) Algorithm implemented with Algorithms 1 and 2; (**b**) algorithm implemented with Algorithms 2 and 3.

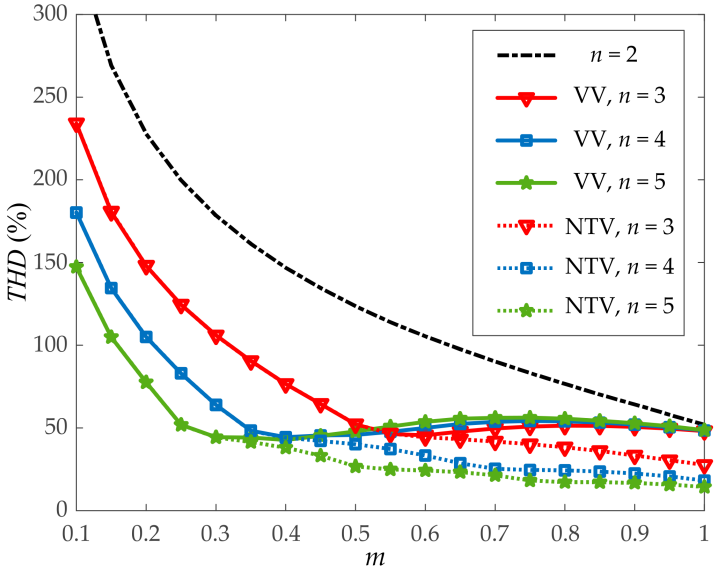


Figure 12. Total harmonic distortion of the line-to-line voltage in a three-phase multilevel NPC DC–AC converter operated with the VVPWM and operated with a reference NTV PWM [17].

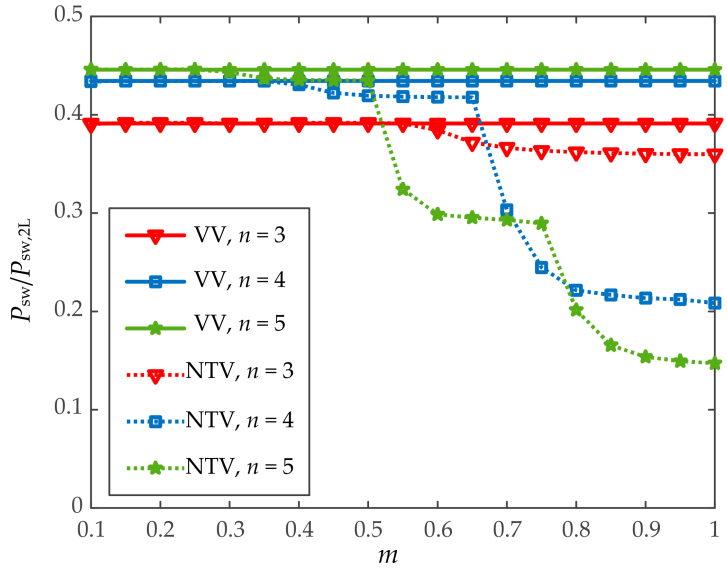


Figure 13. Switching power loss in a three-phase multilevel NPC DC–AC converter operated with the VVPWM and operated with a reference NTV PWM in per unit value of the switching power loss of a two-level converter [17].

Regarding the electromagnetic interference (EMI) performance, both the differential mode noise and common-mode noise of VVPWM-operated NPC DC–AC converters are in general lower than those in the case of a two-level converter, reducing the size of the required EMI filter [35]. Nevertheless, some modulation strategy variants have been conceived to further reduce the common-mode voltage [29,32].

The satisfactory operation of multilevel NPC DC–AC converters with VVPWMs has been extensively experimentally verified in the literature [17–32,35]. Figure 14 illustrates the experimental performance of a five-level three-phase DC–AC inverter feeding a three-phase passive load under a relatively high modulation index value, for which the balancing is not possible using traditional modulation techniques.

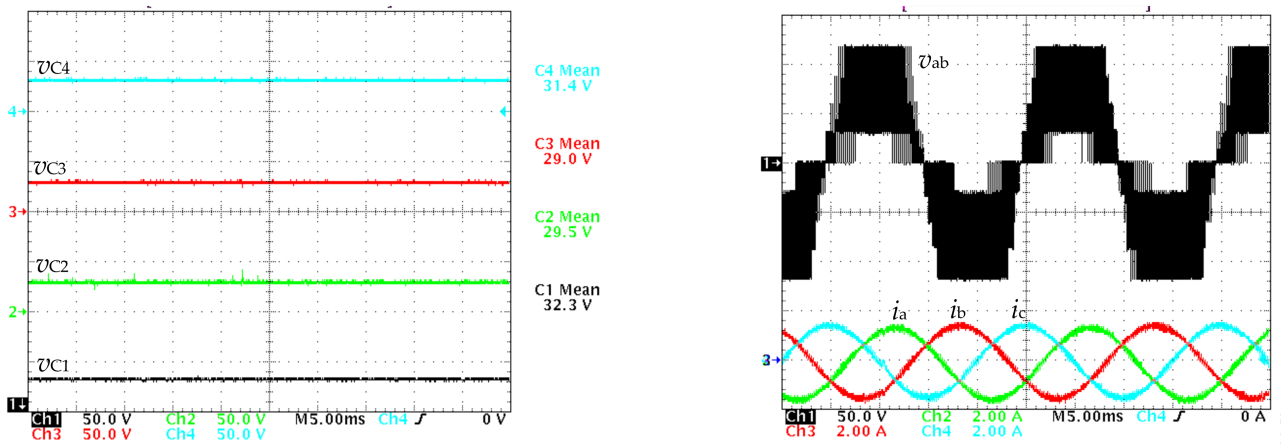


Figure 14. Experimental results of a five-level three-phase DC–AC converter operated with VVPWM under the following conditions: V_{dc} = 120 V, m = 0.75, C = 155 µF, f_s = 5 kHz, and a linear and balanced load with per-phase impedance Z_L = 33.5 Ω ∠8.5° (series R-L load) [17]. (**a**) DC-link capacitor voltages; (**b**) Line-to-line voltage and phase currents.

5. Conclusions

A simple comprehensive formulation of the original VVPWM strategy for multilevel three-phase NPC DC–AC converters has been presented. The formulation is valid for any number of levels and for the full modulation range, including both the undermodulation and overmodulation regions. In the undermodulation range, it is easily extended to any number of phases. This novel formulation is directly based on basic modulating signals representing the normalized value of the desired phase-to-load-neutral voltages, with no direct reference to the SVD. Thus, it is a convenient one-stop source for researchers and practitioners looking for a general, comprehensive, and simple PWM formulation that guarantees proper performance in NPC DC–AC converters. In addition, the proposed formulation may provide additional insight into the features of VVPWM strategies, facilitate the coding and debugging of this PWM strategy, and also facilitate the development of extensions and variants.

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