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A New Realization of Electronically Tunable Multiple-Input Single-Voltage Output Second-Order LP/BP Filter Using VCII

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Abstract: In this paper, a new realization of electronically tunable voltage output second-order low-pass (LP) and band-pass (BP) filter is presented. The circuit has a multiple-input single-output structure, and LP and BP outputs are provided using the same structure. One electronically variable second-generation voltage conveyor (VCII), whose impedance at the Y port can be electronically varied using a control current (I_{con}), two capacitors, and one resistor are used. By changing the value of I_{con}, the impedance value at the Y port can be electronically varied; therefore, the value of ω_0 can be tuned. This feature helps to reduce the number of passive components used. Interestingly, the LP and BP outputs are provided at the low-impedance Z port of the VCII, and there is no need for an extra voltage buffer for practical use. The circuit enjoys a simple realization consisting of only 24 MOS transistors. Simulation results using PSpice and 0.18 μm CMOS parameters are provided. The value of ω_0 can be varied from 1.2 MHz to 1.7 MHz, while I_{con} varies from 0 to 50 μA, with a power consumption variation from 244 μW to 515 μW.

Keywords: band-pass filter; CCII; current mode signal processing; electronically tunable; low-pass filter VCII; second-order filter; voltage conveyor

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1. Introduction

Filter design represents a widespread and important topic, due to the interesting application in communication, measurement, instrumentation, control, and signal processing [1–3]. In recent years, current mode signal processing has been the focus of researchers in the design of various types of active filters. This is attributed to the numerous advantages offered by current mode signal processing, such as simple realization, high-frequency performance, low-voltage operation, etc. [4–9]. Importantly, current mode signal processing provides the opportunity of realizing electronically tunable filters, which are highly suitable for the requirements of full integration. These features have enabled various innovative current mode solutions in the realization of active filters [1–3,10–19].

A survey of the literature shows that considerable effort has been devoted to realizing filter topologies based on various current mode active building blocks (ABBs), such as current buffers (CBs) [1,3], second-generation current conveyors (CCIIs) [8–11], current differential transconductance amplifiers (CDTAs) [13], differential voltage current conveyors (DVCCs) [15,17], current differencing transconductance amplifiers (CCCTAs) [12,18], current feedback operational amplifiers (CFOAs) [19], current differencing buffered amplifiers (CDBAs) [20,21], fully differential CCIIs (FDCCIIs) [22], etc. However, the current mode active filters reported in [1,3–19,22] suffered from a common weakness of applications requiring voltage signals. In these circuits, the output signal was either in current form, making them unsuitable for applications requiring voltage signals, or in voltage form provided on a high impedance port, necessitating additional voltage buffers for practical use. In addition, the circuits reported in [1,3,10,11,15,17–22] were not electronically tunable.

Moreover, the CB-based circuit reported in [3], which was able to realize all-pass and notch functions, required additional current followers (CFs) at the outputs for practical application. In the CCII-based circuit presented in [11], up to five active building blocks were used. The CCCTA- and CDTA-based filters presented in [12,13,18] were implemented using BJT technology. The filter reported in [16] suffered from circuit complications, because the FDCCII used as the active building block was realized using 60 MOS transistors, and thus required a high supply voltage of ±1.65 V. The topology of [17] employed three dual-output DVCC blocks with a total number of 84 transistors. The CFOA-based filter presented in [19] required extra current buffers at the outputs for practical use.

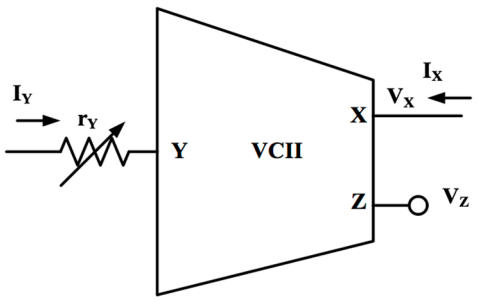
Recently, researchers' focus has been concentrated on the dual circuit of the CCII, referred to as a second-generation voltage conveyor (VCII) [22–27]. Owing to the low-impedance voltage output port, VCII is highly suitable for applications requiring output signal in voltage form. A new research area has opened up related to the design and possible applications of the VCII. VCII-based voltage output second-order high-pass (HP), low-pass (LP), band-stop (BS), band-pass (BP) and all-pass (AP) filters have been reported recently [28,29]. However, these structures include more than one ABB. They also lack electronic tuning capability. In this paper, we aim to present second-order LP and BP filters using only one VCII with electronic tunability. The ω_0 of the proposed filters can be tuned using a control current. The organization of this paper is as follows: in Section 2, the proposed circuit is presented. A non-ideal analysis is given in Section 3. Section 4 includes the simulation results, and finally, Section 5 presents the conclusions.

2. The Proposed Circuit

A symbolic representation and internal structure of an electronically tunable VCII is shown in Figure 1 [23]. An E-VCII consists principally of a current buffer between the Y and X ports, and a voltage buffer between the X and Z ports. In the electronically tunable VCII, the input resistance of the CB is shown by r_Y, which is electronically tunable. Matrix Equation (1) shows the operation of the VCII with electronically tunable impedance at Y:

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} \pm 1 & 0 & 0 \\ 0 & 1 & 0 \\ r_Y & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} \quad (1)$$

In Equation (1), + and − indicate a VCII$^+$ and a VCII$^-$, respectively. There is a current buffer between the Y and X ports with a current gain of unity, while there is a voltage buffer between the X and Z ports with a voltage gain of unity. The resistance at the Y port is shown by r_Y, which is electronically tunable. We take advantage of the electronically tunable r_Y instead of adding an external passive resistor.



(**a**)

Figure 1. *Cont.*

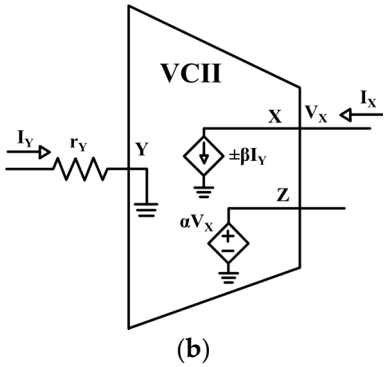


Figure 1. VCII with electronic tunable impedance at the Y port: (**a**) symbolic representation; (**b**) internal structure.

Figure 2 shows the schematic of the proposed VCII$^-$-based BP/LP filter. It is composed of one VCII$^-$, one external resistor, and two grounded capacitors. The internal resistance at Y is shown as r_Y, and is exploited to electronically vary the natural frequency of the filter. BP/LP outputs as voltage signals are produced at the Z port.

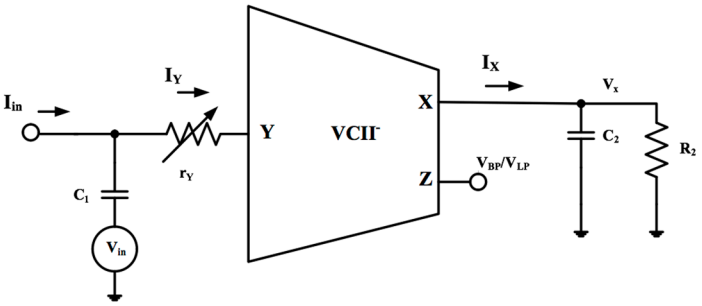


Figure 2. The proposed VCII$^-$-based second-order LP/ BP filter realization.

As can be seen in Figure 3, for I_{in} = 0, there will be a second-order BP transfer function. The analysis of the proposed BP circuit under ideal conditions is as follows:

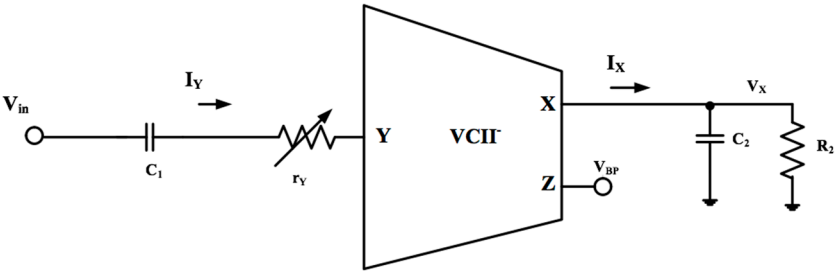


Figure 3. The proposed VCII$^-$-based second-order BP filter realization.

By assuming Y port at ground, for I_Y we have:

$$I_Y = \frac{sC_1}{1 + sC_1 r_Y} V_{in} \tag{2}$$

Using Equation (1):

$$I_X = I_Y \tag{3}$$

Using Equations (2) and (3), V_X is found as:

$$V_X = \frac{sC_1 R_2}{(1 + sC_1 r_Y)(1 + sC_2 R_2)} V_{in} \tag{4}$$

Using Equations (1) and (4), V_{BP} is:

$$V_{BP} = \frac{sC_1R_2}{(1+sC_1r_Y)(1+sC_2R_2)}V_{in} \quad (5)$$

From Equation (5), ω_0 and Q are found, respectively, as:

$$\omega_0 = \frac{1}{\sqrt{C_1r_YC_2R_2}} \quad (6)$$

$$Q = \frac{\sqrt{C_1r_YC_2R_2}}{C_1r_Y + C_2R_2} \quad (7)$$

As can be seen from (6), the value of ω_0 can be electronically tuned by varying r_Y.

If V_{in} = 0 and the input signal is applied as I_{in}, a second-order LP transfer function is achieved, as shown in Figure 4. A similar analysis gives the second-order LP transfer function as:

$$V_{LP} = \frac{R_2}{(1+sC_1r_Y)(1+sC_2R_2)}I_{in} \quad (8)$$

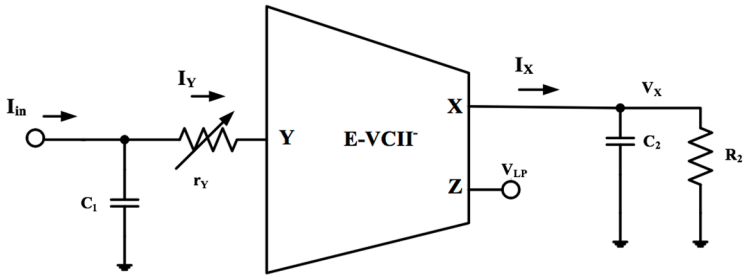


Figure 4. The proposed VCII$^-$-based second-order LP filter realization.

3. Non-Ideal Analysis

The operation of a VCII$^-$ in non-ideal conditions is given by Equation (9). Here, β and α are current gain between the Y and X terminals and voltage gain between the X and Z terminals, respectively. The main parasitic impedances associated with the VCII$^-$ ports are shown by r_x (the parasitic resistance related to X port), C_x (parasitic capacitance related to X port) and r_Y (parasitic resistance related to Y port). The ideal values of r_x and C_x are infinity and zero, respectively.

$$\begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix} = \begin{bmatrix} -\beta & \frac{1}{r_x} + sC_x & 0 \\ 0 & \alpha & 0 \\ r_Y & 0 & 0 \end{bmatrix} \begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} \quad (9)$$

Figure 5 shows the proposed second-order BP filter in which all parasitic elements are modeled. Using Equation (9), the transfer function of Figure 5 is found as:

$$V_{BP} = \frac{s\alpha\beta C_1R_{eq}}{[1+sC_1r_Y)]\,[1+s(C_2+C_X)R_{eq}]}V_{in} \quad (10)$$

where:

$$R_{eq} = r_X||R_2 \quad (11)$$

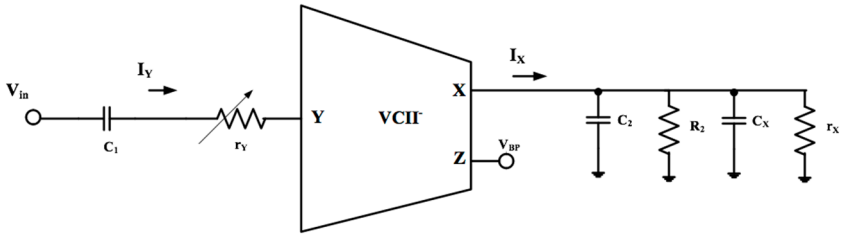


Figure 5. The proposed second-order BP filter with VCII⁻ non-ideal components.

From Equation (9), ω_0 and Q are found, respectively, as:

$$\omega_0 = \frac{1}{\sqrt{C_1 r_Y (C_2 + C_X) R_{eq}}} \tag{12}$$

$$Q = \frac{\sqrt{C_1 r_Y (C_2 + C_X) R_{eq}}}{C_1 r_Y + (C_2 + C_X) R_{eq}} \tag{13}$$

Similar analysis for the proposed second-order LP filter gives:

$$V_{LP} = \frac{\alpha\beta R_{eq}}{(1 + sC_1 r_Y)(1 + s(C_2 + C_X) R_{eq})} I_{in} \tag{14}$$

4. CMOS Implementation of VCII⁻ with Electronically Tunable Impedance at the Y Port

Figure 6 shows the CMOS implementation of VCII⁻ with electronically tunable impedance at the Y port. It consists of 24 MOS transistors. Inversion of the current buffer comprising transistors M_1–M_6 is performed to transfer the Y port input current to the X port. The control current I_{con} is used to change the bias current of common gate transistor M_2; therefore, electronically variable impedance at the Y port is provided. To maintain a constant bias current at the other branches, I_{con} is also applied to node 2; therefore, only the bias current of M_2 is varied. In addition, to maintain a zero offset voltage at the Y port, bias currents of M_1 and M_2 must be kept equal, so I_{con} is also applied to node 1.

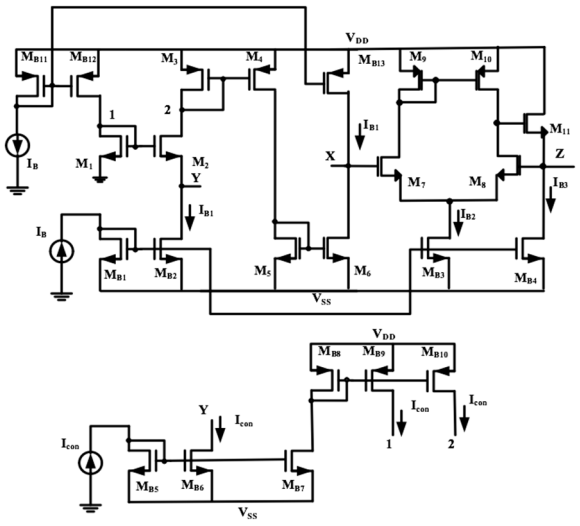


Figure 6. CMOS implementation of VCII⁻ with electronically variable impedance at the Y port. Nodes Y, 1 and 2 from the lower section of the schematic are connected to their counterparts in the upper section of the schematic.

The voltage buffer consists of transistors M_7–M_{11}, which are a differential pair cascaded by a voltage follower. They are connected in a closed loop configuration so as to decrease Z port impedance and improve the overall accuracy of the buffering action of transferring the X node voltage to the Z node. Transistors M_{Bi} for i = 1–12 provide the bias and control currents. The electronically variable impedance at the Y port is given by (with the usual meanings of the symbols):

$$r_Y = \frac{1}{gm_{M2}} = \left[\sqrt{\mu C_{ox}\frac{W_{M2}}{L_{M2}}(I_{B1}+I_{con})}\right]^{-1} \quad (15)$$

5. Proposed LP/BP Second-Order Filter Simulation Results

PSpice simulations of the VCII$^-$ using 0.18 μm CMOS TSMC technology and a supply voltage of ±0.9 V are presented in Figure 6. The transistor sizes for the used PMOS and NMOS transistors were W = 9 μm, L = 0.9 μm and W = 27 μm, L = 0.9 μm, respectively. The values of bias currents were $I_B = I_{B1} = I_{B2} = I_{B3} = 20$ μA. The control current I_{con} was varied from 0 μA to 50 μA. All bias currents were realized by simple current mirrors so as to ensure the best possible voltage swing at each terminal. To validate the proposed tuning technique, a comparison between the theoretical behavior of r_Y according to (15), and the values of the same magnitude extracted from the simulations is presented in Figure 7. In particular, $\mu = \mu_{electrons} = 0.13$ m^2/Vs, $C_{ox} = 9.51 \times 10^{-4}$ F/m^2 are constant values dependent on the technology. As can be seen, the trend between the theoretical and simulated curves matches, while the percentage error always remains below 10%. This error mirrors the inaccuracies of M_{B1}, M_{B2} and M_{B5}–M_{B10}, which generate I_{B1} and I_{con}, directly impacting the simulated value of r_Y.

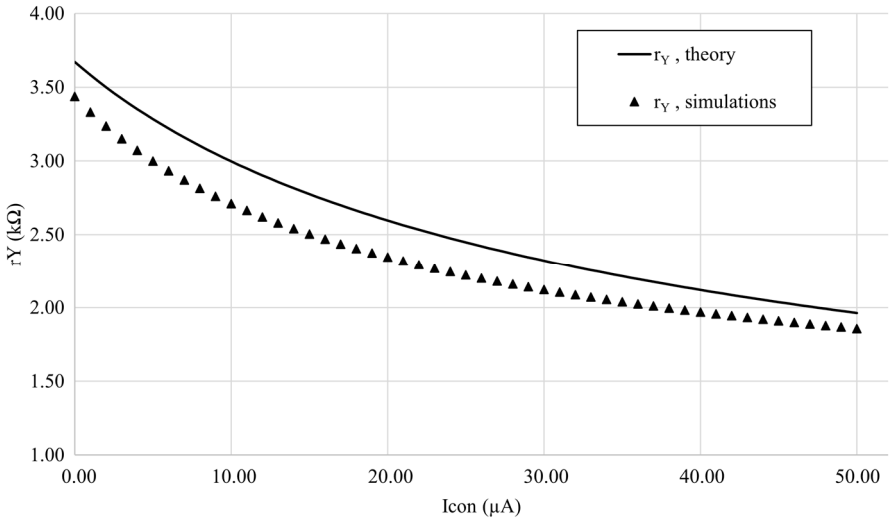


Figure 7. Comparison between simulated and theoretical r_Y values as a function of I_{con}.

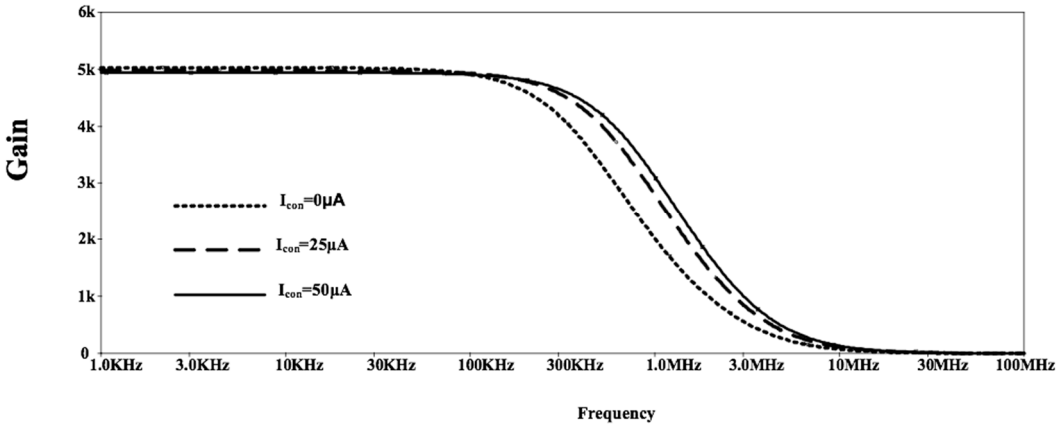
The large signal behavior of the used VCII was evaluated by extracting the slew rate (SR) figures both for the current output, X, and for the voltage output, Z. For the former, a ±20 μA step was used, which corresponds to the full ±I_B range, while for the latter, a ±500 mV step was applied to the X terminal, with a 3 pF capacitive load at Z. The current slew rates were: $SR^+_I = 13 \times 10^3$ A/s and $SR^-_I = -0.64 \times 10^3$ A/s, and the voltage slew rates were: $SR^+_V = 1.4 \times 10^8$ V/s and $SR^-_V = -6.64 \times 10^6$ V/s. As expected, the class A biasing of the input and output stages determines the difference between positive and negative values, with the latter remaining lower due to the sinking capability of the architecture being limited by the biasing current.

Table 1 shows the simulation results for the performance parameters and parasitic elements of the used VCII$^-$.

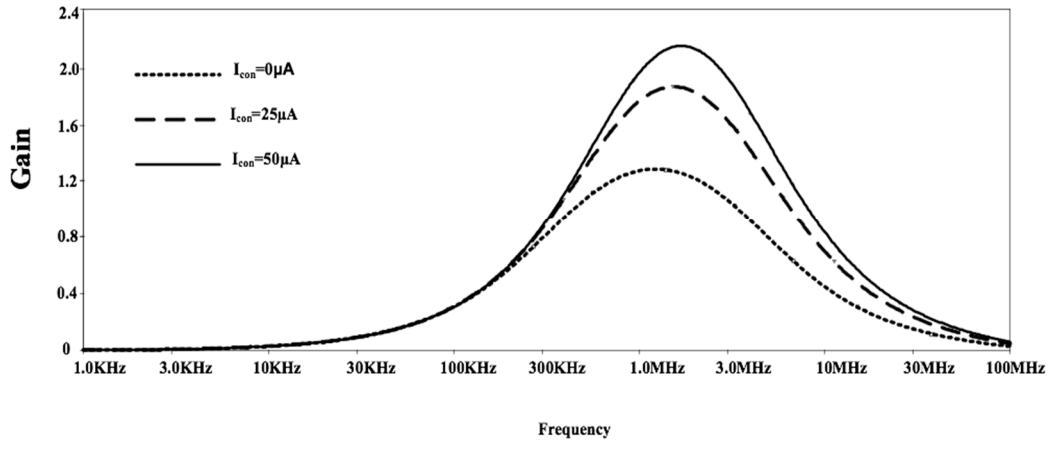
Table 1. The simulated characteristics of VCII$^-$ with electronically variable impedance at the Y port.

Parameter		Value
r_Y	I_{con} = 0 µA	3.43 kΩ
	I_{con} = 25 µA	2.18 kΩ
	I_{con} = 50 µA	1.8 kΩ
r_X		244 kΩ
r_z		48 Ω
α		0.981
β	I_{con} = 0 µA	1.04
	I_{con} = 25 µA	1.03
	I_{con} = 50 µA	1.023
C_x		64 fF
Power dissipation		244–515 µW
SR_I (positive, negative)		13×10^3 A/s, -0.64×10^3 A/s
SR_V (positive, negative)		1.4×10^8 V/s, -6.64×10^6 V/s

The proposed filter presented in Figure 2 was simulated using the VCII$^-$ presented in Figure 6. The values of the passive components were C_1 = 100 pF, C_2 = 10 pF and R_2 = 5 kΩ. Figure 8 shows the AC frequency performance of the LP and BP outputs for different values of I_{con}. On the basis of the simulation results, ω_0 was 1.2 MHz, 1.59 MHz and 1.7 MHz for I_{con} values of 0 µA, 25 µA and 50 µA, respectively. On the basis of Equation (12), the values of ω_0 were 1.22 MHz, 1.54 MHz and 1.69 MHz, respectively. Fortunately, there is good agreement between the simulation and the calculation.



(**a**)



(**b**)

Figure 8. Proposed circuit frequency performance for (**a**) LP and (**b**) BP outputs.

The robustness of the proposed solutions was tested by running 30 Monte Carlo (MC) simulations at each of the fast, typical, and slow corners. PVT combinations were as follows: SS, ±0.85 V, 80 °C; TT, ±0.9 V, 25 °C; FF, ±0.95 V, −20 °C, whereas for the MC analysis, we considered 3% mismatches in V_{th} and C_{ox} of all transistors alongside a 5% variation in the value of the passive elements. The results are summarized in Table 2. As can be seen, the proposed circuit is robust against mismatches.

Finally, Figures 10 and 11 show a time domain example of both the low-pass and band-pass filters. For the LP filter, an input current of 5 µA was used with frequencies of 100 kHz and 3 MHz. I_{con} was set to 50 µA. Similarly, for the BP, an input voltage of 10 mV was applied at three different frequencies, of 1.6 MHz, 1 MHz and 3 MHz. I_{con} was set equal to 50 µA.

Table 2. PVT and Monte Carlo simulation results for the magnitude of the filters and their ω_0.

	Value	Max	Min	Mean
I_{con} = 0 µA	$Magnitude_{BP}$	2.78 dB	1.67 dB	2.16 dB
	$Magnitude_{LP}$	74.16 dBΩ	73.96 dBΩ	74.05 dBΩ
	ω_0	1.25 MHz	1.13 MHz	1.19 MHz
I_{con} = 25 µA	$Magnitude_{BP}$	5.91 dB	4.66 dB	5.23 dB
	$Magnitude_{LP}$	74.05 dBΩ	73.84 dBΩ	73.94 dBΩ
	ω_0	1.55 MHz	1.40 MHz	1.48 MHz
I_{con} = 50 µA	$Magnitude_{BP}$	7.11 dB	5.70 dB	6.36 dB
	$Magnitude_{LP}$	73.94 dBΩ	73.73 dBΩ	73.83 dBΩ
	ω_0	1.70 MHz	1.52 MHz	1.61 MHz

The linearity performance of the proposed circuit was checked for different values of I_{con} at ω_0. The peak-to-peak values of V_{in} and I_{in} were 100 mV and 40 µA, respectively. The resulting THD is reported in Figure 9. As can be seen, the maximum value of THD remained below 4% and 8% for the LP and BP outputs, respectively.

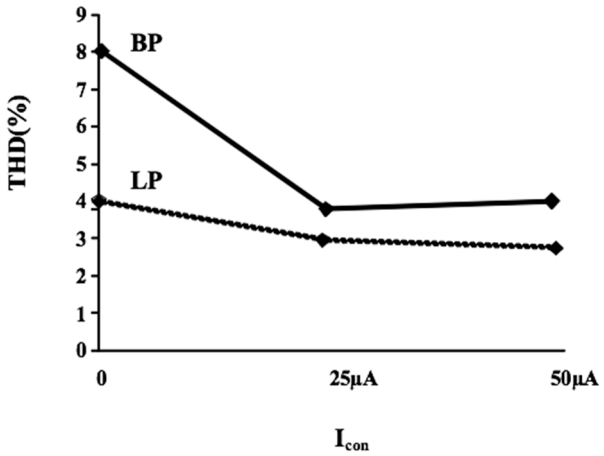


Figure 9. The simulated THD for LP and BP outputs.

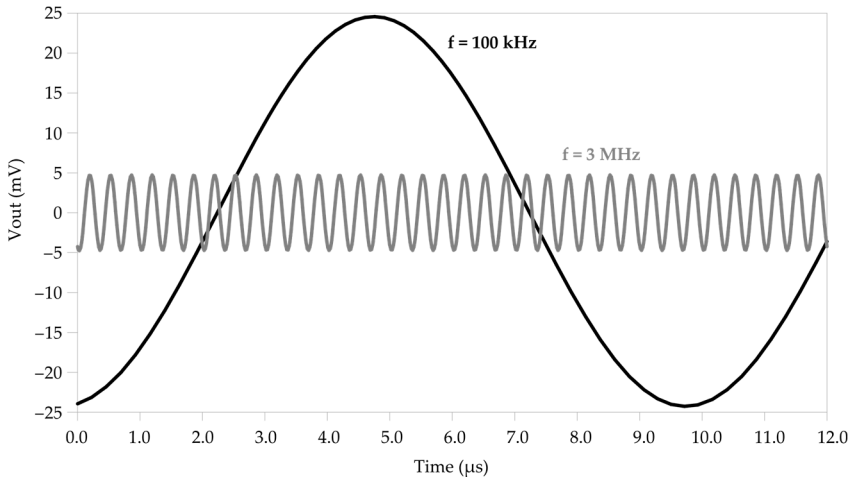


Figure 10. Time domain output for the low-pass configuration.

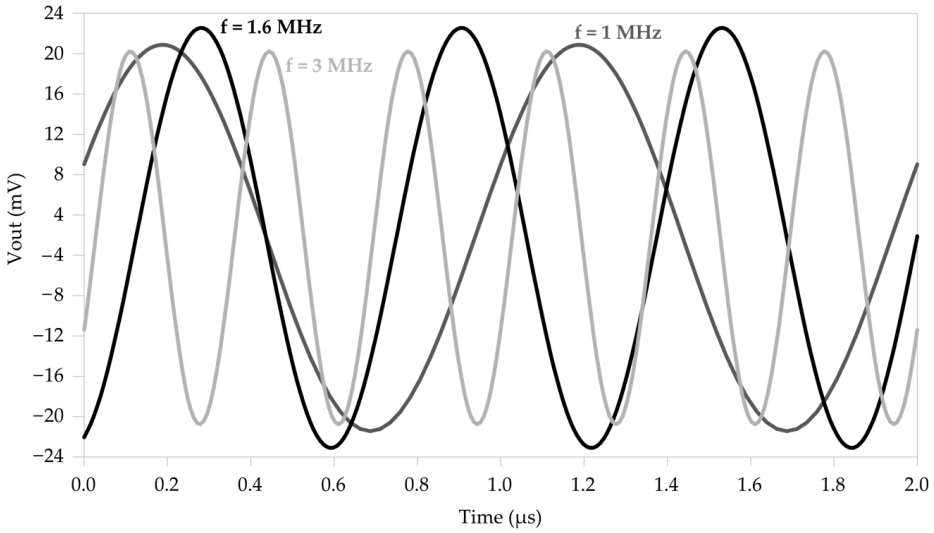


Figure 11. Time domain output for the band-pass configuration.

Table 3 shows a comparison between the proposed circuit and others reported in the literature. As can be seen, the structures proposed in [1,3,13–17] provide output signal in current form, and therefore they are not suitable for applications requiring output signal in voltage form. In addition, the circuit of [3] requires an additional current buffer for practical use. The circuit reported in [10] produces output signal in voltage form; however, it needs extra voltage buffer at the output. Similarly, additional voltage buffer is necessary for the circuits presented in [17,19]. The circuits in [20,21] are not electronically tunable, and they suffer from a high supply voltage requirement. The VCII-based topology of [29] provides BP and LP outputs at the low-impedance Z port of VCII. Unfortunately, it is not electronically tunable. In contrast to other works, the proposed VCII-based circuit is electronically tunable, and does not require additional voltage buffers at the output node. More importantly, by taking advantage of the internal impedance at the Y port, the number of passive components is reduced.

Table 3. Comparison between the proposed circuit and other reported works.

Ref	ABB	#of			Electronic Tunability	Outputs	V_{DD}-V_{SS}	Power Dissipation	Extra VB/CB
		ABB	R	C					
[1]	CF	1	2	2	No	I_{LP}, I_{HP}, I_{BP}	NA	NA	No
[3]	CF	1	4	2	No	I_{AP}, I_{notch}	NA	NA	Yes
[10]	CCII	1	2	2	No	V_{BP}, V_{HP}, V_{LP}	±0.75 V	NA	Yes
[13]	CDTA	2	0	2	yes	I_{BP}, I_{LP}, I_{HP}	±2.5 V	870 µW	No
[15]	VDCC	1	1	2	No	I_{LP}, I_{BP}, I_{HP}, I_{BS}, I_{AP}	±0.9 V	NA	No
[16]	FDCCII	1	2	2	No	I_{LP}, I_{BP}, I_{HP}, I_{BS}, I_{AP}	±1.65 V	2.28 mW	No
[17]	DVCC	3	3	2	No	V_{LP}, V_{BP}, V_{HP}, V_{BR}, V_{AP}	±0.9 V	NA	Yes
[18]	CCCTA	3	0	2	yes	I_{HP}, I_{LP}, I_{BP}	±1.85 V	NA	No
[19]	CFOA	1	3	2	No	V_{BP}, V_{LP}	NA	NA	Yes
[20]	CDBA	3	5	2	No	V_{HP}, V_{BP}, V_{LP}	±1.25 V	NA	No
[21]	CDBA	3	3	2	No	V_{HP}, V_{BP}, V_{LP}	±5 V	NA	No
[29]	VCII	1	2	2	No	V_{BP}, V_{LP}	±1.65 V	700 µW	No
Proposed	VCII	1	1	2	yes	V_{BP}, V_{LP}	±0.9 V	244–515 µW	No

6. Conclusions

In this paper, a new realization of an electronically tunable second-order LP/BP filter using $VCII^-$ with the property of electronically tunable impedance at the Y port is presented. The proposed circuit consists of one $VCII^-$, two capacitors, and one resistor. The output signal is in voltage form provided at the low-impedance Z port of the VCII, which makes it unnecessary to use extra voltage buffer in practical applications. The ω_0 of the proposed transfer functions can be tuned using a control current (I_{con}), by means of which the impedance at the Y port of VCII can be varied. Therefore, the number of passive resistors used is also reduced, resulting in a simpler circuit and a reduced chip area. A non-ideal analysis is provided. Spice simulation results are reported to show the functionality of the proposed structure.

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