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Control of a Modified Switched-Capacitor Boost Converter

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Abstract: Switched-capacitor converters and their alternatives have been shown to provide high efficiency with high power densities on smaller volumes, and can thereby be a suitable choice for energy harvesting. This paper proposes a hybrid power architecture based on a switched-capacitor topology and a boost converter that can be used for such purposes. A switching capacitor circuit can achieve any voltage ratio, allowing a boost converter to increase the input voltage to higher voltage levels. The first stage is unregulated with high-efficiency voltage conversion. The boost stage provides a regulated voltage output on such a converter. Rather than cascading two converters, their operation is integrated for the output voltage regulation. One major problem of switched-capacitor converters is output voltage regulation, which is solved by the interconnection of the power stages. The simplicity and robustness of the solution provide the possibility to achieve higher voltage ratios than cascading boost converters and provide higher efficiency. The converter's size and cost can be improved with the integration of switching capacitors in DC-DC converter structures. A converter prototype has been designed, modelled, and built for the input voltage level of 2 V and power level of 5 W.

Keywords: SC-BC; cascade control; low power; low voltage

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1. Introduction

Renewable energy sources are abundant in our living environment and have been gaining more and more attention in recent years. The electrical energy generated from the sources can be utilised for many purposes, including driving small electronic devices, or even constructing an integrated system operated without bulky batteries or power cables. The power flow fluctuates according to the energy gained, so the power converters connected to such sources have to cope with the provided energy. Energy harvesting on low-voltage energy sources demands the selection of converters that can optimise the power flow. A power converter based on switching capacitors has been chosen for the energy harvesting application. The topologies of converters consisting only of switches and capacitors have long been known and used, mainly in diode-capacitor voltage multipliers [1,2]. Switched-capacitor converters (SCCs) consist of a network of switches and capacitors, where the switches are turned on and off periodically to cycle the network of elements through different topological states.

There are, however, some limitations of the SCC DC-DC converters that have limited their widespread use. The well-known problems connected to the SCCs are the intrinsic loss generated by charging and discharging cycles and the difficulty of regulating the output voltage. In certain topologies, the regulation of the output voltage can only be achieved in a narrow range of input voltages while maintaining good conversion efficiency. One way to overcome these limitations is to use a cascade SCC having a fixed step-up ratio with a switching power converter to extend the input voltage range [3,4] and provide efficient output regulation. The first stage of an SCC is unregulated to allow very high efficiency. The first stage of the combined converter structure also increases the input low voltage levels to more suitable input voltages for the boost converter. In low-voltage

energy harvesting applications, this can provide a crucial advantage. With the switching converter's second stage, the output voltage is regulated to the desired voltage level.

Conventional DC-DC converters based on magnetic components are prevalent in industrial and commercial applications where the magnetic components are the bottleneck in shrinking size, reducing cost, and improving efficiency. Switched-capacitor DC-DC converters present an alternative approach by removing the magnetic components in DC-DC converters. In some cases, some of the switched-capacitor structures have been shown to outperform conventional magnetic-based DC-DC topologies in a wide range of power and voltage levels [5]. Due to the possible size optimisation and comparable efficiency, switched-capacitor converters present an alternative approach in the design of converters.

Several methods can be used to control the voltage output of the SCCs. The most common one is to adjust the switching frequency to control the output impedance of the SCCs. A common solution used in the SCC is to reconfigure the circuit to achieve several discrete conversion ratios [6,7]. This solution is limited and cannot achieve high efficiency over a wide input voltage range. The converter topology is known as described in [1,8], but in the presented circuit, the diodes are replaced by transistors to improve efficiency issues. Moreover, the control algorithm is improved as well with the help of the decoupling of zdT_s, as described in [8,9], to the time interval zT_s when the switched capacitors are charged and the duty ratio of energised interval $(d-z)T_s$; see Figure 1.

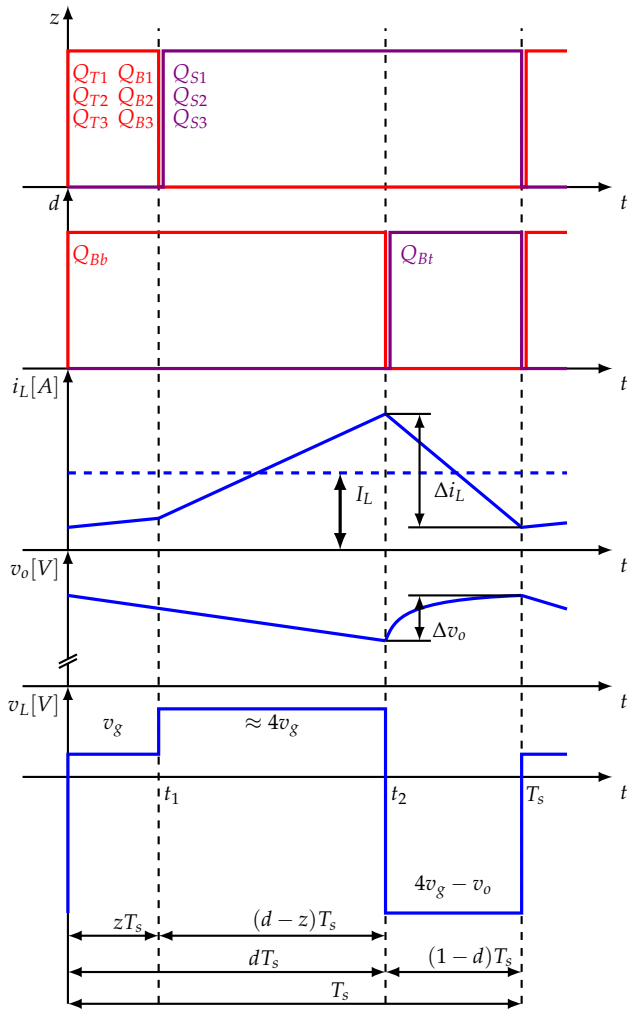


Figure 1. Switching sequences of the converter. The main duty cycles z and d are shown in red; $(1-z)$ and $(1-d)$ are shown in violet; i_L, v_L, and v_o are shown in blue.

The time duration of the first frame controlled by parameter "Z" can be set based on the switched-capacitor capacitance and the chosen switching frequency. Therefore, the converter's design can set the time ratio between the first voltage step and second boost part, which presents an additional advantage in the application of such a converter. In previously published applications, this was not considered, and intermediate voltage has not been stabilised. The constant zT_s interval simplifies the implementation of non-linear control methods, which was relatively complex in [9].

With the voltage increase in the first stage, the boost converter can operate at a relatively low duty cycle. Usually, boost converters alone cannot provide a high DC voltage ratio. They are limited by a maximum duty cycle value due to the latch-up conditions in the converter circuit. Usually, the maximum voltage ratio is around five, but this ratio is practically unrealisable [10] due to regulation requirements where a change in load or line can only be compensated with an additional duty cycle change. Higher duty cycle values are also not desirable due to diode-reverse recovery problems.

Depending on the network topology and the number of switches and capacitors used, efficient step-up or step-down power conversions can be achieved at different conversion ratios. Switched-capacitor converters have become viable where high power densities and high efficiency are required [3,4,11]. The charging loss can be reduced by increasing the switching frequency, increasing the capacitance, or introducing soft switching techniques [12]. The efficiency drops quickly as the conversion ratio moves away from the optimal operation mode for a given topology.

The efficiency of both converter stages is equal to the efficiencies of both structures. This topology can provide high efficiency, high power density, and can potentially be used in low-voltage and low-power converters, targeting energy harvesting applications.

The low voltage rating has been chosen based on the output voltage generation range of thermoelectric generator (TEG) elements. The presented converter structure is suitable for this type of energy harvesting, although energy conversion is not limited to this type of energy source harvesting.

Section 2 presents the combined SCC converter's concept and operating principle with the SC boost converter for the DC-DC voltage conversion. Section 3 provides converter modelling, where the state-space averaging method was used to obtain the static and dynamic characteristics of the converter. The output voltage control based on cascaded PI control is presented in Section 4, where changes are considered in the structure of the SC-BC. Section 5 presents the simulation and experimental results from a prototype with discrete elements, and Section 6 concludes the paper.

2. Operating Principles of the Converter

The switched-capacitor boost converter shown in Figure 2 was introduced in [8], modified, and analysed further in [9]. The converter integrates a switched capacitor circuit (the red frame in Figure 2) and a boost converter (the blue frame in Figure 2).

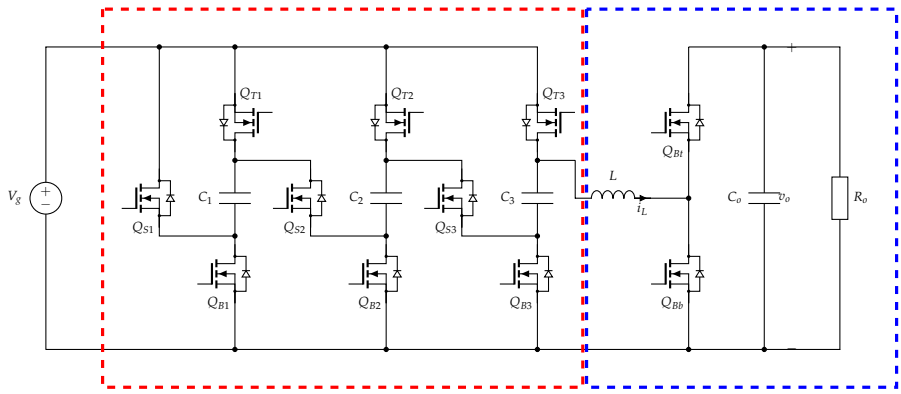


Figure 2. Switched-capacitor boost converter, basic structure of the converter; switched-capacitor circuit in the red frame, boost-converter circuit in the blue frame.

The switched-capacitor (SC) circuit consists of three capacitors C_1, C_2, C_3 and nine switches—six for parallel operation (Q_{T1}, Q_{T2}, Q_{T3}, Q_{B1}, Q_{B2}, Q_{B3}) and three for series operation (Q_{S1}, Q_{S2}, Q_{S3}).

The boost converter (BC) circuit consists of an inductor L, two switches in half-bridge configuration Q_{Bt} and Q_{Bb}, an output filter capacitor C_o, and load resistor R_o. The operation of the converter can be depicted using the diagram shown in Figure 1.

During time interval zT_s, the capacitors are connected in parallel with the voltage source and are charging. The inductor L is also charging along with the capacitors. The gradient of the inductor current i_L is proportional to the voltage source.

During time interval $(1-z)T_s$, the capacitors are connected in series with the voltage source so the inductor L can charge with a higher voltage during the interval $(d-z)T_s$. The gradient of the inductor current i_L is larger.

During the time interval$(1-d)T_s$, the inductor L is connected to the output capacitor C_o and load R_o. The inductor current i_L has a negative gradient and the voltage increases at the output.

3. Converter Modelling

The operation of the converter can be divided into three time intervals, and for each time interval, a subcircuit can be drawn. These subcircuits are shown in Figure 3. The durations of the time intervals for the first, second, and third subcircuits are zT_s, $(d-z)T_s$, and $(1-d)T_s$, respectively.

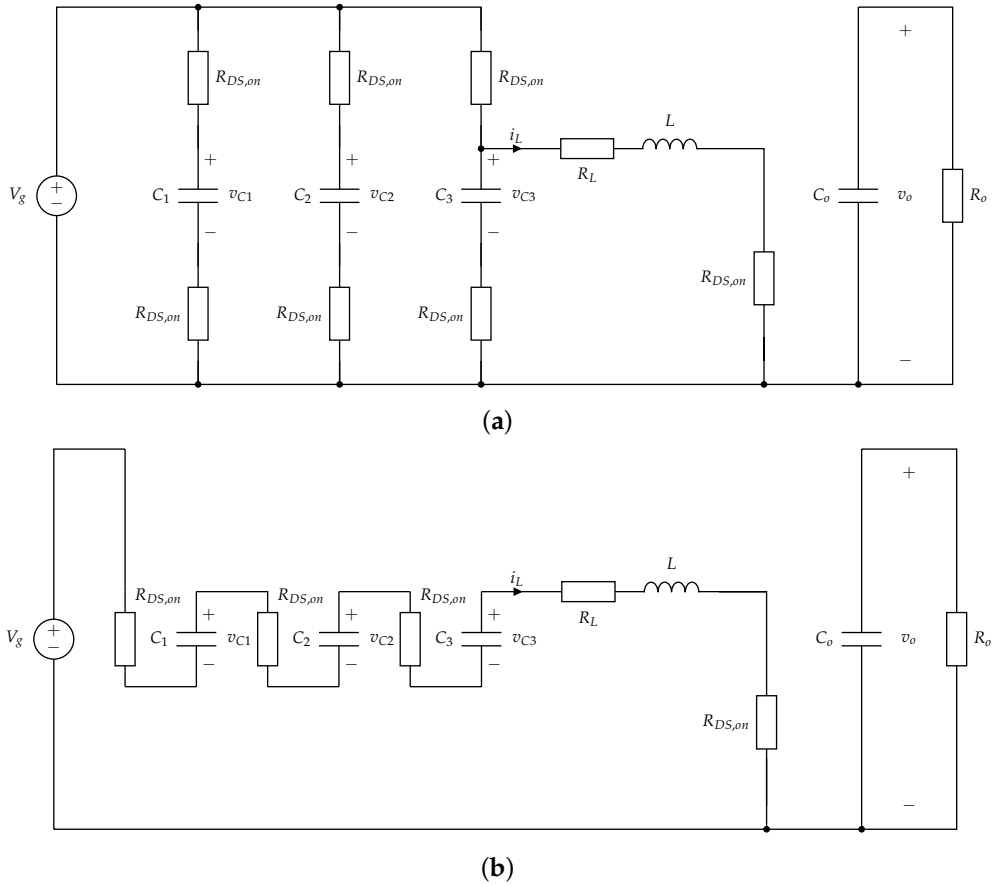
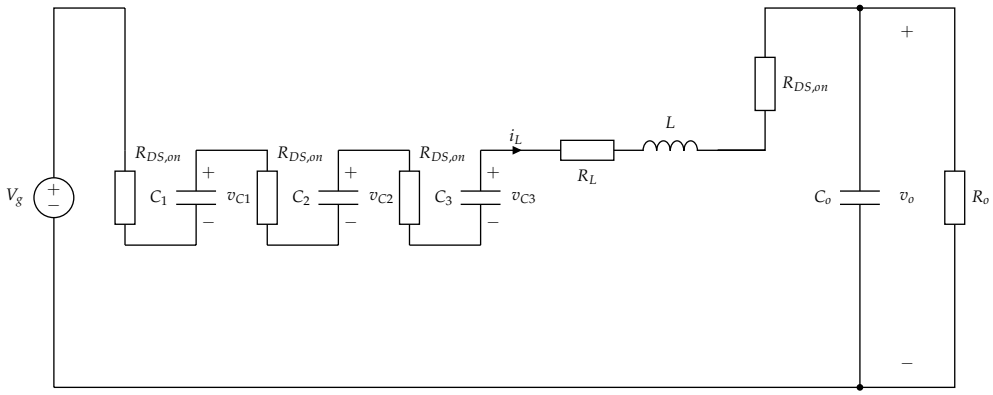


Figure 3. *Cont.*



(**c**)

Figure 3. Subcircuits of the converter; (**a**) subcircuit for time interval $(1-z)T_s$: charging of capacitors C_1, C_2, C_3 and inductor L; (**b**) subcircuit for time interval $(d-z)T_s$: capacitors in series, charging inductor L with higher voltage; (**c**) subcircuit for time interval $(1-d)T_s$: discharging inductor L and boosting voltage.

With the use of the state-space averaging method, the dynamic model and the static characteristics of the converter have been obtained. During the derivation of the equations, it was assumed that the capacitors C_1, C_2, and C_3 were identical, and all MOSFETs used for switching were also identical—all the $R_{DS,on}$ resistances were equal.

3.1. Mathematical Analysis

The converter operation can be divided into three time intervals, represented in Figures 1 and 3. In the first time interval with the duration of zT_s, MOSFETs Q_{T1}, Q_{T2}, Q_{T3}, Q_{B1}, Q_{B2}, Q_{B3}, and Q_{Bb} are switched on. This is represented by the resistors $R_{DS,on}$ in Figure 3a. For simplicity, the resistance $R_{DS,on}$ will be noted as R_Q. The equivalent circuit of this time interval is shown in Figure 3a, and the model, described by state variables v_{C1}, v_{C2}, v_{C3}, i_L, and v_{Co}, can be written as:

$$\frac{dv_{C1}}{dt} = \frac{v_g - v_{C1}}{2R_Q C_1} \tag{1}$$

$$\frac{dv_{C2}}{dt} = \frac{v_g - v_{C2}}{2R_Q C_2} \tag{2}$$

$$\frac{dv_{C3}}{dt} = \frac{v_g - v_{C2}}{2R_Q C_3} \tag{3}$$

$$\frac{di_L}{dt} = \frac{v_g + v_{C3} - i_L(3R_Q + 2R_L)}{2L} \tag{4}$$

$$\frac{dv_{Co}}{dt} = \frac{-v_{Co}}{R_o C_o} \tag{5}$$

In the second time interval with the duration of $(d-z)T_s$, Q_{T1}, Q_{T2}, Q_{T3}, Q_{B1}, Q_{B2}, Q_{B3} are switched off, while Q_{Bb} remains switched on. Q_{S1}, Q_{S2}, and Q_{S3} are switched on. The equivalent circuit of this time interval is shown in Figure 3b, and the model, described by the state variables, can be written as:

$$\frac{dv_{C1}}{dt} = \frac{-i_L}{C_1} \tag{6}$$

$$\frac{dv_{C2}}{dt} = \frac{-i_L}{C_2} \tag{7}$$

$$\frac{dv_{C3}}{dt} = \frac{-i_L}{C_3} \tag{8}$$

$$\frac{di_L}{dt} = \frac{v_g + v_{C1} + v_{C2} + v_{C3} - i_L(4R_Q + R_L)}{L} \tag{9}$$

$$\frac{dv_{Co}}{dt} = \frac{-v_{Co}}{R_o C_o} \tag{10}$$

In the third and final time interval with the duration of $(1-d)T_s$, Q_{Bb} is switched off, and Q_{Bt} is switched on so that the energy stored in the capacitors and inductor can be transferred to the output capacitor and load. The equivalent circuit of this time interval is shown in Figure 3c, and the mode, described by state variables, can be written as:

$$\frac{dv_{C1}}{dt} = \frac{-i_L}{C_1} \tag{11}$$

$$\frac{dv_{C2}}{dt} = \frac{-i_L}{C_2} \tag{12}$$

$$\frac{dv_{C3}}{dt} = \frac{-i_L}{C_3} \tag{13}$$

$$\frac{di_L}{dt} = \frac{v_g + v_{C1} + v_{C2} + v_{C3} - i_L(4R_Q + R_L) - v_{Co}}{L} \tag{14}$$

$$\frac{dv_{Co}}{dt} = \frac{i_L}{C_o} - \frac{v_{Co}}{R_o C_o} \tag{15}$$

Equations (1)–(5) describe the trajectory of state variables in time interval $t \in (0, t_1)$, Equations (6)–(10) in the time interval $t \in (t_1, t_2)$, and Equations (11)–(15) in time interval $t \in (t_2, T_s)$. According to Figure 1, the duty cycles z and d are defined as:

$$z = \begin{cases} 1, & 0 \le t < t_1 \\ 0, & t_1 \le t \le T_s \end{cases} \tag{16}$$

$$d = \begin{cases} 1, & 0 \le t < t_2 \\ 0, & t_2 \le t \le T_s \end{cases} \tag{17}$$

To obtain an average model, the Equations (1)–(5) must be multiplied with the duty cycle signal z, Equations (6)–(10) with the duty cycle signals' combination $(d-z)$, and Equations (11)–(15) with duty cycle signals' combination $(1-d)$. The sum represents a model of the converter as follows:

$$\frac{dv_{C1}}{dt} = \frac{zv_g - zv_{C1} - 2R_Q i_L(1-z)}{2R_Q C_1} \tag{18}$$

$$\frac{dv_{C2}}{dt} = \frac{zv_g - zv_{C2} - 2R_Q i_L(1-z)}{2R_Q C_2} \tag{19}$$

$$\frac{dv_{C3}}{dt} = \frac{zv_g - zv_{C3} - R_Q i_L(2-z)}{2R_Q C_3} \tag{20}$$

$$\frac{di_L}{dt} = \frac{(2-z)v_g + (2-2z)v_{C1} + (2-2z)v_{C2} + (2-z)v_{C3} + i_L(R_Q(5z-8) - 2R_L) + (2d-2)v_o}{2L} \tag{21}$$

$$\frac{dv_o}{dt} = \frac{i_L(1-d)}{C_o} - \frac{v_o}{R_o C_o} \tag{22}$$

By using the state-space averaging method, the converter's operation is also considered by introducing a small signal perturbation around the operating point. Therefore, all state-space variables ($v_{C1}, v_{C2}, v_{C3}, i_L, v_o$), input voltage ($v_g$), and control variables (z, d) in Equations (18)–(22) are described in the form $x = X + \tilde{x}$ [9]. For further calculations, only the average values of state-space variables will be considered, as follows:

$$V_{C1} = \frac{1}{T_s}\int_0^{T_s} v_{C1}dt; \implies v_{C1} \to V_{C1} \tag{23}$$

All state variables shall only be indicated by steady-state operating points:

$$v_{C2} \to V_{C2}; v_{C3} \to V_{C3}; i_L \to I_L; v_g \to V_g; z \to Z; d \to D. \tag{24}$$

By substituting Equations (23) and (24) into Equations (18)–(22), the large-signal non-linear dynamic model of the converter can be obtained:

$$\frac{dV_{C1}}{dt} = \frac{ZV_g - ZV_{C1} - 2R_Q I_L(1-Z)}{2R_Q C_1} \tag{25}$$

$$\frac{dV_{C2}}{dt} = \frac{ZV_g - ZV_{C2} - 2R_Q I_L(1-Z)}{2R_Q C_2} \tag{26}$$

$$\frac{dV_{C3}}{dt} = \frac{ZV_g - ZV_{C3} - R_Q I_L(2-Z)}{2R_Q C_3} \tag{27}$$

$$\frac{dI_L}{dt} = \frac{(2-Z)V_g + (2-2Z)V_{C1} + (2-2Z)V_{C2} + (2-Z)V_{C3} + I_L(R_Q(5Z-8) - 2R_L) + (2D-2)V_o}{2L} \tag{28}$$

$$\frac{dV_o}{dt} = \frac{I_L(1-D)}{C_o} - \frac{V_o}{R_o C_o} \tag{29}$$

3.2. Design of Parameter Z

To ensure that capacitors C_1, C_2, and C_3 are fully charged, a constant duty cycle z shall be set. In order to calculate the value of z, only one branch of the capacitor matrix will be considered, as the capacitor matrix can consist of any number of branches. The number of capacitors in the capacitor matrix is determined by the desired voltage amplification of the converter.

The capacitor branch can be approximated with an RC circuit as shown in Figure 4. The resistance R_{EQ} consists of two $R_{DS,on}$ resistances, marked as R_Q, and the equivalent series resistance of the capacitor.

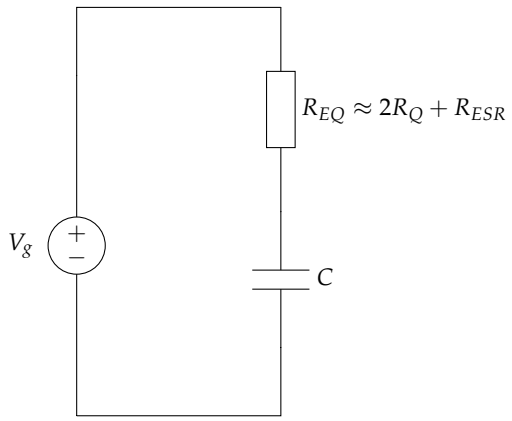


Figure 4. Approximated RC circuit of the capacitor branch.

It shall also be noted that the capacitance in each branch consists of two capacitors. In this way, the R_{ESR} resistance is lowered while the capacitance is increased. In this case,

two capacitors with capacitances $C = 20\,\mu F$ and resistances $ESR = 5\,m\Omega$ were connected in parallel; therefore, the overall capacitance is doubled and the overall resistance of the capacitors is halved.

The capacitor is considered to be fully charged after $t = 5R_{EQ}C$ seconds. With this in mind, a simple equation for determining the duty cycle z is proposed as follows:

$$z_{min} \geq \frac{5R_{EQ}C}{T_s} \tag{30}$$

where R_{EQ} is the equivalent resistance, defined as $R_{EQ} = 2R_Q + R_{ESR}$, C is the capacitance of the capacitor used, and T_s is the switching period of the converter. In the case of this converter, a minimal value of $z = 0.45$ was calculated with the parameters $C = 40\,\mu F$, $R_{EQ} = 22.5\,m\Omega$, and $T_s = 10\,\mu s$.

Based on the switching frequency and the inductors' inductance, care should be taken to select the capacitors with such capacitance, so that the duty cycle z remains relatively low—in our case, under 0.5, to allow sufficient time for inductor charging. The boundary of z was determined experimentally. A method of calculating the branch capacitance of the capacitor matrix is given in [9].

3.3. Comparison to Other Boost Structures

This subsection is dedicated to the analyses of some non-isolated modular boost converter structures found in the relevant literature so that the comparison among them can be adequately made with the possibility to outline certain advantages or drawbacks for potential applications. Table 1 presents a comparison among topologies, where z is a constant, Z presents the minimal duty ratio, N is the number of stages, and n is the number of switched-capacitor cells. The static gain is given for different topologies with regard to the component count and other operating parameters.

All of the topologies presented in Table 1 enable boost operation, where sections of the converter can be organised in modules and replicated to achieve a higher step-up voltage. Each of these boost structures has some convenient features for specific final applications. The cascaded boost topology differs from the rest as the whole section of the boost converter is multiplied to achieve a specific output voltage level. In the remaining topologies, the output voltage is defined by the number of capacitors used in the multiplying voltage section. Compared to other presented topologies, in the SC-BC topology, only one inductor is used, which increases the potential for size optimisation. The high-gain boost topology is closest to the presented SC-BC. As no diodes are used, efficiency can be raised at the expense of the increased complexity of the converter. The drawback of the high-gain boost topology is that the intermediate voltage varies with the duty ratio. With the SC-BC, stable output voltage regulation can be achieved due to the stable intermediate voltage of the switched-capacitor stage. The control design can achieve this by introducing a limited minimal duty ratio. The limitation also presents a drawback and is not a limitation of the converter topology but a limitation set by the control design. The output voltage is defined with the number of capacitors used in the switched-capacitor stage. The voltage stress on the components is highest on the final boost stage, where the levels of remaining components in the switched-capacitor stage can be lower. High output voltages can be achieved by using switched capacitors, but trade-offs must be made between component count, efficiency, and static gain.

Table 1. Comparison with other similar converters.

Characteristic	Topologies of Modular Boost Structures			
	Cascaded boost [13]	Multilevel boost [14]	High gain boost [8]	SC-BC
Voltage stress across switches	V_o	V_o/n	V_o	V_o
Static gain	$(\frac{1}{1-D})^N$	$\frac{n}{1-D}$	$\frac{(n+1)-nzD}{1-D}$	$\frac{(n+1)-nZ}{1-D}$
Number of switches	N, N > 1	1	n + 2	3n + 2
Duty cycle range	0 < D < 1	0 < D < 1	0 < D < 1	Z < D < 1
Number of diodes	N	2n + 1	2n + 1	-
Number of capacitors	N	n + 1	n + 1	n + 1
Operating frequency of magnetics	f_s	f_s	f_s	f_s
Number of inductors	N	N	1	1
Boost modularity	yes	yes	yes	yes

4. Control Algorithm

The control algorithm for an SC-BC converter, presented in [9], is structured as a cascade PI control. The control algorithm changed because the structure of the converter changed slightly due to the synchronous switch stage in the boost converter part, and the fact that the Z duty cycle is always fixed (rather than the product ZD, which changes with the duty cycle D). The changes and the new control algorithm are presented in this section.

Some approximations are used for the derivation of control algorithms, so that the process is less complex. The duty cycle Z is a constant, as it is used to set the charging time for capacitors C_1, C_2, and C_3. Moreover, Equation (28) is simplified with the assumption:

$$V_{C1} \approx V_g; V_{C2} \approx V_g; V_{C3} \approx V_g \tag{31}$$

The simplified system model, used for the control algorithm, is then:

$$L\frac{dI_L}{dt} = (4-3Z)V_g + \frac{5}{2}ZR_QI_L - 4R_QI_L - R_LI_L - V_o(1-D) \tag{32}$$

$$I_L = I_c + I_o \implies I_L = C_o\frac{dV_o}{dt} + \frac{V_o}{R_o} \tag{33}$$

The current control loop was developed using the PI controller and the linearisation method as presented in [15,16], while the voltage control loop was developed using the PI controller. The whole control algorithm is based on the simplified system model represented in Equations (32) and (33).

4.1. Inductor Current (I_L) Control

The inductor current control can be derived using the rearranged Equation (32), rewritten as:

$$L\frac{dI_L}{dt} + ((4-\frac{5}{2}Z)R_Q + R_L)I_L = (4-3Z)V_g - (1-D)V_o \tag{34}$$

The dynamic behaviour of the inductor current is non-linear, so a linearised model was derived from being used with a simple linear controller—a PI controller. The control algorithm block diagram is presented in Figure 5. The right hand side of Equation (34) is represented as:

$$U_{iL} = (4-3Z)V_g - (1-D)V_o \tag{35}$$

The duty cycle $(1-D)$ can be calculated from Equation (35) as:

$$(1-D) = -\frac{1}{V_o}(U_{iL} - (4-3Z)V_g) \tag{36}$$

where the variable U_{iL} is the control variable, and is defined as the output of the controller. The model in Equation (34) can now be represented as a linear system:

$$L\frac{dI_L}{dt} + ((4 - \frac{5}{2}Z)R_Q + R_L)I_L = U_{iL} \tag{37}$$

which, with the use of Laplace transform, results in the following transfer function to be controlled by the controller:

$$G_L = \frac{I_L(s)}{U_{iL}(s)} = \frac{1}{sL + ((4 - \frac{5}{2}Z)R_Q + R_L)} \tag{38}$$

where $I_L(s)$ and $U_{iL}(s)$ are the Laplace transforms of I_L and U_{iL}, respectively.

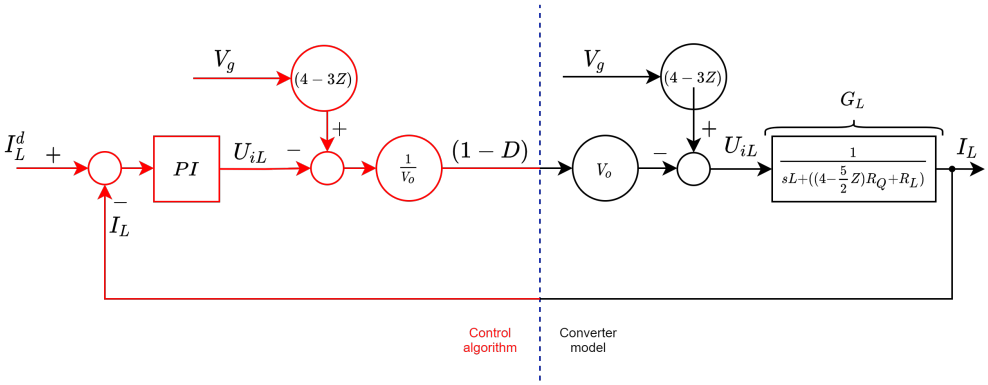


Figure 5. Control algorithm of the inductor current I_L—algorithm in red, converter model in black.

The switching components must be considered as a modulator, which causes the delay T_s [17]. If the switching period is significantly lower than L/R_L or R_oC_o, the modulator transfer function is approximately equal to:

$$G_{sw}(s) = \frac{1 - sT_s/4}{1 + sT_s/4} \approx 1 \tag{39}$$

The measurement of the inductor current I_L must also be considered. A current sensor was used with the bandwidth of $\omega_{mc} = 6.28 \times 10^5$ rad/s. The transfer function of the measurement is presented as:

$$G_{mc}(s) = \frac{1}{sT_{mc} + 1} \tag{40}$$

where $T_{mc} = 1/\omega_{mc}$. The open-loop transfer function $G_{OL}(s)$ is obtained by multiplying $G_{sw}(s)$ presented in Equation (39), $G_L(s)$ presented in Equation (38), and $G_{mc}(s)$ presented in Equation (40) as follows:

$$G_{OL}(s) = G_{sw}(s)G_L(s)G_{mc}(s) \tag{41}$$

The PI controller for the inductor current can be described by the following transfer function:

$$G_{PI\_I} = \frac{U_{iL}(s)}{I_L^d(s) - I_L(s)} = K_{p\_iL}\frac{1 + sT_{i\_iL}}{sT_{i\_iL}} \tag{42}$$

where K_{P_iL} is the controller gain, T_{i_iL} the controller time constant, and $I_L^d(s)$ the Laplace transform of the desired current I_L^d. The complete current mode control block diagram is presented in Figure 6.

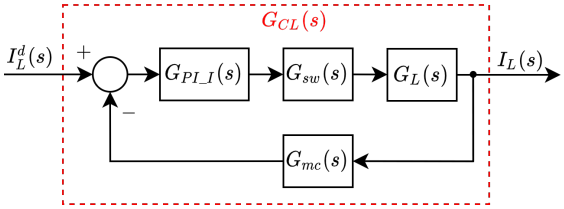


Figure 6. Block scheme—control of the inductor current I_L.

The parameters of the controller have been designed using frequency response analysis, using the bode diagram shown in Figure 7. The controller parameters have been designed at the phase margin of $\Delta\varphi = 45°$ to ensure stability and a fast response. The frequency of the controller has been set to $\omega_c = 7 \times 10^4$ rad s^{-1} to allow for a fast response time, as the current control loop must be faster than the voltage control loop. The values of controller parameters are $K_{p\_iL} = 0.5$ and $T_{i_iL} = 14\,\mu$s.

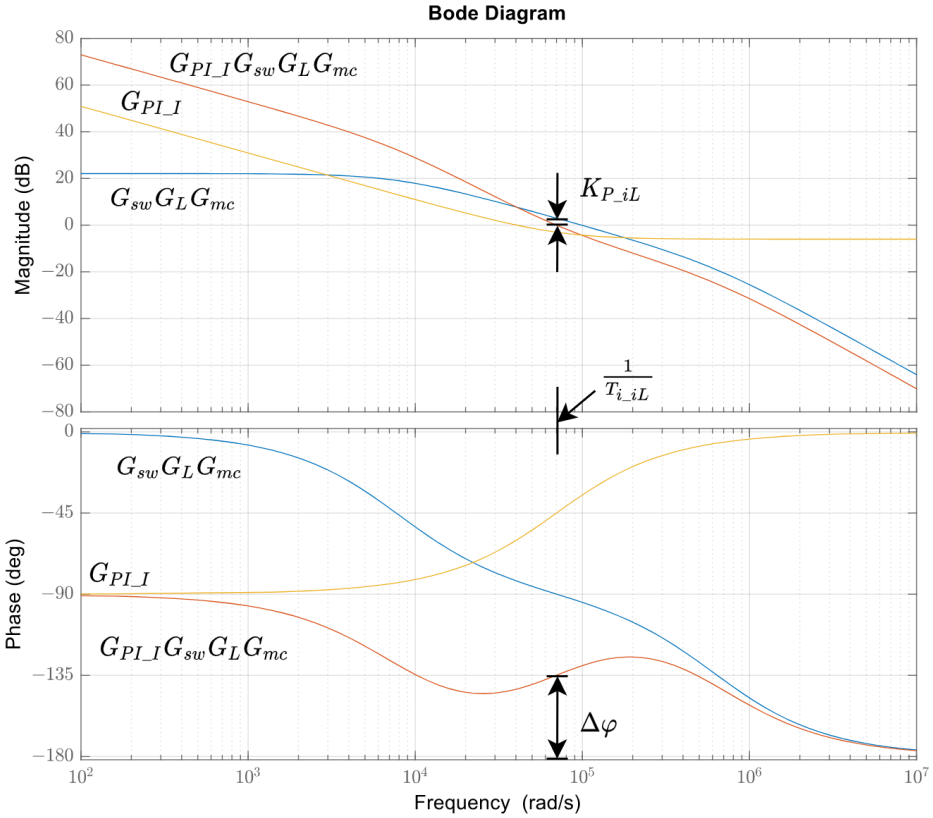


Figure 7. Bode diagram of the current loop.

4.2. Output Voltage (V_o) Control

The output voltage controller was derived using Equation (33). The block scheme of the voltage control loop is depicted in Figure 8. The main transfer function $G_V(s)$ was derived from Equation (33) by using the Laplace transformation and rearranging the terms as:

$$G_V(s) = \frac{V_o(s)}{I_L^d(s)} = \frac{R_o}{sR_oC_o + 1} \tag{43}$$

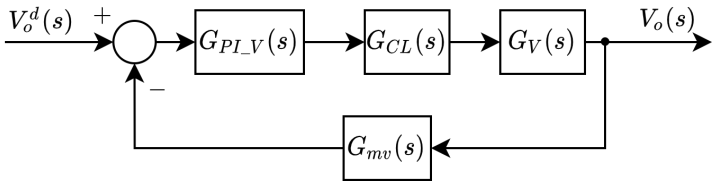


Figure 8. Block scheme—control of the output voltage V_o; control algorithm in red and converter in black.

The transfer function $G_{CL}(s)$ is the closed-loop transfer function of the current control loop and is calculated as:

$$G_{CL}(s) = \frac{I_L(s)}{I_L^d(s)} = \frac{G_{PI\_I}(s)G_L(s)}{1 + G_{PI\_I}(s)G_L(s)} \tag{44}$$

The feedback transfer function representing the voltage measurement has a similar form as the current measurement transfer function used in the current control loop. The bandwidth of the voltage sensor was the same as that of the current sensor, and was $\omega_{mv} = 6.28\,\text{rad/s}$. Then, the transfer function in the feedback loop is:

$$G_{mv}(s) = \frac{1}{sT_{mv} + 1} \tag{45}$$

where $T_{mv} = 1/\omega_{mv}$. The only missing transfer function from Figure 8 is the transfer function of the PI controller, which is written as:

$$G_{PI\_V}(s) = \frac{I_L^d(s)}{V_o^d(s) - V_o(s)} = K_{p\_Vo}\frac{1 + sT_{i\_Vo}}{sT_{i\_Vo}} \tag{46}$$

where K_{p_Vo} is the controller gain and T_{i_Vo} is the controller time constant. $V_o^d(s)$ is the Laplace transform of the desired voltage V_o^d. The bode plot of the voltage control loop is presented in Figure 9, where the $G_{CL}G_VG_{mv}$ curves have been plotted for different load situations. This is shown in Figure 9, where the red line presents the response with nominal load and the yellow dotted line and the blue dotted line present the minimum and the maximum load responses, respectively. The latter was used to design the controller parameters, based on the phase margin principle to ensure stability for all load responses. The phase margin was set to $\Delta\varphi = 50°$ as a starting point from which the controller parameters have been designed. The controller parameters are $K_{p\_Vo} = 0.01$ and $T_{i\_Vo} = 0.67\,\text{ms}$. With the designed parameters, the response time of the controller has been improved, while maintaining the stability of the control.

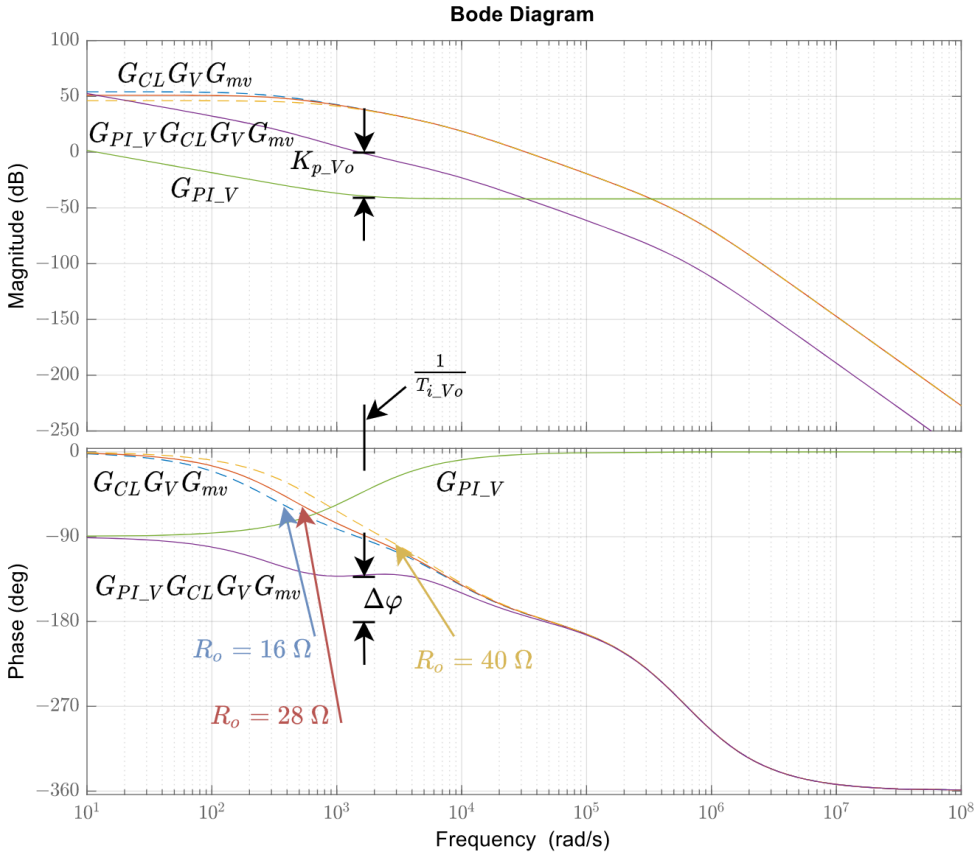


Figure 9. Bode diagram of the voltage loop.

5. Results

A 5 W experimental prototype was built of the SC-BC converter. For simulation results, MATLAB/Simulink was used along with the Simscape Toolbox. The experimental setup shown in Figure 10 consists of multiple building blocks. The block scheme of the setup is presented in Figure 11. The values of the passive components, chosen for the converter, are as follows: $C_1 = C_2 = C_3 = 40\,\mu F$, $L = 10\,\mu H$, $R_L = 50\,m\Omega$, and $C_o = 44\,\mu F$. The base value of the load was set to $R_o = 28\,\Omega$, with the ability to change it to $R_o = 16\,\Omega$ and $R_o = 40\,\Omega$. The switching elements are N-type MOSFETs (Fairchild FDS5672) with an ON resistance of $R_{DS,on} = 10\,m\Omega$, which were controlled using a digital signal controller (Texas Instruments TMS320F28739D) and MOSFET drivers (Silicon Labs Si8232BB). The controller was programmed using the MATLAB/Simulink Embedded Coder (for TI C2000 microcontrollers). The power supply was set to $V_g = 2\,V$. To ensure the operation of the converter, the duty cycle D shall not be lower than the duty cycle Z.

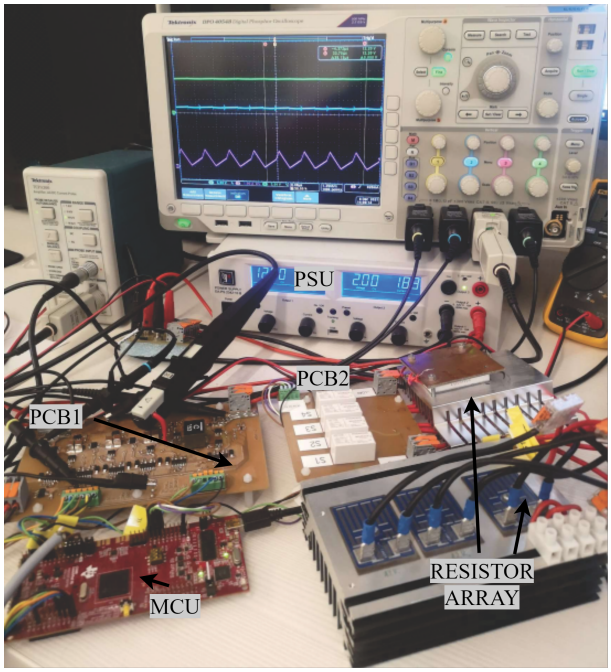


Figure 10. Prototype converter experimental setup.

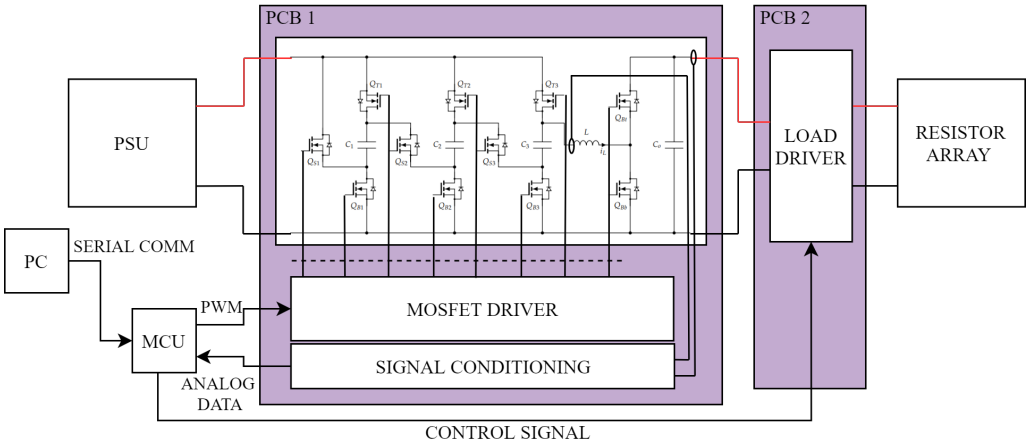


Figure 11. Prototype converter block scheme; PSU—power supply unit, PCB1—SC-BC converter along with MOSFET drivers and measurement circuit, PCB2—load switching electronics, RESISTOR ARRAY—load stage with multiple power resistors, MCU—digital signal processor, controlling subcircuits and connected to a PC via a serial connection to allow parameter changes.

5.1. Static Gain Verification

The static gain characteristic of the converter is shown in Figure 12a. The area marked in red is the area of interest for experimental verification of the static gain of the converter. The duty cycle $Z = 0.45$ was set constant, and the duty cycle D was changing. The output voltage of the converter was measured with a digital multimeter (Fluke 115), and the experimental results are presented in Table 2. The comparison of measured and calculated voltage gains is presented in Figure 12b, where the blue line represents the calculated data and the red markings represent the measured data.

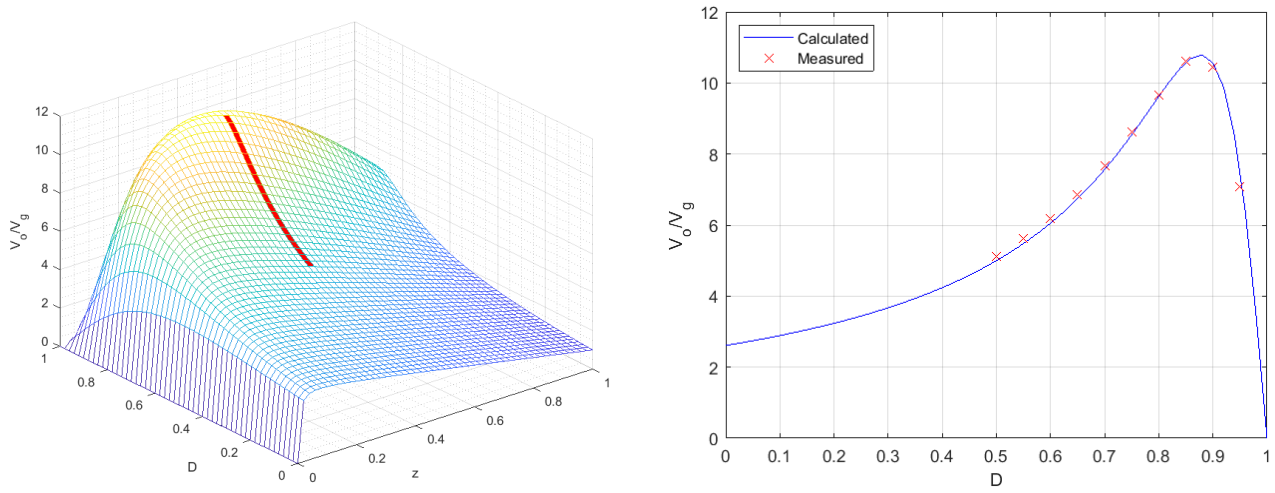


Figure 12. Voltage gain V_o/V_g of the converter; (**a**) calculated static characteristic (function of Z and D); (**b**) static characteristic at $Z = 0.45$—red crosses (measured), blue line (calculated).

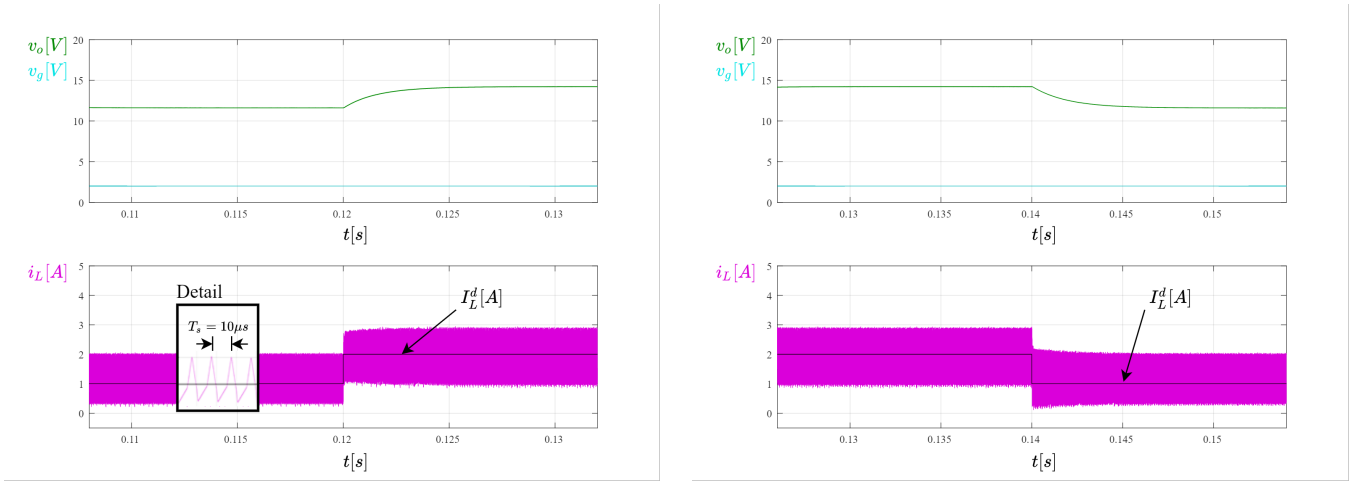
Table 2. Static characteristic measurement result; $V_g = 2\,\text{V}$, $z = 0.45$, and $R_o = 28\,\Omega$.

D	$V_o[V]$	V_o/V_g
0.50	10.37	5.13
0.55	11.35	5.67
0.60	12.45	6.23
0.65	13.73	6.87
0.70	15.41	7.71
0.75	17.32	8.66
0.80	19.36	9.68
0.85	21.24	10.62
0.90	20.90	10.45
0.95	14.15	7.07

The maximal distance between measured data points (red crosses) and calculated gain (blue line) is $\epsilon = \pm 5\,\%$. The measured and calculated data point out that a maximum duty cycle of $D_{max} = 0.85$ is practical for normal converter operation. The duty cycle shall be constrained within the area $D \in (0.45, 0.85)$. Due to the duty cycle constraint, the output voltage is also constrained. According to the theoretical and experimental validation, it can be concluded that the developed gain model gives accurate results.

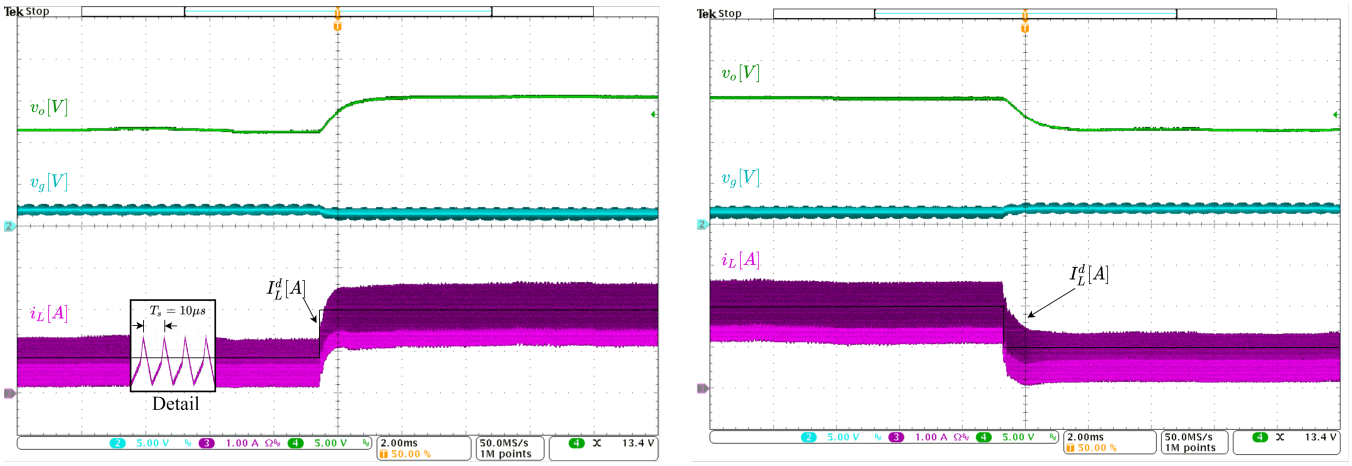
5.2. Inductor Current Control

The inductor current control has been investigated with simulations and afterwards validated with an experiment. The output current I_o (current through the load R_o) has been controlled by controlling the inductor current I_L. The simulation result of a reference change from $I_L^d = 1\,\text{A}$ to $I_L^d = 2\,\text{A}$ is shown in Figure 13a, while the simulation result of a reference change from $I_L^d = 2\,\text{A}$ to $I_L^d = 1\,\text{A}$ is shown in Figure 13b. The corresponding experimental results are shown in Figure 14a,b, respectively. The capacitor charging duty cycle has been set to $Z = 0.45$ and the load resistance was set to $R_o = 28\,\Omega$. In both cases, the simulation and experimental results, the output voltage v_o is presented in green, the input voltage v_g in blue, and the inductor current i_L in violet, along with the reference current I_L^d in black.



(**a**) (**b**)

Figure 13. Simulation results of current control, $Z = 0.45$, $R_o = 28\,\Omega$; (**a**) reference change from 1 A to 2 A; (**b**) reference change from 2 A to 1 A.

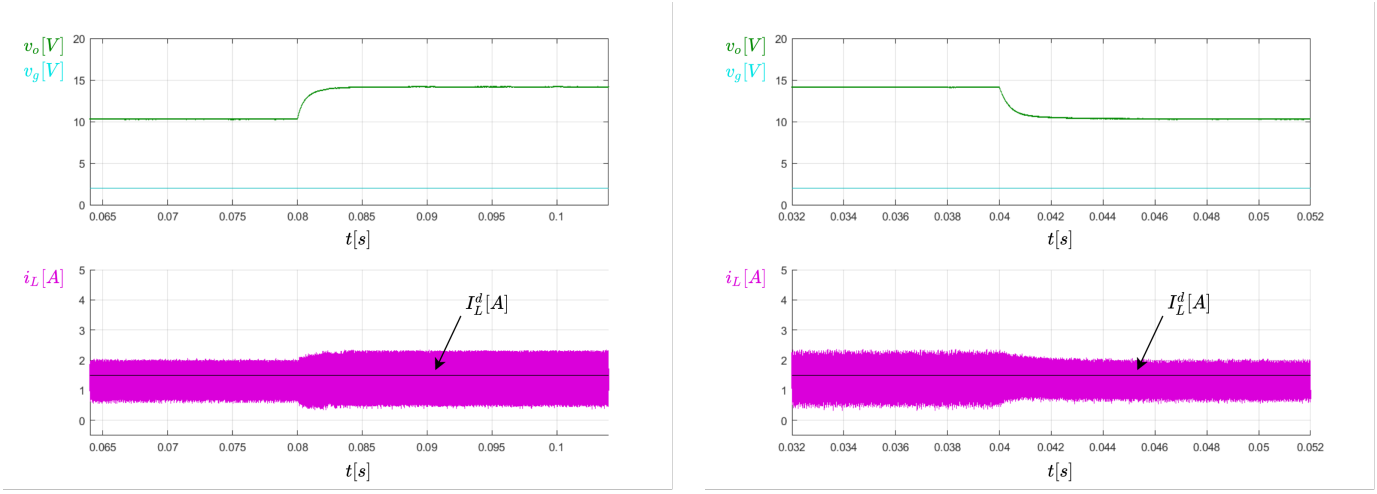


(**a**) (**b**)

Figure 14. Experimental results of current control, $Z = 0.45$, $R_o = 28\,\Omega$; (**a**) reference change from 1 A to 2 A; (**b**) reference change from 2 A to 1 A; x-axis 2 ms, y-axis V_o,V_g-5 V/div, i_L-1 A/div.

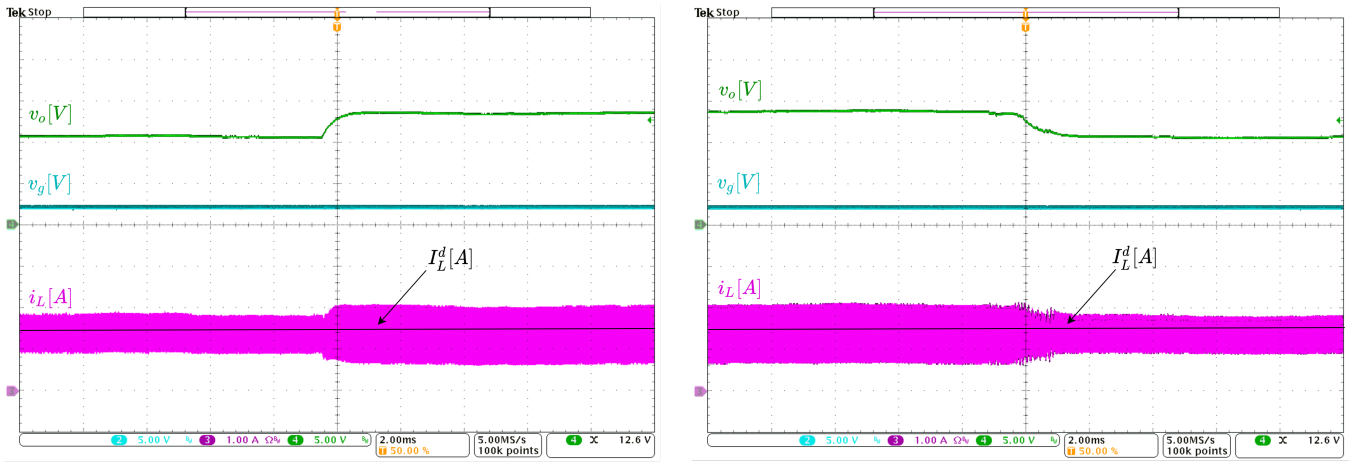
In both cases, the simulations and the experiments, precise tracking of the inductor current can be observed. To represent the switching action of the converter, a detailed cut-out of the inductor current in a smaller time frame was inserted in Figures 13a and 14a to show the behaviour of the inductor current.

The simulation results of load change under operation during current control are shown in Figure 15. Figure 15a shows the results of load change from $R_o = 16\,\Omega$ to $R_o = 28\,\Omega$, while Figure 15b shows the results of the load change from $R_o = 28\,\Omega$ to $R_o = 16\,\Omega$. The experimental results are shown in Figures 16a and 17b, respectively. The reference current was set to $I_L^d = 1.5$ A.



(**a**) (**b**)

Figure 15. Simulation results of current control, $Z = 0.45$, $I_L^d = 1.5$ A; (**a**) load change from 16 Ω to 28 Ω; (**b**) load change from 28 Ω to 16 Ω.



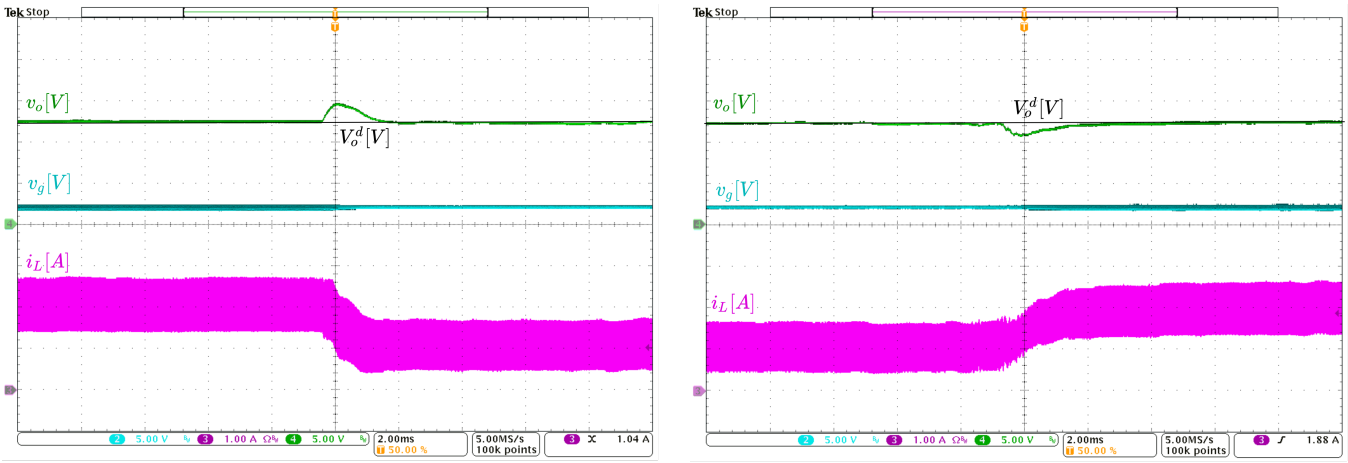
(**a**) (**b**)

Figure 16. Experimental results of current control, $Z = 0.45$, $I_L^d = 1.5$ A; (**a**) load change from 16 Ω to 28 Ω; (**b**) load change from 28 Ω to 16 Ω; x-axis 2 ms, y-axis V_o,V_g-5 V/div, i_L-1 A/div.

Again, the output voltage v_o is shown in green, the input voltage v_g in blue, and the inductor current i_L in violet, while the reference current I_L^d is shown in black. The load variation rejection was completed in approximately 0.5 ms in the change from $R_o = 16\,\Omega$ to $R_o = 28\,\Omega$, and approximately 1 ms in the change from $R_o = 28\,\Omega$ to $R_o = 16\,\Omega$.

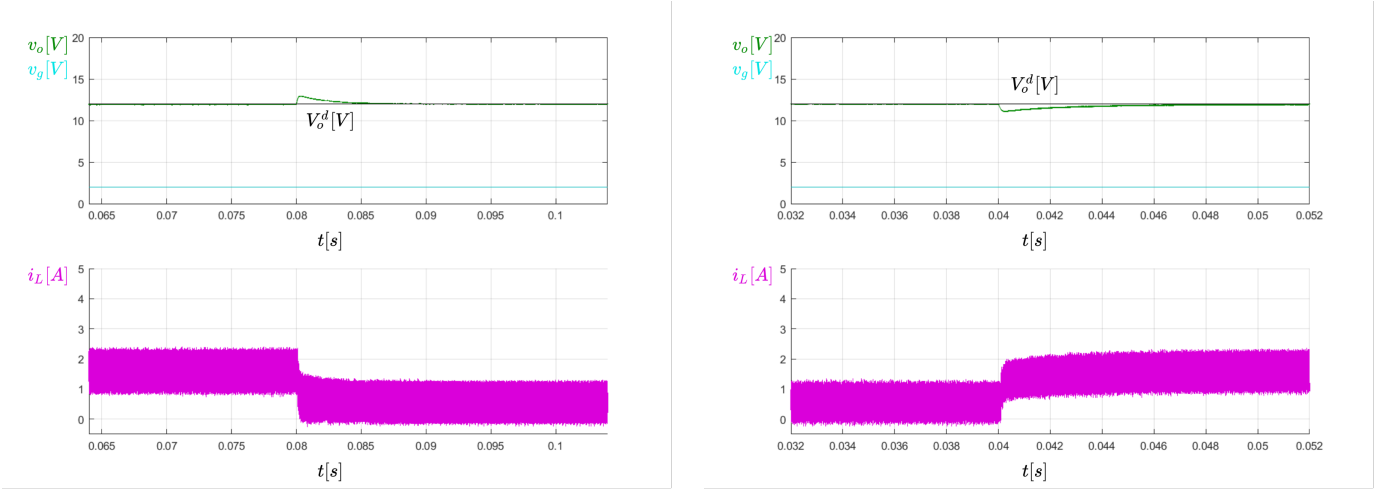
5.3. Output Voltage Control

The output voltage control is demonstrated similarly to the inductor current control, with simulation and experimental results. In this case, however, only load variation detection was tested, since the output voltage reference change is not practical. Figure 18a,b show the simulation results of the load change from $R_o = 16\,\Omega$ to $R_o = 28\,\Omega$ and from $R_o = 28\,\Omega$ to $R_o = 16\,\Omega$, respectively, while the reference output voltage was set to $V_o^d = 12$ V. Figure 17a,b show the experimental results of the aforementioned load changes.



(**a**) (**b**)

Figure 17. Experimental results of voltage control, $Z = 0.45$, $V_o^d = 12\,\mathrm{V}$; (**a**) load change from 16 Ω to 28 Ω; (**b**) load change from 28 Ω to 16 Ω; x-axis 2 ms, y-axis V_o,V_g-5 V/div, i_L-1 A/div.



(**a**) (**b**)

Figure 18. Simulation results of voltage control, $Z = 0.45$, $V_o^d = 12\,\mathrm{V}$; (**a**) load change from 16 Ω to 28 Ω; (**b**) load change from 28 Ω to 16 Ω.

A good load variation rejection can be observed in Figures 17a,b, as the transient was relatively fast, in the range of 2 ms, while the load change was relatively large. The overshoot and undershoot were in the range of 10–15%, which could be improved. In the case of overshoot, the maximum voltage was 13.8 V, which results in a 15% overshoot, and in the case of the undershoot, the lowest voltage was measured in 10.8 V. The undershoot was estimated at 10%. The overshoot and undershoot performance could be improved using a different control algorithm. A sliding mode control algorithm could prove useful for such a non-linear system. Altogether, the reference tracking of the voltage controller was satisfactory.

5.4. Comparison of Control with Similar Converters

Some work regarding the converter presented in [8] was done in [18]. Although the input parameters are not identical to the input parameters of this converter, some comparisons can be made.

A cascaded PI controller approach that was introduced in [9] was revisited and simplified by decoupling the duty cycles Z and D. This paper now presents the simplified version of the cascaded PI control along with the experimental results. The authors of [18]

used a different approach. A cascaded control structure was also implemented; however, a different type of controller has been used for the current control loop.

The inner-current control loop in [18] was synthesised using the sliding-mode approach, which was implemented by using a hysteresis controller. The outer-voltage control loop was implemented using the PI controller. While the experimental results presented in [18] show good tracking, the response times are significantly slower compared to the experimental results presented in this paper. The two, however, cannot be directly compared as some parameters of the converter differ.

To compare the experimental results from [9] to the experimental results in this paper, it can be observed that, in both cases, tracking has been achieved and the response times are similar (the response times in this paper are slightly faster). The difference between the algorithms in [9] and this paper with decoupling duty cycles Z and D is that reduced complexity of the algorithm was achieved.

6. Discussion

By replacing the diode with a MOSFET in the boost converter part of the converter so that the boost converter has a synchronous switching stage, and by setting the duty cycle Z to a constant value, based on the passive components of the converter (the capacitor tank), the converter's properties changed significantly, as opposed to the converter discussed in [9]. In the previous version of the converter, the duty cycle z was multiplied with the boost duty cycle D to obtain the duty cycle ZD. As the multiplication implies, the duty cycle ZD changed with the dynamic of the controller output and could not be set constant. As a consequence, the capacitors in the capacitor tank were being charged for a longer time than needed, or were not charged to their full charge. This led to the non-optimal operation of the converter. By only using the duty cycle Z as the factor to charge and discharge the capacitors in the capacitor tank, a uniform charge on the capacitors can be achieved, and with a more constant voltage at the input of the boost part of the converter. A known control method was used for this type of converter structure, which presents a new approach. Several new advantages are gained regarding the converter operation by decoupling the "Z" and "D" parameters, such as converter design optimisation, the time frame separation of charging and boosting cycle, and intermediate voltage stabilisation, which would require some additional research.

The mathematical model of the converter was rewritten to take into account the change in the operation. The substitution of the boost converter diode, which changed the classical boost converter switching stage to a synchronous one, was also taken into account.

It was found that the MOSFETs' $R_{DS,on}$ resistances had a significant impact on the voltage amplification ratio, as well as the inductors' equivalent series resistance. By minimising the parasitic resistances, i.e., the $R_{DS,on}$ and the R_L resistances, the converter efficiency could be improved, as well as the voltage amplification ratio.

With a new mathematical model, the control algorithm was also modified, as the converter's operation changed. It was found that the converter's output voltage can be controlled by using only the linearisation approach in the inductor current control portion of the control algorithm, as opposed to using the linearisation in both portions (the current and voltage part) of the control algorithm, as presented in [9]. The linearisation part of the current control loop was also simplified in this work due to the decoupling of duty cycles. The presented experimental results show increased performance of the control algorithm as opposed to the results in [9].

In future work, the focus will be on reducing the parasitic resistances of the passive and active components and implementing a non-linear control scheme, such as a Super-Twisting Algorithm, or a similar higher-degree sliding mode control. Furthermore, a battery charging application could be tested.

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