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Novel Approach and Methods for Optimizing Highly Sensitive Low Noise Amplifier CMOS IC Design for Congested RF Environments

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Abstract: This work details the optimization and evaluation of a CMOS low-noise amplifier by developing a new algorithm for the g_m/I_D approach and combining with a modified figure of merit index method. The amplifier includes on-chip matching elements (such as IC inductors) for resonance at the targeted frequencies. The simulation results of the optimized LNA model showed scattering parameter S_{21} = 19.91 dB, noise figure NF = 3.54 dB and excellent linearity for third-order intermodulation parameter IIP3 = 5.89 dBm for the targeted frequency of f_0 = 2.4 GHz.

Keywords: g_m/I_D design; figure of merit; low noise amplifier; RF front-end module; RFIC

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1. Introduction

In the current congested RF spectrum of mobile communications, Internet-of-Things, RADAR, wireless internet, and digital systems can be exposed to various sources of interference, resulting in critical cybersecurity threats [1]. Most of systems utilize RF front-end modules, such as low noise amplifiers (LNAs) and mixer circuits. Reliable modeling and implementation of such integrated circuits are increasingly more challenging due to the evolving submicron technologies. For this reason, our work introduces an efficient optimization technique and analysis of an LNA utilizing the g_m/I_D algorithm and the figure of merit index method combined.

The design concentrates on low noise and high linearity applications to guarantee robustness in congested RF environment while still providing sufficient levels of power gain, bandwidth, and power dissipation. This design methodology is relevant in that it provides a directly applicable and a quantitative way to achieve a target performance of RF mm-wave circuits. Furthermore, it can even be applied to a broad range of transistor-based analog circuits such as amplifiers, regulators, phase-lock loops implemented with deep sub-micron CMOS designs. Previous studies demonstrated the reliability of the g_m/I_D design approach for submicron technologies [2,3]. This design approach characterizes the transistor model for quantitative analysis by developing data charts of pre-evaluated data of g_m/I_D, f_t, and I_D/W.

Based on these data, this methodology leads circuit designers to systematic design procedures which are superior alternatives to the infamous MOSFET square law that does not match with real submicron MOSFET behavior. This is possible since the design approach focuses on key design factors, such as unity gain frequency, transconductance efficiency, and current density of transistor devices, combined with the figure-of-merit index to estimate its maximum potential performance. Often, analog/RF integrated circuits deal with various performance factors, such as gain, linearity, power, and noise. Hence, the designers have to make appropriate decisions to satisfy design requirements and the FoM becomes a clear indicator to quantify the design validity.

The importance of this kind of standardized design approach is becoming more and more important due to two trends: decreases in minimum transistor length L, and

increasing operation frequency in an RF field, reaching the domain of mm-wave frequency. The suggested g_m/I_D-based design methodology combined with the FoM in this paper can be broadly adapted in sub-micron analog circuit designs, overcoming the complexity and ambiguity that so many circuit designs struggle with.

2. Design Topology and Strategies

2.1. Circuit Topology

A cascode amplifier with inductive load and degeneration is appropriate for such a design goal and selected for evaluation in our work. Various different topologies can be applied for the implementation of LNAs, including common source [4,5], common gate [6,7], and cascode amplifiers [8,9]. In addition, resistive feedback [10] and noise-cancelling [11] LNAs are available options depending on the focus of design.

Our model focuses on low noise and high linearity with moderate gain, bandwidth, and power dissipation. The inherent characteristics of a cascode amplifier topology are beneficial in terms of gain, linearity, and bandwidth; hence, our work focus is in the cascode topology, in spite of the slightly higher noise figure due to the addition of one more transistor than common source and common gate structures. Figure 1 shows the circuit schematic of the cascode amplifier. The amplifier incorporates an inductive degeneration component L_S, a gate inductor L_G, and an output resonance inductor L_D. L_G and L_S are designed for 50 Ω input impedance matching purpose. The input impedance of this circuit is equivalent to the equation below.

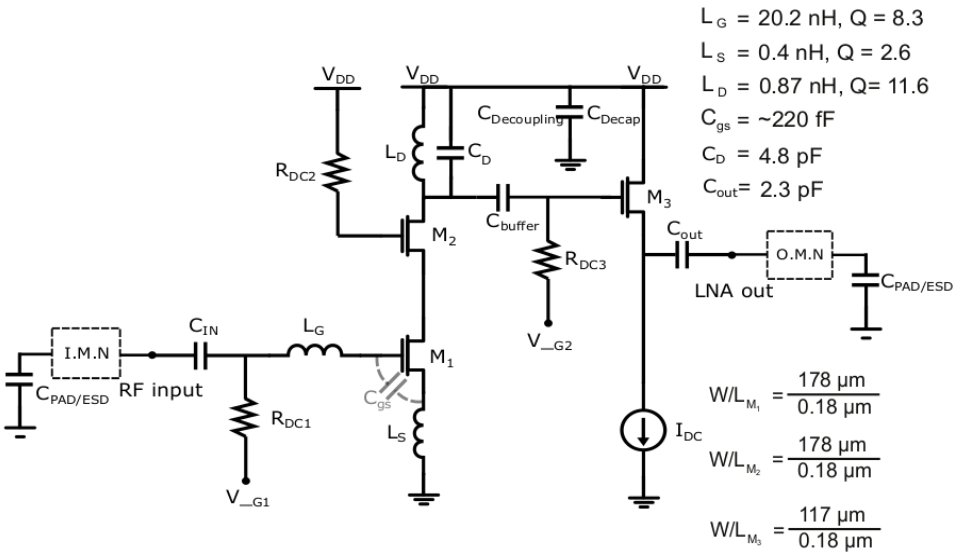

Figure 1. The schematic of cascode amplifier circuit.

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + (\frac{g_{m1}}{C_{gs}})L_s \tag{1}$$

The first and the second term of (1) are cancelled out at the operating frequency f_0 = 2.4 GHz and the real term $(g_m/c_{gs})L_S$ matches to R_S. Similarly the inductive load L_D forms a LC tank with C_{gd} of M2 and C_d at the drain node of the cascode amplifier to resonate at the f_0 = 2.4 GHz. The buffer stage M3 is followed after the cascode amplifier stage for 50 Ω output impedance matching. The width of M1, M2 transistors usually match to accommodate the same amount of current through the transistors. The width determination process of W_{M1}, W_{M2}, and V_{ov} is discussed in the following section. The noise figure is defined in (2).

$$NF = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}(1 + \omega^2 c_{gs}^2 (R_s + R_g)^2)^2 \tag{2}$$

where $K = uC_{ox}\frac{W}{L}$, R_g is gate resistance, R_s is source resistance, γ/α is about 2/3 for long channel device and 2 for short channel device [12]. The second term represents gate induced noise from the gate resistance R_g which can be minimized with efficient layout. With assumption that R_s» R_g , the second term can be neglected. The third term describes the thermal noise from a MOSFET device. At a high frequency, $\omega^2 c_{gs}^2 (R_s + R_g)^2$ » 1 since $\omega > \omega_t$. The linearity IIP3 is difficult to be equated due to its complexity. Although there are multiple factors that affect IIP3 level, the biggest factor would be the nonlinear transconductance term g_{m3}. Suppression of g_{m3} can be key to improving IIP3. In short, it is barely possible to quantify IIP3 into a formula, hence it will be optimized by the g_m/I_D algorithm and the FoM combination.

2.2. Parameters Determination Strategy

The g_m/I_D algorithm suggests a quantitative circuit design guidance for submicron MOSFET devices. To start the g_m/I_D based design, three reference charts need to be generated. These are: g_m/I_D vs. V_{ov} and f_t vs. V_{ov} (Figure 2), I_D/W vs. g_m/I_D (Figure 3) at V_{DS} = 900 mV, L = 180 nm. g_m/I_D vs. V_{ov} describes the transconductance efficiency w.r.t V_{ov} which is equivalent to power efficiency. f_t vs. V_{ov} represents a unity current gain frequency w.r.t V_{ov} that implies a capable maximum speed of MOSFETs. I_D/W vs. g_m/I_D stands for the current density for unit width w.r.t transconductance efficiency serving as a reference to determine device width depending on the V_{ov} and the current. A design flow for this LNA proceeds in the following steps:

Step 1. Set the power budget by setting current I_D through the cascode amplifier.
Step 2. Determine the channel length.
Step 3. Vary V_{ov} and find corresponding g_m/I_D points.
Step 4. Get I_D/W for the g_m/I_D points from step 3.
Step 5. Compute width for the values in step 4.
Step 6. Run simulations on gain, noise figure, and linearity.
Step 7. Evaluate the FoM and finalize parameters.

The design optimization starts with fixing a power budget. A moderate power consumption is desired and was set to $P_{dc} = V_{DD} \times I_D$ = 1.8 V × 5 mA = 9 mW. Thus, the current through the cascode amplifier is fixed to 5 mA based on this definition. The next step is to determine the channel length of M1 and M2. ω_t, i.e., g_m/c_{gs}, is inversely proportional to L^2 and accordingly low ω_t lessens intrinsic gain potential and escalates noise figure as described in (2). To obtain better performance in noise and speed, the channel length is set to the minimum length, L = 180 nm.

Then, V_{ov} is adjusted to find an appropriate g_m/I_D for the design. The data chart (Figure 2) demonstrates the trend as V_{ov} increases, g_m/I_D decreases while f_t increases. In other words, when V_{ov} is high (strong inversion), g_m/I_D is low and f_t is high, while in weak inversion where V_{ov} is low, g_m/I_D is high and f_t is low. Next, the gain, noise, linearity, and power are evaluated, and, finally, the figure of merit FoM, is evaluated from (3) below:

$$FoM = \frac{S_{21} \times IIP3}{(NF - 1) \times P_{DC}} \tag{3}$$

This FoM allows the designer to finalize the appropriate V_{ov} and its corresponding W_{M1}, W_{M2}.

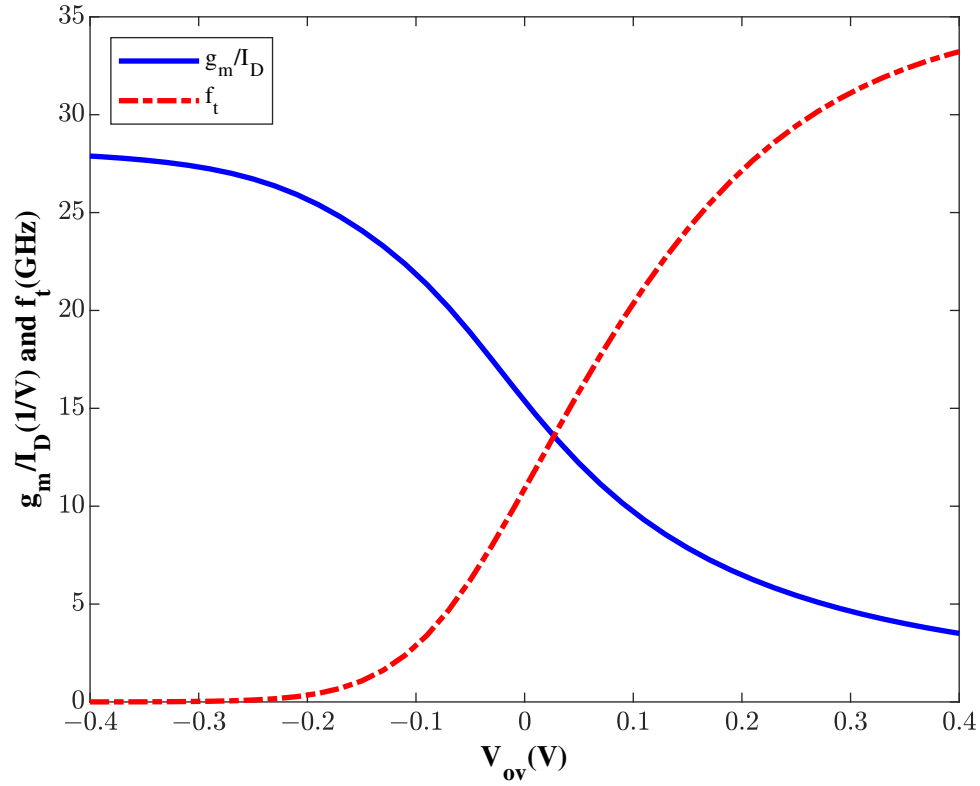

Figure 2. g_m/I_D, f_t vs. V_{ov} data chart.

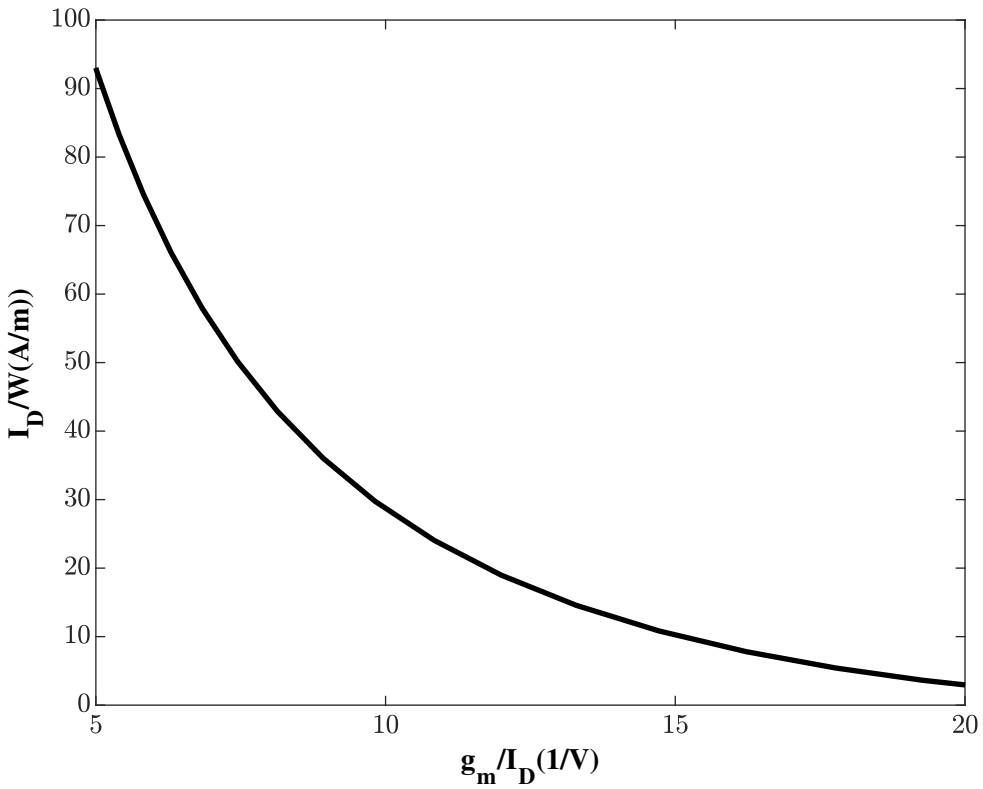

Figure 3. I_D/W vs. g_m/I_D data chart.

3. Simulation Results and Parameter Set-Up

To define the optimal bias point where noise, linearity, and gain level satisfy our targeted performance, simulations of S_{21}, NF, and IIP3 are executed with the V_{ov} values shown in Table 1, and the FoM is computed. By analyzing the results in Table 1, an optimal bias point is defined to be 0.1 V as detailed in Section 3.1 below.

Table 1. The LNA parameters according to V_{ov}.

V_{ov} (V)	g_m/I_D (1/V)	f_t (GHz)	S_{21} (dB)	IIP3 (dBm)	NF (dB)	W (μm)	FoM
0	25.6	2.8	19.72	4.47	4.1	588	3.16
0.05	12.2	11	20.21	4.87	3.98	295	3.67
0.1	10	15.8	19.91	5.89	3.54	178	3.62
0.15	7.9	20	18.62	6.52	5.62	117	2.92
0.2	6.5	24.1	16.6	7.9	6.2	84	2.8
0.25	5.4	27	15.3	8.96	6.45	65	2.79
0.3	4.6	31	13.21	10.21	7.89	74	2.17

3.1. Simulation for Each V_{ov}

The simulation is run on S_{21} (Figure 4), NF (Figure 5) and IIP3 (Figure 6) for V_{ov} from 0 to 0.3 V in 50 mV steps. Table 1 indicates that the FoM is inversely proportional to V_{ov} providing strong insight for a parametric optimization except at V_{ov} = 0 V. However, f_t is too small at V_{ov} = 0 V suggesting the realistic bias point is V_{ov} above 0.05 V. Additionally, the device width for each V_{ov} is computed from the I_D/W chart (Figure 3) and Table 1. P_{DC} is 9 mW for all cases.

Inspecting the results, we see that the best S_{21} and NF response is at V_{ov} = 0.05 V while IIP3 improves as V_{ov} increases. The results verified that the optimal gain and noise occurs at moderate inversion, while the linearity showed better response in the strong inversion layer domain. Hence, the optimal bias point for this application is in a moderate inversion domain corresponding to V_{ov} = 0.1 V, resulting in low noise, high linearity, and moderate gain.

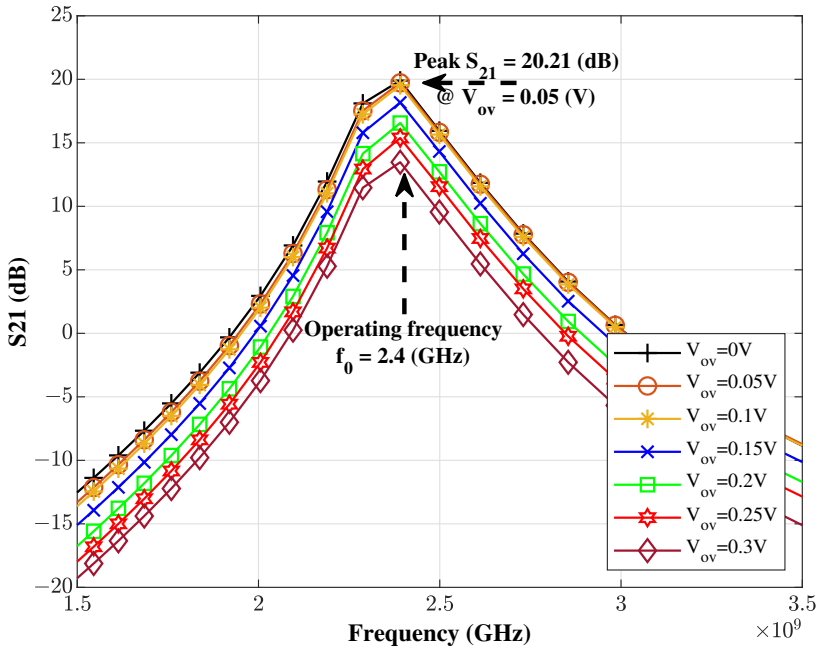

Figure 4. S_{21} vs. frequency.

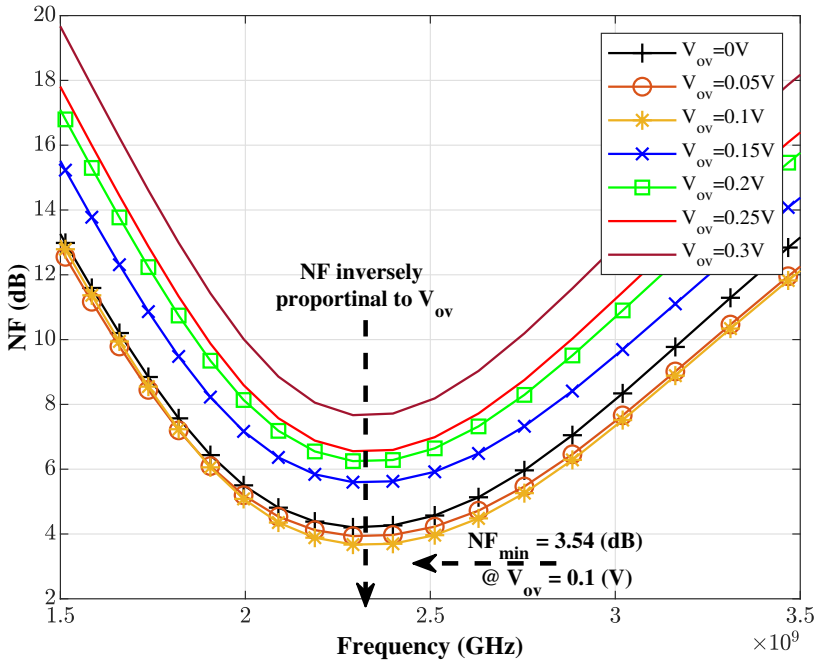

Figure 5. Noise Figure vs. frequency.

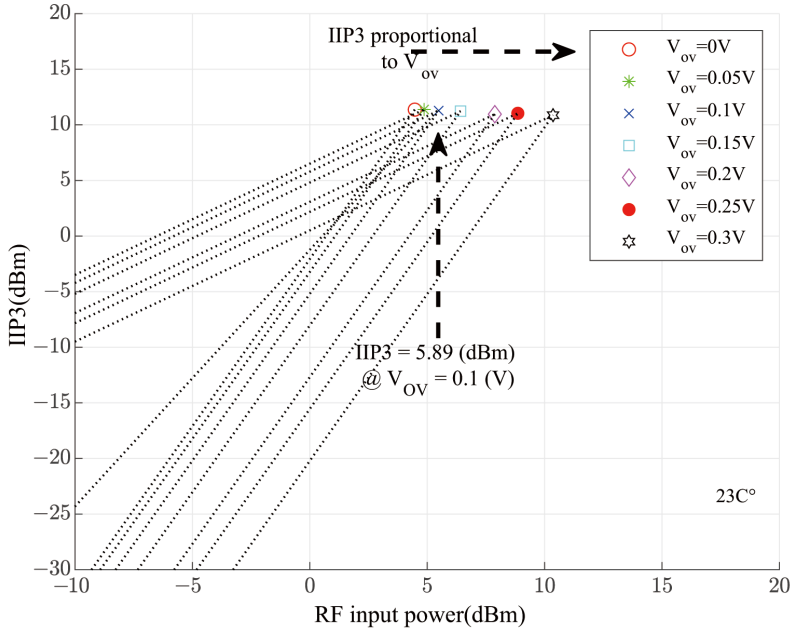

Figure 6. Third-order intercept point vs. V_{ov}.

3.2. Optimized Parameters and Reliability Simulations

Thus, for optimal bias point V_{ov} = 0.1 V, the reference data (Figure 2) and (Figure 3) indicate that g_m/I_D = 10 (m/V), f_t = 20 (GHz), I_D/W = 28 (A/m) for a device width W_{M1}, W_{M2} is 178 µm (Table 1), and for these optimized parameters, S_{21} = 19.91 dB, NF = 3.54 dB, and IIP3 = 5.89 dBm.

Several reliability tests were also carried out, which are: stability, PSRR and PVT simulations. First, stability simulation was performed by validating the K factor and the Δ factor(=B1f) which are equal to

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2|S_{22}||S_{12}|} \quad (4)$$

$$\Delta = 1 + |S_{11}|^2 - |S_{22}|^2 - |D|^2 \quad (5)$$

where $D = |S_{11}S_{22} - S_{21}S_{12}|$. Unconditional stability is secured when both K > 1 and Δ > 0 conditions are satisfied by ensuring no oscillation at any frequency domain. Figures 7 and 8 showed K = 227 and Δ = 0.168, demonstrating the unconditional stability of this LNA. Next is the power supply rejection ratio (PSRR). PSRR represents vulnerability of a system output against power supply noise injection. The lower the PSRR, the more reliable it is against the power supply noise injection. Our result in Figure 9 showed PSRR = −14.16 dB, proving the supply noise reliability of this circuit design. Lastly, process, voltage, and temperature (PVT) variation simulations were performed. A process variation is inevitable within the process of semiconductor fabrication. We used three corners: *tt* (typical) , *ff* (fast), and *ss* (slow) in these simulations. A temperature variation is another inevitable factor in real application. The tests were executed at 27 °C, −23 °C, and 127 °C to demonstrate the circuit operation at any extreme temperature. A voltage variation is a simulation against supply voltage variation where V_{DD} was swept for V_{DD}, $0.9V_{DD}$ and $1.1V_{DD}$ to encounter ±10% variation. In summary, simulations were carried out at three conditions:

1. *tt* (typical-typical), V_{DD}, 27 °C
2. *ss* (slow-slow), $0.9V_{DD}$, −23 °C
3. *ff* (fast-fast), V_{DD}, 127 °C

to reflect the worst case scenarios. Figure 10 summarizes the PVT simulation results for S_{21} and NF and Figure 11 indicates the PVT result for IIP3. The worst case results were S_{21} = 12.4 dB (at condition 2), NF = 3.56 dB (at condition 2), and IIP3 = 5.89 dBm (at condition 1).

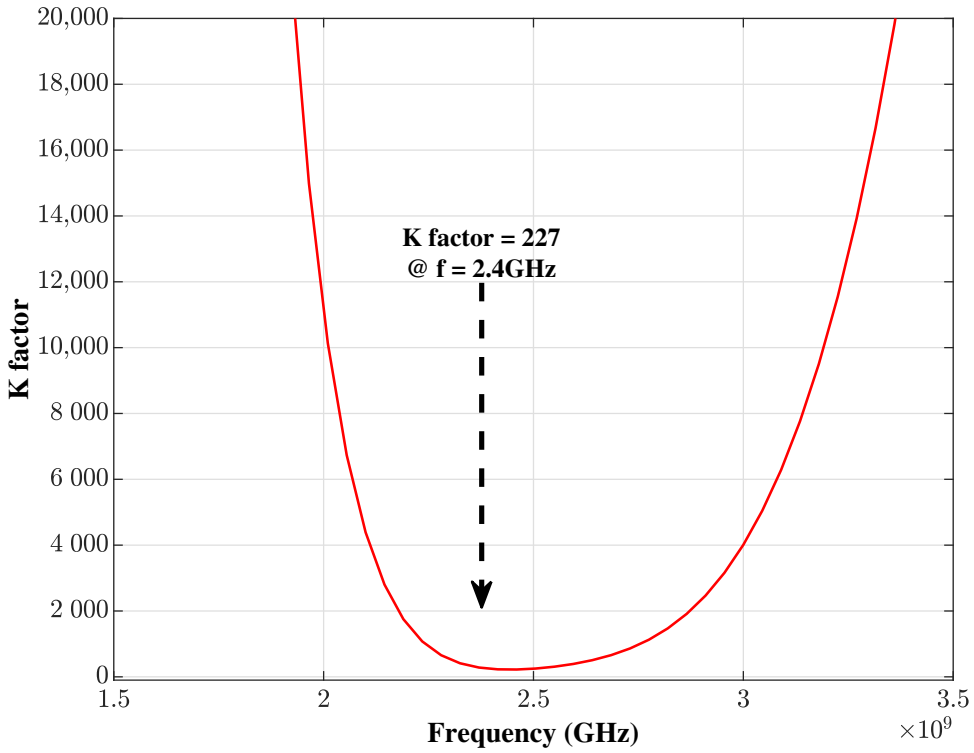

Figure 7. K factor vs. frequency for Stability test.

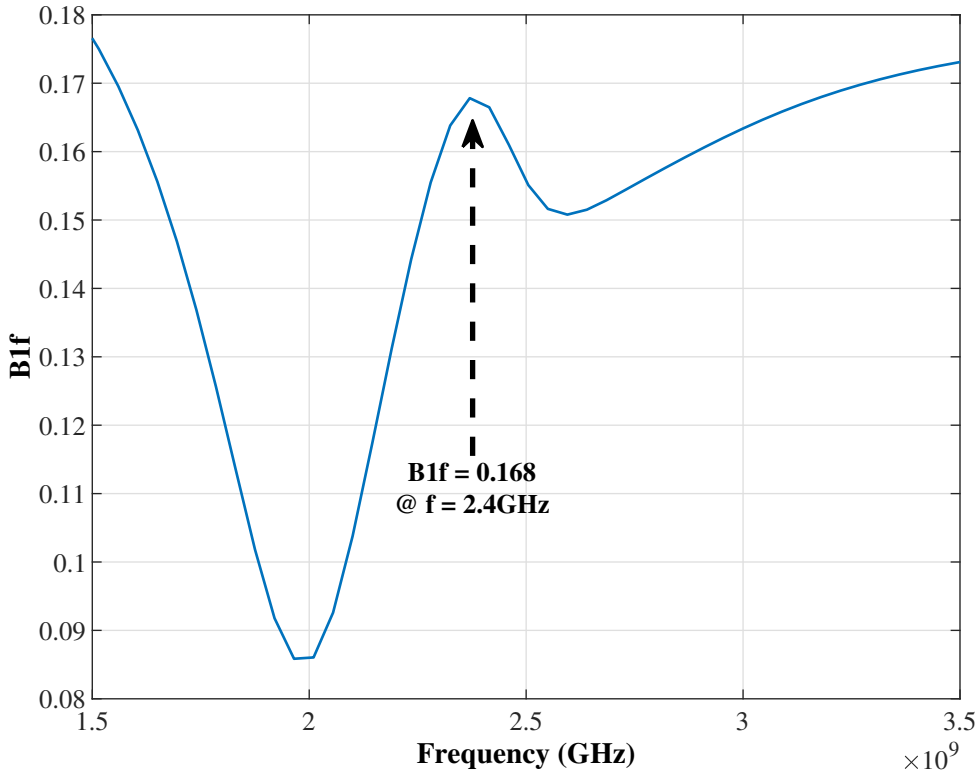

Figure 8. B1f vs. frequency for Stability test.

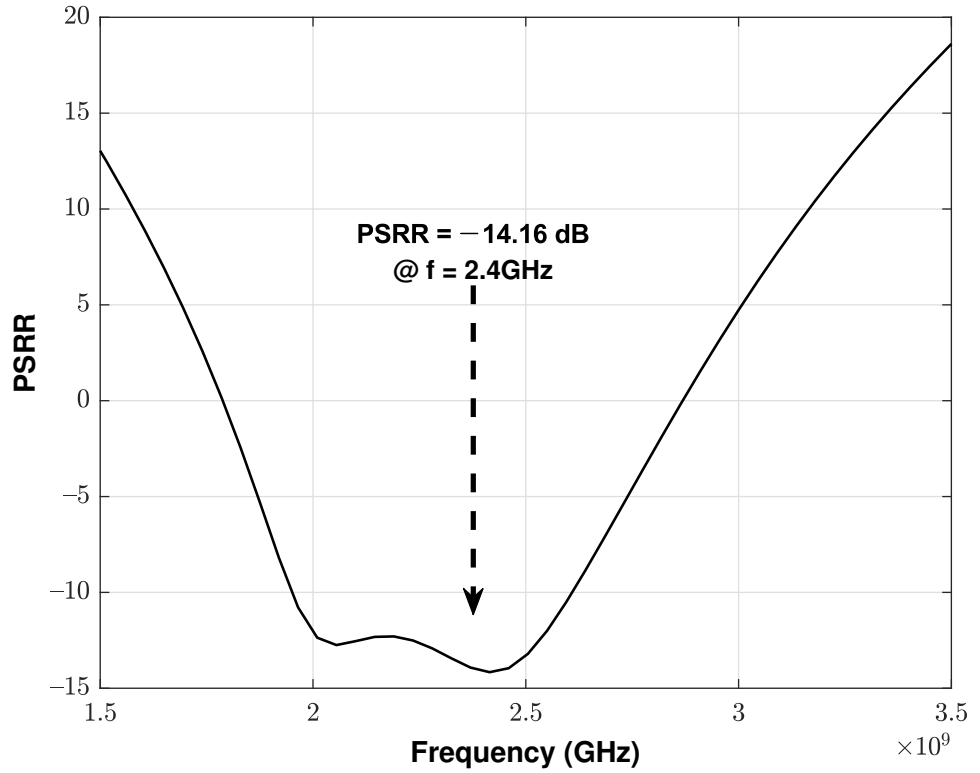

Figure 9. PSRR vs. frequency.

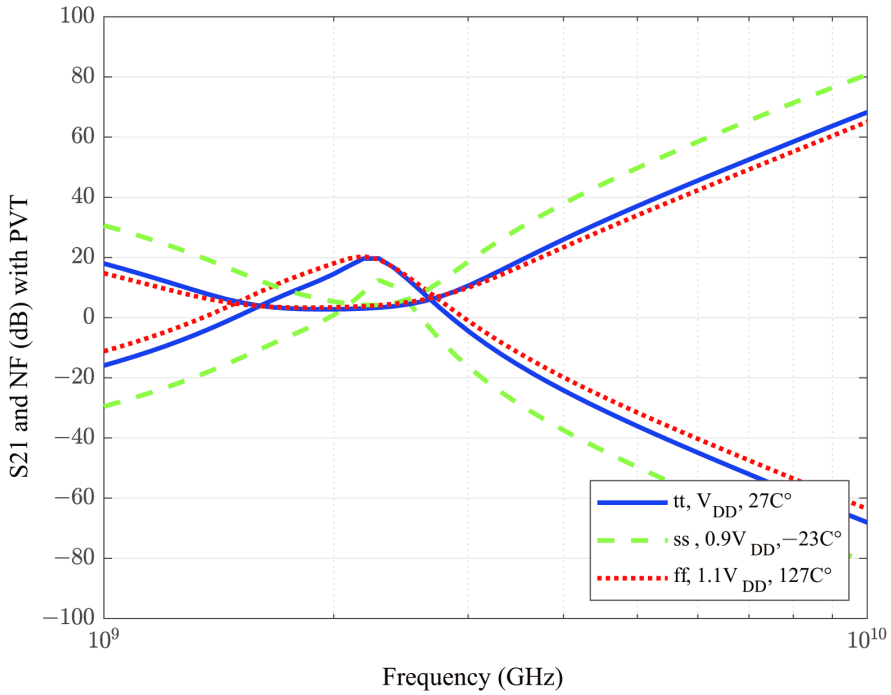

Figure 10. S21 and NF (dB) with PVT vs. frequency.

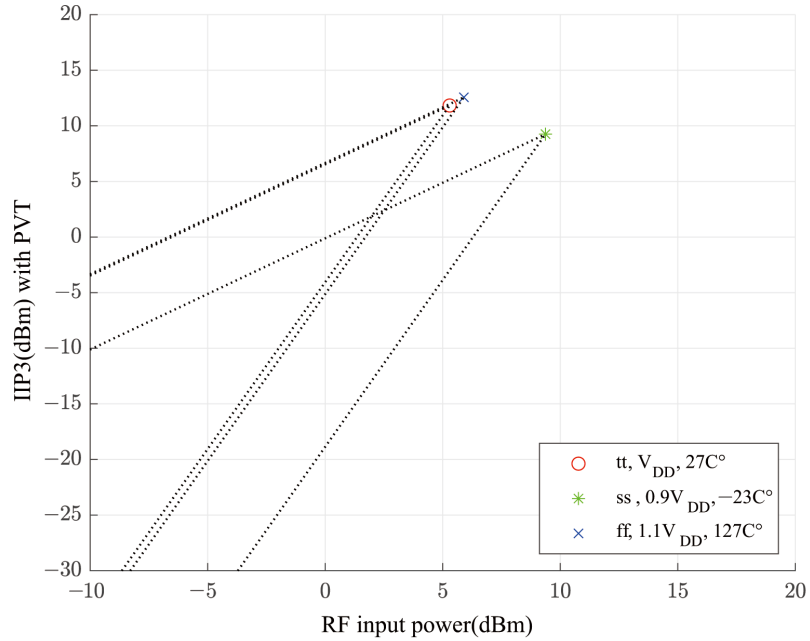

Figure 11. Third-order intercept point with PVT vs. V_{ov}.

The circuit layout is shown in Figure 12 which was designed for the area of approximately 500 µm × 530 µm. The center part shows the core cascode RF NMOS transistors.

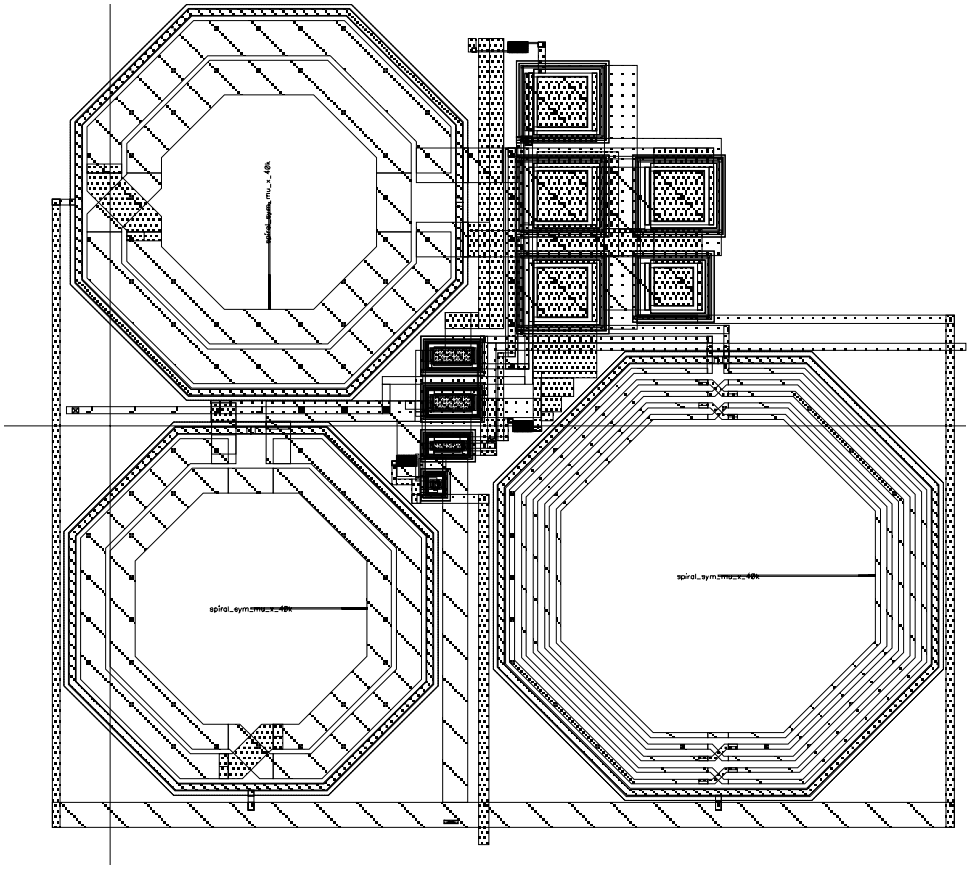

Figure 12. The layout of the designed LNA with the area of 500 µm × 530 µm.

The transistor dimension (located at the center of the layout) is 17 µm × 19 µm which is less than 0.2% of the total area of the LNA. The top left is the drain inductor L_D, and the source inductor L_S is at the bottom left. The gate inductor L_G is located at the bottom right. The drain load capacitor C_D, the input and output capacitors C_{in} and C_{out} and the AC coupling C_{buffer} are shown on the upper right corner. Our simulation results reflected parasitic effects through PEX extraction and the vender provided inductor synthesis tool for EM effect analysis. The circuit is designed based on 180 nm with 1P6M + UTM metal option. All the simulations are performed by Spectre through Cadence ADE tool.

As shown in Table 2 below, the performance of this LNA compares well to performance to previous works [13–19]. Aneja's report utilized the dual band load technique which showed great performance in terms of S_{21}, however its power consumption was excessively high compared to most applications. Park's LNA which included a poly-phase filter revealed excellent power efficiency. However, noise was relatively not satisfactory and linearity was significantly limited. Luo came up with a reconfigurable active inductor for an LNA and proved great S_{21} and NF performance, but at the cost of high power consumption. Liu and Bozorg's works applied the active feed-forward technique and noise reduction technique, respectively. In both works, they showed decent gain and noise responses, however, linearity were limited. Chang's work used a body floating and self-bias technique. It demonstrated excellent power efficiency though gain and its linearity response was not as competitive compared to other works. Finally, Gao's report represented a frequency-selective gain equalization technique in an effort to secure superior gain response. However, the relatively low linearity and high power consumption was not practical. The analysis of previous works compared to our own work proves our excellent results in terms of overall performance which includes S_{21}, NF, IIP3, P_{dc}, and demonstrated superiority of our g_m/I_D and FoM combined design methodology.

Table 2. A comparison table of the LNA and other works.

Reference	S_{21} (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	f_c (GHz)	Supply Voltage (V)	Area (mm^2)	CMOS Tech (nm)
This work	19.91	3.54	5.89	9	2.4	1.8	0.26	180
Aneja [13]	20.1	3	4.9	108	2.4	3	N/A	MIC
Park [14]	49.5	8.2	−25.75	2.16	2.4	0.8	1.16	65
Luo [15]	19	2.65	N/A	20.1	2.4	1.8	0.023	180
Liu [16]	14–17	3.5–5.5	−2.8	9	1–11	1.2	0.061	40
Bozorg [17]	15.2	2.09–3.2	−4.6–3.5	4.5	0.02–4.5	1	0.03	28
Chang [18]	7.5–10.7	3.41	−6.2	3.3	2.4–9.1	1	0.74	180
Gao [19]	20.7	3.26	−12	75	6.5–12	1.3	0.98	55

4. Conclusions

The modeling and evaluation of an LNA is carried out by combining the g_m/I_D algorithm and the FoM index method. The device is based on 180 nm CMOS technology and operates at f_0 = 2.4 GHz. Design parameters were determined using g_m/I_D vs. V_{ov}, f_t vs. V_{ov}, and I_D/W vs. V_{ov} data charts (Figures 2 and 3) and computing the FoM to demonstrate an optimal bias point. The results revealed that optimal values for S_{21} and noise figure were obtained at V_{ov} = 0.1 V (Table 1) where great linearity is obtained without any significant degredation in the S_{21} parameter and noise. A comparison of this LNA and previous works in Table 2 shows high linearity and power efficiency with comparble S_{21} and NF. The figure of merit was computed to guide the parametric optimization. The optimized model showed S_{21} = 19.91 dB, NF = 3.54 dB, $IIP3$ = 5.89 dBm, P_{DC} = 9 mW, verifying the effectiveness of characterization capabilities of the g_m/I_D algorithm process and the FoM index method combined.

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