


Article

A Low-Noise and Monolithic Array Tactile Sensor Based on Incremental Delta-Sigma Analog-to-Digital Converters

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Abstract: A low-noise and monolithic array tactile sensor, in which a tactile sensing unit, a low-noise analog front end (AFE), and a high-resolution delta-sigma analog-to-digital converter ($\Delta\Sigma$ ADC) are fully integrated, is presented in this paper. In this proposed system, compared with a discrete-device-based board-level system, the parasitic effect of a long cable connection can be reduced, and results are more accurate. Furthermore, a smaller system area and a lower power consumption can be achieved in this monolithic system. A discrete-continuous mixed mode bandpass AFE is proposed to filter out low-frequency flicker noise and high-frequency white noise. In order to improve the quantization rate of the sensor readout circuit and further suppress the high-frequency noise, a two-way alternate sample-and-hold circuit scheme is adopted in this design. The proposed tactile sensor is designed and fabricated in a 0.5- μm CMOS (Complementary metal oxide semiconductor) mixed-signal process with a 16×16 array and a total chip area of $1.9 \times 1.9 \text{ cm}^2$. This chip consumes 33.5 mW from a 5 V supply. The measurement results showed that the signal-to-noise and distortion rate (SNDR) was 65.2894 dB and that the effective number of bits (ENoB) was 10.553 dB. Moreover, this sensor could achieve a pressure measurement range of 0.002–0.5 N with a resolution of 0.4 mN.

Keywords: tactile sensor; readout circuit; AFE; $\Delta\Sigma$ ADC



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1. Introduction

In recent years, with the rapid development of intelligent manufacturing, intelligent robots have been developing more rapidly [1,2]. The work of intelligent robots in a complex environment requires precise coordination among various sensors [3–5]. Generally, tactile sensory input is second only to vision as the most important information source for a robot [6]. Hence, intelligent robot tactile sensing technology has received great attention from researchers.

A bionic haptic finger applied to a manipulator is designed in [7], which can measure the stiffness of an object during grasping. However, the tactile sensor can only perform single-touch testing, and its size is $50 \text{ mm} \times 20 \text{ mm} \times 20 \text{ mm}$, which is very large and is not suitable for scenes with limited areas. In [8], a vertically stacked nanocellulose tactile sensor based on the piezoresistive principle was reported with a response time of 40 ms in a range of 0.5–3 kPa. A force sensor was fabricated by using the piezoelectricity of Li-doped ZnO thin films in [9] with MEMS (Micro electro mechanical system) technology. The sensitivity of the force sensor was 46.1 mV/N in a range of 1–5 N. In [10], an active piezoelectric tactile sensor 3D field-coupled thin film transistors was developed with a 4×4 array. The sensor could measure force and temperature at the same time, with a sensitivity of tens of mN in terms of force and a resolution of about 1°C in terms of temperature. Obviously, the sensitivity, measurement range, and size of these tactile sensors cannot meet the application requirements of intelligent robots for accurate force detection. Furthermore,

none of these have a matching signal readout circuit, so these disadvantages limit the practical application of tactile sensors. In [11], a capacitive tactile sensor for pulse diagnosis with a custom CMOS readout circuit was developed. The sensitivity of the sensor could reach 1.57 mV/mmHg, and the minimum detectable pressure and capacitance were at sub-millimeter mercury and sub-fF levels, respectively. However, the CMOS readout circuit and the sensing unit were still connected by a long cable, rendering many parasitic effects unavoidable.

The high cost and low resolution of previously reported tactile sensors hinder their future mass production and practical applications. Therefore, there is an urgent need to develop a new type of tactile sensor capable of detecting a dynamic pressure distribution with a high sensitivity, a fast response, and a realistic distribution in a low-cost manner through a simple fabrication process. In this paper, a monolithic integrated tactile sensor is proposed, in which the tactile sensor unit and the readout circuit are integrated on one chip. This design can improve the resolution of the tactile sensor and reduce the area of the tactile sensor. In addition, compared with tactile sensors that require the additional purchase of signal conditioning circuits, it will be more cost-effective due to the integrated matching readout circuit.

Aiming at the frequency bandwidth requirement (1–1000 Hz) of the signal processed by the tactile sensor and the problem of noise optimization in the circuit, a discrete-continuous mixed mode bandpass AFE is proposed in this paper. The scheme adopts a discrete-mode switched capacitor equivalent resistor circuit, which can achieve a 1-Hz high-pass pole frequency. Compared with the implementation method using pure resistor, this structure can significantly reduce the chip area and design the high-pass pole frequency more accurately. In order to improve the quantization rate of the sensor readout circuit and further reduce the high-frequency noise, an alternate sample-and-hold circuit scheme is adopted in this paper. Furthermore, Adjusting the duty cycle of the switch can achieve anti-aliasing filtering with a lower cut-off frequency.

Aiming at the requirement of integrated on-chip analog-to-digital conversion for tactile sensors with digital output, a high-resolution second-order incremental discrete $\Delta\Sigma$ ADC is designed in this paper to digitize the analog signals generated by the tactile sensors. Incremental $\Delta\Sigma$ ADCs are often the best choice for an array sensor application with low speed and high resolution, whose noise performance is better than that of other ADC structures because of the oversampling and noise-shaping technology [12]. It still retains many of the advantages of $\Delta\Sigma$ ADCs, yet enables offset-free and precise conversions [13]. Moreover, it resets every sampling period of the modulator and the digital decimation filter, so that the digital decimation filter can be achieved with a simple accumulator, which simplifies the design of the decimation filter and greatly reduces the power consumption and area.

The tactile sensor proposed in this paper is designed and fabricated in a 0.5- μm CMOS mixed signal process, with a total chip area of $1.9 \times 1.9 \text{ cm}^2$. Measurement shows that the chip has good performance, so that the research results of this topic can further promote the research and application of robot intelligent perception technology.

The remainder of the paper is organized as follows. The system design of the proposed tactile sensor readout circuits and the noise analysis are described in Section 2. The detailed circuit implementation is shown in Section 3. Section 4 reveals the measurement results. The discussion about the tactile sensor is presented in Section 5. Finally, the drawn conclusions are presented in Section 6.

2. System Design

Figure 1 shows the architecture of the proposed tactile sensor. The readout circuit consists of a MEMS piezoelectric array, an AFE, a $\Delta\Sigma$ ADC, a buffer memory, and a scanning circuit. The entire chip contains 16×16 array units, each of which is identical, including an AFE and a $\Delta\Sigma$ ADC quantization circuit. Through the timing controller, the output of these 256 units can be sent out by 13-bit binary data in one conversion cycle.

Next, the architecture and noise of the main circuit are analyzed, respectively.

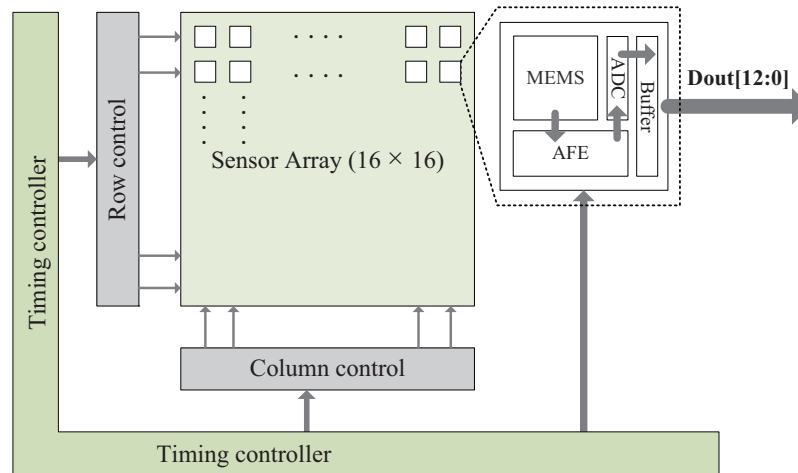


Figure 1. System block diagram of the proposed CMOS tactile sensor readout system.

2.1. Analog Front End

The proposed AFE has a complete and highly integrated system that aims to amplify and sample the output signal of the tactile sensor to form voltage outputs that can be processed by the following $\Delta\Sigma$ ADC. As shown in Figure 2, the proposed AFE includes a charge preamplifier, a variable gain amplifier (VGA), a sample-and-hold (SH) circuit, and an output buffer. The input source of this tactile sensor comes from piezoelectric material, which can be equivalent to a model of a current source and a capacitor in parallel. Due to the characteristics of piezoelectric material, it cannot measure static pressure, so we need a lower cutoff frequency point to suppress low-frequency noise. A simple RC filter circuit can be considered to achieve this lower cut-off frequency. Considering the area limitation, in order to achieve a high resistance, a switched-capacitor circuit was used to design an equivalent large resistance. Another advantage of the switched-capacitor circuit is that the designed resistance is more accurate. By adjusting the switching frequency f_c , the equivalent resistor R_{eq} can be accurately designed. A VGA based on resistor feedback was used to achieve different amplification gain multiples to meet the dynamic range of the following ADC. The following process circuit uses a discrete time $\Delta\Sigma$ ADC, whose input can be regarded as a dc signal, so we need to sample-and-hold the signal voltage in the AFE. The switched-RC sample-and-hold circuit is a suitable choice. It is also a low-pass filter. The low-pass corner can be given by [14]

$$f_{-3dB} = \frac{D}{2\pi R_3 C_4} \tag{1}$$

where D is the duty cycle of the sampling pulse. Thus, the filter cut-off frequency can be changed by adjusting this duty cycle to further suppress the noise appearing on the VGA output. The output buffer is used to improve the driving ability of the AFE. The sensor equivalent current I_p can be expressed as

$$I_p = \frac{dQ}{dt} = d_{33} \cdot \frac{dF}{dt} \tag{2}$$

where d_{33} is the piezoelectric coefficient, and F is the applied perpendicular force.

Usually, the system can be better analyzed in the frequency domain. Therefore, the output voltage $V_o(s)$ can be expressed as

$$V_o(s) \approx \frac{sQ(s)}{(1 + sR_i C_p)(sC_1 + f_c C_2)} \cdot \frac{R_2}{R_1} \cdot \frac{D}{1 + sR_3 C_4} \tag{3}$$

where R_i is used to adjust the bandwidth upper limit cutoff frequency. C_p and C_f are the intrinsic capacitances of the sensor unit and the charge preamplifier feedback capacitance. C_2 is the switched-capacitor, and f_c is the switch frequency. R_2 is a variable resistor.

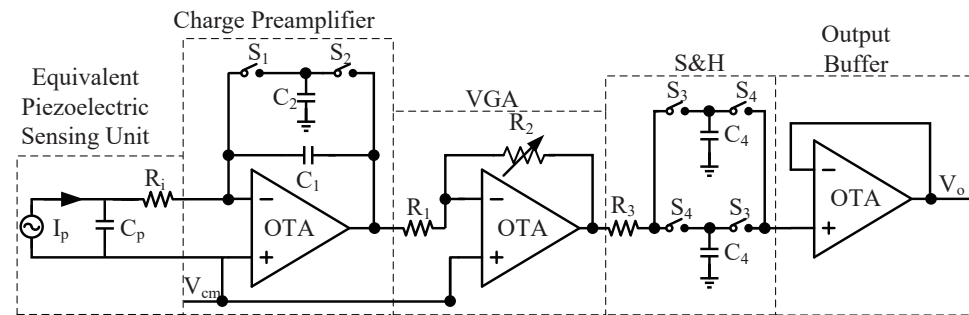


Figure 2. Proposed architecture of the analog front end (AFE).

2.2. IΔΣ ADC

Figure 3 is the system block diagram of a second-order incremental ΔΣ ADC, which contains a second-order delta-sigma modulator and a digital decimation filter. The modulator topology is composed of two discrete time integrators and a single bit quantizer, and the digital filter is made up of a second-order digital integrator. $X(z)$ is the output signal of AFE, and $E(z)$ is the quantization noise introduced by the quantizer. Hence, the output expression $B(z)$ of the delta-sigma modulator in the z-domain is

$$BS(z) = \frac{abz^{-1}}{(1 - b + ab)z^{-2} + (b - 2)z^{-1} + 1} X(z) + \frac{(1 - z^{-1})^2}{(1 - b + ab)z^{-2} + (b - 2)z^{-1} + 1} E(z) \tag{4}$$

$$= STF(z)X(z) + NTF(z)E(z)$$

where a and b are the first and second integrator coefficients, respectively, which are designed by the capacitance ratio of the switched-capacitor integrator. To achieve

$$STF(z) = z^{-1} \tag{5}$$

$$NTF(z) = (1 - z^{-1})^2 \tag{6}$$

$1 - b + ab = 0, b - 2 = 0$ are required. The transfer function of the input signal is different from that of the quantization error. The output of the input signal is delayed by one clock cycle, while the quantization error is modulated by the transfer function $NTF(z)$, which is a high-pass filter. The essence of noise shaping is that the quantized noise spectrum is attenuated at low frequency, which reduces the noise in the low-frequency band. After the output of the modulator passes through a digital filter cascaded by a two-stage integrator, the multi-bit output data can be expressed as

$$D_{out}(z) = \left(\frac{z^{-1}}{1 - z^{-1}} \right)^2 BS(z). \tag{7}$$

From (4) and (7), eventually we can obtain

$$D_{out}(z) = \frac{z^{-3}}{(1 - z^{-1})^2} X(z) + z^{-2}E(z). \tag{8}$$

By doing an inverse z-domain transform on the transfer function $D_{out}(z)$, we can then obtain

$$D_{out}(n) = \sum_{i=0}^{n-1} \sum_{k=0}^{l-1} X(k) + E(k). \tag{9}$$

If the circuit is stable and the quantizer is not overloaded, the quantization noise $E(k)$ is limited to the range $V_{ref}/(n(n-1)/2)$. In the $I\Delta\Sigma$ ADC system, the input signal $X(k)$ can be approximated as a dc signal. According to the quantization noise range, the following can be obtained:

$$\left| X - \frac{D_{out}(n)}{n(n-1)/2} \right| \leq \frac{V_{ref}}{n(n-1)/2}. \tag{10}$$

The left side of the inequality represents the difference between the input signal and the approximate signal of the $I\Delta\Sigma$ ADC, and the right side represents the final quantization error. In order to achieve an N bit quantization resolution, the final quantization error is required to be $V_{ref}/2^{N_{bits}}$. The required oversampling rate (OSR) can then be calculated by the following formula:

$$N_{bits} = \log_2 OSR(OSR - 1) - 1. \tag{11}$$

Theoretically, if the ADC needs a 12-bit linear dynamic range, an oversampling rate of at least 95 will be required. Moreover, with the increase in the order of the modulator, more noise will be suppressed at low frequency. By adding a digital decimation filter behind the modulator, the high-frequency out-of-band noise can be filtered out.

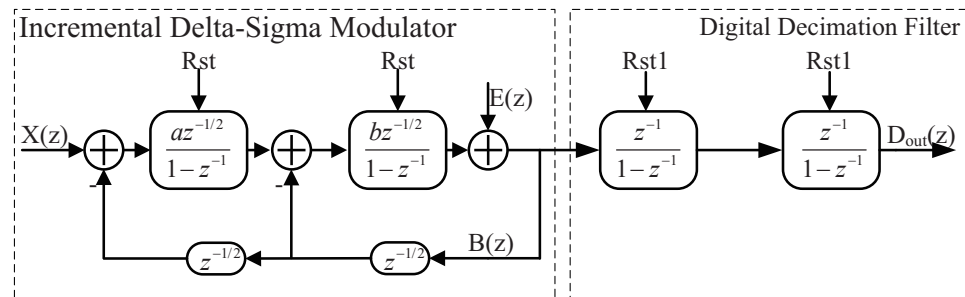


Figure 3. System block diagram of a second-order incremental $\Delta\Sigma$ ADC.

2.3. Noise Consideration

The signal passes through the series of transmission path, which will inevitably introduce some unwanted noise and deteriorate the performance of the chip. In order to design a low-noise readout circuit, it is necessary to analyze the source of noise in the circuit and how part of the noise can be reduced as much as possible. The main noise contribution sources are analyzed below.

2.3.1. Noise in AFE

As the charges pass through this transfer path, a high amount of noise is introduced, such as channel charge injection, thermal noise, and flicker noise. Channel charge injection can be eliminated by combining NMOS and PMOS. Flicker noise is dependent on the surface of the transistor and can be reduced by increasing the input stage. The noise of the preamplifier in AFE is mainly analyzed here, because the noise of the VGA and the noise of the sample-and-hold circuit can be ignored compared with the noise of the preamplifier. A simplified equivalent noise model of the preamplifier is shown in Figure 4. The noise contributed by each component is calculated separately and then added together. The input-referred noise power contributed by switch S1 and S2 can be expressed as [15]

$$\overline{v_{n,S1,2}^2} = \frac{kTC_1^2}{C_{eq}C_p^2} \tag{12}$$

where C_{eq} is the equivalent load capacitance, which depends on the structure of the OTA. For a two-stage OTA, $C_{eq} = C_c$, where C_c is the Miller compensation capacitor.

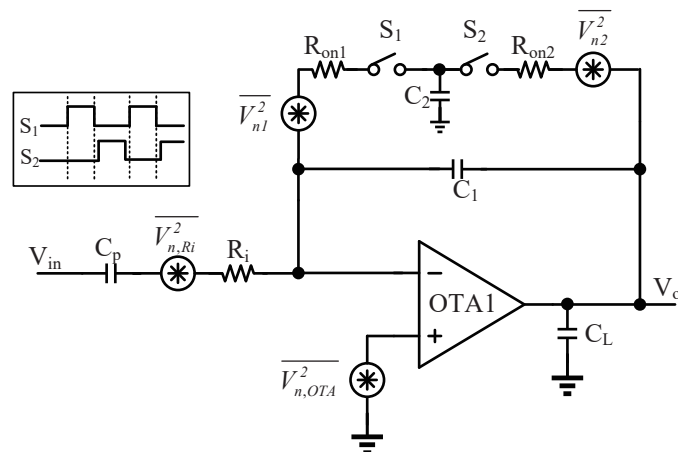


Figure 4. Noise model of the charge preamplifier.

The noise power $v_{n,OTA1}^2$ in C_p introduced from OTA1 can be obtained as (13).

$$\begin{aligned} \overline{v_{n,OTA1}^2} &= \frac{S_{OTA1}(f)}{4\tau} \\ &= \frac{16kT/C_p}{3(g_{m1,OTA1}R_i+1)} \left(1 + \frac{1}{(1+g_{m5,OTA1}R_s)^2} \cdot \frac{g_{m5,OTA1}}{g_{m1,OTA1}} \right. \\ &\quad \left. + \frac{3g_{m5,OTA1}^2}{2(1+g_{m5,OTA1}R_s)^2} \cdot \frac{1}{g_{m1,OTA1}R_s} \right) + \int_0^\infty \frac{K_f}{C_{ox}^2(WL)_{OTA1}} df \end{aligned} \quad (13)$$

where $\tau = (R_i + 1/g_{m1,OTA1})C_{s1}$, the first component is thermal noise, and the second component is flicker noise. K_f is the flicker noise parameter, $K_f = 10^{-31} \text{ F}^2 \text{ V}^2/\text{cm}^2$, and W and L are the effective width and length of the input transistor M1, 2, respectively. The noise power contributed by R_i can be obtained as

$$\overline{v_{n,R_i}^2} = \frac{4kTR_i}{4(R_i + 1/g_{m1,OTA1})C_p} = \frac{kT/C_p}{1 + R_i g_{m1,OTA1}}. \quad (14)$$

Next, the total input-referred noise power is considered. Since these three noises are uncorrelated, their noise power can be superimposed. Therefore, the total noise power can be obtained as

$$\begin{aligned} \overline{v_n^2} &= \overline{v_{n,S_{1,2}}^2} + \overline{v_{n,OTA1}^2} + \overline{v_{n,R_i}^2} \\ &= \frac{16kT}{(3x+3)C_p} \left(1 + \frac{1}{(1+g_{m5,OTA1}R_s)^2} \cdot \frac{g_{m5,OTA1}}{g_{m1,OTA1}} + \frac{3g_{m5,OTA1}^2}{2(1+g_{m5,OTA1}R_s)^2} \cdot \frac{1}{g_{m1,OTA1}R_s} \right) \\ &\quad + \frac{kT}{C_p} \left(\frac{C_1^2}{C_{eq}C_p} + \frac{1}{1+x} \right) + \int_0^\infty \frac{K_f}{C_{ox}^2(WL)_{OTA1}} df \end{aligned} \quad (15)$$

where $x = g_{m1,OTA1}R_i$. Equation (15) implies that noise can be reduced for a large x and a large C_{eq} . Thus, the OTA dominates the noise for $x \ll 1$, while the switch effects dominate for $x \gg 1$. An optimal operating point can be achieved by choosing a smaller switch and increasing the tail current of the OTA. Moreover, if $g_{m5,OTA1}R_s \gg 1$, the noise can be neglected relative to the noise contributed by differential input transistor M1 and M2. Thus, the total input-referred noise of the OTA is reduced.

2.3.2. Noise in $\Delta\Sigma$ ADC

In the $\Delta\Sigma$ ADC, the main noise consists of $1/f$ noise and thermal noise from MOS devices as well as quantization noise introduced by the quantizer. Considering that the noise generated by the first-stage integrator accounts for a relatively high proportion of the overall modulator noise performance, when designing the $\Delta\Sigma$ ADC, the first-stage integrator must be designed well.

Figure 5 shows the simplified first-stage switch-capacitor integrator circuit, which contains an OTA, four switches, and two capacitors. The equivalent noise model is shown in Figure 6, where (a) and (b), respectively, represent the sampling phase and the integral phase. R_{on} is the on-resistance of the switch, which introduces thermal noise. For ease of analysis, we assume that the resistor parameters of all switches are R_{on} .

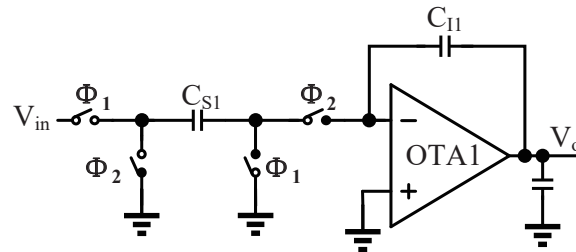


Figure 5. The switched-capacitor integrator circuit.

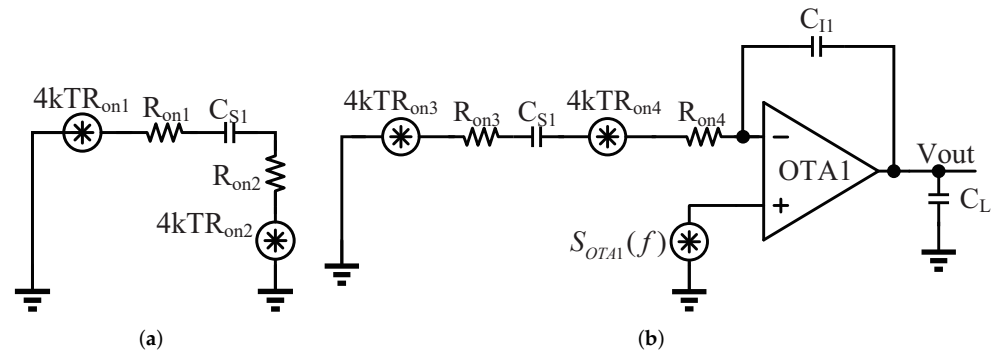


Figure 6. (a) Noise model of the sampling phase. (b) Noise model of the integrating phase.

In the sampling phase (Φ_1 is on, Φ_2 is off), to make the analysis more specific, the noise power spectral density (PSD) of the two resistors can be combined [16]. Therefore, the PSD $S_{C_{s1}}(f)$ on the sampling capacitor can be expressed as follows:

$$S_{C_{s1}}(f) = \frac{8kTR_{on}}{1 + (2\pi f\tau_s)^2} \tag{16}$$

where τ_s is the time constant of the sampling phase, k is the Boltzmann constant, $k = 1.38 \times 10^{-23}$ J/K, T is the absolute temperature of the device in degrees Kelvin, and R_{on} is the on-resistance of MOS transistor. By integrating the power spectral density over the entire frequency band, the noise power in the sampling phase can be derived as

$$\overline{v_{n,C_{s1},samp}^2} = \int_0^\infty \frac{8kTR_{on}}{1 + (2\pi f\tau_s)^2} df = \frac{kT}{C_{s1}} \tag{17}$$

The noise power in the band is

$$\overline{v_{NB}^2} = \frac{kT}{OSR \times C_{s1}} \tag{18}$$

where OSR is the oversampling ratio. In the integration phase (where S_1 is off and S_2 is on), the main sources of noise are the thermal noise from two on switches as well as the flicker noise and thermal noise from the operational transconductance amplifier. In the system, a two-stage operational amplifier with Miller compensation is designed, and this can be approximated to a single pole system. The noise bandwidth in the single pole system is equal to $\pi/2$ times of the corresponding frequency of the pole. Thus, the equivalent noise bandwidth $f_{n,BW}$ can be written as

$$f_{n,BW} = \frac{\pi}{2} BW_{OTA1} = \frac{g_{m,OTA1}}{4C_c} \tag{19}$$

where BW_{OTA1} is the -3 dB bandwidth of OTA1. $g_{m,OTA1}$ is the transconductance of the input transistor. C_c is the compensation capacitance of the two-stage amplifier. The noise power in C_{s1} introduced from OTA1 can also be found.

$$\begin{aligned} \overline{v_{n,OTA1}^2} &= \frac{S_{OTA1}(f)}{4\tau} \\ &= \frac{16kT/C_{s1}}{3(2g_{m1,OTA1}R_{on}+1)} \left(1 + \frac{1}{(1+g_{m5,OTA1}R_s)^2} \cdot \frac{g_{m5,OTA1}}{g_{m1,OTA1}} + \right. \\ &\quad \left. \frac{3g_{m5,OTA1}^2}{2(1+g_{m5,OTA1}R_s)^2} \cdot \frac{1}{g_{m1,OTA1}R_s} \right) + \int_0^\infty \frac{K_f}{C_{ox}^2(WL)_{OTA1}} df \end{aligned} \tag{20}$$

where $\tau = (2R_{on} + 1/g_{m1,OTA1})C_{s1}$. For the thermal noise of the switch, similarly, we combine the thermal noise power spectral density of the switch. Thus, the noise power of the C_{s1} from the on switch in the integration phase can be obtained as

$$\overline{v_{n,C_{s1},int}^2} = \frac{8kTR_{on}}{4(2R_{on} + 1/g_{m1,OTA1})C_{s1}} = \frac{2kT/C_{s1}}{2 + R_{on}g_{m1,OTA1}} \tag{21}$$

Next, the total input-referred noise power is considered. Since these three noise power are uncorrelated, their noise power can be superimposed. Therefore, the total noise power is obtained as follows:

$$\begin{aligned} \overline{v_n^2} &= \overline{v_{n,C_{s1},samp}^2} + \overline{v_{n,OTA1}^2} + \overline{v_{n,C_{s1},int}^2} \\ &= \frac{16kT}{(6x+3)C_{s1}} \left(1 + \frac{1}{(1+g_{m5,OTA1}R_s)^2} \cdot \frac{g_{m5,OTA1}}{g_{m1,OTA1}} + \frac{3g_{m5,OTA1}^2}{2(1+g_{m5,OTA1}R_s)^2} \cdot \frac{1}{g_{m1,OTA1}R_s} \right) \\ &\quad + \frac{(4+x)kT}{(2+x)C_{s1}} + \int_0^\infty \frac{K_f}{C_{ox}^2(WL)_{OTA1}} df \end{aligned} \tag{22}$$

where $x = g_{m1,OTA1}R_{on}$. Similarly, as mentioned before, increasing x can effectively reduce noise, which has an important guiding significance for subsequent circuit implementation.

3. Circuit Implementation

3.1. Second-Order Incremental Delta-Sigma Modulator

Figure 7 shows the circuit diagram of the second-order incremental delta-sigma modulator (IDSMS), which is mainly composed of a two-stage switched-capacitor integrator, a comparator, and a D flip-flop. The switching between sampling and integration of the integrator is achieved by two-phase non-overlapping clocks Φ_1 and Φ_2 . Φ_{1d} and Φ_{2d} are the clock signals of Φ_1 and Φ_2 after a 20 ns falling edge delay, respectively, and they are used to sample the lower plate of the switched capacitor integrator to reduce the influence of the channel charge injection effect related to the input signal.

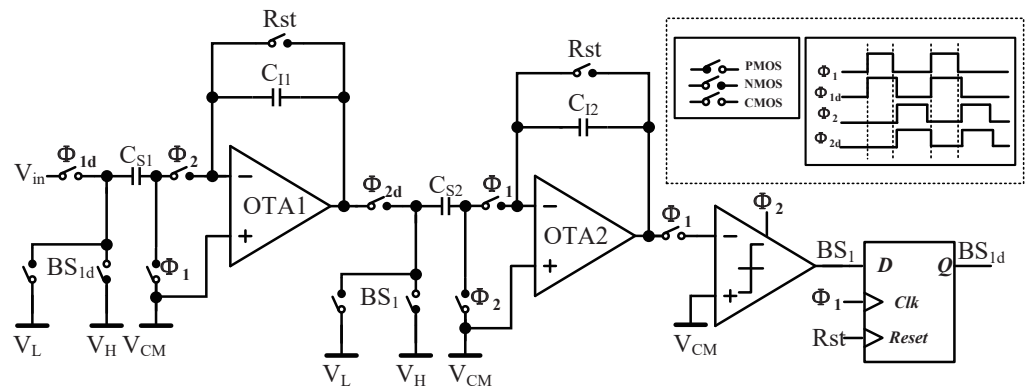


Figure 7. Circuit diagram of the second-order incremental delta-sigma modulator.

Generally, the gain of the operational amplifier is limited, which will result in incomplete charge transfer, thus directly affecting the accuracy of the circuit. Moreover, for different signal input amplitudes, the gain of the OTA is not a constant, which will cause circuit distortion and reduce the linearity of the entire system. In addition, the flicker noise coefficient of NMOS transistors is more than ten times higher than that of PMOS transistors. Hence, in order to obtain a low-noise and high-gain OTA, the designed circuit is shown in Figure 8. The first stage is a high-gain telescopic cascade scheme, where the NMOS active load is a source degenerated with a resistor R_s that helps to reduce the input-referred noise and increase the matching of the circuit. The second stage uses a common source amplifier with Miller-compensated topology. A resistance-capacitance Miller compensation scheme is used between the first-stage output and the second-stage input to increase the phase margin by introducing a negative zero.

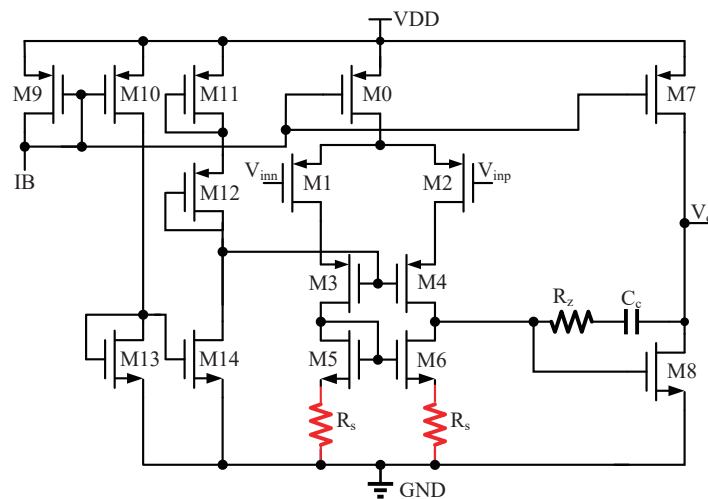


Figure 8. Circuit diagram of the operational transconductance amplifier (OTA1 and OTA2).

In order to simplify the bias circuit, OTA1 and OTA2 use the same structure but different device parameters. Because the second-stage integrator noise will be shaped by the first-stage, OTA2 can be proportionally contracted on the basis of OTA1, which can reduce power consumption.

3.2. Digital Decimation Filter

The digital decimation filter is an indispensable part of the $\Delta\Sigma$ ADC. Its main function is to filter out the high-frequency quantization noise after the noise shaping of the modulator and to reduce the sampling frequency introduced by oversampling. In the time domain, it converts the modulator's bit stream into a multi-bit binary output, which represents the input signal of the piezoelectric sensor. A general decimation filter is a sinc filter composed of a series of integrators and differentiators, but it is not necessary in incremental ADC. A simple counter can be used as a first-order decimation filter for a first-order incremental modulator. However, when a second-order modulator is used, a second-order decimation filter will need to match it. The block diagram of a second decimation filter is shown in Figure 9, which is composed of a ripple counter as the first integrator and an accumulator consisting of an adder and 13-bit registers as the second integrator. The 7-bit + 13-bit full-custom adder used in this paper is shown in Figure 10, which consists of 6 full adders and 7 half adders cascaded. The lowest bit is a half adder, and the highest bit is a half adder without carry function. The second to sixth are full adders, and the rest are half adders. The 13-bit registers are implemented using a standard D flip-flop.

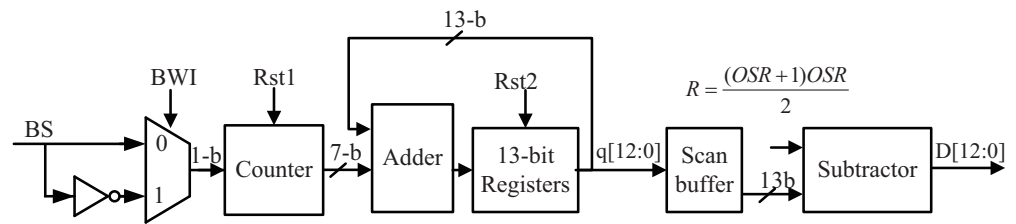


Figure 9. Block diagram of a second digital decimation filter.

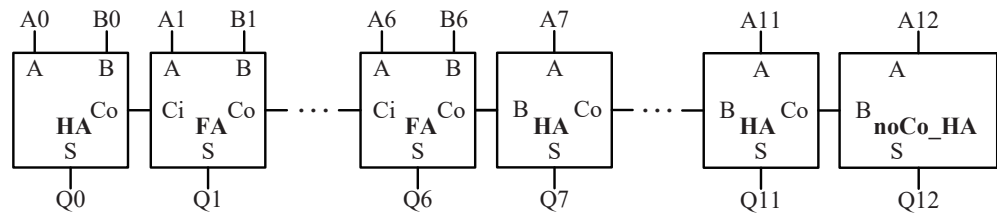


Figure 10. Block diagram of the full custom adder of 7 + 13 bits.

4. Measurement

The proposed tactile sensor readout was fabricated in a 0.5- μm CMOS mixed signal process, i.e., three-metal layer CMOS technology. The prototype chip microphotograph is depicted in Figure 11a with a size of $1.9 \times 1.9 \text{ cm}^2$. To guarantee the noise performance of the AFE, the area of the sampling capacitor has to be increased slightly. Figure 11b demonstrates the measured platform of the real subject with our proposed readout circuit. The input signal generated by the signal generator excites the shaker through the power amp converter and then provides a dynamic pressure input to the chip. The FPGA provides the timing voltage of the chip’s work and collects the output signal. The result of the collection is displayed by the computer. All results are measured at room temperature. The chip operates from a 5 V supply with a total power dissipation of 33.5 mW.

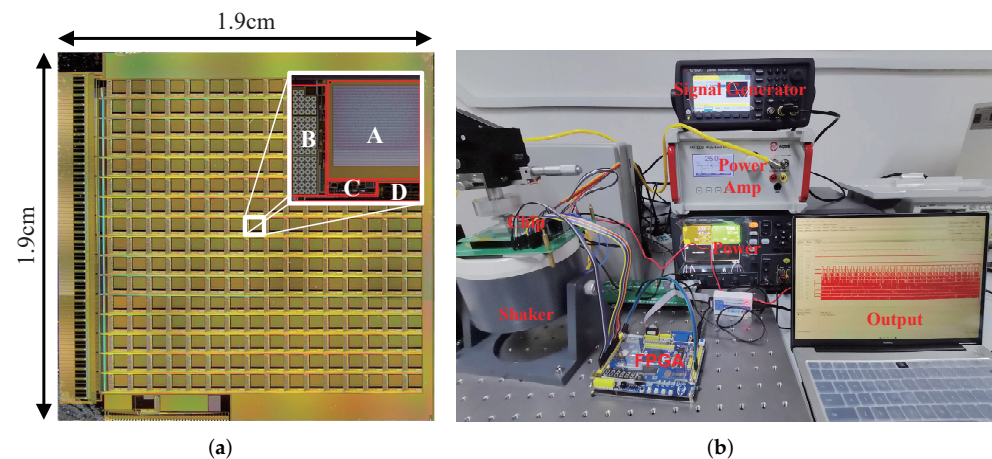


Figure 11. (a) The chip microphotograph. A: Tactile sensor. B: AFE. C: $\Delta\Sigma$ modulator. D: Digital decimation filter. (b) Demonstration of readout circuit measurement.

Figure 12 shows the measured output waveform of the readout circuit. Three sinusoidal signals with different amplitudes were applied as the input at 10 Hz and 100 Hz, respectively. It can be seen from the waveform that the readout circuit is working normally. At the same frequency, the input and output have good linearity.

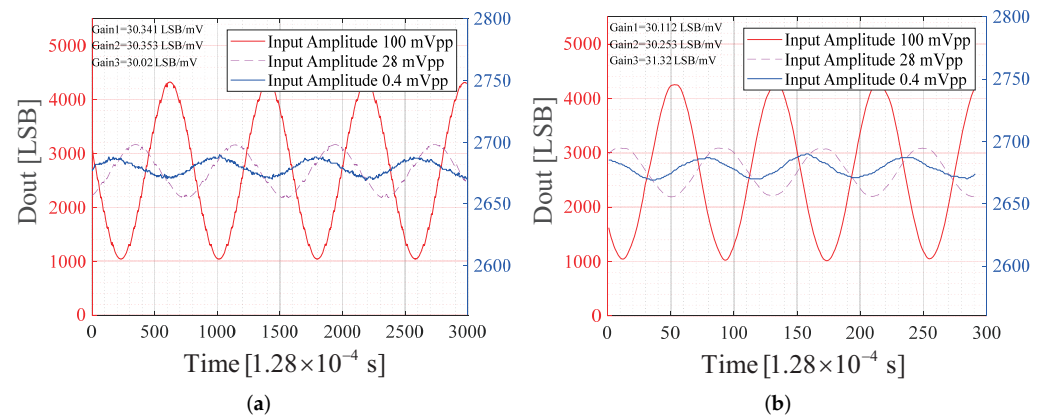


Figure 12. (a) Measured waveform of the readout circuit with the input frequency $f = 10$ Hz. (b) Measured waveform of the readout circuit with the input frequency $f = 100$ Hz.

Figure 13a shows the measured frequency response of the proposed AFE, which demonstrated that it can effectively detect the input signal in the frequency range of 1–1000 Hz and suppress the noise outside the frequency band. Figure 13b shows the measured FFT spectrum of the ADC. A -6 dB sinusoidal wave with a frequency of 1000 Hz was used as the input signal. The $\Delta\Sigma$ ADC achieved an SNDR of 65.2894 dB and an ENOB of 10.5531 bits, which meets the expectations.

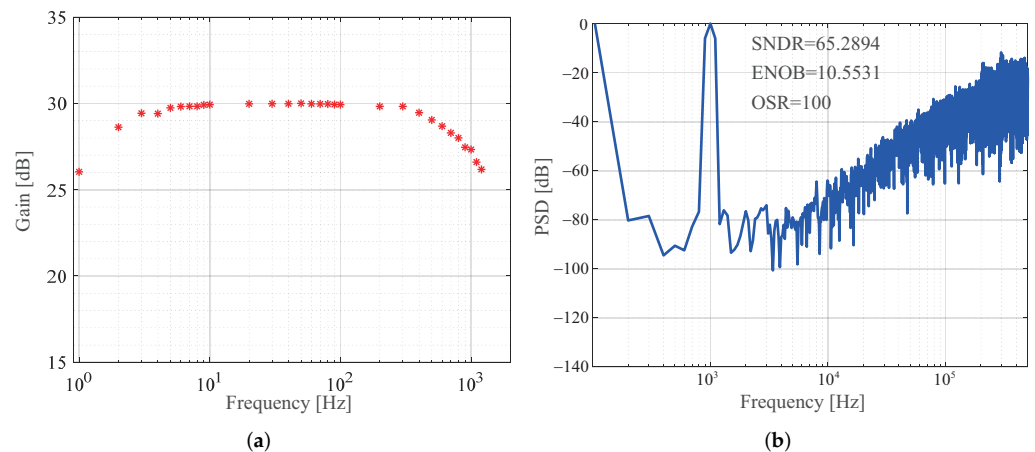


Figure 13. (a) Measured frequency response of the proposed AFE. (b) Measured output spectrum of the ADC.

Figure 14 shows the measured results of the integral and differential non-linearity (INL and DNL) of the ADC through a code density test. The peak INL was $-1.8154/1.511$ LSB, and the INL error was less than 0.1% for a 13-bit ADC. Generally speaking, the nonlinear error of piezoelectric tactile sensors was higher than 0.1%, so this error is completely acceptable.

Figure 15 shows the response of the tactile sensor to the applied external force with the input frequency at 100 Hz. The blue line is a linear function fitted according to the measured value. It can be seen from the figure that the tactile sensor has good linearity in the range of 0.002 to 0.5 N. When the input force continues to increase, the output enters the nonlinear region. The slope of the fitted line is 100,042 LSB/N, which is defined as the sensitivity of this tactile sensor.

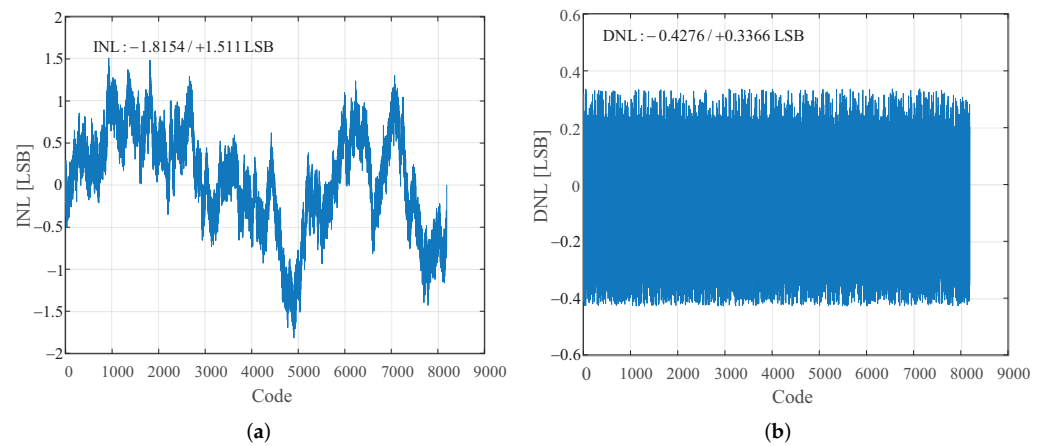


Figure 14. (a) Measured results of integral nonlinearity. (b) Measured results of differential nonlinearity.

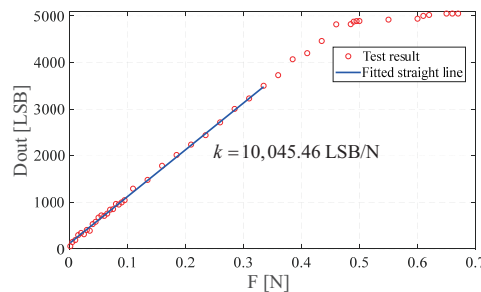


Figure 15. Test results of the tactile sensor response to force.

Other performance results of the sensor are summarized in Table 1. There are few works about fully integrated array tactile sensors. It can be seen from this comparison table that our work showcases the highest number of array cells. Compared with [10,11,17], our sensor outputs the highest SNR in comparison with an analog output. The resolution is also the highest among these works. Although the work [18] achieves the largest ENoB, it consumes too much power. Thus, our work can be competitive in low-noise and power efficiency while achieving a good resolution.

Table 1. Comparison with other state-of-the-art tactile sensors.

	2015 [11]	2016 [17]	2017 [18]	2020 [10]	This Work
Conditioning circuit	Custom CMOS readout circuit	DH5862	DDC112	Discrete device-based	Custom CMOS readout circuit
sensing mode	Off-chip	Off-chip	Off-chip	Off-chip	Monolithic chip
Array size	5 × 5	3 × 2	256	4 × 4	16 × 16
Full range (N)	-	-	-	-	0.65
Bandwidth (Hz)	-	5–400	1000	-	1–1000
Sensitivity	1.57 fF/mmHg	6.62 pC/N	0.6 pC/kPa	45.2 nA/kPa	100,042 LSB/N
Power consumption (mW)	-	-	1792	-	33.5
output signal mode	analog	analog	analog	analog	digital
ADC mode	-	-	ΔΣ ADC	-	ΔΣ ADC
ENoB (bits)	-	-	20	-	10.55
SNR (dB)	-	-	-	-	-
Noise (mV)	1.2 mV	40.35	-	-	64.21

5. Discussion

Firstly, because an unadvanced process is adopted in this work, the system area and power consumption are slightly high. From this point of view, a more advanced process node will be chosen in the future to decrease the overall system area and power

consumption. Meanwhile, the number of sensor array cells can be increased to have a more sensitive force-sensing capability. Secondly, owing to the capacitive coupling between the AFE and the tactile sensing unit, this system can only detect the alternative force signal, so it is not applicable to static force-sensing. To tackle this problem, a variable-resistance-based tactile sensing unit can be utilized to meet wider application scenarios. Thirdly, a column-parallel architecture can be employed to effectively decrease the number of ADCs, so that the area and power consumption of this sensor system can be further decreased. Our ultimate goal is to apply this tactile sensor to intelligent robots.

6. Conclusions

This paper presents a readout circuit for a piezoelectric tactile sensor with low-noise performance. The architecture of the AFE and $\Delta\Sigma$ ADC is analyzed in this paper. An active load degenerated operational transconductance amplifier was used to reduce the system noise. The circuit was designed and fabricated with a 16×16 array by using a $0.5\text{-}\mu\text{m}$ CMOS mixed signal process with a size of $1.9 \times 1.9\text{ cm}^2$. The measurement results show that the SNDR was 65.2894 dB, and the ENOB was 10.553 dB. The piezoelectric sensor proposed in this work can detect the physical properties of objects by collecting pressure. Such a sensor can be used for robotic hands, biomedical applications, and so on.

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