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Analysis and Design of a High-Frequency Isolated Dual-Transformer DC-DC Resonant Converter

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Abstract: This paper presents the operation, analysis, design, simulation, and experimental results for a proposed Dual-Transformer DC-DC Resonant Converter (DTRC). A three-arm bridge is employed on the input side and an H-type bridge is employed on the output side of the DTRC, and the two bridges are connected with two high-frequency (HF) transformers. By optimizing the ratio k of the two HF transformers, the proposed DTRC has a lower boundary power for losing zero-voltage switching (ZVS). That means the DTRC has a wider ZVS operation range and lower switching loss when compared with a traditional soft-switching pulse width modulation (PWM) resonant converter. The operation principle, power transfer, ZVS characteristics, and design procedures are analyzed in detail. Both simulation and experimental results prove the feasibility and superiority of the proposed Dual-Transformer DC-DC Resonant Converter.

Keywords: dual-transformer topology; resonant DC-DC converter; zero-voltage switching (ZVS); backflow power minimization

1. Introduction

An isolated DC-DC power converter is an essential part of the power systems applied in many fields, such as electric vehicles, energy storage systems, and distribution systems [1]. For these applications, an isolated DC-DC power converter can meet the requirements of galvanic isolation and power conversion [2,3]. Among various isolated DC-DC power converter topologies, high-frequency (HF) soft-switching pulse-width-modulation (PWM) DC-DC converters have become a universal solution due to their advantages such as low conduction loss, high power density, and high efficiency [4,5].

As bidirectional soft-switching PWM DC-DC converters, dual active bridge (DAB) converters are the most appealing due to their symmetrical topology, relatively simple structure, and inherent features. Many modulation schemes have been proposed for DAB converters, such as single-phase-shift modulation (SPS) and multi-phase-shift modulation (MPS). With more degrees of freedom and independent control variables of these modulation methods, control strategies for different optimization goals have been reported [6,7], such as minimum reactive current and power [8,9], minimum conduction loss [10], and a full power operation range for soft switching [11]. Nevertheless, the power calculation of these optimization methods is complex, and the operational mode is variable. Depending on the fundamental optimal method-based universal mode [12], a duty cycle modulation is proposed in [13]. Although the calculation becomes less complex, the soft-switching range is limited when the converter operation gain is nonoptimal. Simplified control strategies conflict with a wide zero-voltage switching (ZVS) range for traditional DC-DC resonant converters. Thus, a modified topology of the conventional DAB is proposed in [14] to widen the ZVS range. However, the adopted hybrid control method is also complex.

Apparently, these topologies and control strategies are complicated and cannot solve problems effectively. Another soft-switching PWM resonant topology, *LLC* resonant converters, have received more attention due to ZVS being achievable for switches and zero-current switching (ZCS) being realizable for diodes. For an *LLC* resonant converter, the soft-switching operation of all the switches and rectifier diodes can be achieved when designed in a proper working area [15–17]. Nevertheless, the circulation current will be enormous if the switching frequency operates far from the resonant frequency, narrowing the voltage regulation range and influencing performance. In [18,19], the related *LLC* converters are modified to enhance the efficiency over a wide load range, but the topology and control methods are very complex. A backflow power analysis method was proposed in [20] to increase the efficiency of *LLC* resonant converter. Based on the analysis of the internal relationship between the converter variables, the method can reduce the backflow power by optimizing the resonant parameters. However, the method neglects the influence of the magnetizing current during the deadtime. This results in the switches not meeting ZVS in the designed region. In [21], a combination control scheme of pulse frequency modulation (PFM) and SPS was proposed to ensure operation over a wide range. Furthermore, the paper also proposed a burst-mode control to maintain performance under light-load conditions. Nevertheless, the regulation capability of the hybrid control weakens at light load, and the proposed control method is complex in the reverse mode of an *LLC* resonant converter. Therefore, an *LLC* resonant converter with an auxiliary capacitor was proposed to improve the regulation capability in [22]. However, the influence of the coupling was ignored. In [23], a dual half-bridge *LLC* resonant converter was proposed to increase the efficiency. By making two resonant tanks work in different modes, ZVS for primary switches and ZCS for secondary diodes are achieved over the full power range. Nevertheless, the paper does not take into account the problem of the balance and equalization between two resonant tanks.

The concept of dual-transformer DC-DC converters has spread over the years [24–28]. In [24], a fixed-frequency dual-transformer *LLC* converter was studied. The converter can suppress the peak current and widen the ZVS operating range. However, there is always a high circulation current in the system, which causes high conduction loss. In [25], the dual-transformer structure can ensure soft switching under a wide range of loads. Nevertheless, the active switches cannot achieve their ZVS at light load when operating in buck mode. For this, an improved topology and optimized modulation method [26] were provided to make sure the converter operates stably in buck-boost mode. However, the power density becomes very low due to the complicated secondary side circuit. Further, the ZVS conditions were not improved either. A dual-transformer converter with discontinuous conduction mode operation is reported in [27] to reduce the filter size and improve performance. Additionally, in [28], a control law was proposed to simplify the topology structure and to reduce the degrees of freedom. Although most switches can achieve a wide ZVS range, the ZVS range of switches on the primary side is limited in reverse mode, and conduction loss is increased.

This paper proposes a new dual-transformer topology to improve the performance. The voltage stress on the transformers is greatly decreased by disassembling an HF transformer into two HF transformers. The current stress and backflow power on the secondary side are naturally minimized due to the topology structure. By optimizing the ratio k of two HF transformers, the proposed DTRC has a lower boundary output power of losing ZVS. Therefore, the ZVS operation range of the converter is widened, resulting in reduced switching loss and increased efficiency. Compared to a traditional soft-switching PWM resonant converter, the performance of the proposed converter is much better. The outline of the paper is as follows. Section 2 presents the topology and the operating principle of the proposed converter. Section 3 describes the steady-state analysis and the ZVS switching constraints to obtain the power transfer characteristics. In Section 4, the selection and design of the parameters with detailed procedures are given. Finally, simulation and experimental results from actual tests on a prototype converter are provided in Section 5.

2. Topology Details and Operation of the DTRC

The proposed Dual-Transformer DC-DC Resonant Converter (DTRC) consists of a three-arm-bridge circuit and an H-bridge circuit, as shown in Figure 1. On the primary side, it has four active switches $M_A \sim M_D$, and each switch has a body diode ($d_A \sim d_D$) and a parasitic capacitor ($C_{MA} \sim C_{MD}$). In addition, the three-arm bridge can be seen as two identical half-bridge circuits. Four diodes $d_1 \sim d_4$ form the H-bridge circuit on the secondary side. The three-arm bridge and H-type bridge are connected by two HF transformers, T_1 and T_2. On the primary side of T_1 and T_2, two identical half-bridge circuits are connected in parallel. The neutral voltage point is shared by two half-bridge circuits and two capacitors, C_1 and C_2. The resonant tank (L_r and C_r) is connected in series on the secondary side of T_1 and T_2. The currents of two half-bridge circuits reflected on the secondary side are equal to the resonant current i_r due to the series connection on the secondary side. The turns ratio of T_1 is $n_1 : 1$, while T_2 is $n_2 : 1$.
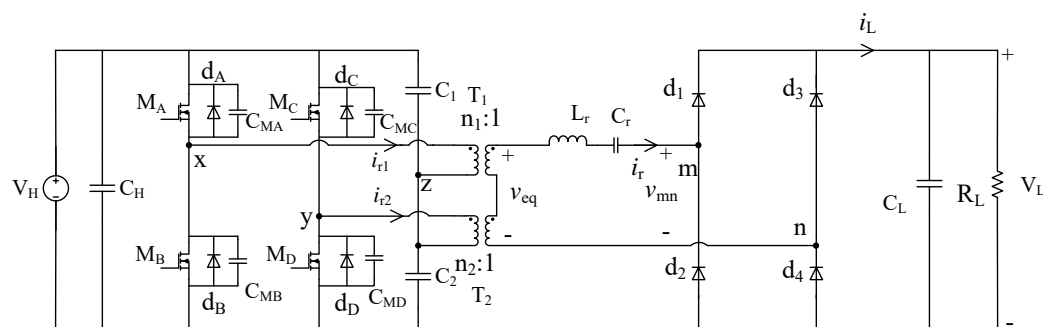

Figure 1. The topology of the Dual-Transformer DC-DC Resonant Converter.

The steady-state operation waveforms of the DTRC are shown in Figure 2. Fixed-switching-frequency gating signals with 50% duty cycle are given to switches $M_A \sim M_D$. Switches M_A, M_B, and M_C, M_D are complementarily conducted, i.e., switching signals on the same bridge arm are 180° out of phase. The mid-point voltages v_{xz} and v_{yz} are generated by the parallel connection. Their amplitudes are equal to $V_H/2$. Phase-shifted gating signals are given to arm M_C, M_D, causing a phase-shifted angle α between the voltages v_{xz} and v_{yz}. The output voltage V_L can be regulated by changing the phase-shift angle α. Due to four diodes forming the circuit, rectification is realized naturally on the secondary side of the DTRC. Thus, the resonant current i_r is in phase with the voltage v_{mn}. The voltage v_{mn} generated on the secondary side lags behind the mid-point voltage v_{xz} by phase-shift angle γ, which is defined as the time delay from the rising edge of M_A to the zero-crossing point of i_r.

As shown in Figure 2, there are six operation intervals in one switching cycle. The equivalent circuits for these intervals are shown in Figure 3. For convenience, several assumptions are made: (1) All the active and passive components and HF transformers are ideal. (2) The dead-gap effect and effects of all parasitic capacitors ($C_{MA} \sim C_{MD}$) are neglected. (3) Residual capacitors (C_H, C_1, C_2, C_L) are large enough to maintain the voltages.
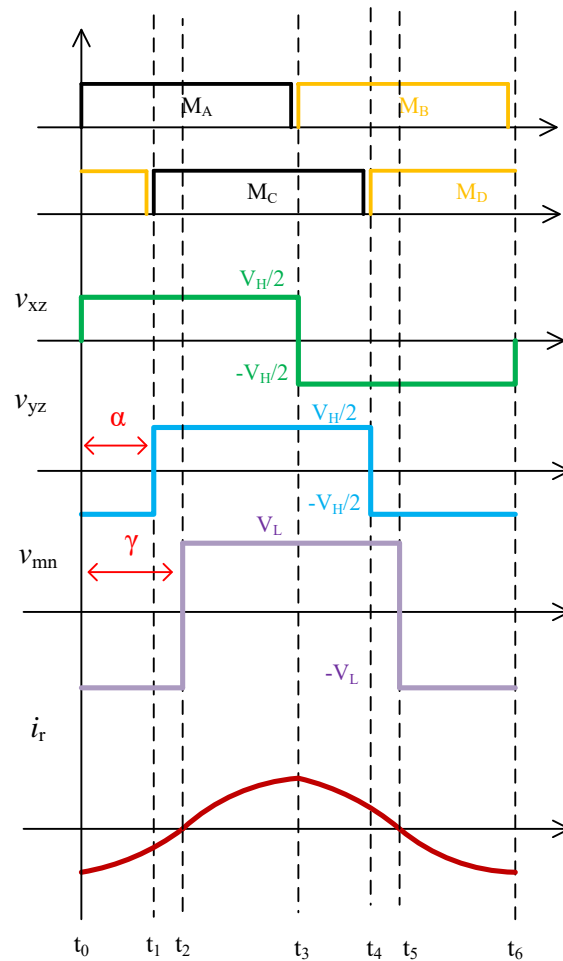
Figure 2. The steady-state operation waveforms of the DTRC.

Interval 1 (t_0–t_1) (Figure 3a): Before t_0, switches M_B and M_D were conducted. At $t = t_0$, M_B is turned off and M_A is turned on. The current flows through d_A. The resonant current i_r is negative and increases gradually. On the secondary side, the resonant current flows through diodes d_2 and d_3; therefore, the voltages $v_{xz} = +V_H/2$, $v_{yz} = -V_H/2$, $v_{mn} = -V_L$. This interval ends when M_D is turned off and M_C is turned on.

Interval 2 (t_1–t_2) (Figure 3b): In this interval, M_D is turned off and M_C is turned on. The resonant current i_r is constantly negative and gradually increasing. Meanwhile, it flows through diodes d_2 and d_3. Therefore the voltage $v_{mn} = -V_L$. The currents flow through d_A and d_C on the primary side. The mid-point voltages $v_{xz} = +V_H/2$, $v_{yz} = +V_H/2$. This interval ends when i_r reaches 0.

Interval 3 (t_2–t_3) (Figure 3c): Compared with Interval 2, the resonant current changes the polarity in this interval. It increases from 0 to positive and flows through diodes d_1 and d_4. The switch currents become positive and flow through M_A and M_C, so the voltages $v_{xz} = +V_H/2$, $v_{yz} = +V_H/2$, $v_{mn} = +V_L$. This interval ends when M_A is turned off and M_B is turned on.

Interval 4 (t_3–t_4) (Figure 3d): This interval begins when M_A is turned off and M_B is turned on forcibly. The current is shifted from M_C to d_B, which enables the zero-voltage turn-on of M_B. There is no change on the secondary side except for a gradual decrease in the resonant current. The voltages $v_{xz} = -V_H/2$, $v_{yz} = +V_H/2$, $v_{mn} = +V_L$. This interval lasts until M_C is turned off and M_D is turned on.

Interval 5 (t_4–t_5) (Figure 3e): The new interval begins when the gating signal of M_C is removed. M_D is turned on with ZVS. There is still no change on the primary side. The voltages $v_{xz} = -V_H/2$, $v_{yz} = -V_H/2$, $v_{mn} = +V_L$. At the end of this interval, $t = t_5$, and the resonant current reaches 0.

Interval 6 (t_5–t_6) (Figure 3f): Although the resonant current reached 0 at the end of the last interval, M_B and M_D remain turned on. On the secondary side, the resonant current decreases and flows through d_2 and d_3. The diodes d_1 and d_4 are turned off with ZCS. The voltages $v_{xz} = -V_H/2$, $v_{yz} = -V_H/2$, $v_{mn} = -V_L$. This interval ends when M_B is turned off and M_A is turned on. This completes the operation of the DTRC in one switching cycle.
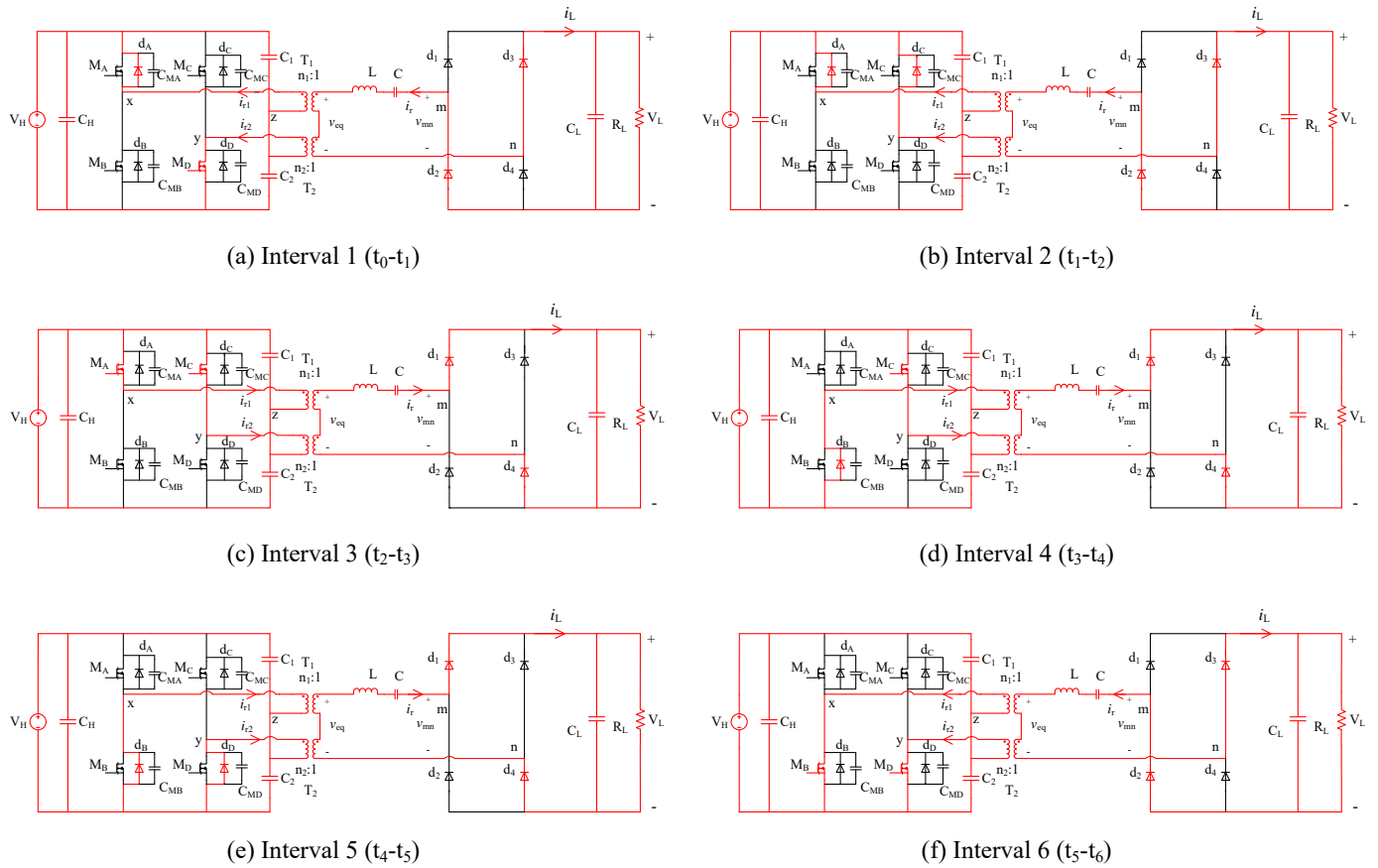
(a) Interval 1 (t_0-t_1)

(b) Interval 2 (t_1-t_2)

(c) Interval 3 (t_2-t_3)

(d) Interval 4 (t_3-t_4)

(e) Interval 5 (t_4-t_5)

(f) Interval 6 (t_5-t_6)

Figure 3. The equivalent circuits during different intervals of DTRC.

3. Steady-State Analysis and the ZVS Regions of the DTRC

3.1. Steady-State Analysis

To simplify the calculation, the fundamental harmonics approximation (FHA) approach is used due to the nearly sinusoidal waveforms of voltages/currents in the DTRC. Further, parameters on the primary side of HF transformers are transferred to the secondary side for ease of analysis. It is assumed that all of the active and passive components and HF transformers are ideal, and the dead-gap effect is ignored, too. To make analysis more convenient, all parameters are normalized using the following base values:

$$V_B = \frac{V_H}{n_1}; \quad Z_B = R_L; \quad I_B = \frac{V_B}{Z_B}; \quad \omega_B = \omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{1}$$

where $R_L = V_L^2/P_r$ is the full-load resistance on the secondary side, and P_r is the rated power. The turns ratios of two HF transformers are $n_1 : 1$ and $n_2 : 1$, respectively, and the parameter k is defined as $k = n_2/n_1$. The voltage gain M of the DTRC is defined as:

$$M = \frac{n_1 V_L}{V_H} \tag{2}$$

The normalized values of reactance can be shown as:

$$X_{Lr,pu} = QF, X_{Cr,pu} = -\frac{Q}{F} \tag{3}$$

where $F = \omega_s/\omega_r$, $Q = \omega_r L_r/R_L$ are the normalized switching frequency and quality factor, respectively.

The FHA equivalent circuit of the DTRC is given in Figure 4. For the resonant tank attached on the secondary side, it is more convenient that the mid-point voltages v_{xz} and v_{yz} reflect onto the secondary side. The normalized expressions of the reflected voltage sources $v'_{xz,pu}$ and $v'_{yz,pu}$ are given by:

$$
\begin{aligned}
v'_{xz,pu}(\omega_s t) &= \frac{1}{n_1} v_{xz,pu}(\omega_s t) = \frac{2}{\pi} \sin(\omega_s t) \\
v'_{yz,pu}(\omega_s t) &= \frac{1}{n_2} v_{yz,pu}(\omega_s t) = \frac{2}{k\pi} \sin(\omega_s t - \alpha)
\end{aligned}
\tag{4}
$$

Defining $v_{eq,pu}$ as the equivalent voltage source of $v'_{xz,pu}$ and $v'_{yz,pu}$, it is expressed as:

$$v_{eq,pu}(\omega_s t) = \frac{2}{\pi}\sqrt{\frac{2}{k}\cos\alpha + (\frac{1}{k})^2 + 1}\sin(\omega_s t - \arctan(\frac{\frac{1}{k}\sin\alpha}{1 + \frac{1}{k}\cos\alpha})) \tag{5}$$

The normalized voltage source $v_{mn,pu}$ is obtained as:

$$v_{mn,pu}(\omega_s t) = \frac{4M}{\pi}\sin(\omega_s t - \gamma) \tag{6}$$

According to Figure 4, the normalized resonant current $i_{r,pu}$ is written as:

$$i_{r,pu}(\omega_s t) = \frac{v_{eq,pu}(\omega_s t) - v_{mn,pu}(\omega_s t)}{j(QF - \frac{Q}{F})} \tag{7}$$
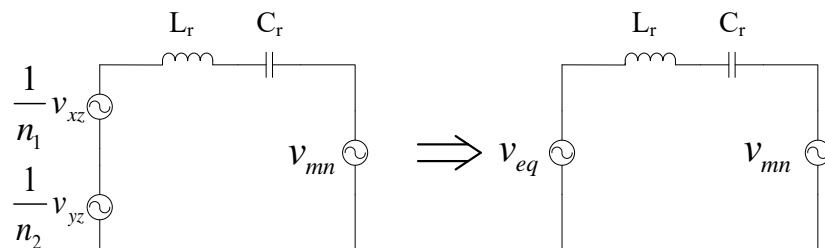

Figure 4. The FHA equivalent circuit of the DTRC.

After simplifying the equation, the resonant current is:

$$i_{r,pu}(\omega_s t) = I_{r,pu} \cdot \cos(\omega_s t + \angle i_{r,pu}) \tag{8}$$

where the peak value of the resonant current $I_{r,pu}$ and the phase angle $\angle i_{r,pu}$ are shown as follows:

$$
\begin{aligned}
I_{r,pu} &= \frac{2}{\pi(QF - \frac{Q}{F})}\sqrt{4M^2 - 4M\frac{1}{k}\cos(\gamma - \alpha) - 4M\cos\gamma + \frac{2}{k}\cos\alpha + (\frac{1}{k})^2 + 1} \\
\angle i_{r,pu} &= \arctan(\frac{2M\sin\gamma - \frac{1}{k}\sin\alpha}{1 + \frac{1}{k}\cos\alpha - 2M\cos\gamma})
\end{aligned}
\tag{9}
$$

Thus, the normalized output power can be expressed as:

$$P_{L,pu} = \frac{4M}{\pi^2(QF - \frac{Q}{F})}(\sin\gamma + \frac{1}{k}\sin(\gamma - \alpha)) \tag{10}$$

Due to the diodes' rectification on the secondary side, the resonant current i_r is in phase with the voltage v_{mn}. Thus, the resonant current i_r equals zero at t_2:

$$i_{r,pu}(\omega_s t_2) = i_{r,pu}(\gamma) = 0 \tag{11}$$

which means the phase angle of i_r is equal to $\gamma + \frac{\pi}{2}$:

$$\left|\angle i_{r,pu}\right| = \gamma + \frac{\pi}{2} \tag{12}$$

Then, the relationship between α, γ and M can be expressed as:

$$2M = \cos\gamma + \frac{1}{k}\cos(\gamma - \alpha) \tag{13}$$

Combining (10) with (13), the normalized output power can be calculated as (14). It is clear that the value of the output power is controlled only by the phase-shifted angle α.

$$P_{L,pu} = \frac{4M}{\pi^2(QF - \frac{Q}{F})}\sqrt{(\frac{1}{k})^2 + \frac{2}{k}\cos\alpha - 4M^2 + 1} \tag{14}$$

3.2. ZVS Region

The essential condition of ZVS operation for each switch is that the switch current ought to be negative when the switch is turned on. To achieve ZVS, the resonant current should be negative for M_A and M_C while positive for M_B and M_D at the turn-on moment. Thus, the ZVS constraints for the switches $M_A \sim M_D$ of the DTRC are simplified as follows: ZVS of M_A and M_C requires $i_r < 0$, while that of M_B and M_D requires $i_r > 0$. The constraints can be expressed as follows:

$$\begin{cases} i_r(t_0) < 0 \\ i_r(t_1) < 0 \\ i_r(t_3) > 0 \\ i_r(t_4) > 0 \end{cases} \Rightarrow \begin{cases} i_r(t_0) = -i_r(t_3) < 0 \\ i_r(t_1) = -i_r(t_4) < 0 \end{cases} \tag{15}$$

Then, the ZVS conditions for the switches of the DTRC are summarized in Table 1.

Table 1. The ZVS conditions for the switches.

Switches	ZVS Conditions
M_A, M_B	$2M\cos\gamma - \frac{1}{k}\cos\alpha - 1 < 0$
M_C, M_D	$2M\cos(\gamma - \alpha) - \cos\alpha - \frac{1}{k} < 0$

The ZVS operation regions for the trajectory of the output power transfer are shown in Figure 5. The red line represents the ZVS operation boundary of M_A, M_B, and the cyan line is the boundary of M_C, M_D. The region where switches $M_A \sim M_D$ will lose ZVS are marked in the figure. The black line represents the trajectory of the power transfer. The blue intersection of three lines indicates the zero power, i.e., $P_L = 0$. It can be seen that the power point is moving away from the ZVS boundary of M_A, M_B with the increasing power level, which means the switches M_A and M_B always work in ZVS operation. Meanwhile, part of the black line is in the area where M_C and M_D lose ZVS. That means M_C and M_D will lose ZVS at partial loads.
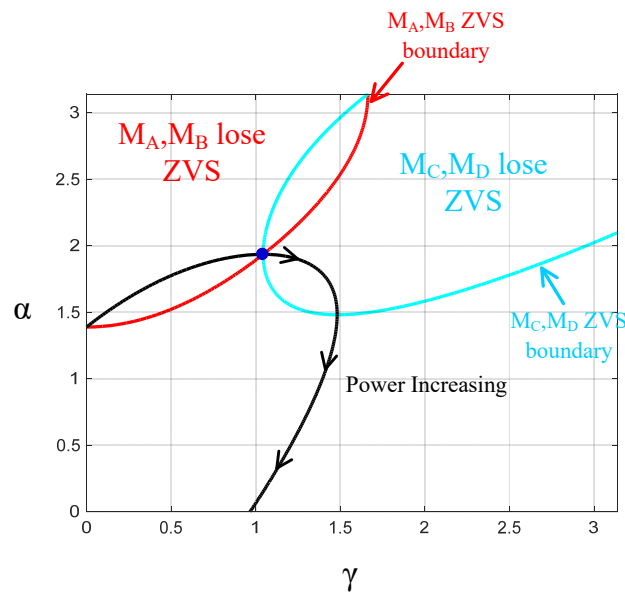
Figure 5. The ZVS operation regions for the trajectory of the power transfer.

4. Design Procedures

4.1. Selection of k

From the steady-state and ZVS region analysis, it is found that the proposed DTRC operates as the conventional soft-switching PWM resonant converter when $k = 1$. In order to compare the performances of the DTRC and the PWM converter, the total loss of two converters is analyzed next.

The total loss of the resonant converter is mainly divided into two aspects: the conduction loss and the switching loss. Combining (9) with (13), the normalized root mean square (RMS) value of resonant current $I_{r,rms,pu}$ can be expressed as:

$$I_{r,rms,pu} = \frac{2}{\sqrt{2}\pi(QF - \frac{Q}{F})}\sqrt{(\frac{1}{k})^2 + \frac{2}{k}\cos\alpha - 4M^2 + 1} \tag{16}$$

From (14) and (16), the relationship between the output power and the RMS value of the resonant current is shown as (17):

$$I_{r,rms,pu} = \frac{\sqrt{2}\pi \cdot P_{L,pu}}{4M} \tag{17}$$

It can be seen that the RMS value of resonant currents through the DTRC and the PWM converter will be the same if they have the same output power P_L; so the different values of k do not affect the RMS value of resonant current. Therefore, there is no apparent difference in conduction loss between the DTRC and the PWM converter.

Consequently, the switching loss becomes the principal portion of the total loss for two converters. Due to the diodes' circuit on the secondary side, the operation of the converter must meet the requirement of expression (13), i.e., the diodes' rectification. According to Figure 5, it is possible to lose ZVS of the switches M_C and M_D at light load for two converters. Thus, the boundary output power of losing ZVS for each converter can be predicted by the following conditions:

$$\begin{cases} 2M\cos(\gamma - \alpha) - \cos\alpha - \frac{1}{k} = 0 \\ 2M = \cos\gamma + \frac{1}{k}\cos(\gamma - \alpha) \end{cases} \tag{18}$$

Then, the boundary output power of losing ZVS for the proposed DTRC is expressed as:

$$P_{L,ZVS,pu} = \frac{4M}{\pi^2(QF - \frac{Q}{F})}\sqrt{1 - (2M - \frac{1}{k})^2} \tag{19}$$

When $k = 1$, the DTRC works as the PWM converter. Let k be equal to 1 in expression (19), the boundary output power of losing ZVS for the traditional PWM converter can be simplified as:

$$P_{t,ZVS,pu} = \frac{8M}{\pi^2(QF - \frac{Q}{F})}\sqrt{M - M^2} \tag{20}$$

Once the voltage gain M is determined, the boundary output power of losing ZVS for the traditional PWM converter is specific while uncertain for the DTRC due to k. Thus, the performance of the DTRC is decided by k. Set D as the ratio of the boundary output power of losing ZVS between the DTRC and the traditional PWM converter as follows:

$$D = \frac{2\sqrt{M - M^2}}{\sqrt{1 - (2M - \frac{1}{k})^2}} \tag{21}$$

Taking $M = 0.5$ as an example, the relationship between D and different k is shown in Figure 6. According to (21), $D > 1$ means the boundary output power of losing ZVS for the DTRC is lower than that for the PWM converter. That means the DTRC has a wider ZVS operation range when $D > 1$. As shown in Figure 5, the ZVS constraint of switches M_C is the same as M_D for the DTRC and the traditional PWM resonant converter. Even at 50% load, it is possible for M_C and M_D to lose their ZVS. The values of D represent the multiple of the boundary output power of the PWM converter. For example, if the ZVS boundary power of the PWM converter is 100 W when D = 2, the boundary power of the DTRC will only be 50 W. According to expression (21), the value of D will be large enough at $k = 0.5$, which means the DTRC can hardly lose ZVS. In order to validate the above analysis, $M = 0.5$, $k = 0.5$ are selected to compare the switching loss (ZVS operation) of the DTRC and traditional soft-switching PWM converter.
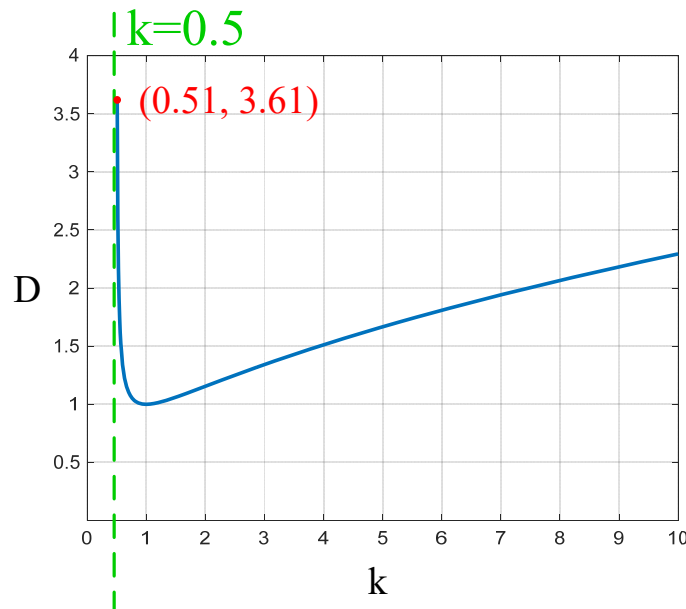

Figure 6. The ratio of the boundary output power for losing ZVS at different values of k.

Figure 7 shows the variation ranges of $P_{L,pu}$ and α when M and k change. Once M and k are determined, the normalized output power $P_{L,pu}$ will only be regulated by the phase angle α according to (14). Figure 7 demonstrates that the DTRC has a broader operating range and more extensive power range when $M = 0.5$, $k = 0.5$. It also can be found that the

peak output power when $M = 0.5$, $k = 0.5$ is always greater than others. Therefore, in this case, the output power of DTRC can be easily regulated.
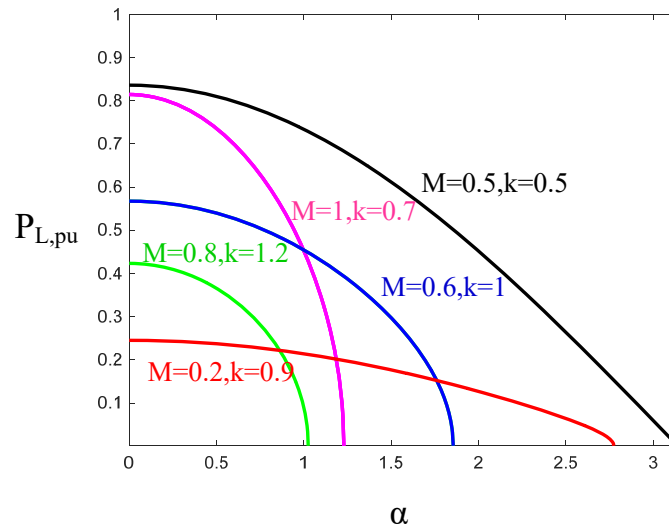

Figure 7. The variation ranges of $P_{L,pu}$ and α at different values of M and k.

4.2. Design Example

To validate the theoretical analysis of the DTRC, a converter is designed as follows: the rated output power $P_r = 200$ W, input voltage $V_H = 150$ V, output voltage $V_L = 80$ V, switching frequency $f_s = 100$ kHz, and values of $M = 0.5$, $k = 0.5$ are chosen. The selection value of the normalized switching frequency F should be greater than one but close to one to regulate ZVS operation of the converter and to reduce the circulation of the switches on the primary side. The appropriate Q value is selected to reduce the resonant current and voltage peak and to improve the power factor. In this paper, $Q = 1$ and $F = 1.4$ are chosen.

For the proposed DTRC, $V_H = 150$ V, $V_L = 80$ V, $P_r = 200$ W, $f_s = 100$ kHz, $M = 0.5$, and $k = 0.5$. Thus, the turns ratio of T_1 can be calculated by M, and it is shown as follows:

$$M = \frac{n_1 V_L}{V_H} = 0.5 \tag{22}$$

which turns out to be:

$$n_1 = \frac{M V_H}{V_L} = 0.9375 \tag{23}$$

Thus, the turns ratio of T_2 can be written as:

$$n_2 = k n_1 = 0.46875 \tag{24}$$

The base value of the voltage

$$V_B = \frac{V_H}{n_1} = 160V \tag{25}$$

the load resistance

$$R_B = R_L = \frac{V_L^2}{P_r} = 32\Omega \tag{26}$$

and the current

$$I_B = \frac{V_B}{R_B} = 5A \tag{27}$$

Therefore, the base value of the output power will be:

$$P_B = \frac{V_B^2}{R_B} = 800W \tag{28}$$

The values of the resonant tank are calculated as:

$$F = \frac{\omega_s}{\omega_r} = \frac{2\pi f_s}{\sqrt{L_r C_r}} = 1.4$$

$$Q = \frac{\omega_r L_r}{R_L} = 1$$

(29)

The values of the resonant tank are solved as:

$$L_r = 71.3\mu H$$

$$C_r = 69.63nF.$$

(30)

5. Simulation and Experimental Results

5.1. Simulation Results

The ZVS region and the power lines of k and α are shown in Figure 8. The switches M_A and M_B consistently achieve ZVS no matter what the value of k is, as shown in Figure 5. The shaded area represents that M_C and M_D lose ZVS. The red dashed lines are the power lines of 200 W, 150 W, 100 W, and 50 W, respectively. According to Figure 8, the purple line $k = 1$ has four intersections with four power lines, and the intersections are all located in the shaded area. That means switches M_A and M_B achieve ZVS, while M_C and M_D lose ZVS during the four power conditions when $M = 0.5$. For the traditional soft-switching PWM converter, i.e., $k = 1$, switches M_C and M_D lose ZVS at light load or even half load. The conclusion conforms to how a traditional soft-switching PWM converter performs. For the proposed DTRC, four intersections are located out of the shaded area at $k = 0.5$. That means all the switches work in ZVS operation under different loads.
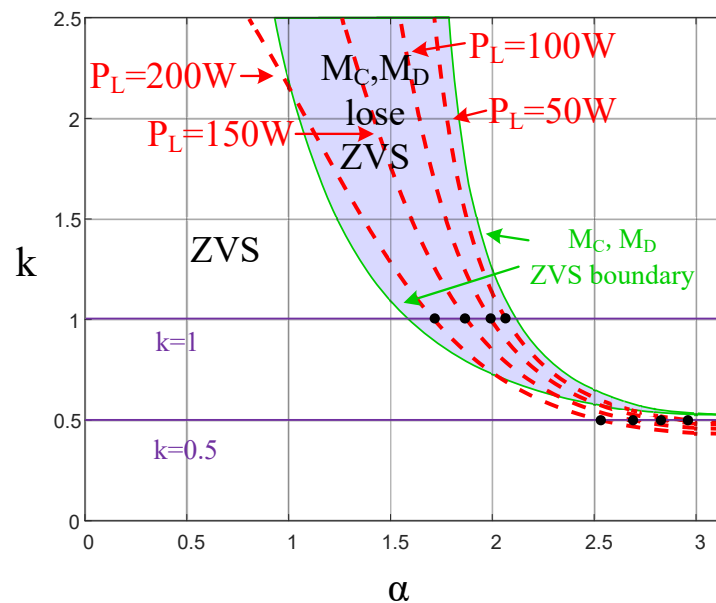

Figure 8. The ZVS region and the power lines of k and α.

To show the relationship more clearly, the comparison between the traditional PWM converter ($k = 1$) and the DTRC ($k = 0.5$) is shown in Figure 9. Figure 9a shows the ZVS region and the power lines when $k = 1$ at $M = 0.5$. Switches M_A, M_B continuously meet ZVS when k takes different values. The blue line is the ZVS boundary of switches M_C, M_D. The area where M_C, M_D lose ZVS is marked in the figure. The dashed lines in magenta are the different power lines. As shown in Figure 9, the values of α and γ that allow the converter to achieve the required power are restricted due to rectification of the secondary-side H-type bridge, i.e., the green line in the figure. In Figure 9a, four power lines, 200 W, 150 W, 100 W, and 50 W, have four intersections with the rectification path. All of the intersections

are located in the areas where M_A, M_B achieve ZVS while M_C, M_D lose ZVS when $k = 1$. In Figure 9b, the intersections are located where M_A, M_B, M_C, and M_D all work in ZVS operation when $k = 0.5$.

In this paper, PSIM software is used to perform the simulation. Simulations are done for four cases: 200 W, 150 W, 100 W, and 50 W. The critical simulation waveforms of the midpoint voltages (v_{xz} and v_{yz}), the secondary side square-wave voltage (v_{mn}), the resonant current (i_r), the output current (i_L), and the currents through four active switches ($M_A \sim M_D$) and four diodes ($d_1 \sim d_4$) at $k = 0.5$ when $M = 0.5$ are shown in Figure 10, respectively. The output voltage V_L is regulated at 80 V. The output current i_L realizes the rectification, and the diodes $d_1 \sim d_4$ achieve ZCS on the secondary side. The switches on the primary side all work in ZVS operation at the four power conditions. All waveforms are matched with what is expected.
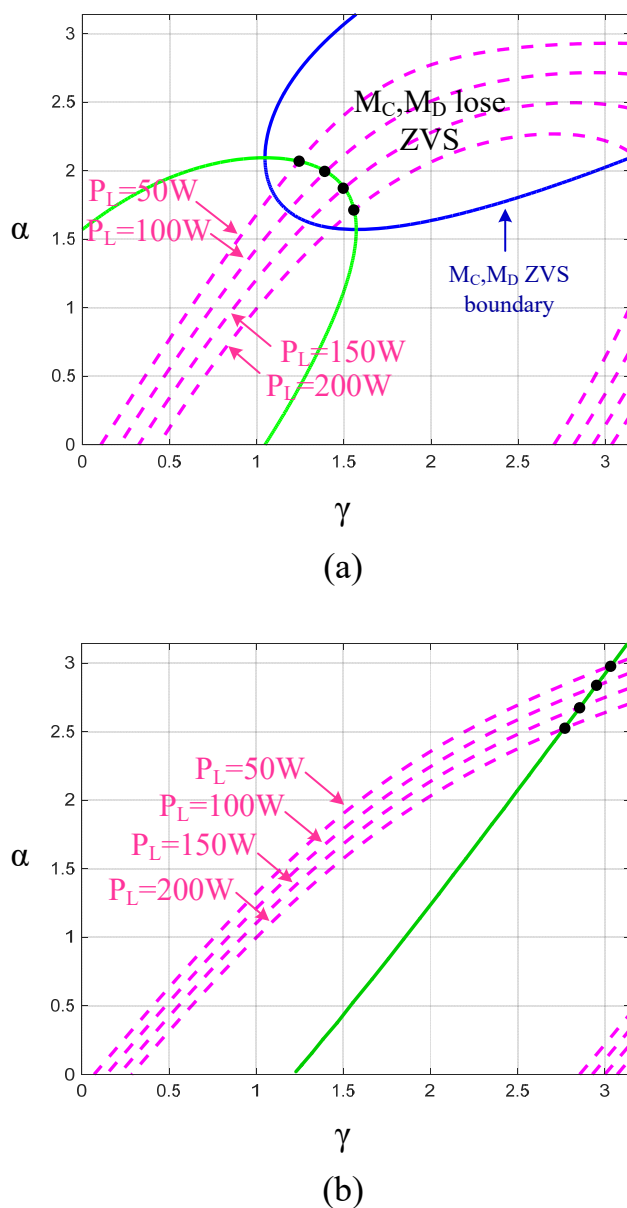

(a)

(b)

Figure 9. The ZVS region and the power lines of α and γ at $M = 0.5$: (**a**) $k = 1$; (**b**) $k = 0.5$.

The voltages v_{xz} and v_{yz} have a phase shift α, and their amplitudes are $V_H/2 = 150$ V$/2$ = 75 V. The voltage v_{mn} lags behind v_{xz} a phase-shifted angle γ, and its amplitude is 80 V. The resonant current i_r is approximately sinusoidal. Further, Figure 10 demonstrates ZVS
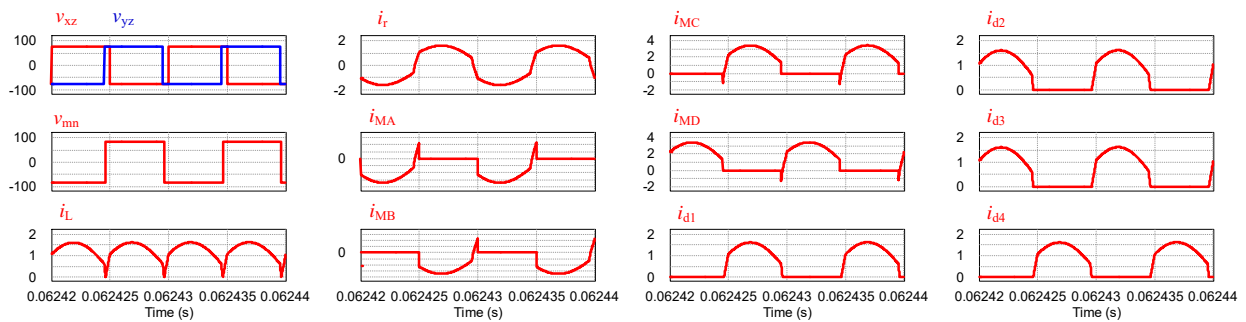
for $M_A \sim M_D$ since their body-parallel diodes conduct before the switches start conducting. For the converter, the current stress decreases with lower power, and the output current i_L has almost no circulation during each cycle.
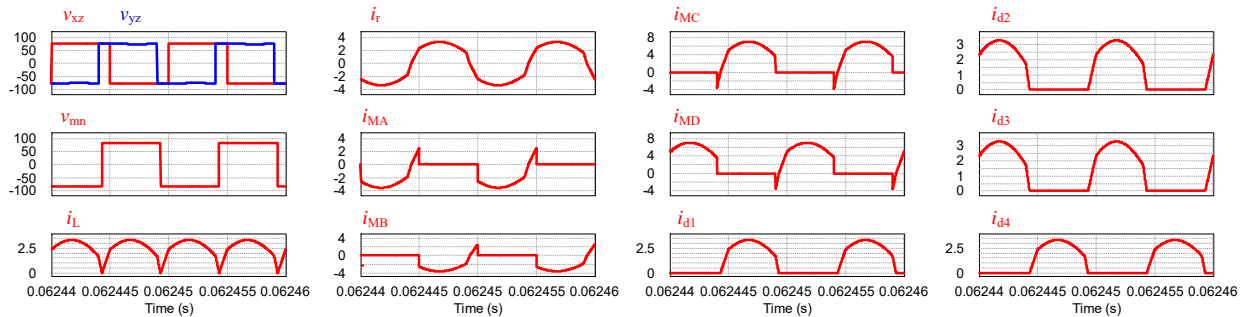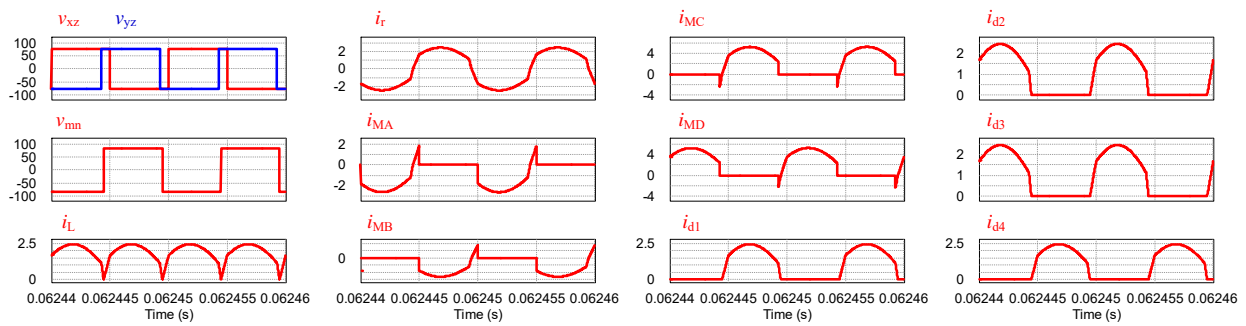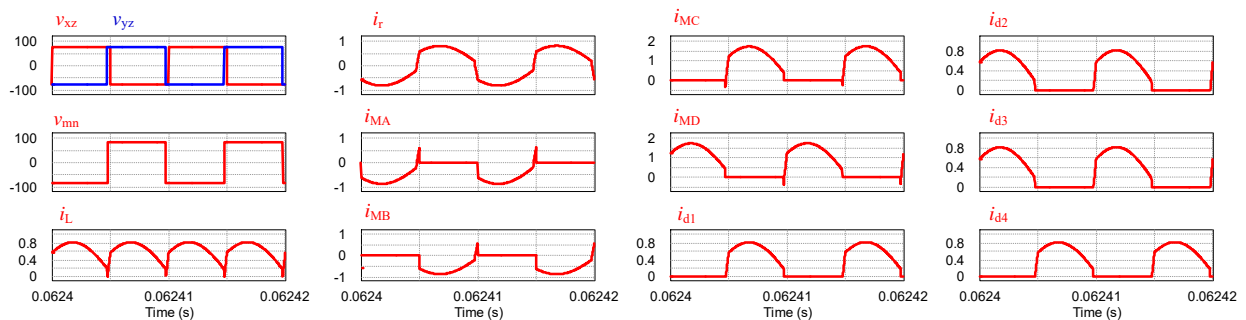

Figure 10. The key simulation waveforms of the DTRC at $k = 0.5$ when $M = 0.5$: (**a**) 200 W; (**b**) 150 W; (**c**) 100 W; and (**d**) 50 W.

5.2. Experiment Results

A 200 W, 150 V input, 80 V output, switching at 100 kHz, experimental dual-transformer DC-DC resonant converter was built in the laboratory based on the design parameters obtained in Section 4. Some details are provided to verify the performance of the proposed DTRC in the following. Figure 11 shows the experimental prototype divided into four parts: the FPGA controller, the primary and secondary side bridge circuits, the HF transformers, and the *LC* resonant tank. The critical parameters of the experimental prototype are summarized in Table 2. The control platform is an FPGA development board, in which HF gating signals for the MOSFETs are generated. The resonant inductor L_r comprises two transformer leakage inductors and an external inductor.

Table 2. Parameters of the prototype.

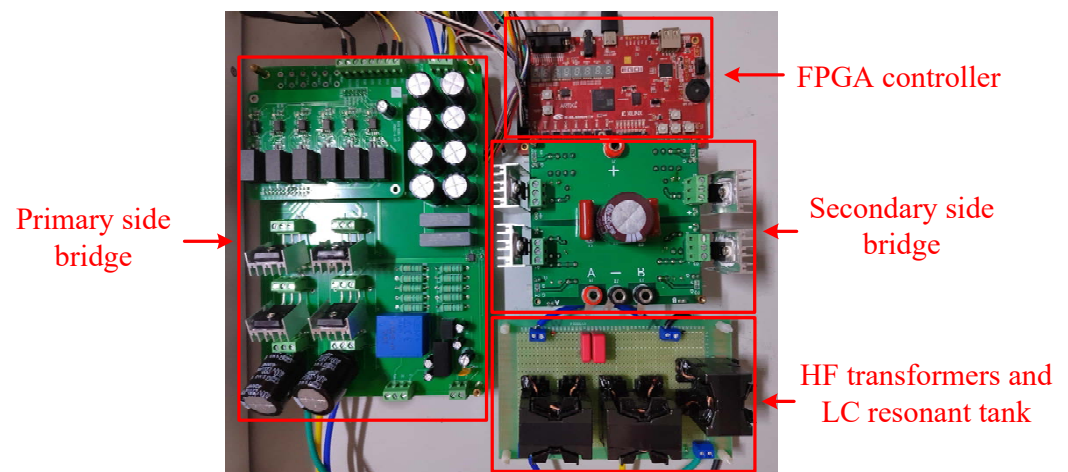| Parameter	Value
Input voltage (V_H)	150 V
Output voltage (V_L)	80 V
Rated power (P_r)	200 W
Switching frequency (f_s)	100 kHz
Turns ratio of the transformer T_1 (n_1:1)	30:32
Turns ratio of the transformer T_2 (n_2:1)	15:32
Resonant inductor (L_r)	71.3 μH
Resonant capacitor (C_r)	69.63 nF
Primary-side switches ($M_A \sim M_D$)	C3M0025065D (650 V/97 A)
Secondary-side diodes ($d_1 \sim d_4$)	MBR40250G (250 V/40 A)

Figure 11. The experimental prototype of the proposed converter.

Figure 12a–d illustrate the gating signals $v_{g,M_A} \sim v_{g,M_D}$ of the active switches $M_A \sim M_D$ at different power levels from 100% load to 25% load, respectively. Power devices M_A, M_B and M_C, M_D work complementarily with a fixed duty cycle of 0.5. Figure 13 provides the measured results of mid-point voltages v_{xz}, v_{yz} and currents i_{r1}, i_{r2} on the primary side. Figure 13a shows the full-load case. The primary-side full-bridge circuit is seen as two half-bridge circuits. Two capacitors C_1, C_2 share the midpoint, so the amplitudes of two voltages $v_{xz} = v_{yz} = V_H/2 = 150\,\text{V}/2 = 75\,\text{V}$. The current i_{r1} is different from i_{r2} due to different transformer ratios of the two HF transformers T_1, T_2, and the RMS values of resonant currents i_{r1}, i_{r2} are $I_{r1,rms} = 2.84$ A, $I_{r2,rms} = 5.61$ A. The theoretical RMS values are $I_{r1,rms} = 2.96$ A, $I_{r2,rms} = 5.92$ A. It can be seen that there is not much difference between the theoretical and experimental results. Figure 13b–d provides the waveforms at 75%, 50%, and 25% load. The amplitudes of the voltages remain.
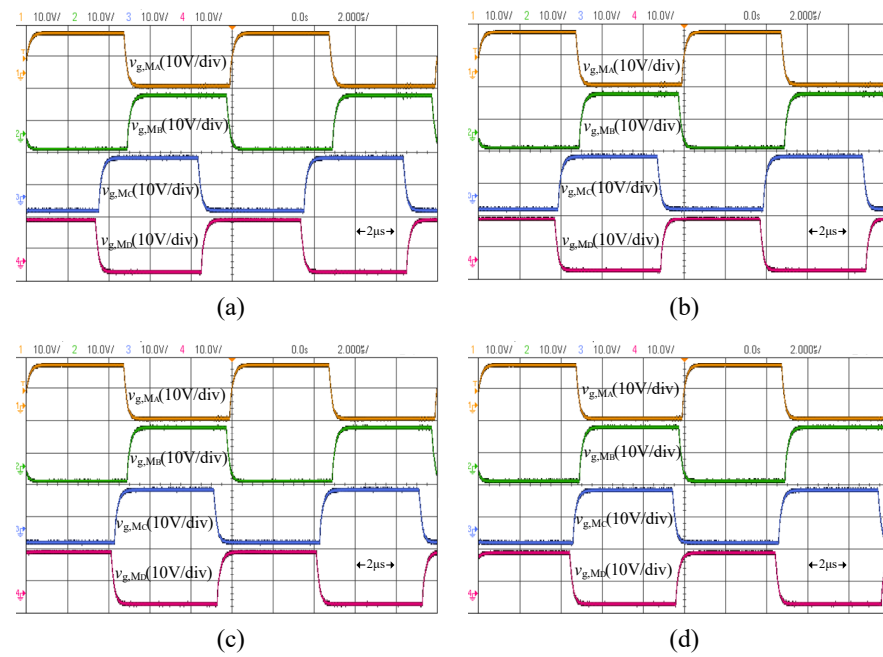
Figure 12. Experimental gating signals $v_{g,M_A} \sim v_{g,M_D}$ at different power levels: (**a**) 200 W, (**b**) 150 W, (**c**) 100 W, and (**d**) 50 W.
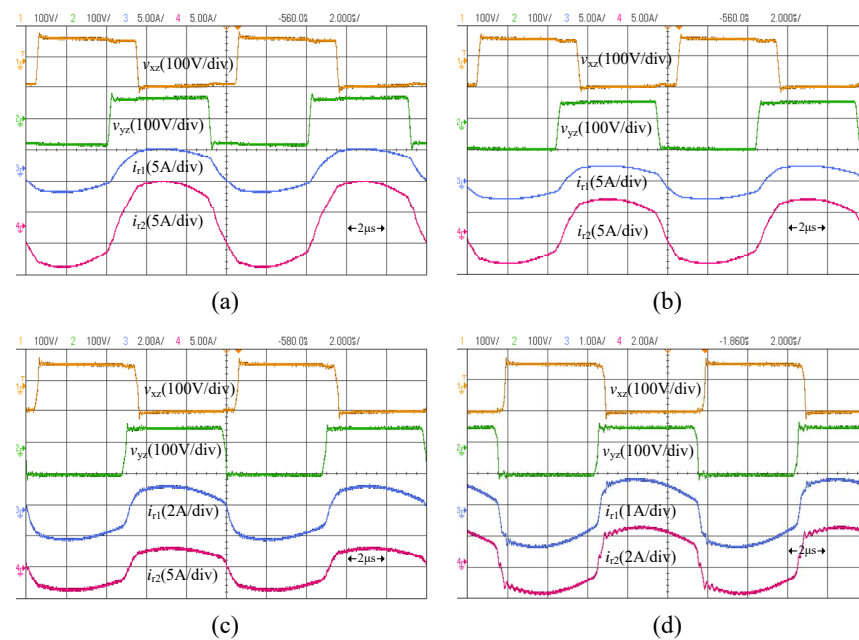

Figure 13. Experimental mid-point voltages v_{xz}, v_{yz} and current results i_{r1}, i_{r2} at different power levels: (**a**) 200 W, (**b**) 150 W, (**c**) 100 W, and (**d**) 50 W.

The RMS values of current i_{r1} are 2.13 A, 1.38 A, and 0.73 A, and those of i_{r2} are 4.28 A, 2.75 A, and 1.45 A, respectively, which also matches the theoretical values well. Furthermore, it can be observed that the resonant currents are negative for M_A and M_C while positive for M_B and M_D at the turn-on moment. That is to say, ZVS operation of all the active switches is achieved at the four power conditions. Figure 14a–d show the tested results of square voltage v_{mn}, capacitor voltage v_{Cr}, and resonant current i_r on the secondary side when the output power ranges from 200 W to 50 W. The amplitudes of

the secondary side voltage v_{mn} are kept at 80 V under different load conditions. The RMS values of resonant current i_r at 100% to 25% rated power are 2.67 A, 2.03 A, 1.31 A, and 0.68 A, respectively. The results are almost the same as the theoretical results. The voltage v_{mn} is in phase with the resonant current i_r. The capacitor voltage v_{Cr} and resonant current i_r are nearly sinusoidal, confirming resonance operation. Figure 15a–d demonstrate the gating signals and switch voltages of M_A and M_B under different loads. The gating signals and switch voltages of M_C and M_D are not given due to having the same waveforms as M_A and M_B except for the phase-shift angle α. Load voltage is maintained at 80 V by increasing the phase angle α when the loads are reduced. The operation performance with full ZVS operation and circulation current minimization is realized. All experimental results match the theory and simulation well. The efficiency of the DTRC at four power levels is shown in Figure 16. The recorded efficiencies at 200 W, 150 W, 100 W, and 50 W are 94.02%, 95.36%, 96.16%, and 90.87%, respectively. Since ZVS operation is achieved and switching loss is reduced, the overall efficiency of the DTRC exceeds 90%.
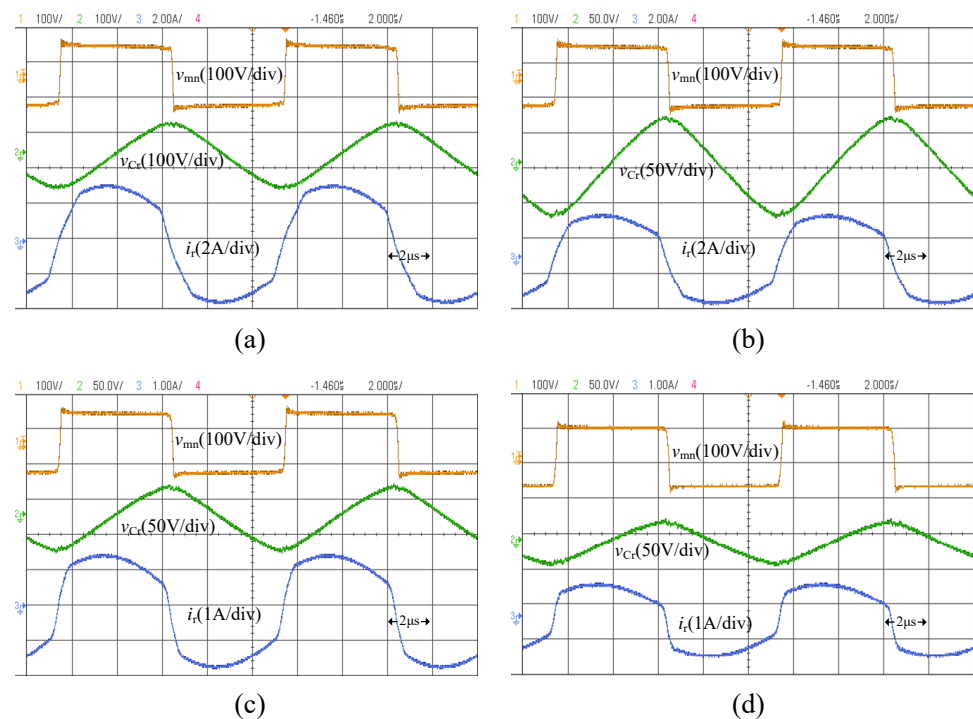

(a)

(b)

(c)

(d)

Figure 14. Experimental square voltage v_{mn}, capacitor voltage v_{Cr}, and resonant current i_r at different power levels: (**a**) 200 W, (**b**) 150 W, (**c**) 100 W, and (**d**) 50 W.
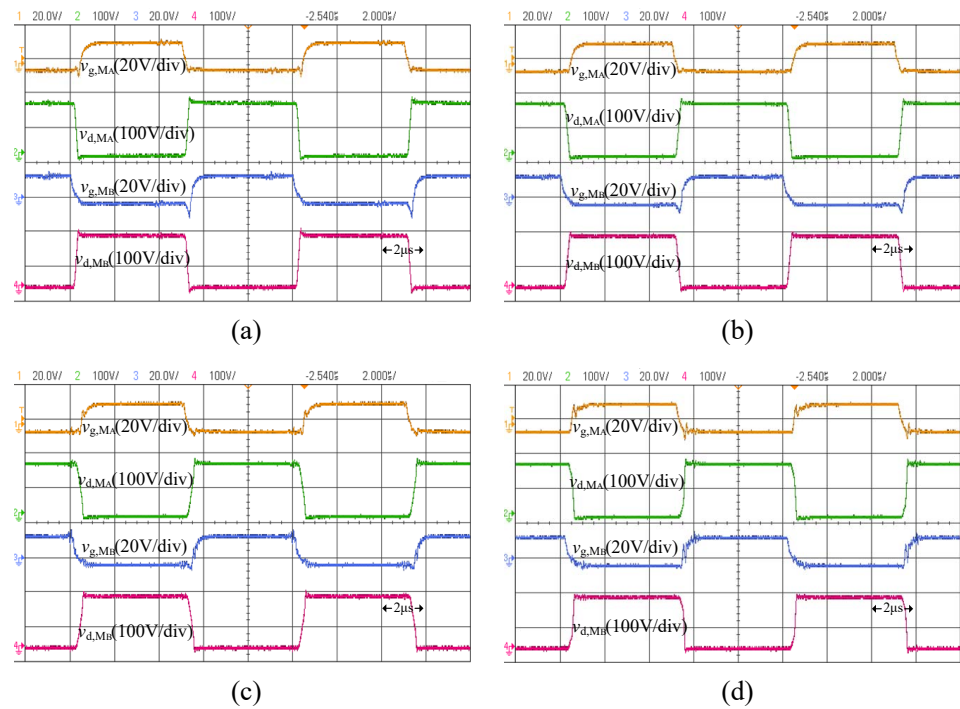
Figure 15. Experimental waveforms v_{g,M_A}, v_{d,M_A}, v_{g,M_B}, and v_{d,M_B} of M_A and M_B at different power levels: (**a**) 200 W, (**b**) 150 W, (**c**) 100 W, and (**d**) 50 W.
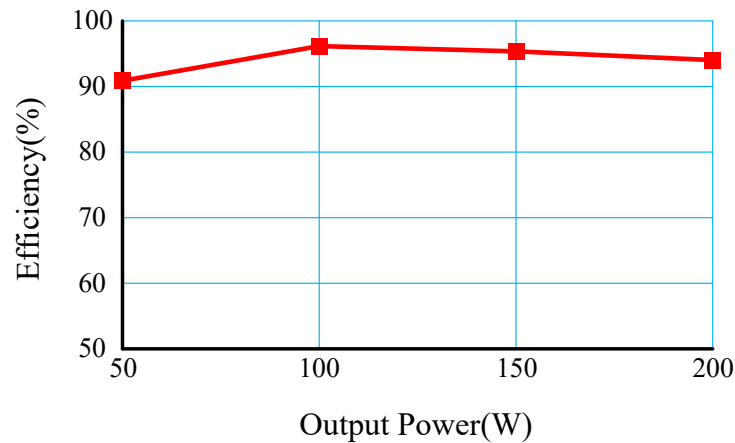

Figure 16. Measured efficiency under four load levels of DTRC.

The performance comparison between the proposed DTRC and some converters mentioned in Section 1 is given in Table 3. The degrees of freedom of [14] are more than those of other converters, which causes control complexity. Moreover, the soft-switching conditions are not better than others' because of the non-resonant structure. The topology of the three-phase two-tank *LLC* converter [18] and the dual-transformer *LLC* converter [24] both have two transformers, which is similar to the proposed DTRC. However, the cost is higher due to more switches and inductors.

Table 3. Comparison with other converters.

Topology	Hybrid Dual Active Bridge Converter [14]	Three-Phase Two-Tanks *LLC* Converter [18]	Dual-Transformer *LLC* Converter [24]	Proposed Dual-Transformer Resonant Converter
Voltage gain	0.25∼0.5	1∼2	1∼2	0.5∼1
Control variables	4	2	2	2
Number of MOSFETs	6	6	4	4
Number of diodes	0	4	4	4
Transformers	1	2	2	2
Modulation	MPS	PFM	MPS	SPS
Resonant components	0	4	2	2
Soft switching	ZVS	ZVS	ZVS and ZCS	ZVS and ZCS
Cost	Medium	High	High	Low

6. Conclusions

This paper proposes a new Dual-Transformer DC-DC Resonant Converter that features asymmetrical turns ratios of the HF transformers. By setting k as the ratio of two transformers, more freedom was provided to optimize the DTRC. Due to the features of the structure, the converter can operate with low voltage stress and minimal backflow power without any control strategy. Compared with the conventional soft-switching PWM resonant converter, the DTRC can widen the ZVS operation range and reduce the switching loss. Even at a very light load, the DTRC can still keep all active switches working in ZVS operation. Naturally, the backflow power on the output side is almost eliminated. Experimental measurements validated the theoretical analysis and demonstrated the features of the proposed DTRC.

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