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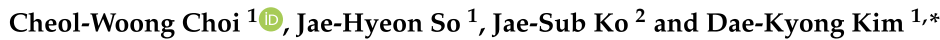
Influence Analysis of SiC MOSFET's Parasitic Capacitance on DAB Converter Output



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Abstract: This paper proposes the influence analysis of silicon carbide (SiC) MOSFET's parasitic output capacitance on a dual active bridge (DAB) converter. Power converters are required for DC grids and energy storage. Because SiC metal-oxide-semiconductor FETs (MOSFETs) have lower on-state resistance and faster reverse recovery time than Si MOSFETs, they can be controlled with lower losses and higher frequencies. MOSFETs have a parasitic capacitance. Because of the output parasitic capacitance, the switch voltage does not rise instantaneously during switching but has a delay. The output parasitic capacitance of the switch depends on its drain-to-source voltage, and this parasitic capacitance affects the output of the DAB converter by delaying the switch voltage. In this paper, in order to analyze the effect of the parasitic capacitance on the DAB converter output, the delay time was calculated through a formula, and this value was compared with a simulated value. In addition, the effect of the parasitic capacitance of the SiC MOSFET on the output of the DAB converter was presented by comparing the actual output voltage with the ideal output voltage and analyzing the effect of the output voltage according to the delay.

Keywords: DC–DC converter; DAB converter; SiC MOSFET; parasitic capacitance

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1. Introduction

Recently, interest in renewable energy, electric vehicles, and microgrids has increased owing to environmental issues and carbon-neutral policies. DC power is increasing owing to the increase in renewable energy sources, and the number of devices using DC is also increasing; therefore, the demand for DC power distribution and energy storage is increasing. Power converters, such as bidirectional DC–DC converters, are required for DC grids and energy storage [1–4].

Dual active bridge (DAB) converters have been proposed for high-power density high-power conversion systems [5–7], and many studies have been conducted because of the advantage of performing bidirectional power transfer with a simple structure [8]. A DAB converter consists of a full-bridge switch across a high-frequency transformer. It has full-bridge switches at both ends, transmits power using the leakage inductance of the transformer, and uses a series inductor to obtain the necessary inductance [5,9].

The DAB converter transfers power bidirectionally by using the phase shift between the primary and secondary side switches. Switches use metal–oxide–semiconductor field effect transistors (MOSFETs) or insulated-gate bipolar transistors [10,11]. A high switching frequency is required for high-efficiency, high-density power conversion. Silicon carbide (SiC) MOSFETs, which are SiC-based power semiconductors, have attracted attention as next-generation semiconductors, along with gallium-nitride-based power semiconductors [12,13]. They have a higher breakdown voltage than conventional Si-based switches but a low loss because of their low on-resistance ($R_{DS(ON)}$) and excellent heat dissipation characteristics, so it is possible to achieve high system efficiency and density using high frequencies [14].

The phase control of the DAB converter uses single-phase-shift (SPS) control for ease of control. The SPS method also helps achieve zero-voltage switching (ZVS) over a wide area when the input/output voltage ratio is 1 [15–18].

A MOSFET has a structure in which an oxide film and a PN junction are formed, and a diode is embedded. Parasitic capacitance exists between the gate, drain, and source owing to the capacitances of the oxide film and PN junction. This parasitic capacitance affects electromagnetic emission and the drain–source voltage rise and fall times [19]. Parasitic capacitors cause switch turn-on and turn-off transients and considerably increase switching energy losses [20]. Additionally, improved dynamic performance is required when controlling power flow in aerospace applications [21,22].

Therefore, in this paper, the effect of parasitic capacitance on the output is analyzed when the DAB converter is controlled by the commonly used SPS method. First, an equation for calculating the delay time of switch voltage change caused by parasitic capacitance and leakage reactance resonance is presented, and the results are compared with the result of the simulation. In addition, the effect of the parasitic capacitance on the DAB output is compared and analyzed through simulation and experiment. The results analyzed through this paper can be applied as considerations for precisely controlling DAB and reducing loss.

Section 2 describes the DAB converter operating characteristics. Section 3 discusses the parasitic capacitance of switches. Section 4 reports the switch parasitic capacitance analysis simulation results and experimental results. Section 5 presents the conclusion.

2. Operation Characteristics of DAB Converter

Figure 1 shows a DAB converter circuit. The DAB converter is an isolated bidirectional DC–DC converter that consists of a full-bridge switch and an additional series inductor across a high-frequency transformer. All switches of the DAB converter use a 50% duty ratio and transfer bidirectional power using the phase shift (ϕ) between the primary and secondary side voltages [23]. If the phase of the primary side is faster than that of the secondary side, power is transferred from the primary to the secondary side. If the phase of the secondary side is faster, power is transferred from the secondary to the primary side. The voltage difference caused by the phase shift is applied to the inductor, which stores energy and delivers power based on the phase shift.

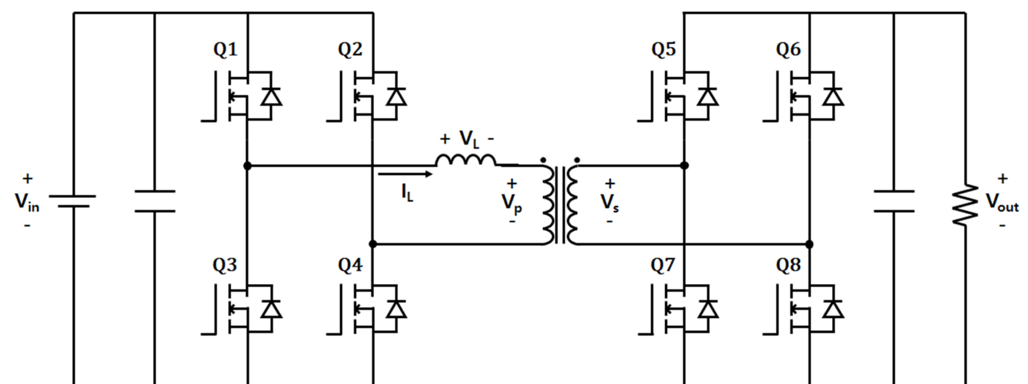


Figure 1. DAB converter circuit.

Figure 2 shows the operating waveform according to the SPS switch control of the DAB converter [5]. The SPS control method is widely used as the simplest method for transferring power with only a phase shift between the primary- and secondary-side switches.

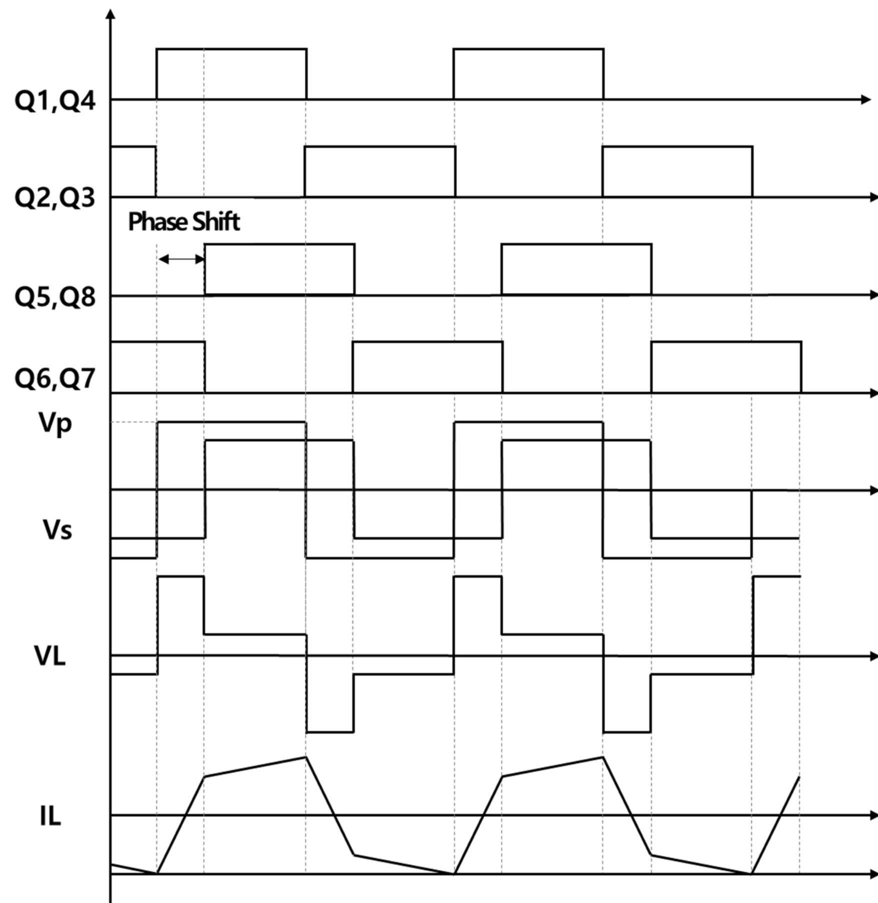


Figure 2. SPS control DAB converter operation waveform.

3. Parasitic Capacitance of Switches

Figure 3 shows the parasitic components of the MOSFET. In MOSFETs, the gate, drain, and source are insulated by an oxide film, and there is a freewheeling diode between the drain and source. When the switch is off, the energy stored in the inductor flows through the freewheeling diode. The parasitic components are divided into the input parasitic capacitance ($C_{iss} = C_{gs} + C_{gd}$), output parasitic capacitance ($C_{oss} = C_{ds} + C_{gd}$), and return parasitic capacitance ($C_{rss} = C_{gd}$). Because of the parasitic capacitance, the voltage across the switch does not instantaneously rise or fall during switching but changes with a delay owing to the effect of the parasitic capacitance.

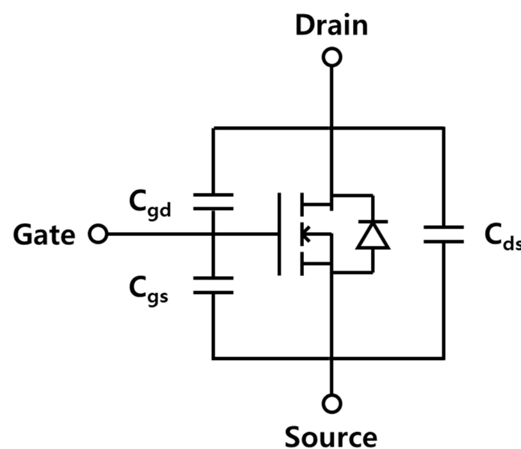


Figure 3. Parasitic components of MOSFET.

Figure 4 shows the equivalent circuit according to the switching operation of the DAB converter when the parasitic capacitance in the SiC MOSFET is considered. The full-bridge switch of the DAB converter operates in a complementary manner. If the switches of the legs are turned on at the same time, the switches can burn out and have dead time. During the dead time, all switches are turned off, and the parasitic capacitance of the switch is charged and discharged because of the energy stored in the inductor in the previous state. The parasitic capacitors of switches Q2 and Q3 are charged such that the voltage across the switch becomes equal to the input voltage. The parasitic capacitors of switches Q1 and Q4 are discharged, the diode is turned on, and the voltage across the switch is kept close to 0 V. With this operation, the DAB converter achieves ZVS.

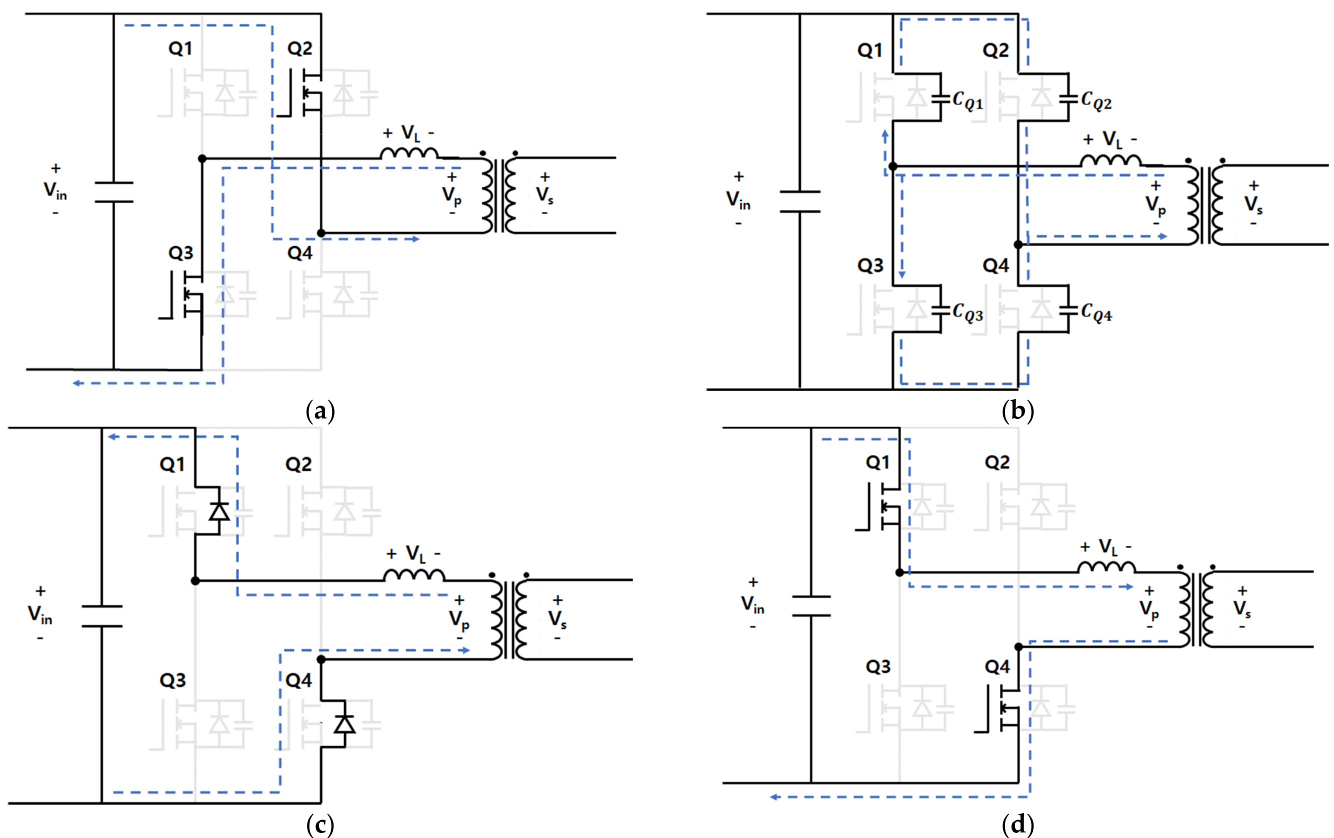


Figure 4. Equivalent circuit according to switching operation: (**a**) Q2,Q3 switches ON, Q1,Q4 switches OFF; (**b**) operation of parasitic capacitors during dead time; (**c**) operation of switches diode dead time; (**d**) Q1,Q4 switches ON, Q2,Q3 switches OFF.

In the equivalent circuit in Figure 4b, during dead time, the output capacitance (C_Q) of the SiC MOSFET is in series resonance with the leakage inductance (L_L), and the resonance frequency (f_r) is as follows.

$$f_r = \frac{1}{2\pi\sqrt{L_L C_Q}} \quad (1)$$

The current flowing by the leakage inductance charges and discharges the parasitic capacitance of the switching element during the dead time. When all the parasitic capacitances of the switching elements are the same and the loss is ignored, the relationship between the current (I_L) flowing through the leakage inductance and the current (I_C) flowing through the parasitic capacitance is as follows.

$$I_L = \frac{1}{2} I_C \quad (2)$$

The energy stored in the leakage inductance must be equal to or greater than the energy required to charge and discharge the parasitic capacitance during the dead time for ZVS operation. Therefore, the relationship between the energy stored by the leakage inductance and the energy supplied to the parasitic capacitance can be expressed using Equation (3). Here, K is the number of switches, I_{Lp} is the peak value of the inductor current, and V_{Qp} represents the peak value of the voltage across the parasitic capacitance.

$$\frac{1}{2}I_L I_{Lp}^2 \geq K\frac{1}{2}C_Q V_{Qp}^2 \tag{3}$$

In the DAB converter, leakage inductance current changes as follows. If the ratio of the primary voltage and the secondary voltage considering the $K = V_p/nV_s$ is set to 1 for the efficiency and wide ZVS range of the DAB converter, Equation (5) becomes 0.

As a result, the change in leakage inductance current is expressed by Equation (4), and the maximum value of leakage inductance current can be expressed by Equation (6).

$$0 \sim \phi : \Delta I_L = \frac{V_L}{Z_L}\phi,\ V_L = V_P + nV_s \tag{4}$$

$$\phi \sim (\pi - \phi) : \Delta I_L = \frac{V_L}{Z_L}(\pi - \phi),\ V_L = V_p - V_s \tag{5}$$

$$I_{LP} = \frac{\Delta I_L}{2} = \frac{V_p + nV_s}{Z_L \times 2} \times \phi \tag{6}$$

In general, a DAB converter is configured as a full bridge using four switching elements on the primary side, so a K of 4 is used. Using the above conditions and Equation (3), the parasitic capacitance voltage V_{Qp} can be obtained as shown in Equation (7).

The parasitic capacitance voltage can be expressed as follows using the resonant frequency of Equation (1) and the peak voltage of Equation (7).

$$V_{Qp} \leq \sqrt{\frac{L_L \times I_{LP}^2}{K \times C_Q}} = \sqrt{\frac{L_L \times I_{LP}^2}{4 \times C_Q}} \tag{7}$$

Because the parasitic capacitance voltage is charged up to the input voltage or discharged from the input voltage to 0 during the dead time, when the condition of Equation (9) is applied to Equation (8), the time for the parasitic capacitance voltage to rise can be calculated as in Equation (10). The time in Equation (10) eventually becomes a delay time that impedes the voltage change because the voltage does not change instantaneously and rises for a certain time.

$$V_Q = V_{Qp}\sin(2\pi f_r \times t) \tag{8}$$

$$V_Q = V_{in} \tag{9}$$

$$t = \frac{\sin^{-1}\left(\frac{V_{in}}{V_{Qp}}\right)}{2\pi f_r} \tag{10}$$

Figure 5 shows the voltage characteristics of the DAB converter according to the delay time. The delay of the primary-side switch voltage decreased the magnitude of the inductor voltage, but the delay of the secondary-side switch voltage increased the magnitude of the inductor voltage. So, area A represents the effect of the primary-side parasitic capacitance on the leakage inductance voltage, and area B appears due to the impact of the secondary-side parasitic capacitance; when both areas are the same, the effect of the voltage delay due to the parasitic capacitance can be compensated.

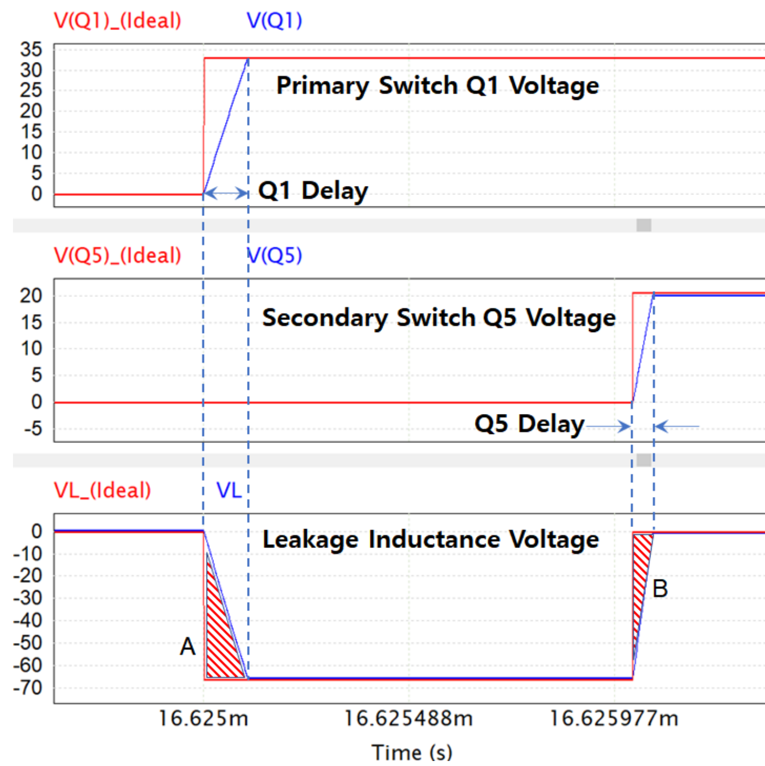


Figure 5. Voltage characteristics of the DAB converter according to the delay time.

To satisfy this condition, the delay time due to the secondary-side parasitic capacitance must be the same as the primary-side delay time, and considering the turns ratio, the following conditions can be created.

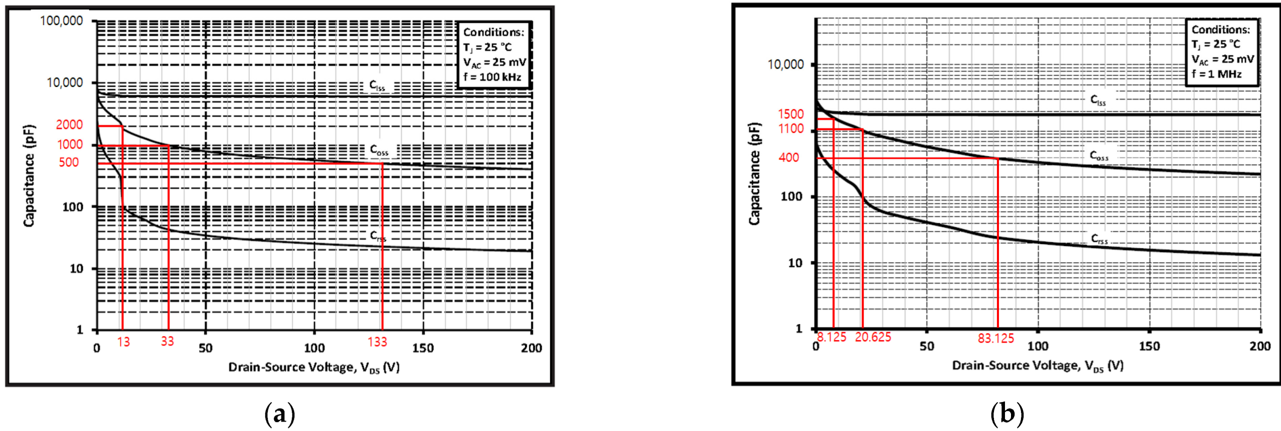
$$t_p = \frac{\sin^{-1}\left(\frac{V_{in}}{V_{Qpp}}\right)}{2\pi f_{rp}} = t_s = \frac{\sin^{-1}\left(\frac{V_{out}}{V_{Qps}}\right)}{2\pi f_s} = \frac{\sin^{-1}\left(\frac{V_{in}\times\frac{1}{n}}{V_{Qpp}\times\frac{1}{n}}\right)}{2\pi f_s} \tag{11}$$

For t_p and t_s to be equal, f_{rp} and f_{rs} must be equal. Using this condition, the optimal size of the secondary parasitic capacitance based on the primary parasitic capacitance or the optimal size of the primary parasitic capacitance based on the secondary parasitic capacitance can be calculated.

$$f_{rp} = \frac{1}{2\pi\sqrt{L_L \times C_{Qp}}} = f_{rs} = \frac{1}{2\pi\sqrt{\frac{1}{n^2}L_L \times C_{Qs}}} \tag{12}$$

$$C_{Qp} = \frac{1}{n^2} \times C_{Qs} \text{ or } C_{Qs} = n^2 C_{Qp} \tag{13}$$

Figure 6 shows the parasitic capacitance according to the drain–source voltage of the SiC MOSFET used in this study. Considering the operating voltage of the DAB converter, the primary-side switch was a Cree C3M0016120K, and the secondary-side switch was a Cree C3M0030090K. The parasitic capacitance of the MOSFET changes according to the drain–source voltage of the switch, and the parasitic capacitance decreases as the voltage increases.



(**a**) (**b**)

Figure 6. Parasitic capacitance by drain–source voltage of MOSFET: (**a**) C3M0016120K; (**b**) C3M0030090K.

Table 1 lists the output parasitic capacitances of the switch according to the input and output voltages of the DAB converter. To analyze the effect of parasitic output capacitance, 2 times and 0.5 times of parasitic capacitance were selected based on 1 nF. It was configured based on the voltages when the parasitic capacitances of the primary-side switch were 2, 1, and 0.5 nF [24,25].

Table 1. Output parasitic capacitances according to drain–source voltage.

C3M006120K		C3M0030090K	
V_{DS}	C_{oss}	V_{DS}	C_{oss}
13 V	2 nF	8.125 V	1.5 nF
33 V	1 nF	20.625 V	1.1 nF
133 V	0.5 nF	83.125 V	0.4 nF

4. Effect Analysis of Switch Parasitic Capacitance through Simulation and Experiment

Figure 7 shows the DAB converter simulation circuit, which was configured considering the dead time and parasitic capacitance of the switch.

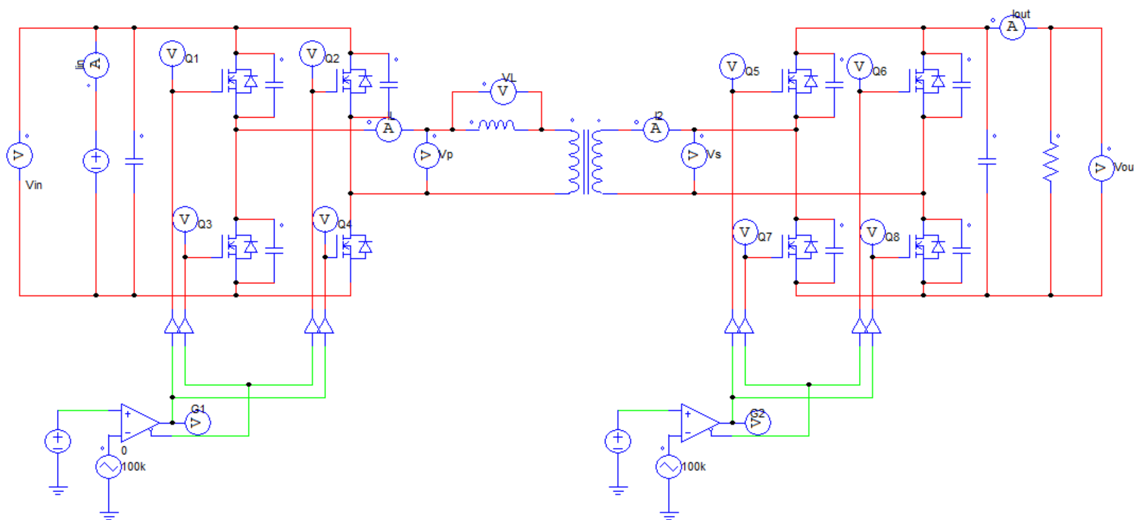


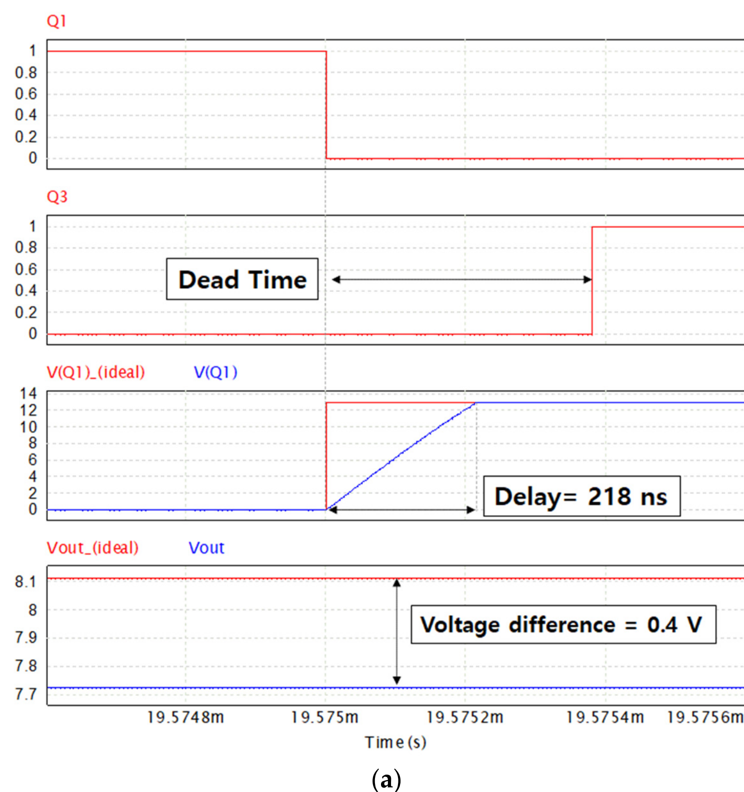
Figure 7. Simulation circuit structure.

Table 2 lists the simulation conditions and the output capacitances according to the switch voltages in Table 1.

Table 2. DAB converter specification.

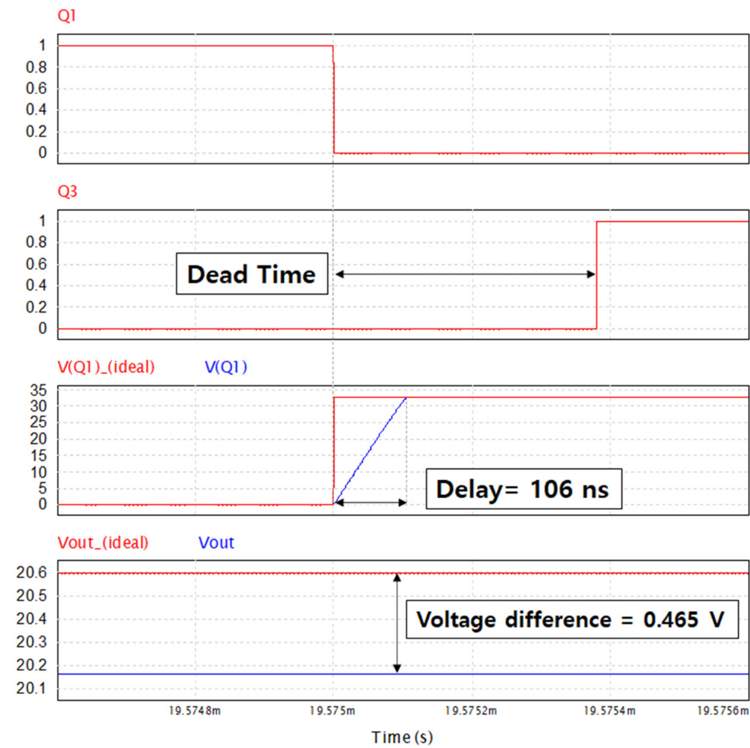
Parameter	Symbol	Value
Input voltage	V_{in}(V)	13~33
Output voltage	V_{out}(V)	8.125~83.125
Switching frequency	F_{SW}(kHz)	100
Number of turns	n(turn)	1.6
Leakage inductance	L_L(uH)	52
Dead time	D_T(ns)	380
Primary-side output capacitance	C_{Qp}(nF)	0.5~2
Secondary-side output capacitance	C_{Qs}(nF)	0.4~1.5
Load	R_{Load}(Ω)	25

Figure 8 shows the results based on the simulation conditions. It shows the waveform of the switch of the first leg on the primary side. During the dead time, the energy stored in the inductor in the previous state charges the parasitic capacitance of the switch, and the voltage across the switch increases to the input voltage because of the parasitic capacitance. The voltage does not change instantaneously according to the parasitic capacitance of the switch; however, the parasitic capacitance is charged and delayed. The delay in the rising voltage is affected by the parasitic capacitance, which varies with input voltage. The lower the input voltage, the larger the parasitic capacitance and voltage delay. When the input voltage is 13 V, it has the largest difference compared with the rated output voltage.



(**a**)

Figure 8. *Cont.*



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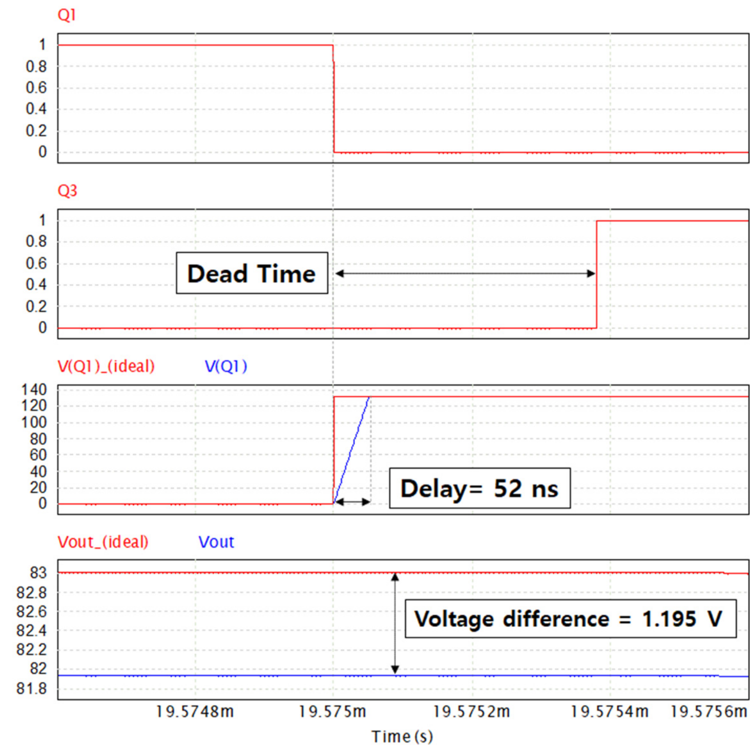


(**c**)

Figure 8. Simulation waveform and result: (**a**) input voltage 13 V; (**b**) input voltage 33 V; (**c**) input voltage 133 V.

Table 3 shows a comparison between the delay time calculated using Equation (10) and the delay time measured through the simulation. The delay time calculated using Equation (10) and the time measured through the simulation are almost the same.

Table 3. Delay time calculated using equation.

V_{in}[V]	Calculation Using Equation (10)	Simulation
13	$\phi = \frac{\pi}{2}(1-\sqrt{1-(\frac{8\times100k\times52\mu\times2.64}{1.6\times13\times8.125}})) = 0.2042\pi$ $f_r = \frac{1}{2\pi\sqrt{52\times10^{-6}\times2\times10^{-9}}} = 493{,}518.528\text{Hz}$ $I_{Lp} = \frac{(13+1.6\times8.125)\times0.2042\pi}{2\times2\pi\times100k\times52\mu} = 0.25525$ $V_{Qp} = \sqrt{\frac{52\times10^{-6}\times0.25525^2}{4\times2\times10^{-9}}} = 20.578$ $t = \frac{\sin^{-1}(\frac{13}{20.578})\times\frac{2\pi}{360}}{2\pi\times493{,}518} = 220.52\text{ns}$	218 ns
33	$t = \frac{\sin^{-1}\left(\frac{33}{73.875}\right)\times\frac{2\pi}{360}}{2\pi\times697{,}940} = 105.59\text{ns}$	106 ns
133	$t = \frac{\sin^{-1}\left(\frac{133}{421.068}\right)\times\frac{2\pi}{360}}{2\pi\times987{,}037} = 51.82\text{ns}$	52 ns

Table 4 shows the simulation results of the output voltage difference caused by the parasitic capacitance.

Table 4. Simulation results considering parasitic capacitance.

Input Voltage	Ideal Output Voltage	Simulation Output Voltage	Difference
13 V	8.125 V	7.72 V	4.98%
33 V	20.625 V	20.17 V	2.2%
133 V	83.125 V	81.9 V	1.47%

Figure 9 shows the experimental configuration used in this study, where three experiments were conducted with input voltages of 13, 33, and 133 V using a DC power supply. An oscilloscope was used to check the operating waveform and input/output voltage, and a power analyzer was used.

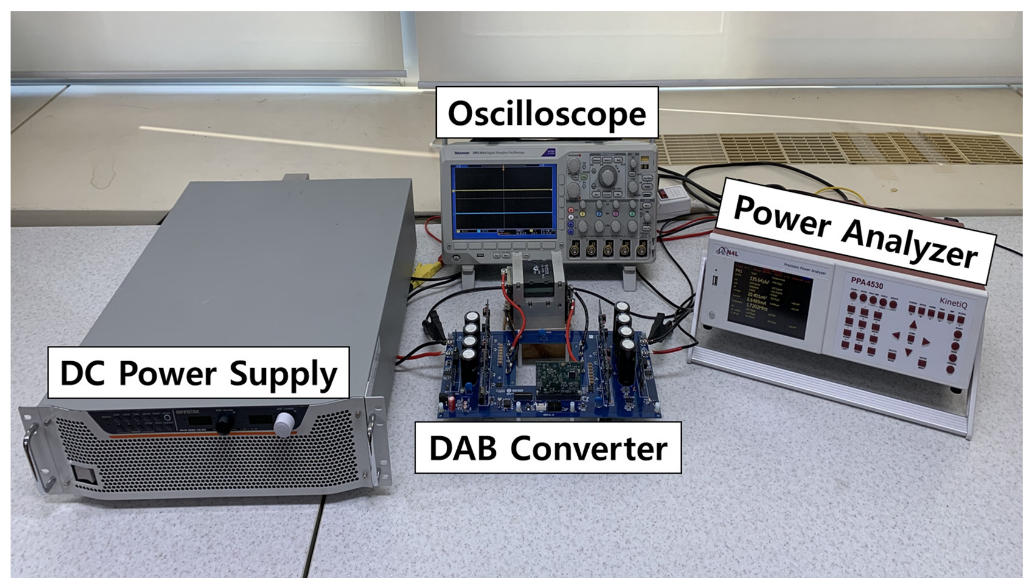


Figure 9. DAB converter experimental setup.

Figure 10 shows the waveforms of the experimental results and the voltage waveforms between the high- and low-side gate–source of the first leg of the primary side and the drain–source voltage of the first switch. During the dead time, the voltage of the switch rises to the input voltage, and a delay in the rising voltage appears because of the parasitic

capacitance. The lower the voltage input to the switch, the more delay that occurs because of the influence of the output capacitor. The higher the input voltage, the shorter the delay time.

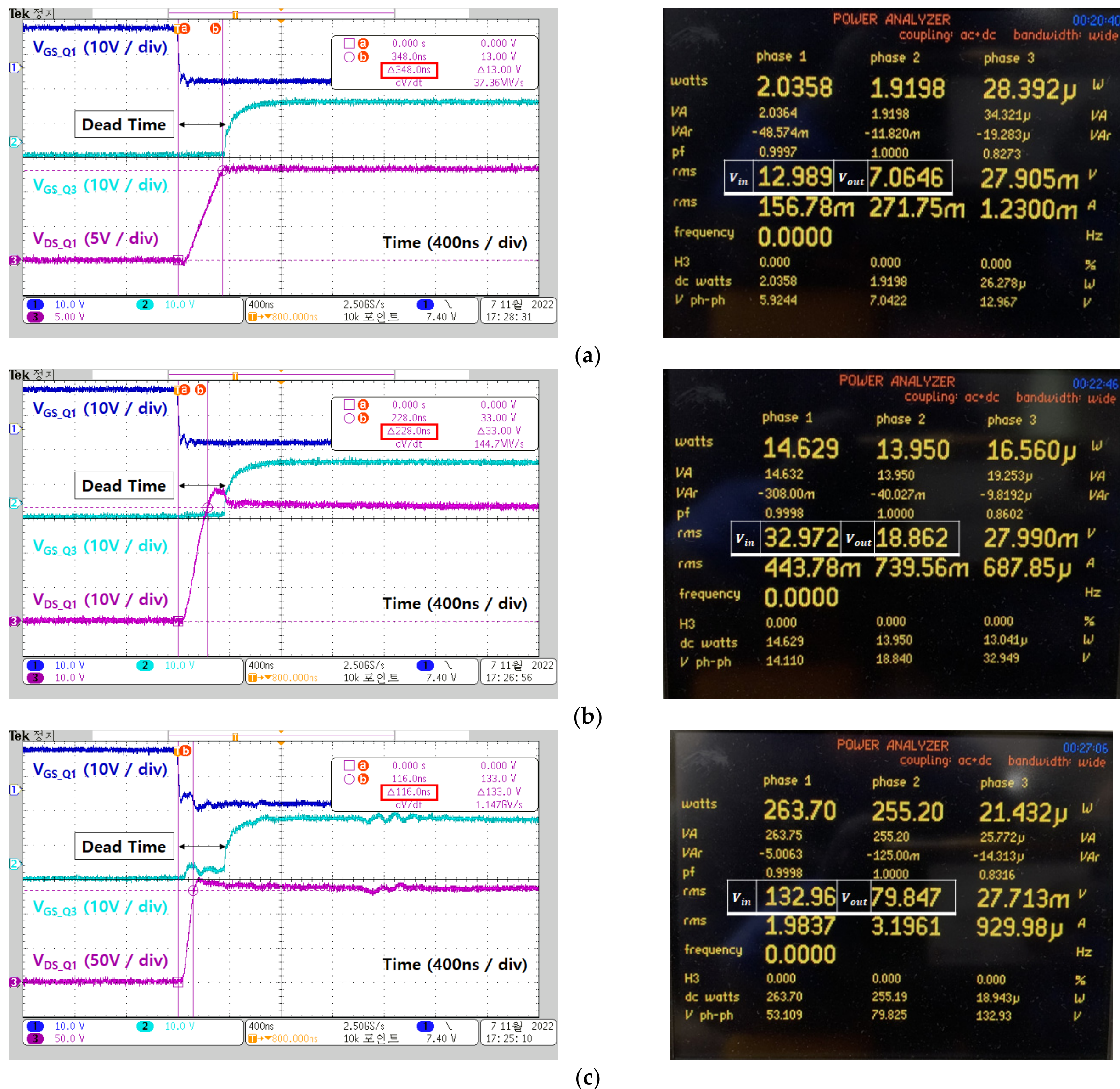


Figure 10. Experimental waveforms and input–output voltage: (**a**) input voltage 13 V; (**b**) input voltage 33 V; (**c**) input voltage 133 V.

Table 5 lists the input and output voltages based on the experimental conditions. The lower the input voltage, the greater the difference from the rated output voltage; the higher the input voltage, the smaller the difference.

Table 5. Experiment results.

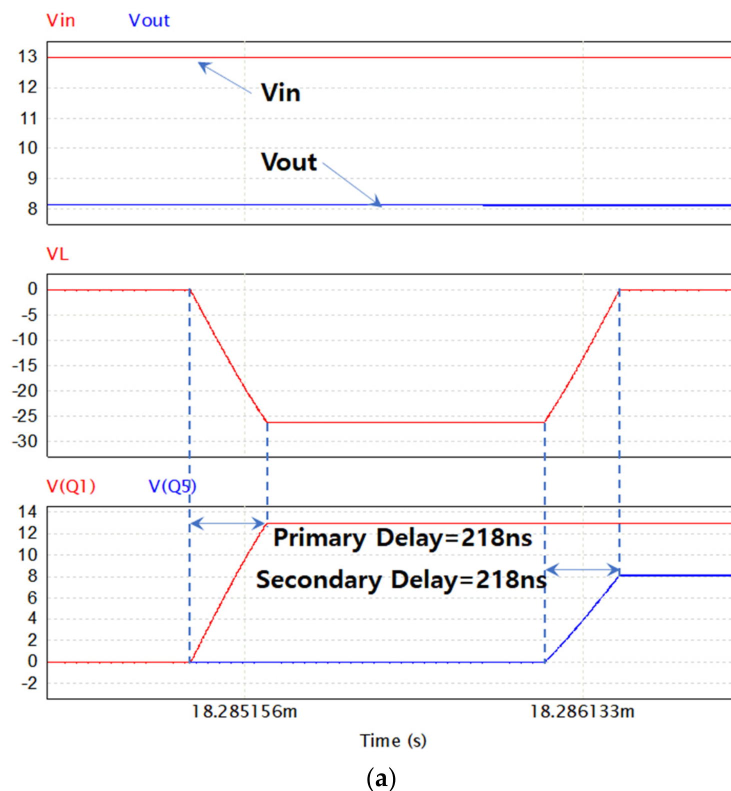
Input Voltage	Ideal Output Voltage	Experiment Output Voltage	Difference
13 V	8.125 V	7.06 V	13.1%
33 V	20.625 V	18.86 V	8.55%
133 V	83.125 V	79.84 V	3.95%

When DAB is controlled only with the parasitic capacitance of the primary and secondary SiC MOSFETs, the output voltage has an error with the rated value. In order to solve this problem, it is necessary to adjust the first or second value to the size of the optimal parasitic capacitance suggested in the paper. Table 6 shows the capacitance additionally required on the secondary side when considering the optimum parasitic capacitance condition.

Table 6. Optimum parasitic capacitance condition.

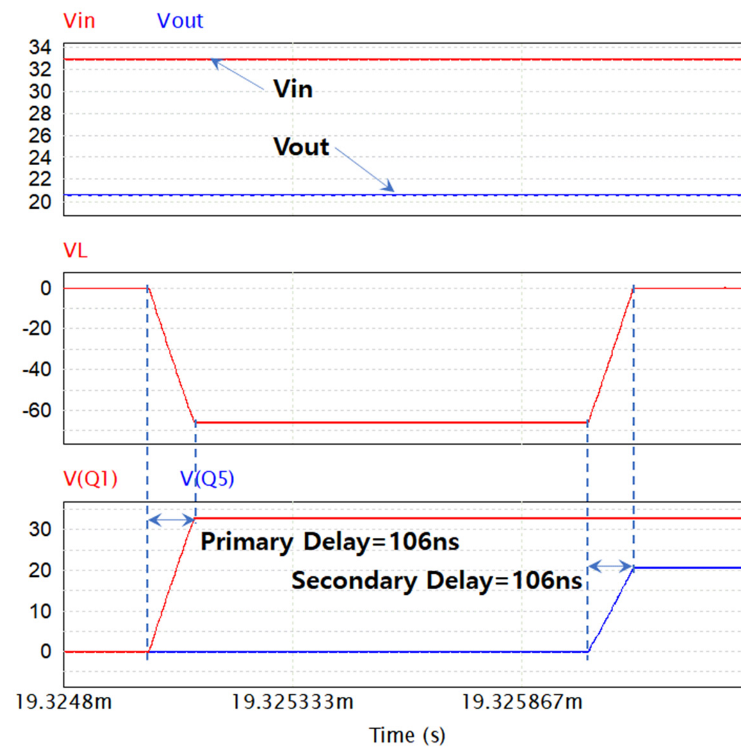
Input Voltage	C_{Qp}	C_{Qs}	Optimal C_{Qs}	Add C_{Qc}
13 V	2 nF	1.5 nF	5.12 nF	3.62 nF
33 V	1 nF	1.1 nF	2.56 nF	1.46 nF
133 V	0.5 nF	0.4 nF	1.28 nF	0.88 nF

Figure 11 shows the voltage response characteristics of the DAB converter when the secondary-side parasitic capacitance is set to the optimum capacitance. When the secondary side parasitic capacitance is set to an optimal value, the primary-side delay time and the secondary-side delay time appear identical. Table 7 shows the output voltage comparison when set to the optimum parasitic capacitance. When the secondary-side parasitic capacitance is optimally set, there is almost no difference between the secondary-side rated voltage and actual voltage.



(a)

Figure 11. *Cont.*



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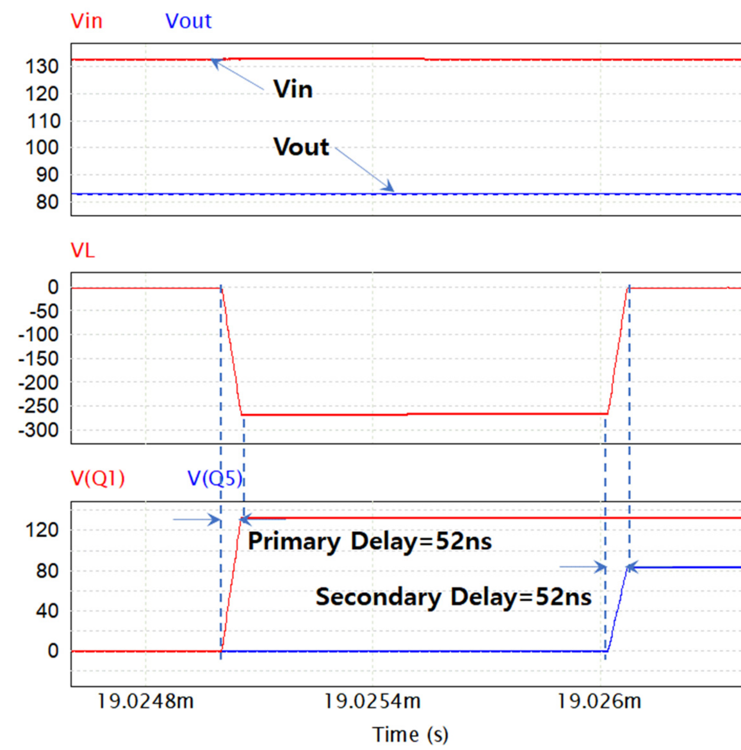

(**c**)

Figure 11. Voltage characteristics of the DAB converter with optimal parasitic capacitance: (**a**) input voltage 13 V; (**b**) input voltage 33 V; (**c**) input voltage 133 V.

Table 7. Simulation results by optimum parasitic capacitance.

Input Voltage	Ideal Output Voltage	Simulation Output Voltage	Difference
13 V	8.125 V	8.152 V	0.33%
33 V	20.625 V	20.641 V	0.07%
133 V	83.125 V	83.129 V	0.005%

5. Conclusions

The output characteristics of the DAB converter were analyzed according to the parasitic capacitance, which varies according to the voltage applied to the switch.

The MOSFET used in the DAB converter has a parasitic capacitance; therefore, the voltage of the switch does not rise instantaneously but rises with a delay. It was confirmed that the output voltage was lower than the rated output voltage owing to the delay in the switch voltage rise. A difference occurred according to the voltage applied to the switch: the larger the parasitic capacitance, the larger the voltage difference.

The experiment confirmed that a maximum voltage difference of 13.1% occurred over the rated output voltage for a 13 V input. It was proved that, in the DAB converter, a difference in output voltage resulting from the parasitic capacitance according to the input voltage occurs, and it must be considered.

Future plans include studying the compensation of the output characteristics owing to the delay in the voltage rise of the switch caused by the parasitic capacitance.

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References

1. Zhao, B.; Yu, Q.; Sun, W. Extended-Phase-Shift Control of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid. *IEEE Trans. Power Electron.* **2012**, *27*, 4667–4680. [CrossRef]
2. Akar, F.; Tavlasoglu, Y.; Ugur, E.; Vural, B.; Aksoy, I. A Bidirectional Nonisolated Multi-Input DC–DC Converter for Hybrid Energy Storage Systems in Electric Vehicles. *IEEE Trans. Veh. Technol.* **2016**, *65*, 7944–7955. [CrossRef]
3. Ríos, S.J.; Pagano, D.J.; Lucas, K.E. Bidirectional Power Sharing for DC Microgrid Enabled by Dual Active Bridge DC-DC Converter. *Energies* **2021**, *14*, 404. [CrossRef]
4. Sim, J.; Lee, J.Y.; Jung, J.H. Isolated three-port DC–DC converter employing ESS to obtain voltage balancing capability for bipolar LVDC distribution system. *J. Power Electron.* **2020**, *20*, 802–810. [CrossRef]
5. De Doncker, R.W.A.A.; Divan, D.M.; Kheraluwala, M.H. A three-phase soft-switched high-power-density DC/DC converter for high-power applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63–73. [CrossRef]
6. Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M.; Baumann, E.D. Performance characterization of a high-power dual active bridge DC-to-DC converter. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1294–1301. [CrossRef]

7. Guidi, G.; Pavlovsky, M.; Kawamura, A.; Imakubo, T.; Sasaki, Y. Efficiency optimization of high power density Dual Active Bridge DC-DC converter. In Proceedings of the The 2010 International Power Electronics Conference-ECCE ASIA-, Sapporo, Japan, 21–24 June 2010; pp. 981–986. [CrossRef]
8. Cho, Y.-W.; Cha, W.-J.; Kwon, J.-M.; Kwon, B.-H. High-Efficiency Bidirectional DAB Inverter Using a Novel Hybrid Modulation for Stand-Alone Power Generating System with Low Input Voltage. *IEEE Trans. Power Electron.* **2016**, *31*, 4138–4147. [CrossRef]
9. Cougo, B.; Kolar, J.W. Integration of Leakage Inductance in Tape Wound Core Transformers for Dual Active Bridge Converters. In Proceedings of the 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg, Germany, 6–8 March 2012; pp. 1–6.
10. Saeed, M.; Rogina, M.R.; Rodríguez, A.; Arias, M.; Briz, F. SiC-Based High Efficiency High Isolation Dual Active Bridge Converter for a Power Electronic Transformer. *Energies* **2020**, *13*, 1198. [CrossRef]
11. Tripathi, A.K.; Mainali, K.; Patel, D.C.; Kadavelugu, A.; Hazra, S.; Bhattacharya, S.; Hatua, K. Design Considerations of a 15-kV SiC IGBT-Based Medium-Voltage High-Frequency Isolated DC–DC Converter. *IEEE Trans. Ind. Appl.* **2015**, *51*, 3284–3294. [CrossRef]
12. Xue, F.; Yu, R.; Huang, A.Q. A 98.3% Efficient GaN Isolated Bidirectional DC–DC Converter for DC Microgrid Energy Storage System Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9094–9103. [CrossRef]
13. Dao, N.D.; Lee, D.C.; Phan, Q.D. High-Efficiency SiC-Based Isolated Three-Port DC/DC Converters for Hybrid Charging Stations. *IEEE Trans. Power Electron.* **2020**, *35*, 10455–10465. [CrossRef]
14. Krismer, F.; Kolar, J.W. Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications. *IEEE Trans. Ind. Electron.* **2012**, *59*, 2745–2760. [CrossRef]
15. Chen, X.; Xu, G.; Han, H.; Liu, D.; Sun, Y.; Su, M. Light-Load Efficiency Enhancement of High-Frequency Dual-Active-Bridge Converter Under SPS Control. *IEEE Trans. Ind. Electron.* **2021**, *68*, 12941–12946. [CrossRef]
16. Hou, N.; Song, W.; Wu, M. Minimum-Current-Stress Scheme of Dual Active Bridge DC–DC Converter with Unified Phase-Shift Control. *IEEE Trans. Power Electron.* **2016**, *31*, 8552–8561. [CrossRef]
17. Xu, G.; Sha, D.; Xu, Y.; Liao, X. Dual-transformer-based DAB converter with wide ZVS range for wide voltage conversion gain application. *IEEE Trans. Ind. Electron.* **2017**, *65*, 3306–3316. [CrossRef]
18. Choi, W.; Rho, K.-M.; Cho, B.-H. Fundamental Duty Modulation of Dual-Active-Bridge Converter for Wide-Range Operation. *IEEE Trans. Power Electron.* **2016**, *31*, 4048–4064. [CrossRef]
19. Rajeswari, P.; Manikandan, V. Analysis of effects of MOSFET parasitic capacitance on non-synchronous buck converter electromagnetic emission. *Ain Shams Eng. J.* **2022**, 102041. [CrossRef]
20. Huang, X.; Ji, S.; Palmer, J.; Zhang, L.; Tolbert, L.M.; Wang, F. Parasitic Capacitors' Impact on Switching Performance in a 10 kV SiC MOSFET Based Converter. In Proceedings of the 2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018; pp. 311–318. [CrossRef]
21. Naayagi, R.T.; Forsyth, A.J.; Shuttleworth, R. Bidirectional control of a dual active bridge DC–DC converter for aerospace applications. *IET Power Electron.* **2012**, *5*, 1104–1118. [CrossRef]
22. Naayagi, R.T.; Forsyth, A.J.; Shuttleworth, R. High-Power Bidirectional DC–DC Converter for Aerospace Applications. *IEEE Trans. Power Electron.* **2012**, *27*, 4366–4379. [CrossRef]
23. Qin, H.; Kimball, J.W. Generalized Average Modeling of Dual Active Bridge DC–DC Converter. *IEEE Trans. Power Electron.* **2012**, *27*, 2078–2084. [CrossRef]
24. Wolfspeed C3M0016120K Datasheet. Available online: https://assets.wolfspeed.com/uploads/2020/12/C3M0016120K.pdf (accessed on 2 December 2022).
25. Wolfspeed C3M0030090K Datasheet. Available online: https://assets.wolfspeed.com/uploads/2020/12/C3M0030090K.pdf (accessed on 2 December 2022).

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