

Article

A Single-Stage Bimodal Transformerless Inverter with Common-Ground and Buck-Boost Features

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Abstract: This paper proposes a single-phase, single-stage common-ground inverter with a non-electrolytic capacitor and buck-boost ability. The proposed single-stage inverter is employed by a boost stage DC-DC converter and bimodal circuit, which makes it satisfactory for PV systems with a wide input voltage range and lower switch voltage stress. The leakage current of the proposed single-stage inverter can effectively suppress because the parasitic capacitor between the PV panel and the ground is shortened. In addition, the proposed single-stage inverter does not include electrolytic capacitors, which reduces the equivalent series resistance of electrolytic capacitors and also the size of the inverter system. The topology, operating principle, and PWM control method of the proposed single-stage inverter are given. The design guidelines of components and comparative studies of the proposed single-stage inverter are provided. A 500 W laboratory prototype of the proposed single-stage inverter is built to verify the correctness of the simulation and theoretical analysis.

Keywords: transformerless inverter; single-stage; buck-boost ability; improved control; capacitor size



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1. Introduction

Nowadays, the issue of energy is becoming a major concern for the speedy development of human society. The over-exploitation of traditional energy sources causes many environmental problems, which significantly affect the development of society. Therefore, a stable and environmentally friendly energy needs to be researched and developed. Renewable energy sources have been widely used in the world; among them, solar energy has many advantages in terms of reserves, environmental protection, and ease of development [1–5]. As a fundamental component of solar energy production, photovoltaic (PV) inverter has attracted the interest of many scholars. According to the structure of the inverter, PV inverters can be divided into isolated and non-isolated types. Due to the transformer's high impedance characteristic, the common-mode (CM) leakage current in the isolating inverter is effectively blocked. However, transformers have disadvantages such as substantial volume, difficult installation, high price, and even high electromagnetic interference (EMI). Therefore, non-isolated inverters without transformers draw progressive attention [6] due to their simple structure, high efficiency, and low price. Single-stage non-isolated inverters are a popular and greatly improved power conversion solution for power conversion efficiency since there is no additional power processing stage and transformer loss. Nevertheless, it also causes problems such as CM leakage current and changing voltage capability [7–14].

The high leakage current value will cause the shutdown of the PV system, poor quality of grid current, and personal safety problems [15,16], so leakage current elimination is always an important issue of non-isolated PV inverters. Theoretically, the leakage current can be suppressed by changing the control method to decoupling the dc side and the ac side or creating generating constant common-mode voltage, such as the structures proposed in [17,18]. Also, the mid-point clamping technique clamps the ac output of the

inverter to the mid-point of the dc bus, which is also considered a method to suppress leakage current. However, this method requires more capacitors on the dc busbar side; the value of the capacitor needs to be considered to balance the voltage across the capacitors. Besides the above limitation, this method also leads to the problem of grid-connected current dc injection. Therefore, complex control algorithms are required [19–21]. The solutions mentioned above can only ensure that the leakage current is as small as possible compared to the allowable standard. Nevertheless, since PV systems are installed outdoors, weather factors such as temperature and humidity cause a change to the grounded parasitic capacitor of the PV array, which can easily cause excessive leakage current and system safety problems [18]. Another method to improve the leakage current suppression effectively, this method is realized by directly connecting the negative rail of the PV and the grid neutral, which can directly short the parasitic capacitor. Consequently, the leakage current can be eliminated effectively. The virtual dc bus [22], flying capacitor [23], and charge pump circuit [24] inverters have good leakage current suppression, but they can only perform in buck condition. To extend the input voltage range, it is necessary an additional dc-dc converter.

Besides, the half-bridge impedance source inverter introduced in [25] uses only two switches but requires two input sources, and there are too many inductors and diodes in this structure. The inverter proposed in [26] has buck-boost and suppress leakage currents features with only three switches, but it uses too many magnetic components. The three-switch inverter reported in [27] has the same number of switches as the inverter in [26] but high voltage stress on components. The single-phase, single-stage buck-boost inverter [28,29] is implemented with the common-ground feature. However, five power switches are required, and three of them are operated at high switching frequencies. A flying inverter is proposed in [30], using five switches, with two of them operating at high frequency. However, having three devices conduct at the same time reduces efficiency. The structure introduced in [31], using six switches and an inductor, can eliminate the leakage current by the common grounding. Nevertheless, two input sources are required. Furthermore, using ac switches easily makes open-circuit and short-circuit problems. The inverter introduced in [32] can limit leakage current by active virtual ground but not completely suppress it. In [33], the structure uses five switches, of which four are ac switches, four inductors, and four diodes. Moreover, the voltages stress across components is relatively high, so the loss of the inverter is high. In [34], a bimodal transformerless inverter (BTI) with a common ground feature is presented. The BTI has a simple structure and achieves high efficiency, but this structure only operates when the output voltage is less than the input voltage. In order to extend the range of the input voltage, a boosting stage needs to be added. However, the conventional two-stage BTI requires a large DC-link capacitor. This paper presents a proposed single-stage BTI, which reduces the DC-link capacitor size and the voltage stress on the components, thereby increasing the system's efficiency.

2. Principle Buck-Boost Bimodal Transformerless Inverter

2.1. Circuit Description

Figure 1 illustrates the circuit structure of the proposed single-stage buck-boost BTI (BB-BTI) with common-ground characteristics. A basic boost dc-dc converter is used to produce the single-polarity rectified sinusoidal voltage in the boost mode, and a BTI circuit is used to produce a sinusoidal voltage in the buck mode. The conventional boost dc-dc converter is built mainly by the power switches S_1 , the diode D_1 , and the inductor L_1 . The BTI includes the power switches S_2 , S_3 , and S_4 , the capacitor C_2 , and the inductor L_2 . L_f and C_f filter the voltage ripple of output voltage v_o .

The operation principles of two-stage and single-stage BB-BTI are different. In a conventional two-stage BB-BTI, the switch S_1 always operates at high frequency with the constant duty cycle so that the voltage on the DC-link capacitor is maintained at a set voltage value, which requires that the DC-link voltage is always greater than the output voltage. In addition, maintaining a constant DC-link voltage at high voltage requires a large

capacitance value, which increases the DC-link capacitor’s size. In a proposed single-stage BB-BTI, the switch S_1 only operates at high frequency when the input voltage is lower than the output voltage, the difference between the duty ratio of switch S_1 in the proposed single-stage BB-BTI is constant, and in conventional two-stage BB-BTI is variant.

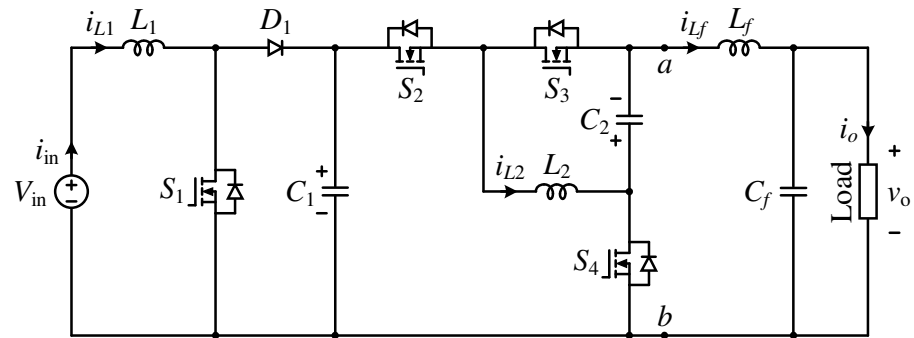


Figure 1. The proposed single-phase BB-BTI.

2.2. Operation Principles

Figure 2 illustrates the key waveforms of the PWM strategy and control signals when the proposed single-stage BB-BTI operates with an input voltage V_{in} lower than the utility sine wave v_o , where V_o is the magnitude of the voltage v_o , V_{in} depicts the input voltage, V_{C1} is the voltage across capacitor C_1 , and v_{ab} is the inverter output voltage. In Figure 2a, the voltage across capacitor C_1 is a straight line. In Figure 2b, the voltage of capacitor C_1 is equal to the input voltage V_{in} and only varies between θ_1 and θ_2 .

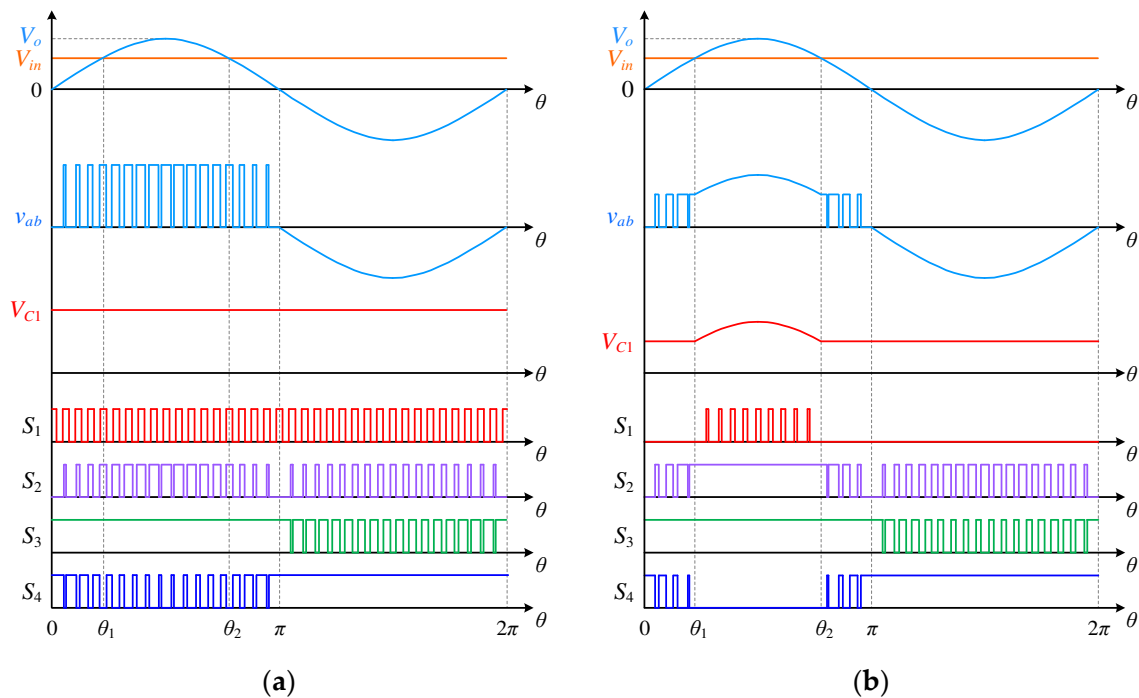


Figure 2. PWM control method for (a) conventional two-stage BB-BTI and (b) the proposed single-stage BB-BTI.

Besides, the states of S_1 and S_2 in Figure 2a change in the full cycle, while the state of S_1 in Figure 2b changes only from θ_1 to θ_2 , and S_2 is kept ON from θ_1 to θ_2 . The state of S_4 in Figure 2a change from 0 to π , while the state of S_4 in Figure 2b is kept OFF from θ_1 to θ_2 .

The operating modes of the proposed single-stage BB-BTI can be divided into three modes, which include boost, buck, and buck-boost modes. The operating states of the proposed single-stage BB-BTI are shown in Figure 3.

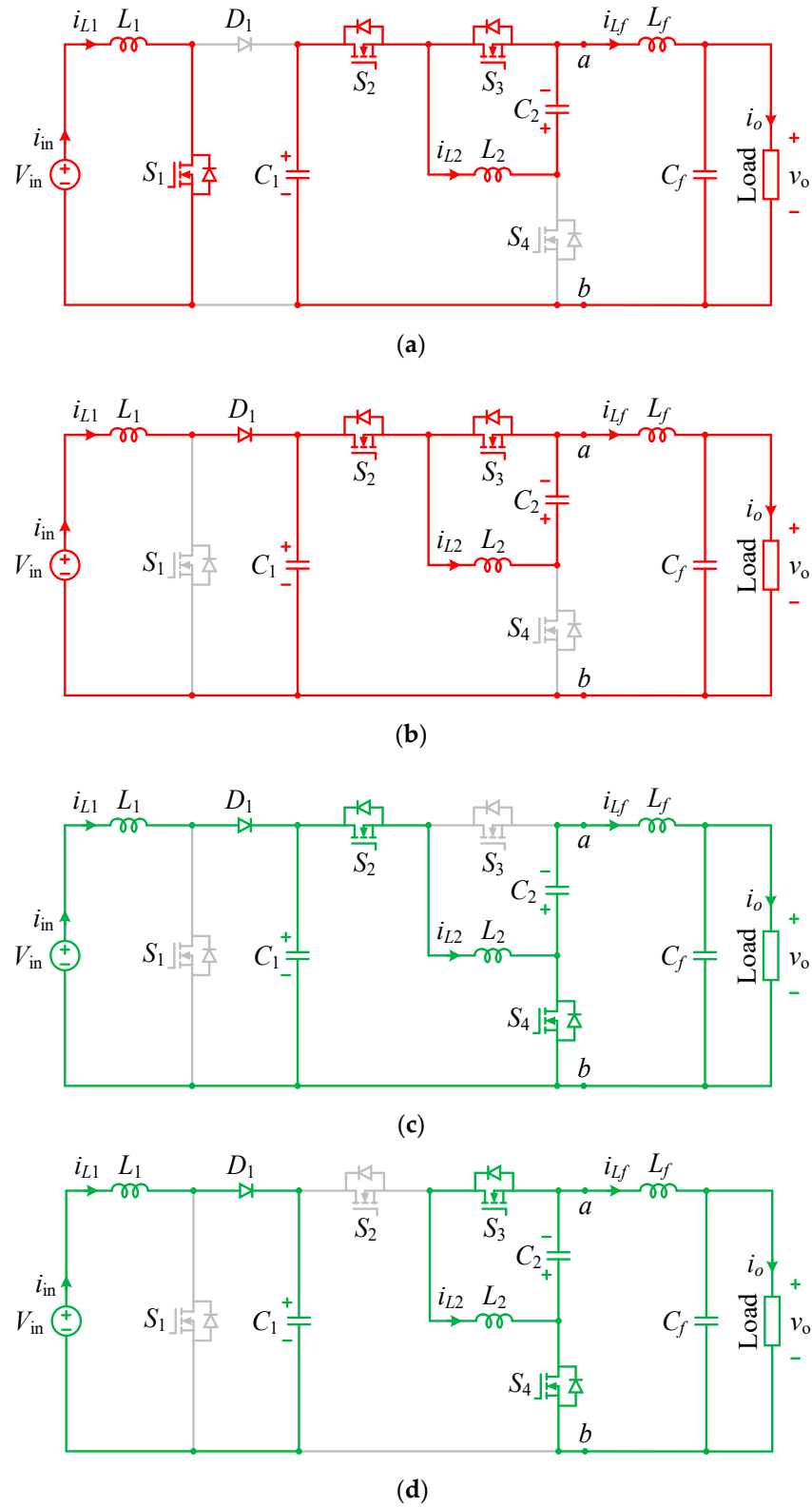


Figure 3. Circuit states of the proposed single-stage BB-BTI. (a) State 1 of boost mode, (b) State 2 of boost mode, and state 1 of buck mode, (c) State 1 of buck-boost mode, (d) State 2 of buck and buck-boost modes.

Boost mode (θ_1 – θ_2):

The states in boost mode are shown in Figure 3a,b. In this mode, the inductor is stored energy by the high-frequency operation of switch S_1 . The switches S_2 and S_3 are ON, and switch S_4 is OFF. As can be seen in Figure 2b, the voltages across capacitor C_1 have a curve shape, which has a peak value equal to the peak of the voltage v_o . The inductor L_2 current and capacitor C_2 voltage are zero.

State 1 (Figure 3a):

The switch S_1 is ON. The diode D_1 is reverse-biased. The inductor L_1 is stored energy from the voltage V_{in} , and the current i_{L1} increases. The switches S_2 and S_3 are ON, and switch S_4 is OFF. The capacitor C_1 transferred energy to the load through switches S_2 and S_3 , and L_f . The equations in this state can be written as:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} \\ L_2 \frac{di_{L2}}{dt} = -v_{C2} \\ L_f \frac{di_{Lf}}{dt} = v_{C1} - v_o \end{cases} \quad (1)$$

$$\begin{cases} C_1 \frac{dv_{C1}}{dt} = -i_{Lf} \\ C_2 \frac{dv_{C2}}{dt} = i_{L2} \\ C_f \frac{dv_{Cf}}{dt} = i_{Lf} - i_o \end{cases} \quad (2)$$

State 2 (Figure 3b):

The switches S_1 and S_4 are OFF. Inductor L_1 and source connected in series. The diode D_1 is forward-biased. The capacitor C_1 and output load are supplied from inductor L_1 and the input source. The voltage across the capacitor C_1 is higher than the source voltage because of the additional voltage from the inductor L_1 , the current i_{L1} decreases. The related equations are as follows:

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C1} \\ L_2 \frac{di_{L2}}{dt} = -v_{C2} \\ L_f \frac{di_{Lf}}{dt} = v_{C1} - v_o \end{cases} \quad (3)$$

$$\begin{cases} C_1 \frac{dv_{C1}}{dt} = i_{in} - i_{Lf} \\ C_2 \frac{dv_{C2}}{dt} = i_{L2} \\ C_f \frac{dv_{Cf}}{dt} = i_{Lf} - i_o \end{cases} \quad (4)$$

By considering the volt-second balance of inductors. v_{C1} , v_{C2} is calculated as follows:

$$\begin{cases} v_{C1} = \frac{V_{in}}{1-d_{B0}} \\ v_{C2} = 0 \end{cases} \quad (5)$$

The output voltage in this mode is given as follows:

$$v_o = \frac{V_{in}}{1-d_{B0}} \quad (6)$$

where d_{B0} denotes the duty cycle of switch S_1 .

Buck mode (0 – θ_1 and θ_2 – π):

The states in Buck mode are shown in Figure 3b,d. The diode D_1 is forward-biased, and the switch S_1 is completely OFF. The voltages on C_1 are equal to the input voltage. Both S_2 and S_4 operate at high-frequency. The current i_{L2} and voltage v_{C2} are zero.

State 1 (Figure 3b):

In this case, the states of the switches are the same as state 2 in boost mode. However, the voltage of C_1 is equal to voltage V_{in} , and the voltage of L_1 is close to zero because switch S_1 is OFF and the ripple voltage of C_1 is small. The energy from the source is transferred to the output load. Switch S_4 is OFF, and the voltages on capacitor C_2 and inductor L_2 are zero. The equations in this state are similar to Equations (3) and (4).

State 2 (Figure 3d):

In this state, switches S_1 and S_2 are OFF and switches S_3 and S_4 are ON. The voltage on capacitor C_1 is maintained at the input voltage through inductor L_1 and diode D_1 , and the inverter output voltage is zero ($v_{ab} = 0$). The equations in this state can be derived as

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C1} \\ L_2 \frac{di_{L2}}{dt} = -v_{C2} \\ L_f \frac{di_{Lf}}{dt} = -v_{C2} - v_o \end{cases} \quad (7)$$

$$\begin{cases} C_1 \frac{dv_{C1}}{dt} = i_{in} \\ C_2 \frac{dv_{C2}}{dt} = i_{L2} + i_{Lf} \\ C_f \frac{dv_{Cf}}{dt} = i_{Lf} - i_o \end{cases} \quad (8)$$

By applying the volt-second balance on inductors L_1, L_2 , one can obtain,

$$\begin{cases} v_{C1} = V_{in} \\ v_{C2} = 0 \end{cases} \quad (9)$$

The output voltage in this mode is given as follows:

$$v_o = d_{Bu} V_{in} \quad (10)$$

where d_{Bu} is the duty cycle of switch S_2 in the positive half cycle.

Buck-Boost mode ($\pi-2\pi$):

In Figure 3c,d, the states in buck-boost mode are shown. In this mode, the diode D_1 is forward-biased, switch S_1 is completely OFF, while switch S_4 is completely ON. The voltages on C_1 are equal to the input voltage. Both switches, S_2 and S_3 , operate at high-frequency. The capacitor C_2 is charged by the energy from inductor L_2 . The voltage of C_2 is equal to the voltage v_o .

State 1 (Figure 3c):

Switches S_1 and S_3 are OFF and switches S_2 and S_4 are ON. The diode D_1 is forward-biased, and the voltage of the capacitor C_1 is equal to the input voltage. The inductor L_2 is stored energy from the source and capacitor C_1 . The capacitor C_2 discharges energy to the output load. The current through inductor L_2 increases linearly. The differential equations are obtained as

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C1} \\ L_2 \frac{di_{L2}}{dt} = v_{C1} \\ L_f \frac{di_{Lf}}{dt} = -v_{C2} - v_o \end{cases} \quad (11)$$

$$\begin{cases} C_1 \frac{dv_{C1}}{dt} = i_{in} - i_{L2} \\ C_2 \frac{dv_{C2}}{dt} = i_{Lf} \\ C_f \frac{dv_{Cf}}{dt} = i_{Lf} - i_o \end{cases} \quad (12)$$

State 2 (Figure 3d):

This state is similar to state 2 in buck mode. However, in this state, the energy of the inductor L_2 is non-zero. The inductor L_2 supplies energy to the capacitor C_2 and the output load. The current i_{L2} decreases linearly. The differential equations are obtained as

$$\begin{cases} L_1 \frac{di_{L1}}{dt} = V_{in} - v_{C1} \\ L_2 \frac{di_{L2}}{dt} = -v_{C2} \\ L_f \frac{di_{Lf}}{dt} = -v_{C2} - v_o \end{cases} \quad (13)$$

$$\begin{cases} C_1 \frac{dv_{C1}}{dt} = i_{in} \\ C_2 \frac{dv_{C2}}{dt} = i_{L2} + i_{Lf} \\ C_f \frac{dv_{Cf}}{dt} = i_{Lf} - i_o \end{cases} \quad (14)$$

By applying the volt-second balance on inductors L_1 and L_2 . The equations of this mode are derived as follows:

$$\begin{cases} v_{C1} = V_{in} \\ v_{C2} = V_o \end{cases} \quad (15)$$

The output voltage is given as follows:

$$v_o = \frac{d_{BB} V_{in}}{d_{BB} - 1} \quad (16)$$

where d_{BB} is the duty cycle of switch S_2 in the negative half cycle.

The output voltage and the modulation index (M) of the proposed single-stage BTI are supposed to be

$$v_o = V_o \sin\theta \quad (17)$$

$$M = \frac{V_o}{V_{in}} \quad (18)$$

As visualized in Figure 4. The resulting duty cycles of the proposed single-stage BTI are calculated based on (18) as

$$d_{Bo} = \begin{cases} 0, & 0 < \theta \leq \theta_1 \text{ and } \theta_2 < \theta \leq 2\pi \\ 1 - \frac{1}{M \sin\theta}, & \theta_1 < \theta \leq \theta_2 \end{cases} \quad (19)$$

$$d_{Bu} = \begin{cases} M \sin\theta, & 0 < \theta \leq \theta_1 \text{ and } \theta_2 < \theta \leq \pi \\ 1, & \theta_1 < \theta \leq \theta_2 \\ 0, & \pi < \theta \leq 2\pi \end{cases} \quad (20)$$

$$d_{BB} = \begin{cases} 0, & 0 < \theta \leq \pi \\ \frac{M \sin\theta}{M \sin\theta - 1}, & \pi < \theta \leq 2\pi \end{cases} \quad (21)$$

The transition angles from boost mode to buck mode are given by

$$\begin{cases} \theta_1 = \sin^{-1}\left(\frac{1}{M}\right) \\ \theta_2 = \pi - \sin^{-1}\left(\frac{1}{M}\right) \end{cases}, M \geq 1 \quad (22)$$

From (19)–(21), the maximum values of the duty cycles can be calculated as follows:

$$D_{Bo.max} = \begin{cases} \frac{M-1}{M}, & M > 1 \\ 0, & M \leq 1 \end{cases} \quad (23)$$

$$D_{Bu.max} = \begin{cases} 1, & M \geq 1 \\ M, & M < 1 \end{cases} \quad (24)$$

$$D_{BB.max} = \frac{M}{M+1} \quad (25)$$

Figure 4 shows the d_{Bo} , d_{Bu} , and d_{BB} of BB-BTI for a peak output voltage of 156 V and an input voltage of V_{in} of 80 V. For $v_o > V_{in}$, d_{Bo} varies from 0 at $v_o = 80$ V to 0.487 at $v_o = 156$ V. For $v_o < V_{in}$, d_{Bu} varies from 0 at $v_o = 0$ V to 1 at $v_o = 80$ V, and for $v_o < 0$, d_{BB} varies from 0 at $v_o = -156$ V to 0.66 at $v_o = -156$ V.

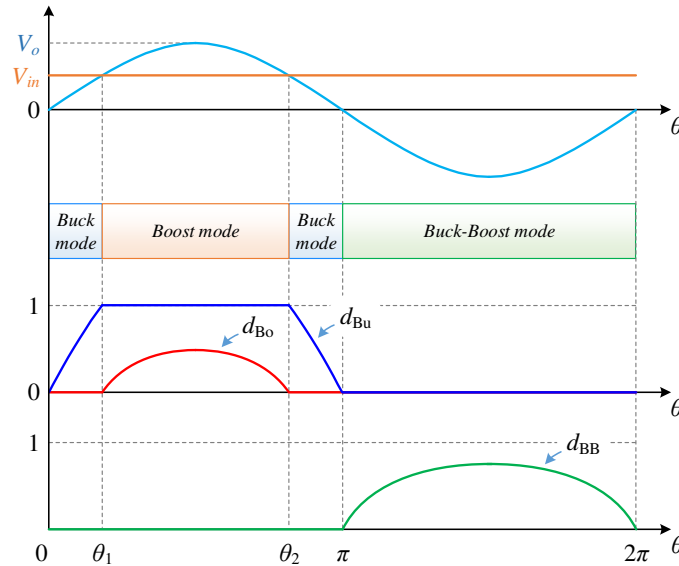


Figure 4. Variation of the duty cycles with the output voltage of the proposed single-stage BB-BTI.

3. Component Selection

3.1. Inductor

Regarding (2), (4), (8), (12), and (14), the inductor currents, i_{L1} and i_{L2} , can be expressed as:

$$i_{L1} = \begin{cases} i_o d_{Bu}, & 0 < \theta \leq \theta_1 \text{ and } \theta_2 < \theta \leq \pi \\ \frac{i_o}{1-d_{Bo}}, & \theta_1 < \theta \leq \theta_2 \\ \frac{i_o d_{BB}}{d_{BB}-1}, & \pi < \theta \leq 2\pi \end{cases} \quad (26)$$

$$i_{L2} = \begin{cases} i_o (d_{Bu} - 1), & 0 < \theta \leq \theta_1 \text{ and } \theta_2 < \theta \leq \pi \\ 0, & \theta_1 < \theta \leq \theta_2 \\ \frac{i_o}{d_{BB}-1}, & \pi < \theta \leq 2\pi \end{cases} \quad (27)$$

According to (20), (21), (26), and (27), the current of the inductors, L_1 and L_2 , are given as follows:

$$i_{L1} = I_o M \sin^2 \theta \quad (28)$$

$$i_{L2} = \begin{cases} I_o M \sin^2 \theta - I_o \sin \theta, & 0 < \theta \leq \theta_1 \text{ and } \theta_2 < \theta \leq 2\pi \\ 0, & \theta_1 < \theta \leq \theta_2 \end{cases} \quad (29)$$

The high-frequency inductor current ripple can be considered as follows:

$$\Delta i_{L1} = \frac{V_{in} d_{Bo}}{L_1 f_s} \quad (30)$$

$$\Delta i_{L2} = \frac{V_{in} d_{BB}}{L_2 f_s} \quad (31)$$

By replacing (19) and (21) with (30) and (31), we can also write

$$\Delta i_{L1} = \frac{(M - 1) V_{in}}{M L_1 f_s} \quad (32)$$

$$\Delta i_{L2} = \frac{MV_{in}}{(M + 1)L_2f_s} \tag{33}$$

The final value of L_1 , and L_2 are designed as:

$$L_1 = \frac{(M - 1)V_{in}}{Mf_s\Delta i_{L1}} \tag{34}$$

$$L_2 = \frac{MV_{in}}{(M + 1)f_s\Delta i_{L2}} \tag{35}$$

3.2. Capacitor

Using (5), (9), and (15), the voltage of capacitors C_1 and C_2 can be derived

$$v_{C1} = \begin{cases} V_{in}, & 0 < \theta \leq \theta_1 \text{ and } \theta_2 < \theta \leq 2\pi \\ v_o, & \theta_1 < \theta \leq \theta_2 \end{cases} \tag{36}$$

$$v_{C2} = \begin{cases} 0, & 0 < \theta \leq \pi \\ v_o, & \pi < \theta \leq 2\pi \end{cases} \tag{37}$$

The ripple voltage of the capacitors C_1 and C_2 can be written as:

$$\Delta v_{C1} = \begin{cases} \frac{i_o d_{B0}}{C_1 f_s}, & v_o > 0 \\ \frac{i_o d_{BB}}{C_1 f_s}, & v_o < 0 \end{cases} \tag{38}$$

$$\Delta v_{C2} = \frac{i_o d_{BB}}{C_2 f_s} \tag{39}$$

Maximum values of Δv_{C1} and Δv_{C2} are achieved when $d_{BB} = D_{BB,max}$ ($\theta = 3\pi/2$). The capacitance of the capacitors can be expressed as:

$$\Delta v_{C1} = \frac{MI_o}{(M + 1)C_1 f_s} \tag{40}$$

$$\Delta v_{C2} = \frac{MI_o}{(M + 1)C_2 f_s} \tag{41}$$

The value of the capacitors C_1 and C_2 can be expressed as

$$C_1 = \frac{MI_o}{(M + 1)\Delta v_{C1} f_s} \tag{42}$$

$$C_2 = \frac{MI_o}{(M + 1)\Delta v_{C2} f_s} \tag{43}$$

3.3. Switches and Diode

The drain-source voltages of switches are given as follows:

$$\begin{cases} V_{S1} = V_{S4} = V_{D1} = V_o \\ V_{S2} = V_{S3} = V_{in} + V_o \end{cases} \tag{44}$$

The currents of switches are given as

$$\begin{cases} I_{S1} = I_{D1} = MI_o \\ I_{S2} = I_{S3} = (M + 1)I_o \\ I_{S4} = (M + 2)I_o \end{cases} \tag{45}$$

4. Comparison

4.1. Comparison with the Two-Stage Bimodal Inverter

Table 1 demonstrates the comparison between the conventional two-stage BB-BTI and the proposed single-stage BB-BTI. The proposed single-stage BB-BTI requires three small capacitors, while the conventional two-stage BB-BTI needs two small and one bulky capacitor. For a better comparison, the voltage stress for switches and capacitors is calculated. The specific results for $M = 1.95$ for conventional two-stage BB-BTI and proposed single-stage BB-BTI are shown in Table 2. From Table 2, the maximum voltage stress on switches of conventional two-stage BB-BTI equal $2.16V_o$, while this stress is limited to $1.51V_o$ for the proposed single-stage BB-BTI. In addition, the voltage stress across capacitors of the conventional two-stage BB-BTI reaches to $1.16V_o$, while this stress in the proposed single-stage BB-BTI is limited to V_o . Therefore, the proposed single-stage BB-BTI can be implemented with switches and capacitors of significantly lower voltage. Consequently, the costs are decreased in the proposed single-stage BB-BTI compared to the conventional two-stage BB-BTI.

Table 1. Comparison of conventional two-stage BB-BTI with the proposed single-stage BB BTI.

Voltage Stress	Conventional Two-Stage BB BTI	Proposed Single-Stage BB BTI
S_1, S_4	$\frac{1}{M(1-d_{Bo})} V_o$	V_o
S_2, S_3	$\frac{1+M(1-d_{Bo})}{M(1-d_{Bo})} V_o$	$\frac{M+1}{M} V_o$
C_1	$\frac{1}{M(1-d_{Bo})} V_o$	V_o
C_2	V_o	V_o

Table 2. Comparison of conventional two-stage BB-BTI with the proposed single-stage BB-BTI with the same modulation index.

Voltage Stress	Two-Stage BB BTI ($M = 1.95, d_{Bo} = 0.56$)	Proposed Single-Stage BB BTI ($M = 1.95, D_{Bo,max} = 0.487$)
S_1, S_4	$1.16V_o$	V_o
S_2, S_3	$2.16V_o$	$1.51V_o$
C_1	$1.16V_o$	V_o
C_2	V_o	V_o

4.2. Comparison with Other Buck-Boost Common-Ground Inverters

To show the potential of the proposed single-stage BB-BTI, a comparison with other inverters has been summarized in Table 3. Comparison criteria such as the number of diodes, switches, capacitors, inductors, the total number of devices, voltage stress across diodes and switches, total standing voltage (TSV) [35] and the presented efficiency. The common-ground-type transformerless inverter in [23] has the least total number of devices, and the number of switches and diodes is equal to the proposed single-stage BB-BTI. However, this topology requires an input voltage greater than the output voltage. Besides, a large value capacitor is required to generate a voltage in the negative half of the output, which is also a disadvantage.

Table 3. Comparison between the proposed single-stage BB-BTI and other common-ground transformerless inverters.

Topology	[23]	[30]	[31]	[32]	[33]	[29]	Proposed BB-BTI
Diodes	1	2	0	0	4	3	1
Switches	4	5	6	8	5	5	4
Capacitors	2	1	3	1	2	2	3
Inductors	1	2	1	2	4	3	3
Total Devices	8	10	10	11	15	13	11
Diodes stress	$D_1: V_{in}$	$D_1: V_{in} + V_o$ $D_2: V_o$	-	-	$D_1-D_4: V_{in} + V_o$	$D_1: V_o$ $D_2: V_{in} + V_o$ $D_3: V_o - V_{in}$	$D_1: V_o$
Switches stress	$S_1-S_4: V_{in}$	$S_1: V_{in} + V_o$ $S_2-S_5: V_o$	$S_1, S_2: V_{in}$ $S_3-S_6: V_{in} + V_o$	$S_1-S_4: V_{in} + V_o$ $S_5-S_8: V_o$	$S_1-S_5: V_{in} + V_o$	$S_1, S_2: V_{in} + V_o$ $S_3-S_5: V_o$	$S_1, S_4: V_o$ $S_2, S_3: V_{in} + V_o$
TSV	$4V_{in}$	$1V_{in} + 5V_o$	$6V_{in} + 4V_o$	$4V_{in} + 8V_o$	$5V_{in} + 5V_o$	$2V_{in} + 5V_o$	$2V_{in} + 4V_o$
PresentedEfficiency	99.2% @1kW	-	95.9% @0.4kW	95.7% @0.8kW	96.74% @0.4kW	97.1% @0.45kW	96.5% @0.5kW

The inverters presented in [30,31] have the same total number of devices; the topology presented in [30] uses one more diode and one switch than the proposed single-stage BB-BTI. The single-stage bidirectional buck-boost inverters in [31] use only an inductor and do not use diodes, but two input sources or two large capacitors are required. In [32], the topology uses the most number of switches, there are four switches with voltage stress reaches ($V_{in} + V_o$), and two inductors are used. However, the leakage current is not completely eliminated. The topology presented in [33] uses the most diodes; the diodes and switches in this structure all have a voltage of ($V_{in} + V_o$), so the inverter loss is high. The topology presented in [29] includes two boost and one buck converter. However, this topology uses more than two diodes and one switch, which makes the total components of this topology much more than the proposed single-stage BB-BTI. In addition, the proposed single-stage BB-BTI has a lower TSV and efficiency compared to other studies. Through the comparison required in Table 3, the proposed single-stage BB-BTI has shown outstanding advantages such as the low number of components, small capacitors and buck-boost capability.

5. Simulation and Experimental Results

5.1. Simulation Results

Simulations were conducted using PSIM 9.1.1 (Troy, MI, USA) to verify the operation of the proposed single-stage BB-BTI. The parameters for the simulation are $L_1 = 0.5$ mH, $L_2 = 0.3$ mH, $L_f = 0.3$ mH, $C_1 = 5$ μ F, $C_2 = 5$ μ F, $C_f = 2$ μ F, and $R = 24$ Ω . The output frequency and switching frequency are set at 50 Hz and 30 kHz, respectively. The forward voltage of diode D_1 is 1 V. The drain-to-source on-resistance of switches S_1 and S_4 are 25.5 m Ω , and for S_2, S_3 are 45 m Ω .

Figures 5 and 6 show the simulation results when $V_{in} = 80$ V and $V_{in} = 220$ V, respectively. In Figures 5a and 6a, the driving waveform of switches S_1-S_4 is shown. Figures 5b and 6b show the voltages stress across switches S_1-S_4 . Figures 5b and 6b show the current of inductors L_1 and L_2 and the voltage across capacitors C_1 and C_2 . In Figures 5d and 6d, the waveforms in this figures are the voltage of diode D_1 , the inverter output voltage, v_{ab} , the output voltage, v_o , and the output current, i_o .

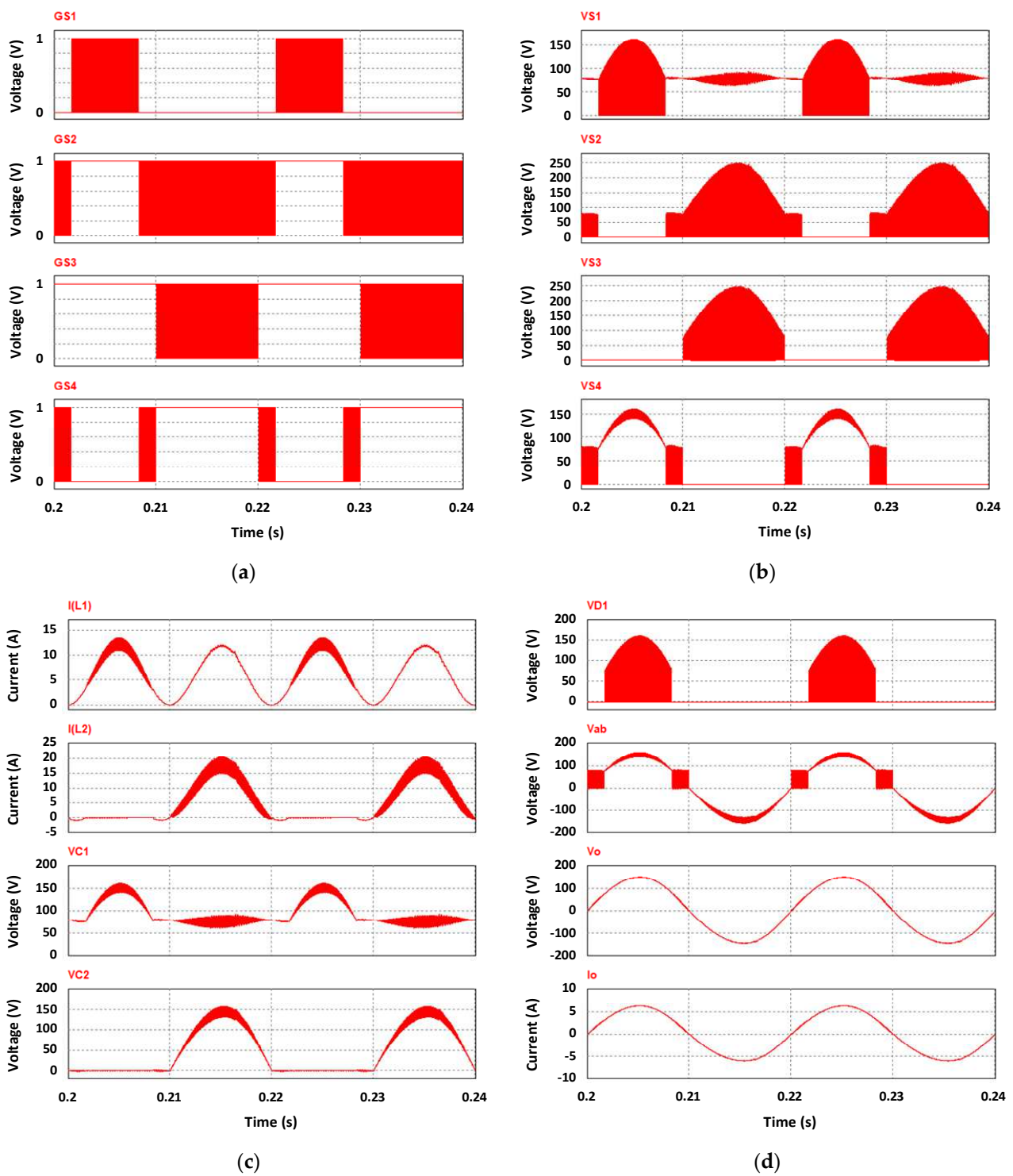


Figure 5. Simulation results for the proposed single-stage BB-BTI when $V_{in} = 80$ V. (a) Control signals of S_1 , S_2 , S_3 , and S_4 . (b) Voltages V_{S1} , V_{S2} , V_{S3} , and V_{S4} . (c) currents i_{L1} , i_{L2} , and voltages v_{C1} , v_{C2} . (d) Voltages V_{D1} , v_{ab} , and v_o , and current i_o .

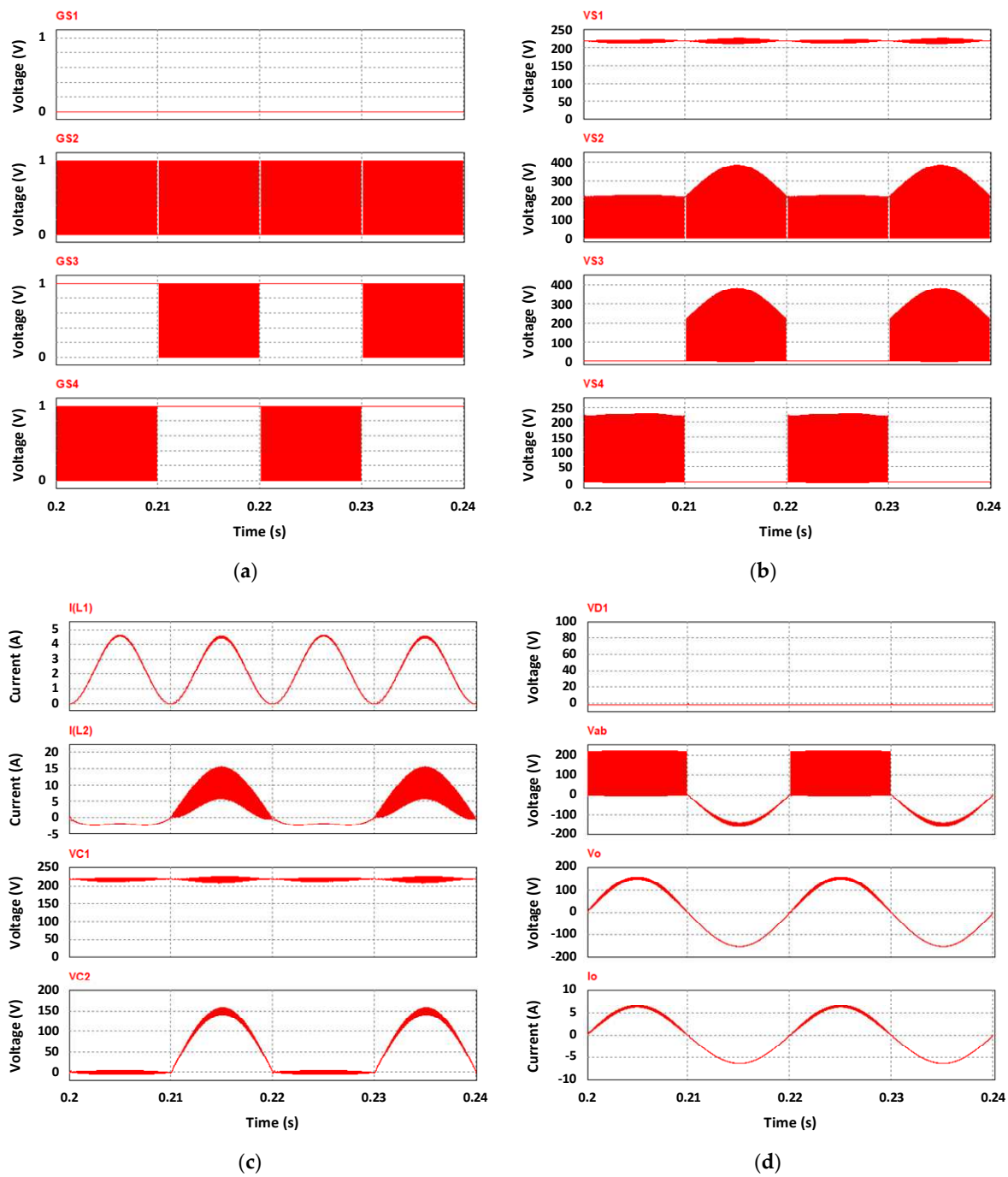
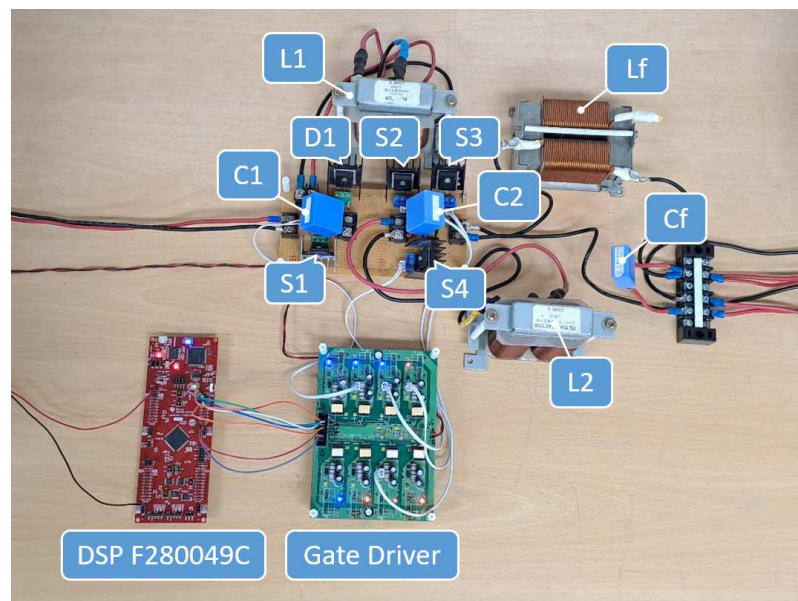


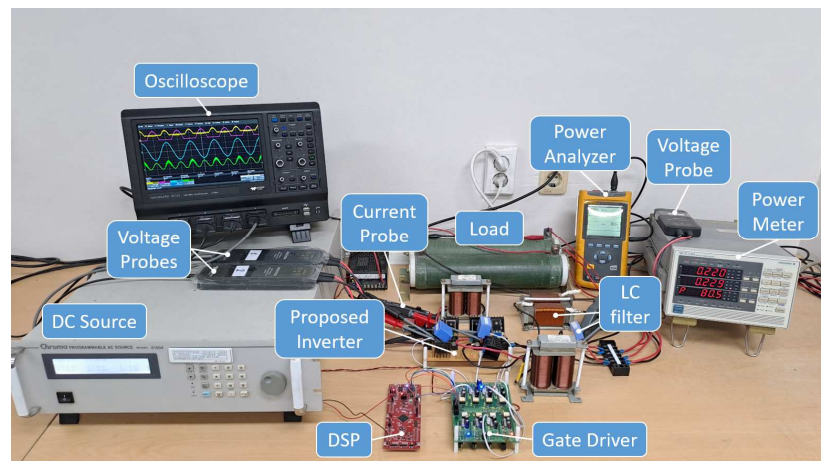
Figure 6. Simulation results for the proposed single-stage BB-BTI when $V_{in} = 220$ V. (a) Control signals of $S_1, S_2, S_3,$ and S_4 . (b) Voltages $V_{S1}, V_{S2}, V_{S3},$ and V_{S4} . (c) currents $i_{L1}, i_{L2},$ and voltages v_{C1}, v_{C2} . (d) Voltages $V_{D1}, v_{ab},$ and $v_o,$ and current i_o .

5.2. Experiment Results

To further validate the proposed single-stage BB-BTI analysis and its control, a 500 W concept-proof laboratory prototype is illustrated in Figure 7 with the components detailed in Table 4. The control platform is DSP F280049C. Chroma 61604 provides dc power. The input and output powers are measured by the WT230 Digital Power Meter. The output current harmonics are measured by Fluke 43 B. The load resistance of 25 Ω (where two resistors of 50 Ω in parallel) was used as the output load.



(a)



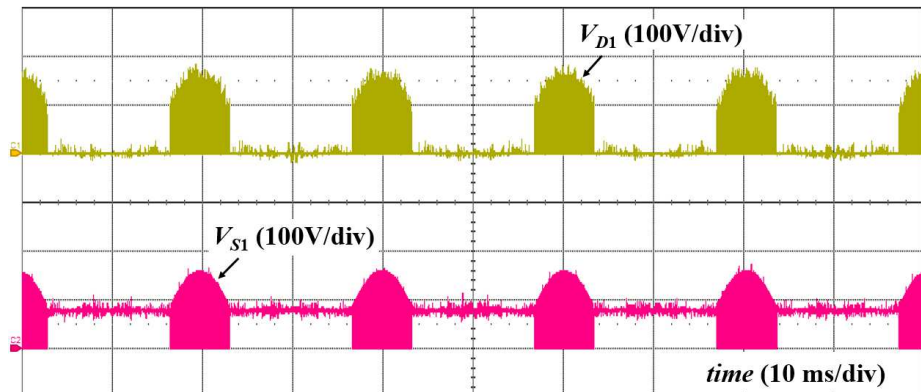
(b)

Figure 7. Photo of the laboratory prototype. (a) Prototype. (b) Measurement setup.

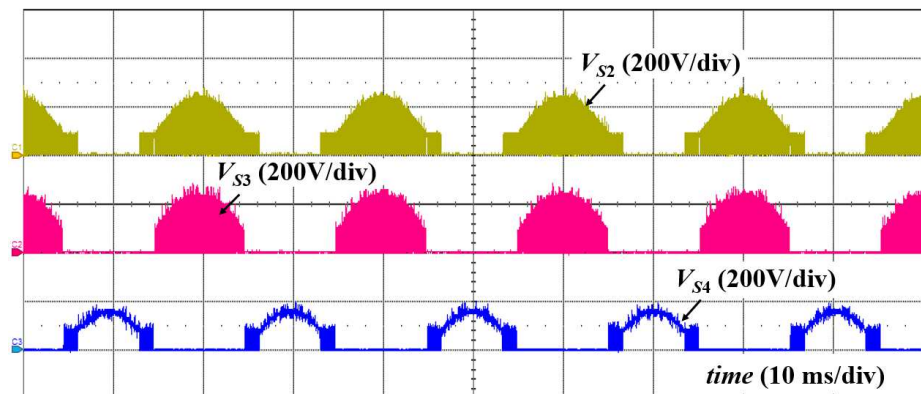
Table 4. Parameters for the experiment.

Parameter	Symbol	Value
Input voltage	V_{in}	80–220 V
Output voltage	v_o	110 Vrms
Output frequency	f_o	50 Hz
Switching frequency	f_s	30 kHz
Output power	P_o	500 W
Diode	D_1	STTH6003 (300 V, 60 A, $V_F = 1$ V)
Switches	S_1, S_4	IRFP4868PbF (300V, 70 A, $R_{dson} = 25.5$ m Ω)
	S_2, S_3	IPW60R045CPA (600 V, 60 A, $R_{dson} = 45$ m Ω)
Inductors	L_1	0.5 mH
	L_2, L_f	0.3 mH
Capacitors	C_1, C_2	5 μ F
	C_f	2 μ F

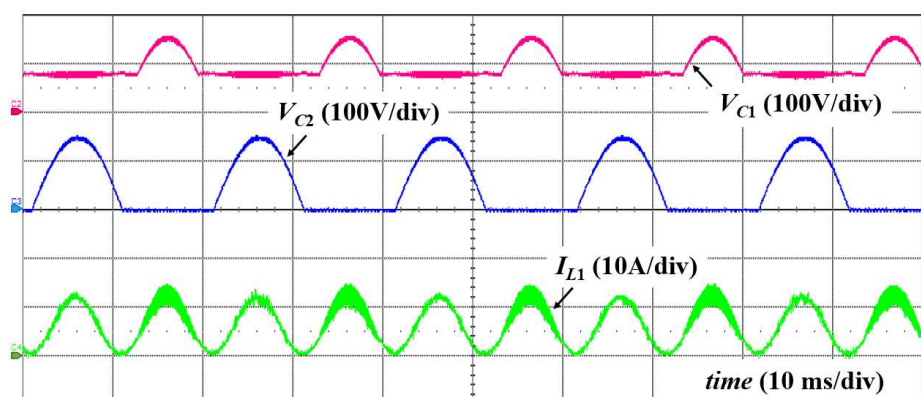
As shown in Figure 8, the experimental results with $V_{in} = 80$ V and the modulation index $M = 1.95$. Figure 8a indicates the voltage of the diode D_1 and the voltage of the switch S_1 . Figure 8b shows the voltage of switches S_2 , S_3 , and S_4 . The peak voltage of D_1 , S_4 , and S_1 are about 156 V. The peak voltages of S_2 and S_3 are about 235 V. Figure 8c illustrates the voltage of capacitors C_1 and C_2 and the current through the inductor L_1 . The voltage stress of capacitors is about 155 V. The current through the inductor L_1 varies from 0 to 14 A, and the average current of the inductor L_1 is 6.1 A. Figure 8d shows the output voltages v_{ab} , v_o , and current through the inductor L_2 . The THD values of the output voltage v_o are 1.82%. The average current through the inductor L_2 is 5.02 A, and the peak current is about 22 A.



(a)

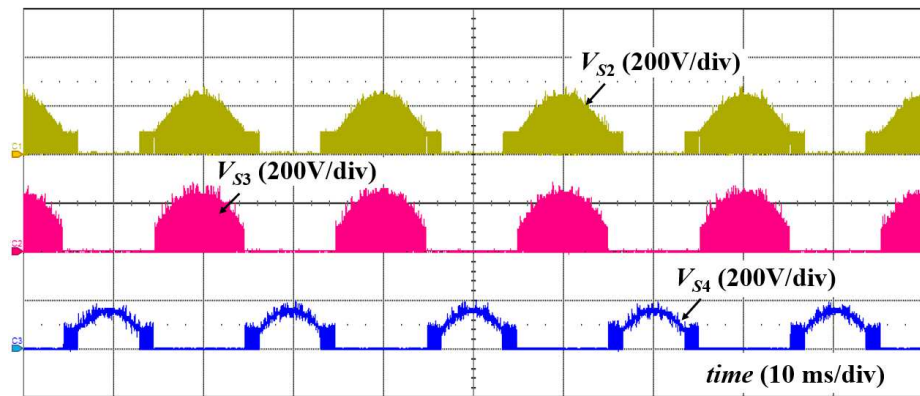


(b)



(c)

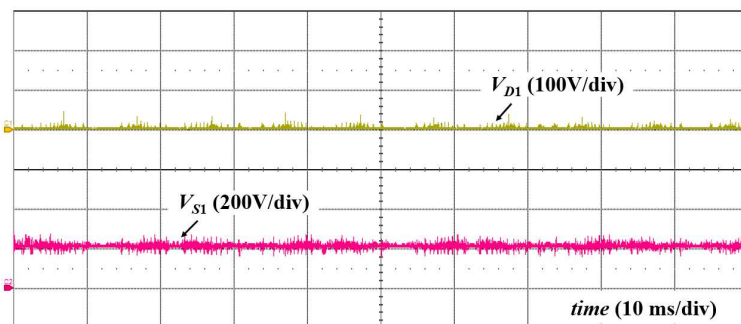
Figure 8. Cont.



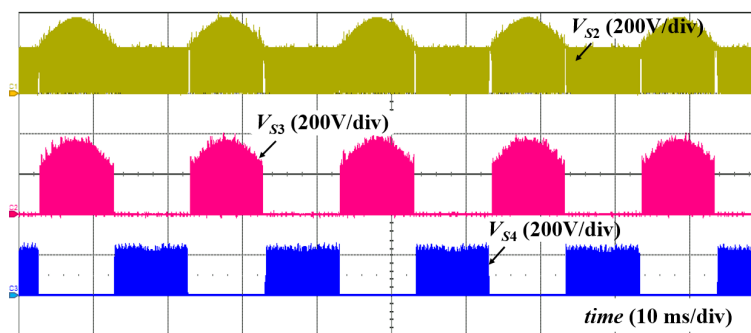
(d)

Figure 8. Experimental results with $V_{in} = 80$ V. (a) Diode D_1 and switch S_1 voltage. (b) Switches S_2, S_3, S_4 voltage. (c) Capacitors C_1, C_2 voltage, and inductor L_1 current. (d) inverter output voltage v_{ab} , load voltage v_o , and inductor L_2 current.

Figure 9 shows the experimental results with $V_{in} = 220$ V, corresponding to the modulation index $M = 0.71$. As shown in Figure 9a,b, the voltage stress on S_1 and S_4 is equal to the input voltage. The voltage stress on S_2 and S_3 is equal to the sum of the input and output voltages. Figure 9c shows the voltage of capacitors C_1 and C_2 and the current through the inductor L_1 . The average current of the inductor L_1 is 2.35A. As indicated in Figure 9d, the output voltages v_{ab}, v_o , and current through the inductor L_2 . The THD value of the output voltage v_o is 1.1%. The average current through the inductor L_2 is 2.32 A, and the peak current is about 16 A.

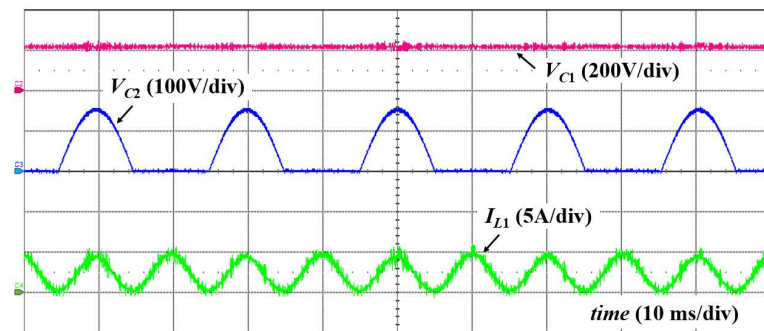


(a)

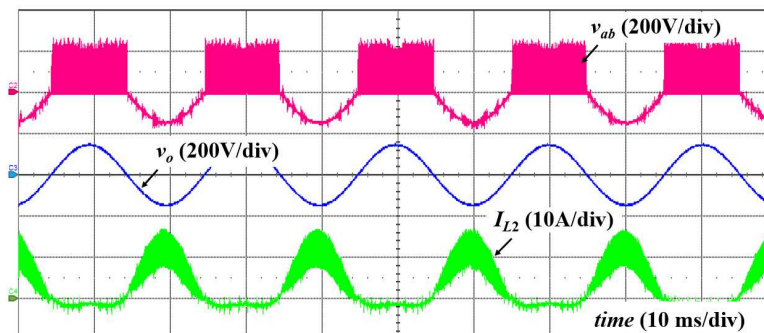


(b)

Figure 9. Cont.



(c)



(d)

Figure 9. Experimental results with $V_{in} = 220$ V. (a) Diode D_1 and switch S_1 voltage. (b) Switches S_2, S_3, S_4 voltage. (c) Capacitors C_1, C_2 voltage, and inductor L_1 current. (d) inverter output voltage v_{ab} , load voltage v_o , and inductor L_2 current.

As indicated in Figure 10, the efficiency of the proposed single-stage BB-BTI in case of input voltage at 80 V and 220 V, the output voltage is considered at 110 Vrms. The efficiency results show that the efficiency when the input voltage is 80 V is lower than the input voltage of 220 V. The peak efficiencies are 96% and 96.5% at 80 V and 220 V, respectively.

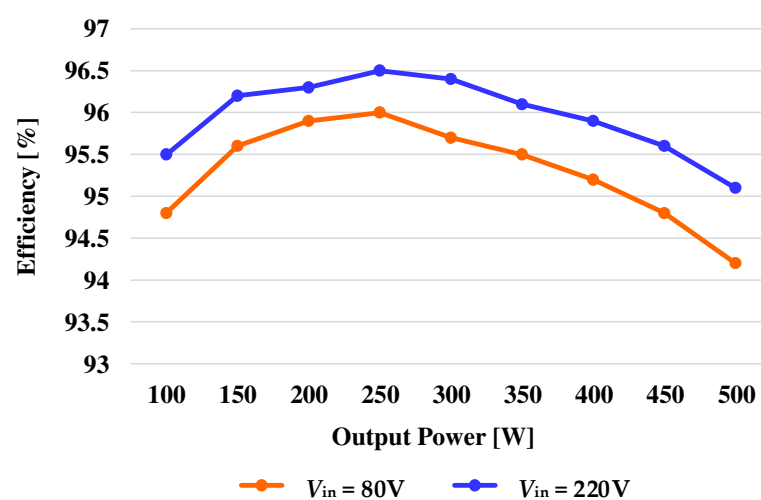


Figure 10. Measured experimental efficiency.

The distribution of power loss of the proposed single-stage BB-BTI based on the parameters shown in Table 4 is shown in Figure 11.

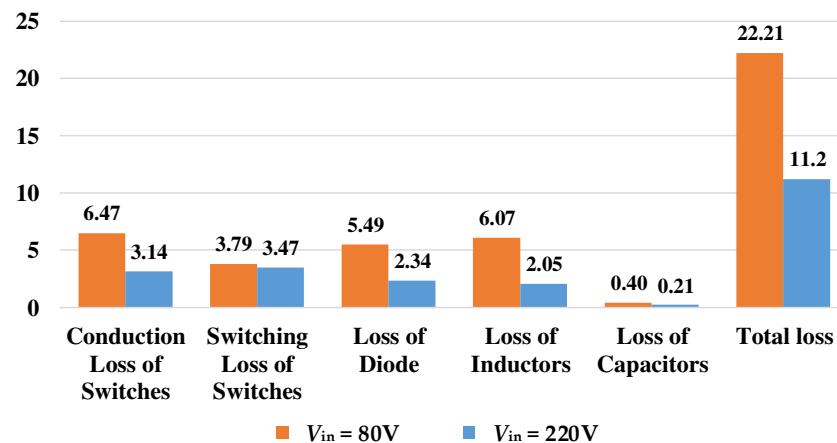


Figure 11. Distribution of power loss.

6. Conclusions

This paper presented the proposed single-phase, single-stage BB-BTI. The proposed inverter provides common ground and buck-boost capability. Compared with the conventional two-stage BB-BTI, the proposed single-stage BB-BTI has lower voltage stress on the switches and capacitors. Furthermore, the switching operation in the proposed single-stage BB-BTI is significantly less than in conventional two-stage BB-BTI, thereby improving efficiency and reducing filter inductor. The circuit does not contain an electrolytic capacitor, which reduces the volume and improves the life of the inverter. Mathematical analysis, design consideration, and comparison with existing common-ground single-phase inverters were performed. Finally, the simulation and experimental results were presented to confirm the performance of the proposed single-stage BB-BTI.

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References

- Jo, K.Y.; Duong, T.D.; Choi, J.-H. Emerging technologies in power systems. *Electronics* **2022**, *11*, 71. [\[CrossRef\]](#)
- Can, E. The design and experimentation of the new cascaded DC-DC boost converter for renewable energy. *Int. J. Electron.* **2019**, *106*, 1374–1393. [\[CrossRef\]](#)
- Can, E. A new multi-level inverter with reverse connected dual dc to dc converter at simulation. *Int. J. Model. Simul.* **2022**, *42*, 34–46. [\[CrossRef\]](#)
- Duong, T.D.; Nguyen, M.K.; Tran, T.T.; Choi, J.H.; Lim, Y.C. Transformerless High Step-Up DC-DC Converters with Switched-Capacitor Network. *Electronics* **2019**, *8*, 1420. [\[CrossRef\]](#)
- Duong, T.D.; Nguyen, M.K.; Nguyen, T.T.; Cha, H.; Lim, Y.C.; Choi, J.H. Switching-Cell Structure Based Generic Five-Level Current Source Inverter. *IEEE Trans. Ind. Electron.* **2022**, 1–10. [\[CrossRef\]](#)
- Alluhaybi, K.; Batarseh, I.; Hu, H. Comprehensive review and comparison of single-phase grid-tied photovoltaic microinverters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 1310–1329. [\[CrossRef\]](#)
- Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [\[CrossRef\]](#)
- Duong, T.D.; Nguyen, M.K.; Tran, T.-T.; Vo, D.-V.; Lim, Y.C.; Choi, J.-H. Topology Review of Three Phase Two-Level Transformerless Photovoltaic Inverters for Common-Mode Voltage Reduction. *Energies* **2022**, *15*, 3106. [\[CrossRef\]](#)

9. Nguyen, M.K.; Duong, T.D.; Lim, Y.C.; Choi, J.H. High voltage gain quasi-switched boost inverters with low input current ripple. *IEEE Trans. Ind. Inform.* **2019**, *15*, 4857–4866. [[CrossRef](#)]
10. Vo, D.-V.; Nguyen, M.-K.; Do, D.-T.; Choi, Y.-O. A Single-Phase Nine-Level Boost Inverter. *Energies* **2019**, *12*, 394. [[CrossRef](#)]
11. Tran, T.T.; Nguyen, M.K.; Duong, T.D.; Choi, J.H.; Lim, Y.C.; Zare, F. A Switched-Capacitor Voltage-Doubler Based Boost Inverter for Common-Mode Voltage Reduction. *IEEE Access* **2019**, *7*, 98618–98629. [[CrossRef](#)]
12. Duong, T.D.; Nguyen, M.K.; Tran, T.T.; Lim, Y.C.; Choi, J.H.; Wang, C. Modulation techniques for modified three-phase quasi-switched boost inverter with common-mode voltage reduction. *IEEE Access* **2020**, *7*, 160670–160683. [[CrossRef](#)]
13. Tai, T.T.; Nguyen, M.K.; Duong, T.D.; Lim, Y.C.; Choi, J.H. A switched-capacitor-based six-level inverter. *IEEE Trans. Power Electron.* **2022**, *37*, 4804–4816.
14. Liu, C.; Wang, Y.; Cui, J.; Zhi, Y.; Liu, M.; Cai, G. Transformerless photovoltaic inverter based on interleaving high-frequency legs having bidirectional capability. *IEEE Trans. Power Electron.* **2016**, *31*, 1131–1142. [[CrossRef](#)]
15. Wang, L.; Shi, Y.; Shi, Y.; Xie, R.; Li, H. Ground leakage current analysis and suppression in a 60-kW 5-Level T-Type transformerless SiC PV inverter. *IEEE Trans. Power Electron.* **2018**, *33*, 1271–1283. [[CrossRef](#)]
16. Guo, X. Three-phase CH7 inverter with a new space vector modulation to reduce leakage current for transformerless photovoltaic systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 708–712. [[CrossRef](#)]
17. Yang, B.; Li, W.; Gu, Y.; Cui, W.; He, X. Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system. *IEEE Trans. Power Electron.* **2012**, *27*, 752–762. [[CrossRef](#)]
18. Kerekes, T.; Teodorescu, R.; Rodríguez, P.; Vázquez, G.; Aldabas, E. A new high-efficiency single-phase transformerless PV inverter topology. *IEEE Trans. Ind. Electron.* **2011**, *58*, 184–191. [[CrossRef](#)]
19. Dong, H.; Xie, X.; Jiang, L.; Jin, Z.; Zhao, X. An electrolytic capacitor-less high power factor LED driver based on a ‘one-and-a-half stage’ forward-flyback topology. *IEEE Trans. Power Electron.* **2018**, *33*, 1572–1584. [[CrossRef](#)]
20. Tian, K.; Wu, B.; Narimani, M.; Xu, D.; Cheng, Z.; Zargari, N.R. A capacitor voltage-balancing method for nested neutral point clamped (NNPC) inverter. *IEEE Trans. Power Electron.* **2016**, *31*, 2575–2583. [[CrossRef](#)]
21. Tang, Y.; Yao, W.; Loh, P.C.; Blaabjerg, F. Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination. *IEEE Trans. Ind. Electron.* **2016**, *63*, 1016–1026. [[CrossRef](#)]
22. Gu, Y.; Li, W.; Zhao, Y.; Yang, B.; Li, C.; He, X. Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems. *IEEE Trans. Power Electron.* **2013**, *28*, 793–805. [[CrossRef](#)]
23. Siwakoti, Y.P.; Blaabjerg, F. Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2018**, *65*, 2100–2111. [[CrossRef](#)]
24. Ardashir, J.F.; Sabahi, M.; Hosseini, S.H.; Blaabjerg, F.; Babaei, E.; Gharehpetian, G.B. A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 5403–5414. [[CrossRef](#)]
25. Zhu, X.; Zhang, B.; Qiu, D. A new half-bridge impedance source inverter with high voltage gain. *IEEE Trans. Power Electron.* **2019**, *34*, 3001–3008. [[CrossRef](#)]
26. Kim, K.; Cha, H.; Kim, H. A new single-phase switched-coupled-inductor DC–AC inverter for photovoltaic systems. *IEEE Trans. Power Electron.* **2017**, *32*, 5016–5022. [[CrossRef](#)]
27. Sarikhani, A.; Takantape, M.M.; Hamzeh, M. A Transformerless Common-Ground Three-Switch Single-Phase Inverter for Photovoltaic Systems. *IEEE Trans. Power Electron.* **2020**, *35*, 8902–8909. [[CrossRef](#)]
28. Vo, D.-V.; Nguyen, M.-K.; Duong, T.-D.; Tran, T.-T.; Lim, Y.-C.; Choi, J.-H. A Novel Single-Stage Common-Ground Transformerless Buck-Boost Inverter. *Electronics* **2022**, *11*, 829. [[CrossRef](#)]
29. Yao, Z.; Wang, Z. Single-Stage Doubly Grounded Transformerless PV Grid-Connected Inverter with Boost Function. *IEEE Trans. Power Electron.* **2022**, *37*, 2237–2249. [[CrossRef](#)]
30. Karschny, D. Flying Inductor Topology. DE 196 42 522 C1, 23 April 1998.
31. Khan, A.A.; Lu, Y.W.; Eberle, W.; Wang, L.; Khan, U.A.; Agamy, M.; Cha, H. Single-Stage Bidirectional Buck–Boost Inverters Using a Single Inductor and Eliminating the Common-Mode Leakage Current. *IEEE Trans. Power Electron.* **2020**, *35*, 1269–1281. [[CrossRef](#)]
32. Ho, C.N.M.; Siu, K.K.M. Manitoba Inverter—Single-Phase Single Stage Buck-Boost VSI Topology. *IEEE Trans. Power Electron.* **2019**, *34*, 3445–3456. [[CrossRef](#)]
33. Ahmed, H.F.; El Moursi, M.S.; Zahawi, B.; Al Hosani, K. Single-Phase Photovoltaic Inverters with Common-Ground and Wide Buck–Boost Voltage Operation. *IEEE Trans. Ind. Inform.* **2021**, *17*, 8275–8287. [[CrossRef](#)]
34. Liu, Y.; Zhou, Y.; Guo, B.; Wang, H.; Su, M.; Liang, X.; Pan, X. Bimodal Transformerless Inverter with Three Switches. *IEEE Trans. Ind. Electron.* **2022**, *69*, 8972–8983. [[CrossRef](#)]
35. Gupta, K.K.; Ranjan, A.; Bhatnagar, P.; Sahu, L.K.; Jain, S. Multilevel inverter topologies with reduced device count: A review. *IEEE Trans. Power Electron.* **2016**, *31*, 135–151. [[CrossRef](#)]

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