Communication

W-Band GaN HEMT Switch Using the State-Dependent Concurrent Matching Method

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Abstract: In this study, a W-band GaN single-pole single-throw (SPST) switch was designed. To realize the pass and isolation modes of the SPST switch, we proposed the design technique of a unit branch consisting of one transistor and one transmission. The characteristic impedance and length of the transmission line were determined by the impedance and the angle at which the straight line connecting the impedances of the on and off states of the transistor meets the real axis of the Smith chart. Using the design technique, the matching networks for the pass and isolation modes of the switch are concurrently completed. In order to improve the insertion loss and isolation characteristics of the switch, the size of the transistor and the number of unit branches were investigated. To verify the feasibility of the proposed design technique, we designed the W-band SPST switch using a 100 nm GaN HEMT process. The measured insertion loss and isolation were below 2.9 dB and above 23.5 dB, respectively, in the frequency range from 91 GHz to 101 GHz.

Keywords: GaN; isolation; insertion loss; switch; W-band

1. Introduction

With the innovative development of military science and technology, research on explorers and trackers for the efficient operation of precision launch and hitting systems is being actively conducted. In particular, millimeter wave searchers and tracers are designed mainly using a 96 GHz frequency with low atmospheric loss and a short wavelength. Accordingly, it is essential to develop it as a millimeter-wave monolithic integrated circuit (MMIC) to ensure compact size and excellent performance.

MMICs for such explorers and trackers include power amplifiers, low-noise amplifiers, and switches. In particular, the switch affects the output power of the transmitter and the noise figure of the receiver. The switches require high isolation and high power handling capability and low insertion loss. Switches using p-i-n diodes capable of ensuring good isolation characteristics even at high frequencies have been reported [1–3]. However, p-i-n diode switches are not suitable for military millimeter wave searcher and tracking devices where high power is essential because the p-i-n diodes are incompatible with microwave integrated circuits [4]. Therefore, when a p-i-n diode is used, a switch cannot be integrated with other circuits such as power amplifiers and low-noise amplifiers. In this case, additional power loss and bandwidth reduction may occur during the modularization process of connecting the transceiver circuits and the switch [5]. This problem becomes more serious in the W-band with a high operating frequency. Therefore, research on switches using high electron-mobility transistor (HEMT) devices compatible with MMIC is being actively conducted [4,6–13]. In particular, gallium nitride (GaN) HEMT has a faster switching speed and high band gap characteristics compared to silicon-, gallium arsenide (GaAs)-, and silicon germanium (SiGe)-based devices. Accordingly, GaN HEMT can handle high power at a high operating frequency such as a W-band [14]. As a result, GaN HEMT can be regarded as one of the promising candidate devices among the MMICs for explorers

and trackers. In this work, we conducted a study on a single-pole single-throw (SPST) switch using GaN HEMT.

In this study, we proposed a design methodology that can achieve simultaneous matching for on and off states of traveling-wave-type SPST switches using the GaN HEMT process. The design methodology utilizes the parasitic components of GaN HEMT and additional transmission lines. Many studies related to the design methodologies for traveling-wave type switches have already been introduced [15,16]. However, most of the previous works are based on mathematical methodology. In this study, for the design of the traveling-wave type switch, we proposed a technique to design the characteristic impedance and length of the transmission line from impedances at on and off states of transistors using the Smith chart.

2. Proposed Design Technique of the W-Band Switch

The design process of the proposed methodology can be summarized as follows. The key components of the proposed switch are transistors and transmission lines. At this time, the transmission line is connected in series with the drain of the transistor. First, impedances according to the on and off states of the transistor are checked on the Smith chart. Thereafter, the impedance of each state is connected in a straight line on the Smith chart. The point where the straight line connecting the two impedances meets the real axis of the Smith chart is referred to as the characteristic impedance of the transmission line. In addition, the length of the transmission line is determined by the angle between this straight line and the real axis. In this way, impedance matching for the on and off state of the traveling-wave-type SPST switch may be achieved simultaneously. The following describes the actual design process of the proposed design methodology.

The designed switch consists of a unit branch as shown in Figure 1. The transmission line of TL_S connects the port of the RF_{IN} and the port of the RF_{OUT}. For 50 Ω load impedance, the transmission line of TL_S was designed to have a characteristic impedance of 50 Ω. In the final optimization process of the switch, the length of the TL_S was adjusted to improve the input and output return losses. In Figure 2, the equivalent circuit of the unit branch is shown. In the case of the unit branch, it is composed of an HEMT transistor and a transmission line of TL_P. The transmission line of TL_P connects the drain of the transistor and the transmission line of TL_S. The transistor and TL_P determine the pass and isolation mode characteristics of the entire traveling-wave-type SPST switch.
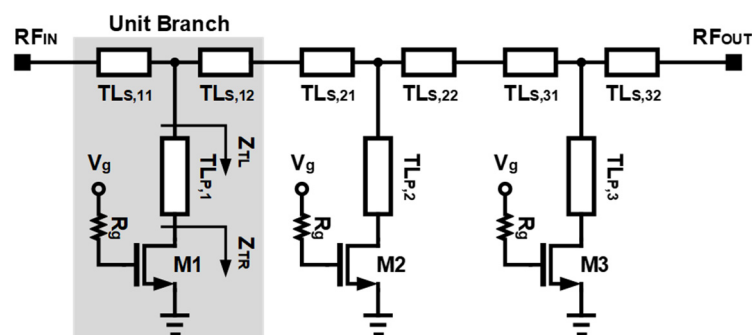

Figure 1. Schematic of the designed W-band SPST switch.

As illustrated in Figure 2, $Z_{TR,ON}$ and $Z_{TR,OFF}$ are impedances due to the parasitic components of the transistor depending on the on and off states of the transistor, respectively. In Figure 2, for the convenience of analysis, it is assumed that the ground connected to the source of the transistor is ideal. When the transistor is on, the transistor is equivalent to the inductance (L_M) and the resistance (R_{ON}). On the other hand, when the transistor is off, the transistor is equivalent to inductance (L_M), capacitance (C_{OFF}), and resistance (R_{OFF}) [4,14,17,18]. Here, the transistor in the off state may be modeled in parallel with the resistance and the capacitance. However, in this study, the transistor in the off state

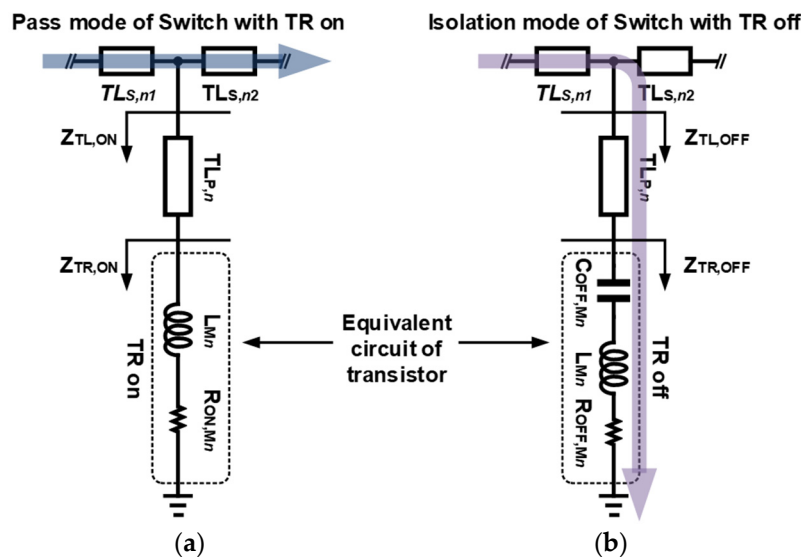was modeled with a series circuit of resistance and capacitance through parallel-to-series conversion.

Figure 2. Equivalent circuit according to the transistor being on and off: (**a**) pass and (**b**) isolation modes of the SPST switch.

Figure 3 shows the tendency of impedance change according to the on and off state of the transistor. In Figure 3, the values of $Z_{TR,ON}$ and $Z_{TR,OFF}$ are not actual values but are values for conceptualizing the proposed design technique. When points $Z_{TR,ON}$ and $Z_{TR,OFF}$ on the Smith chart were connected in a straight line, the impedance of the point where the straight line and the real axis of the Smith chart meet was set as the characteristic impedance value of the TL_P. Thereafter, the impedances of $Z_{TR,ON}$ and $Z_{TR,OFF}$ were moved on the real axis using the θ value adjusted according to the length of the TL_P.
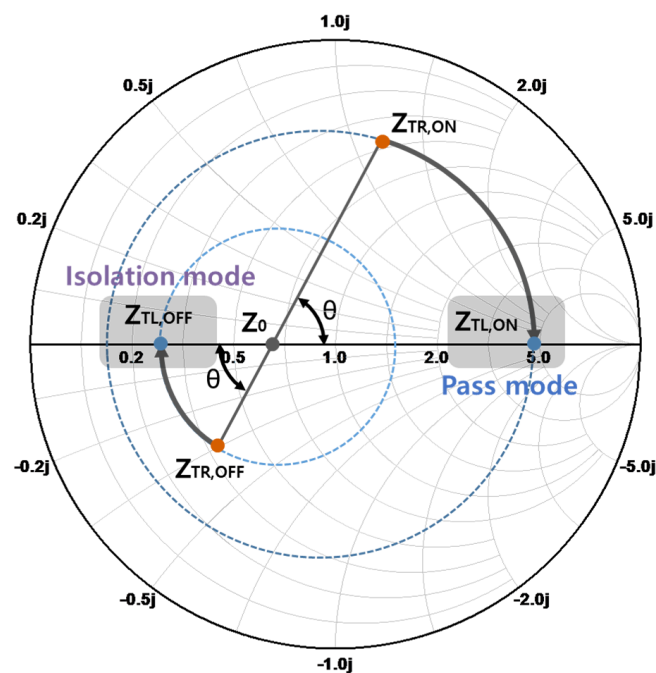

Figure 3. Impedances according to the on and off state of the transistors and the impedance changes due to TL_P.

If l is the length of the TL_P, the equations for determining the characteristic impedance, Z_0, and θ of TL_P are as follows:

$$Z_{TR,ON} = a + jb, \quad Z_{TR,OFF} = c + jd, \quad \beta = \frac{\theta}{l} \tag{1}$$

$$Z_{TL,ON} = Z_0 \frac{a + j(b + Z_0 \tan \beta l)}{Z_0 + j(a + jb) \tan \beta l}, \quad Z_{TL,OFF} = Z_0 \frac{c + j(d + Z_0 \tan \beta l)}{Z_0 + j(c + jd) \tan \beta l} \tag{2}$$

$$
\begin{aligned}
Z_0^2 \tan \beta l + b\left(1 - \tan^2 \beta l\right) Z_0 - \left(a^2 + b^2\right) \tan \beta l = 0 \\
Z_0^2 \tan \beta l + d\left(1 - \tan^2 \beta l\right) Z_0 - \left(c^2 + d^2\right) \tan \beta l = 0
\end{aligned} \tag{3}
$$

$$Z_0^2 = \begin{cases} \frac{d(a^2+b^2) - b(c^2+d^2)}{d-b} & \text{for } \tan \beta l \gg 1, \ \tan \beta l \ll 1 \\ \sqrt{a^2 + b^2} = \sqrt{c^2 + d^2} & \text{for } \tan \beta l \cong 1 \end{cases} \tag{4}$$

$$\tan \beta l = \begin{cases} \frac{|Z_0|}{b}\left(1 - \frac{(a^2+b^2)(d-b)}{d(a^2+b^2) - b(c^2+d^2)}\right) & \text{for } \tan \beta l \gg 1 \\ 1 & \text{for } \tan \beta l \cong 1 \\ -\frac{(d-b)}{(a^2+b^2) - (c^2+d^2)}|Z_0| & \text{for } \tan \beta l \ll 1 \end{cases} \tag{5}$$

The $Z_{TR,ON}$ and $Z_{TR,OFF}$ moved by the TL_P are shown in Figure 3 as $Z_{TL,ON}$ and $Z_{TL,OFF}$, respectively. From the perspective of the whole SPST switch, $Z_{TL,ON}$ has a relatively high resistance and $Z_{TL,OFF}$ has a relatively low resistance, so the on and off states of the transistor were used as the pass and isolation modes of the switch, respectively, as shown in Figure 3. Consequently, the proposed design technique of the switch could realize the pass and isolation modes of the switch by adjusting the characteristic impedance and length of the transmission line, TL_P according to the on and off impedances of the transistor.

3. Design of the W-Band SPST Switch

A W-band SPST switch based on the 100 nm GaN HEMT process was designed using the proposed design methodology for the switch. First, we investigated the transistor size of the unit branch to obtain low insertion loss and high isolation performance in the pass and isolation modes of the SPST switch as shown in Figure 4.
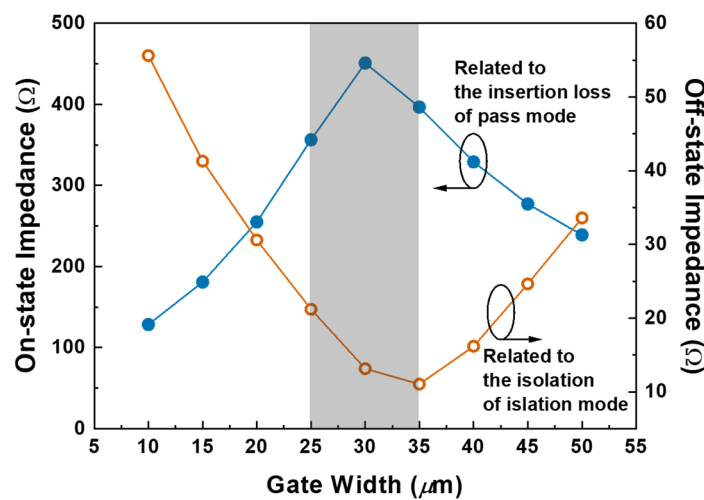

Figure 4. Impedance of the transistor according to the gate width with the gate length of 100 nm and the operating frequency of 96 GHz.

As previously described, the proposed switch operates in pass mode when the transistor is off. Conversely, the switch operates in isolation mode when the transistor is on. Therefore, it is advantageous for the individual transistors that make up the switch

to have high and low impedances in the on and off states, respectively. Figure 4 shows the impedance of the transistor according to the gate width of the transistor when the transistor is in the on and off states. As shown in Figure 4, the insertion loss and isolation characteristics can be improved when the gate width is from 25 μm to 35 μm. In this study, 30 μm was used as the initial value of the gate width, while the gate length and operating frequency were 100 nm and 96 GHz, respectively.

The unit branch with a transistor of 30 μm gate length was designed, as illustrated in Figure 5, using the proposed design methodology. The source of the transistor is connected to the ground through the back via a hole. Here, the effect of the back via the hole provided for ground in the GaN HEMT process was considered. The on and off states of the transistor are controlled by the gate voltage, and the gate is connected to the voltage source through R_g of 5 kΩ. In Figure 5, the impedance trajectory at the unit branch is shown using the Smith chart. The actual design process shown in Figure 5 is very similar to the conceptual diagram of the proposed design methodology shown in Figure 3.
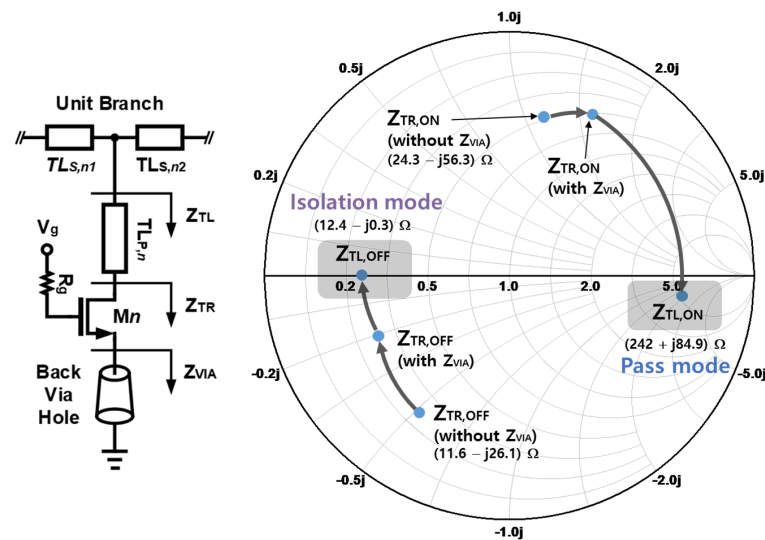

Figure 5. Unit branch design: impedance matching process.

As the next step, the number of unit branches constituting the SPST switch was determined through the insertion loss and isolation characteristics. As shown in Figure 6, as the number of unit branches increases, the isolation characteristic improves, but the insertion loss degrades, so we chose the number of unit branches to be three.
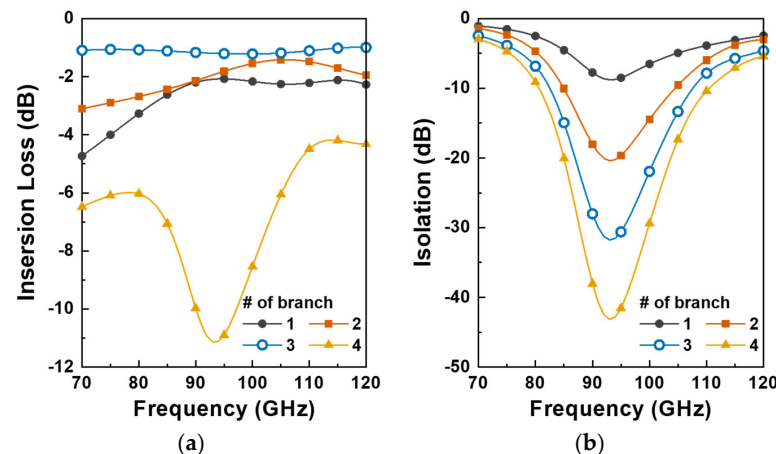

Figure 6. Switch characteristics based on the number of unit branches: (**a**) insertion loss and (**b**) isolation.

As a result, the schematic of the designed SPST switch is configured as shown in Figure 1. However, the size of the transistor slightly changed during the final detailed tuning process. Finally, the used gate widths of M1, M2, and M3 were 25 μm, 30 μm, and 25 μm, respectively.

4. Measurement Results

We designed a W-band SPST switch using a 100 nm GaN HEMT process to verify the feasibility of the proposed design technique. Figure 7 shows the chip photograph of the designed SPST switch with a chip size of 1.13×0.67 mm^2 including test pads. For measurement, Rohde & Schwarz's ZVA67 network analyzer and ZVA-Z110E converter were used. For the measurement of power handling capability, a driver amplifier and an attenuator were used. The gate voltages for the isolation and pass modes were -1.4 V and 0 V, respectively.
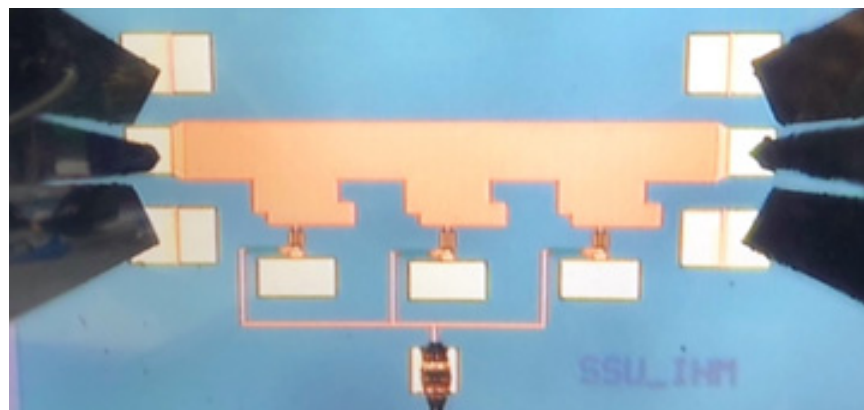

Figure 7. Chip photograph of the designed switch (chip size: 1.13×0.67 mm^2).

Figure 8 shows the measured insertion loss and isolation characteristics. The measurement results showed a similar tendency to the simulation as a whole, although the insertion loss was somewhat degraded compared to the simulation results. Insertion loss and isolation were measured below 2.9 dB and above 23.5 dB, respectively, in the range of operating frequencies from 91 GHz to 101 GHz.
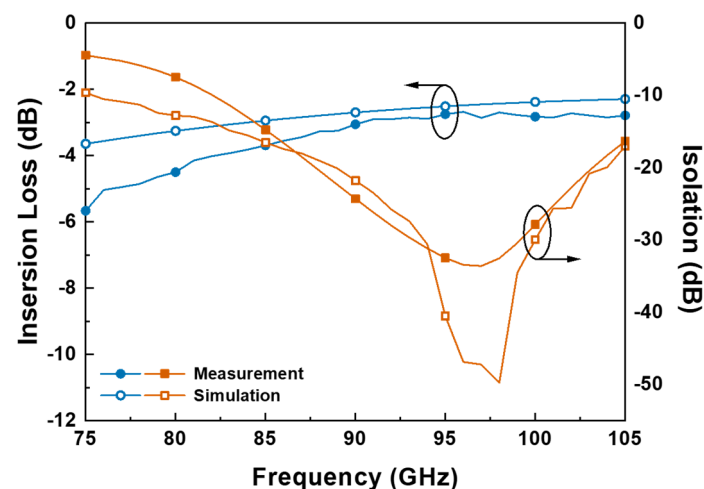

Figure 8. Measurement results: insertion loss and isolation.

As shown by the measured S-parameters of Figure 9, both S$_{11}$ and S$_{22}$ were measured to be -10 dB or less in the measurement frequency range of 75 GHz to 105 GHz.
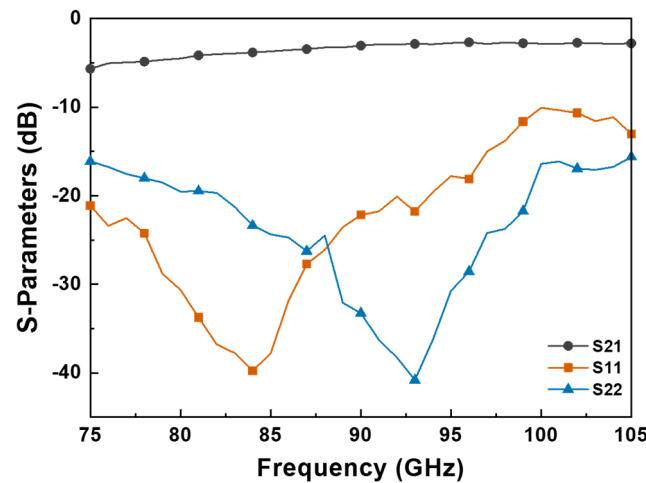
Figure 9. Measurement results: S-parameters.

Figure 10 shows the measured output power according to the input power in the operating frequency of 96 GHz. In general, when the switch operates in pass mode while the transistor constituting the switch is off, the power handling capability is limited by the breakdown voltages between the drain-source or drain-gate of the transistors. On the other hand, in this study, it is advantageous in terms of power handling capability because the switch operates in pass mode while the transistors constituting the switch are on. At the 96 GHz operating frequency, the output power of the switch has a loss of 2.68 dB compared to the input power. As shown in Figure 10, 0.23 dB compression was measured at an output power point of 12.4 dBm with 14.9 dBm input power. The higher output power could not be measured due to the power limit of the equipment we used. Therefore, the input P_{1dB} and output P_{1dB} of the designed switch may be higher than 14.9 dBm and 12.4 dBm, respectively.
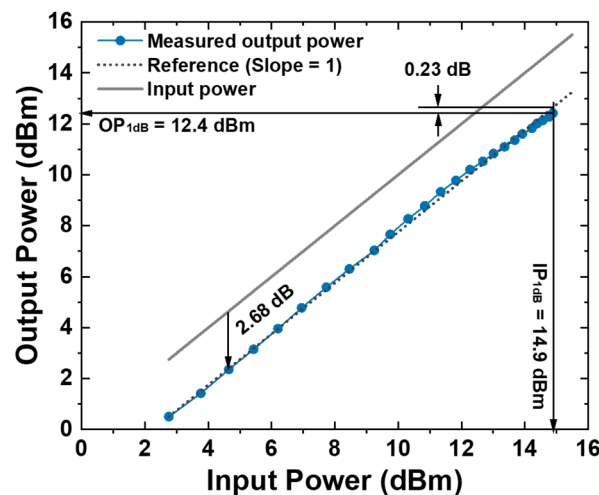

Figure 10. Measurement results: output power according to the input power.

Table 1 summarizes the performance of state-of-the-art switches. As shown in Table 1, the designed switch has a somewhat narrow operating frequency range, but has reasonable insertion loss and isolation, and the input P_{1dB} of the switch also exceeds 14.9 dBm. In addition, if the gate length of the GaN HEMT used in the switch decreases, the on-resistance decreases. Therefore, when using GaN HEMT with a reduced gate length, insertion loss is expected to be improved in the pass mode of the switch.

Table 1. Performance comparison of state-of-the-art GaN switches.

	[19]	[20]	[20]	[20]	This Work
Structure	SPST	SPST	SPST	SPDT	SPST
Tech. (nm)	40	40	40	40	100
Freq. (GHz)	60–110	75–110	75–110	75–110	91–101
Insertion loss (dB)	0.9–1.4	0.9–3.5	1.0–2.2	1.8–8.0	<2.9
Isolation (dB)	>9	25–30	15–20	30–40	>23.5
IP_{1dB} (dBm)	>24	>10 [1]	>10 [1]	>10 [1]	>14.9 [2]
Chip size (mm^2)	0.544	-	-	-	0.757 (0.306 [3])

[1] Peak large-signal values, [2] limited by available source power, and [3] core size.

5. Conclusions

In this study, for the design of a W-band SPST switch, a design technique for determining the characteristic impedance and length of a transmission line after confirming the impedance of the transistor has been proposed. The proposed design methodology consists of one transistor and one transmission line. At this time, the transmission line is connected in series with the drain of the transistor. The characteristic impedance and length of the transmission line were determined by the impedance and the angle at which the straight line connecting the impedances of the on and off states of the transistor meets the real axis of the Smith chart. Accordingly, the impedance matching networks of the on and off states of the traveling-wave-type SPST switch were simultaneously completed. In addition, in order to improve the pass and isolation mode characteristics of the switch, the transistor size was investigated, and the number of unit branches was optimized. As a result, the switch was designed with a total of three unit branches using the proposed design technique. The measured insertion loss and isolation were below 2.9 dB and above 23.5 dB, respectively, in the frequency range from 91 GHz to 101 GHz. The measured output P_{1dB} was higher than 12.4 dBm in the operating frequency of 96 GHz.

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