

Supplementary Materials

Sidewall Modification Process for Trench Silicon Power Devices

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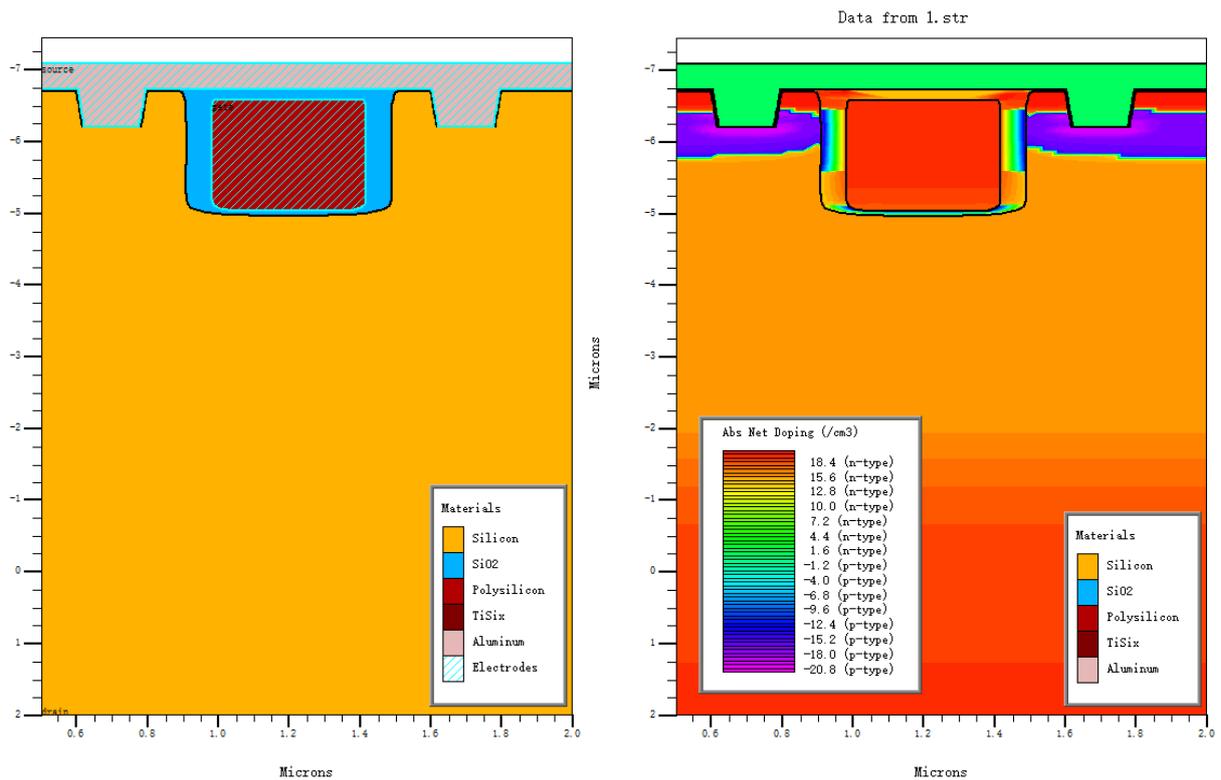
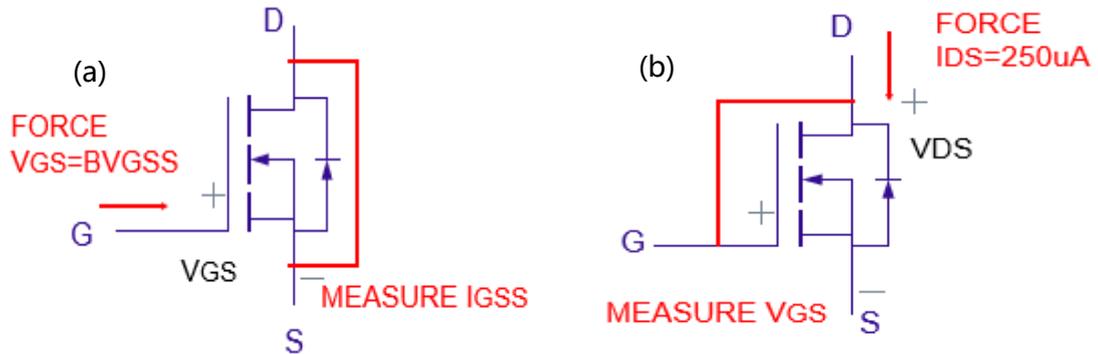


Figure S1. TCAD simulation result of Trench mosfet structure (left); net doping concentration of device (right).

Figure S2a shows IGSS measurement for trench MOSFET device, IGSS measures the leakage current between gate and source (I_{GS}). Since short circuit is applied between drain and source, the leakage current will generate when increasing voltage is applied between gate and source; Figure S2b illustrates threshold voltage (V_{GS-ID_S}) measurement for trench

MOSFET device, threshold voltage measures minimum gate-to-source voltage (V_{GS}) that is needed to create a conducting path between the source and drain terminals. Since short circuit is applied between drain and gate, the leakage current will generate when increasing voltage is applied between gate and drain. The initial current I_{DS} input will be 250uA, increase the gate-source voltage (V_{GS}) until the drain current (I_D) reaches 1mA.



Once this value is reached, measure V_{GS} immediately.

Figure S2. The schematic of IGSS(a) and V_{th} (b) measurement.

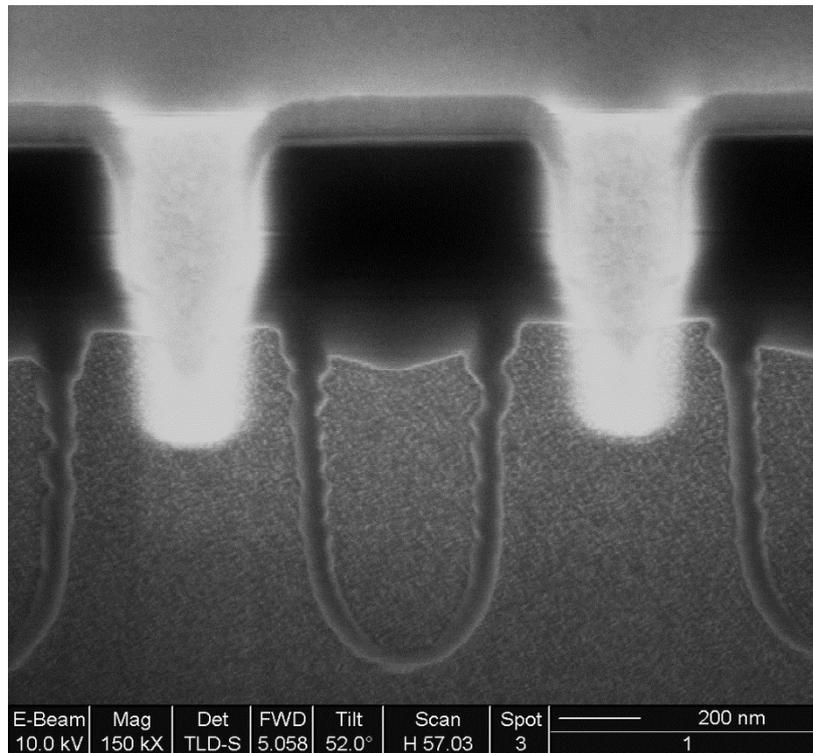


Figure S3. The microscope-SEM image with repeating experiment by using Table 1 recipe.

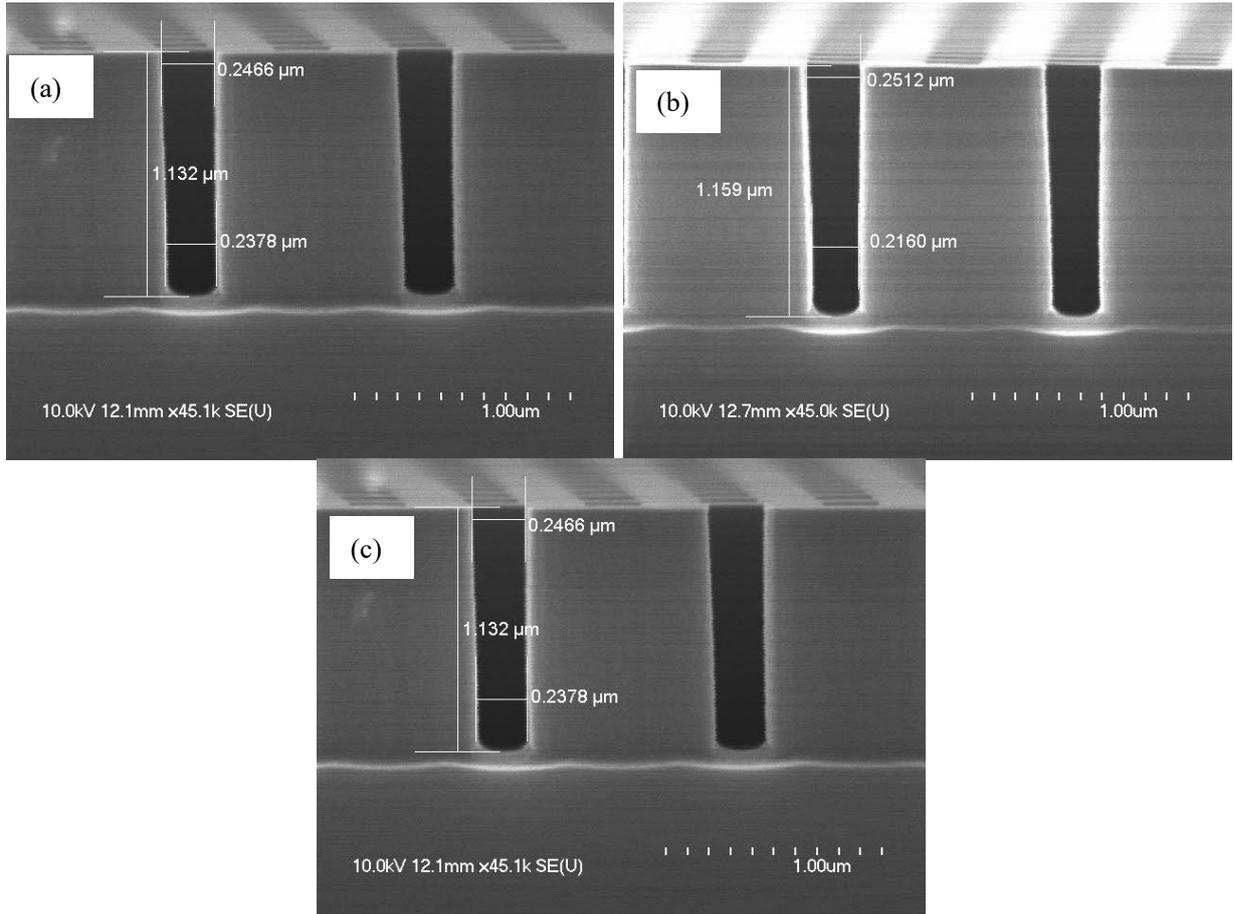


Figure S4. SEM images of Structure wafers: (a)RF power change; (b)Pressure change; (c)Temperature change; there are no more obvious modification by changing the parameter of RF power, pressure and temperature.

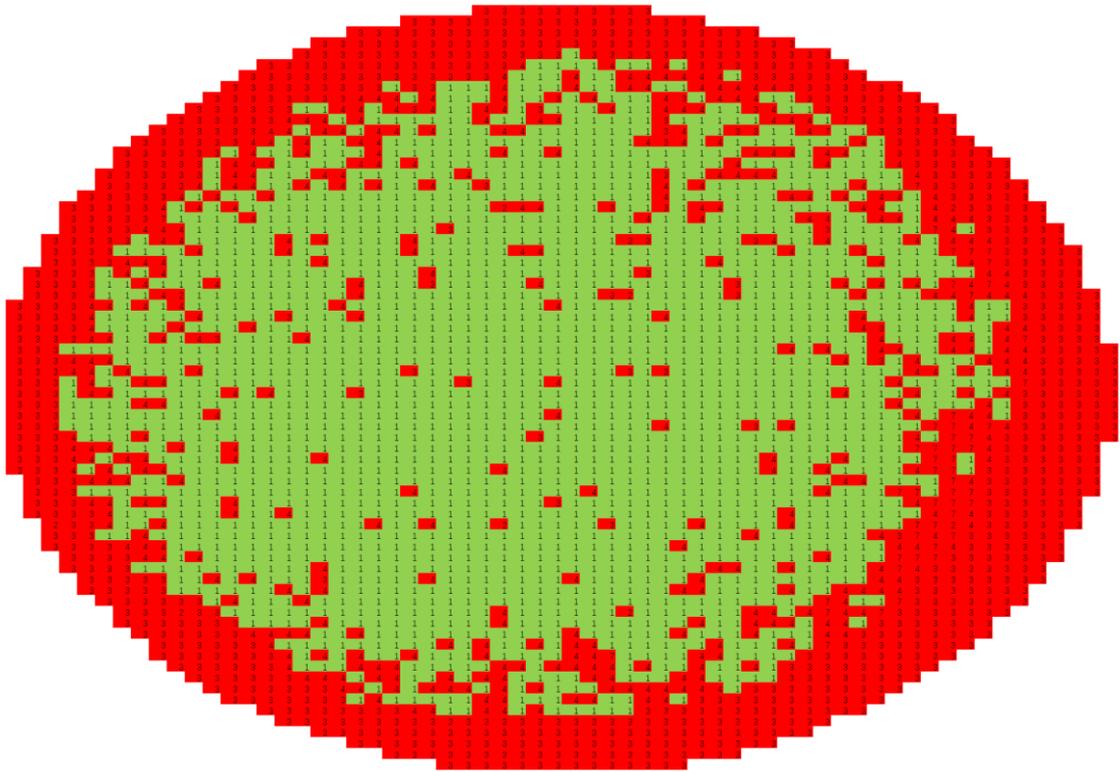


Figure S5. bin-map distribution of yield result for the device using initial etching recipe;(red: failed sample; green: passed sample), the overall yield is about 57.27%.

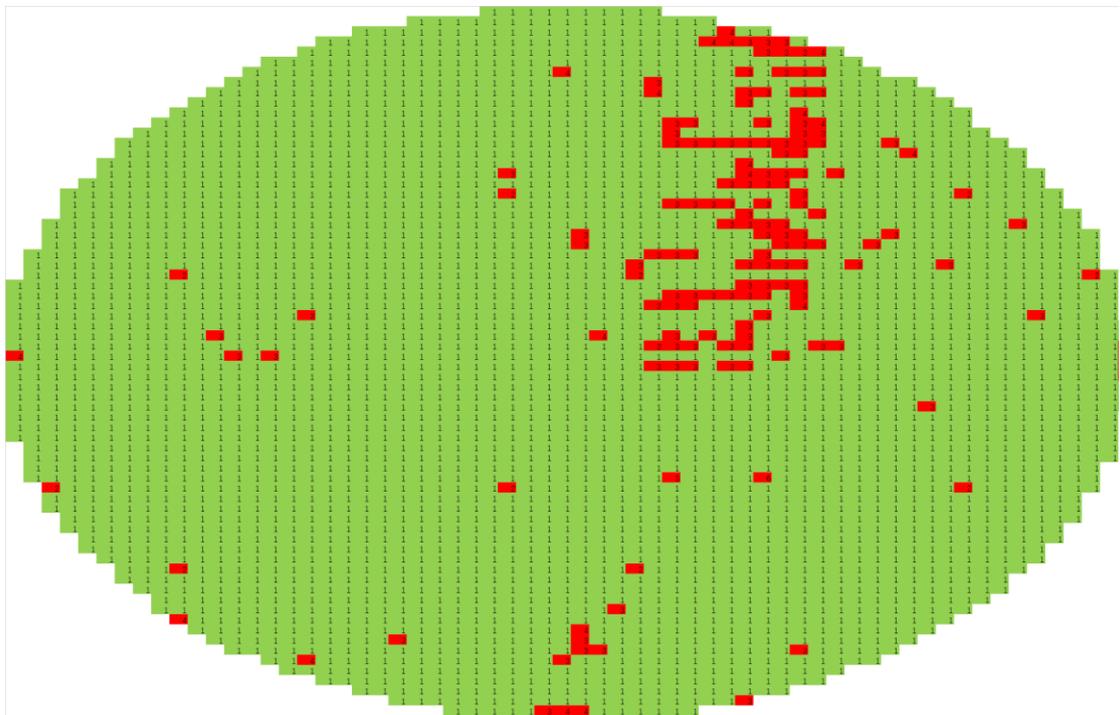


Figure S6. bin-map distribution of yield result for the device using updated etching recipe;(red: failed sample; green: passed sample), the overall yield is about 95.29%.