

# Supplementary Materials

## Sidewall Modification Process for Trench Silicon Power Devices

Lei Jin <sup>1,2,\*</sup>, Zhuorui Tang <sup>3,4</sup>, Long Chen <sup>1</sup>, Guijiu Xie <sup>5</sup>, Zhanglong Chen <sup>1</sup>, Wei Wei <sup>1</sup>, Jianghua Fan <sup>1</sup>, Xiaoliang Gong <sup>1</sup> and Ming Zhang <sup>2,6,\*</sup>

<sup>1</sup> 48th Research Institute of China Electronics Technology Group Corporation, Changsha 410111, China; chenlong@cs48.com (L.C.); chenxl01@cs48.com (Z.C.); weiwei@cs48.com (W.W.); fanjh@cs48.com (J.F.); gongxl@cs48.com (X.G.)

<sup>2</sup> Key Laboratory for Micro-/Nano-Optoelectronic Devices of Ministry of Education, School of Physics and Electronics, Hunan University, Changsha 410082, China

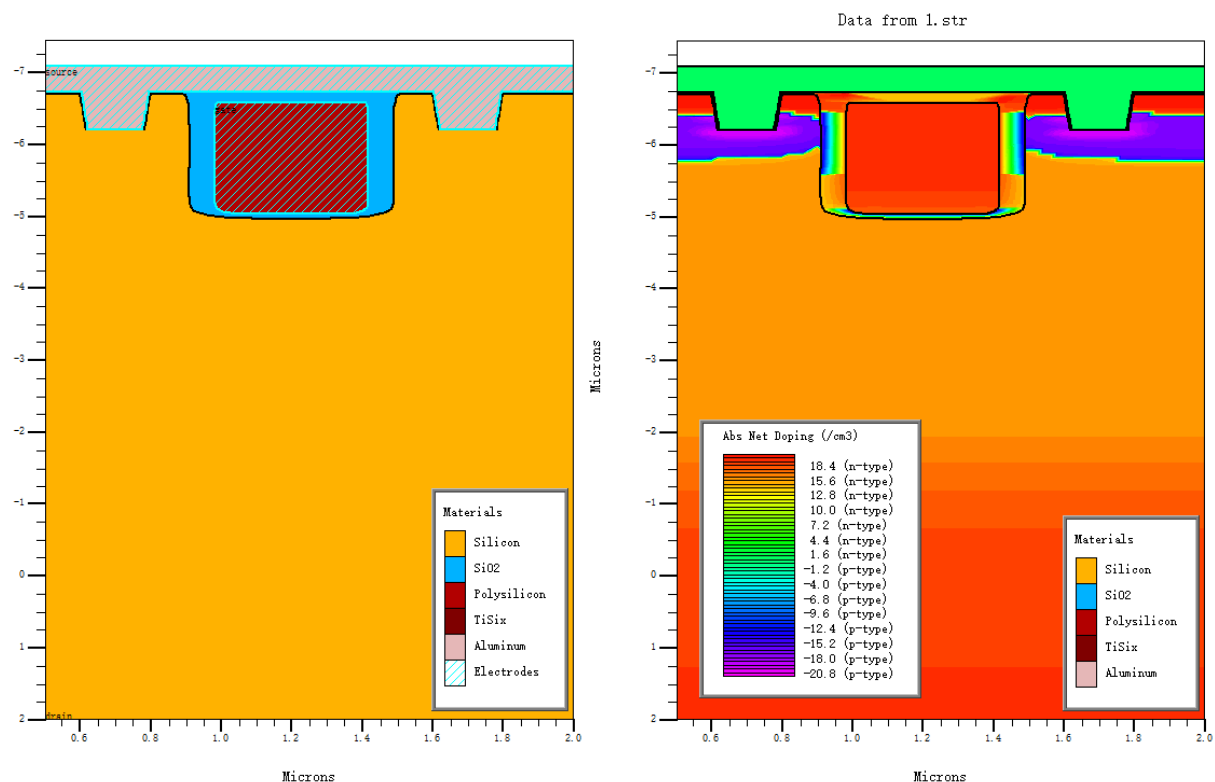
<sup>3</sup> Institute of Wide Bandgap Semiconductors and Future Lighting, Academy for Engineering & Technology, Fudan University, Shanghai 200433, China; zrtang21@m.fudan.edu.cn

<sup>4</sup> Jihua Laboratory, Foshan 528200, China

<sup>5</sup> CETC Electronics Equipment Group Co., Ltd., Beijing 100176, China; xiegj@cs48.com

<sup>6</sup> Changsha Semiconductor Technology and Application Innovation Research Institute, College of Semiconductors (College of Integrated Circuits), Hunan University, Changsha 410082, China

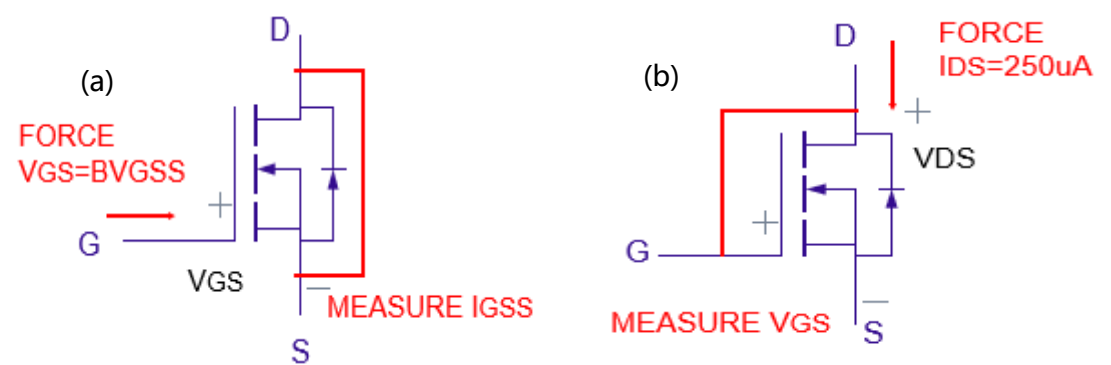
\* Correspondence: jinlei@cs48.com (L.J.); zhangming@hnu.edu.cn (M.Z.)



**Figure S1.** TCAD simulation result of Trench mosfet structure (left); net doping concentration of device (right).

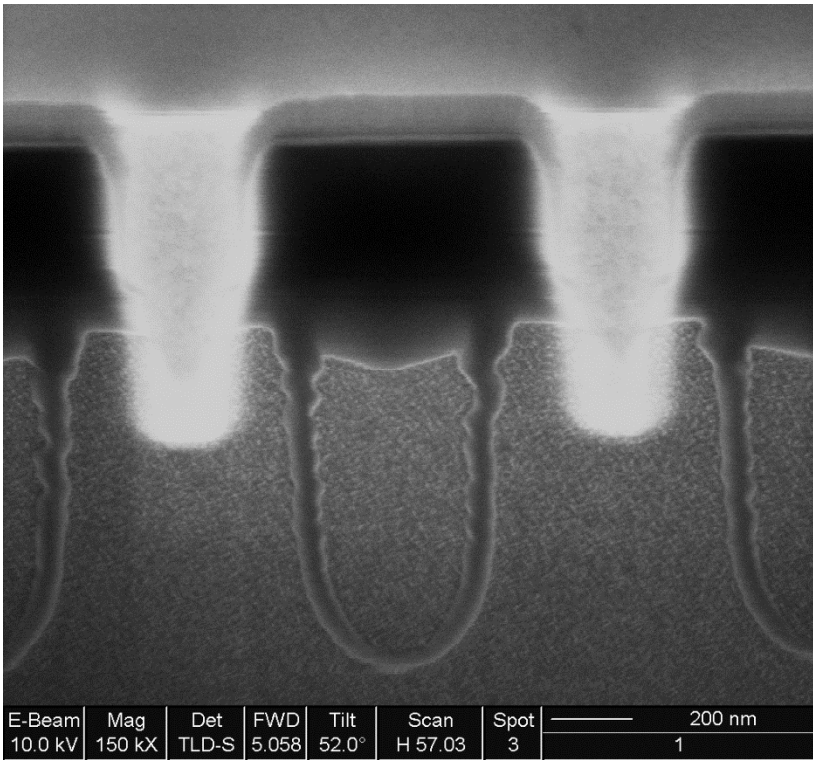
Figure S2a shows IGSS measurement for trench MOSFET device, IGSS measures the leakage current between gate and source ( $I_{GS}$ ). Since short circuit is applied between drain and source, the leakage current will generate when increasing voltage is applied between gate and source; Figure S2b illustrates threshold voltage ( $V_{GS}-I_{DS}$ ) measurement for trench

MOSFET device, threshold voltage measures minimum gate-to-source voltage ( $V_{GS}$ ) that is needed to create a conducting path between the source and drain terminals. Since short circuit is applied between drain and gate, the leakage current will generate when increasing voltage is applied between gate and drain. The initial current  $I_{DS}$  input will be 250uA, increase the gate-source voltage ( $V_{GS}$ ) until the drain current ( $I_D$ ) reaches 1mA.

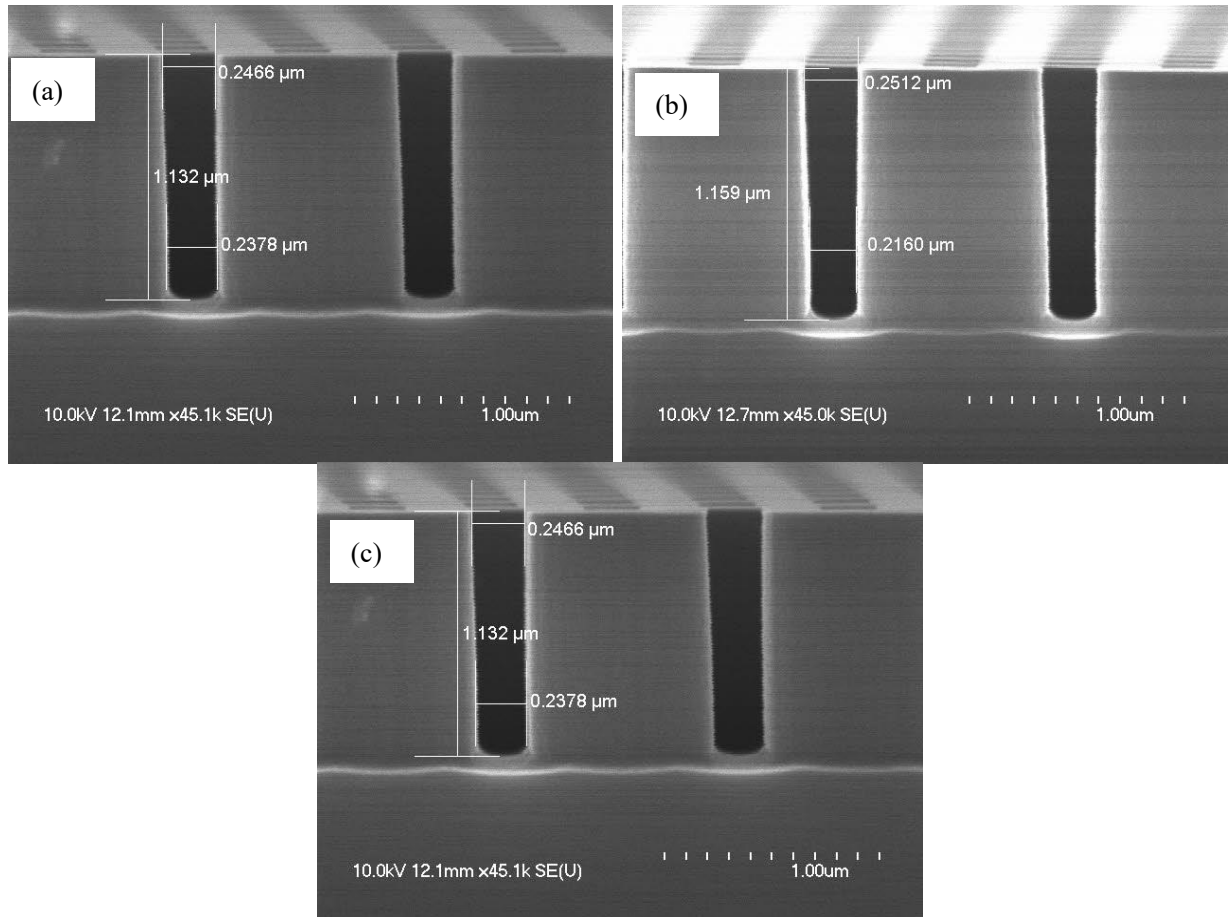


Once this value is reached, measure  $V_{GS}$  immediately.

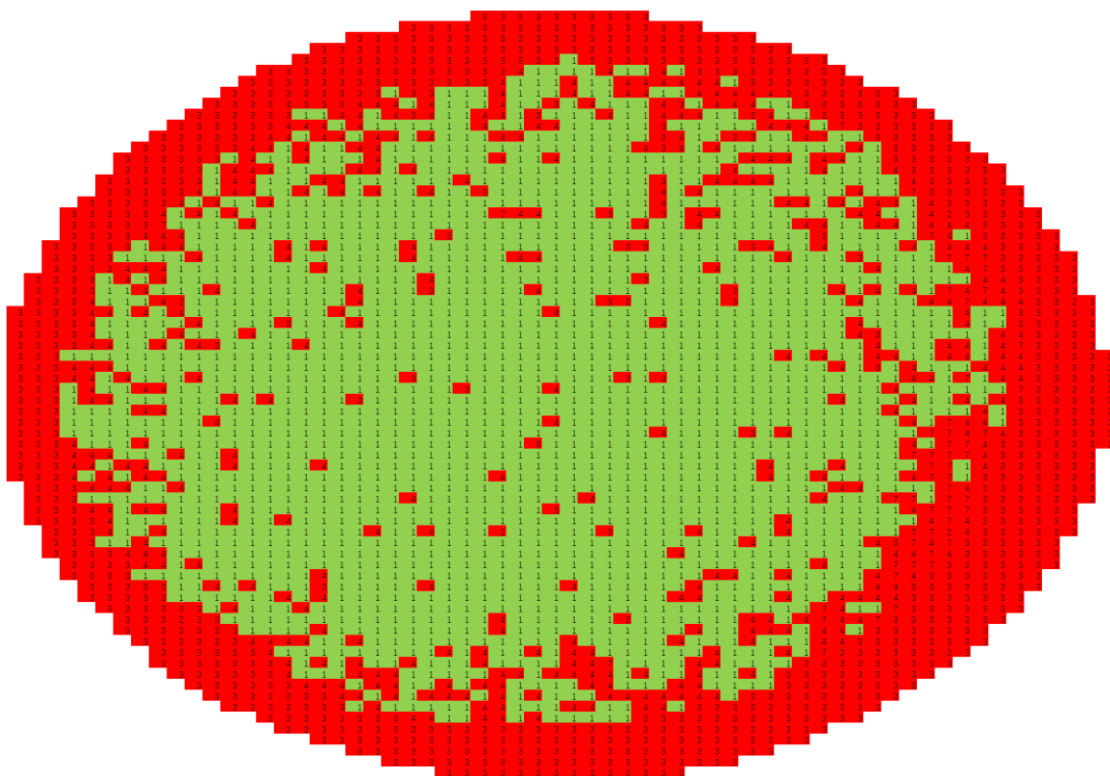
**Figure S2.** The schematic of IGSS(a) and  $V_{th}$ (b) measurement.



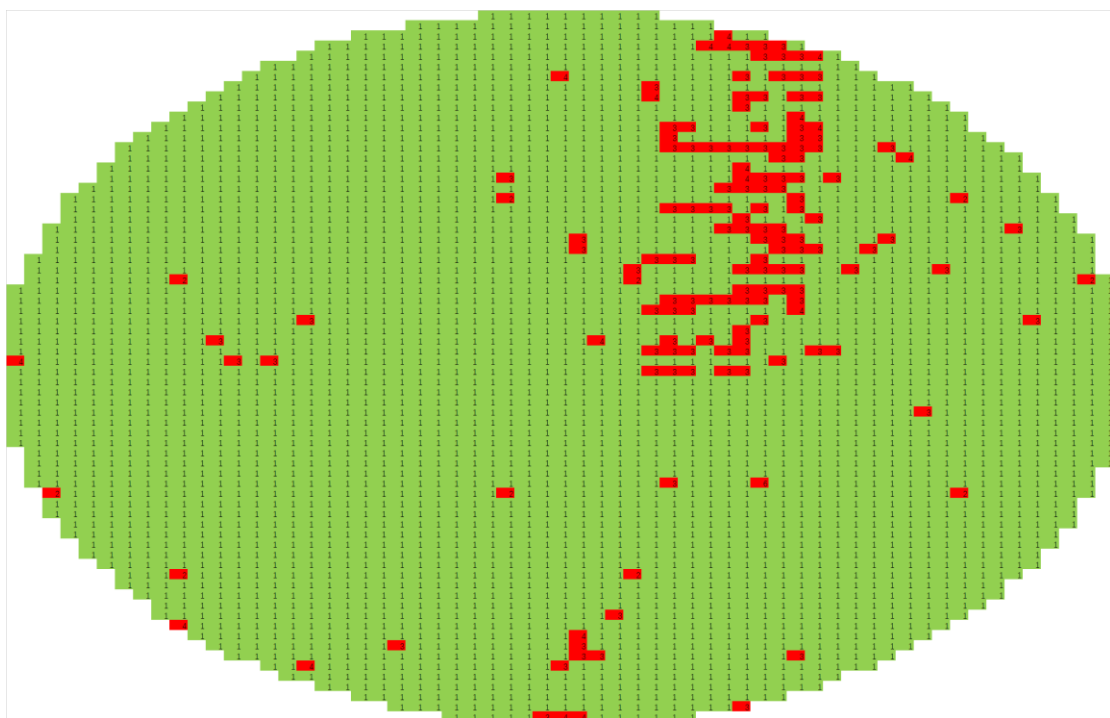
**Figure S3.** The microscope-SEM image with repeating experiment by using Table 1 recipe.



**Figure S4.** SEM images of Structure wafers: (a)RF power change; (b)Pressure change; (c)Temperature change; there are no more obvious modification by changing the parameter of RF power, pressure and temperature.



**Figure S5.** bin-map distribution of yield result for the device using initial etching recipe;(red: failed sample; green: passed sample), the overall yield is about 57.27%.



**Figure S6.** bin-map distribution of yield result for the device using updated etching recipe;(red: failed sample; green: passed sample), the overall yield is about 95.29%.