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A Robust LC-π Matching Network for 112 Gb/s PAM4 Receiver in 28 nm CMOS

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Abstract: This article presents analysis, design details, and simulation results of an impedance matching network designed for a 112 Gb/s pulse-amplitude-modulation-4 (PAM4) receiver using an LC-π structure. We designed the bonding wire as a part of the matching network, which reduced design pressure on the equalizer as there will be no need to compensate the loss of the chip package. To avoid robustness issues caused by the fluctuation of the bonding wire inductance, the matching network is designed to bw adjustable by the capacitance on *PCB* and the terminal resistance. We analyzed the parasitics in the layout and the influence of nearby and dummy metals and obtained reliable simulation results through electromagnetic field simulation. This matching network is designed with a 28 nm CMOS process. Post-layout simulation results show that with bonding wire inductance changing from 150 pH to 250 pH, it can always meet CEI-112G-XSR-PAM4 Extra Short Reach Interface requirements.

Keywords: wireline receiver; broadband impedance matching; LC passive filter; bonding wire; robustness

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1. Introduction

At present, the speed of a high-speed serial interface (SerDes) has developed to 112–224 Gb/s PAM4 [1–6], which requires 28–56 GHz analog bandwidth. The parasitic capacitance at input/output ports becomes intolerable for such high-speed signal. As shown in Figure 1, C_{PCB} represents the parasitic capacitance of *PCB*, C_{PAD} and C_{ESD} represents the parasitic capacitance of *PAD* and *ESD* device, C_{IN} represents the input capacitance of the internal circuit, C_{Rt} represents the parasitic capacitance of Rt array, and L_{bond} represents the parasitic inductance of the bonding wire [7,8]. The capacitance reduces the bandwidth and causes impedance mismatch, which directly limits the data rate and cause reflection. In addition, the parasitics of bonding wires have rarely been mentioned in previous articles. This leads to two problems. First, omitting the parasitics of bonding wires leads to inaccurate models, which may cause design failures; additionally, the inductance value of the bonding wire can fluctuate severely during the packaging process, so the robustness of the matching network becomes a problem.

Figure 2 shows common matching networks for high-speed SerDes, ignoring the influence of the parasitic inductance of the bonding wire. At 28–56 Gb/s, only one inductor is needed for impedance matching, called inductive peaking [9–11]. As the frequency increases, the impedance of the inductor increases. Therefore, it compensates for the impedance reduction caused by the capacitor. As date rates increase to 56–112 Gb/s, t-coils are widely used [12–15]. Composed of two coupled inductors, t-coils can achieve better impedance matching and wider bandwidth. Extending the bandwidth to 112–224 Gb/s, t-coils cannot meet the bandwidth demand, either. The LC-π matching networks become a trend [6,7,16]. Using more inductors, LC-π matching networks divide the capacitance to smaller segments, which forms a structure similar to a distributed circuit, thus achieving higher bandwidth.

In this paper, we compared and analyzed the existing LC-π matching networks, then we proposed an LC-π matching network that takes the bonding wire inductance into account. We designed the bonding wire as a part of the matching network, which reduced the design pressure on the equalizer as there will be no need to compensate for the loss of the chip package. However, due to packaging process variations, the value of the bonding wire inductance often exhibit significant fluctuations, which causes challenges to robustness. Therefore, we proposed a matching network that can be optimized by adjusting the capacitance on *PCB* and the terminal resistance after tap-out, and thus the robustness is enhanced. For the layout design, we analyzed the influence of the parasitics, nearby signal paths and dummy metals. To obtain more reliable simulation results, electromagnetic field simulation tools are used for the post-layout simulation. Designed with a 28 nm CMOS process, the simulation results show that with the bonding wire inductance changing from 150 pH to 250 pH, this matching network can always meet CEI-112G-XSR-PAM4 Extra Short Reach Interface requirements [17].

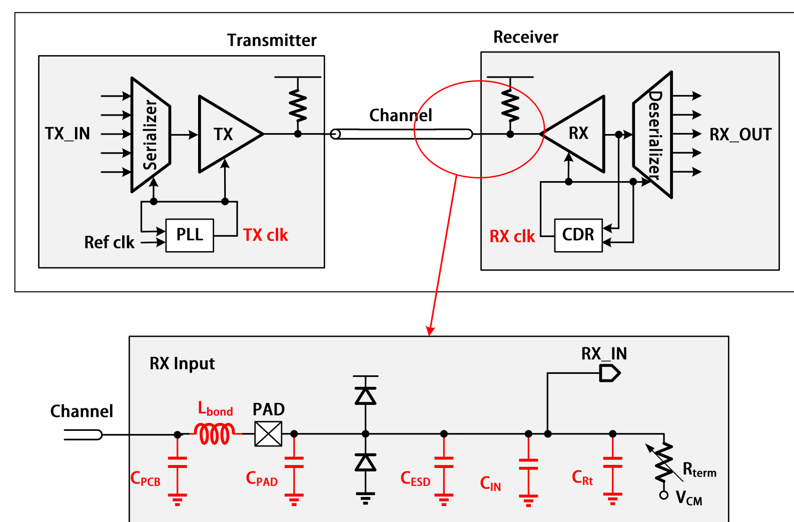

Figure 1. Block diagram of the SerDes transceiver and parasitic at the input port of receiver.

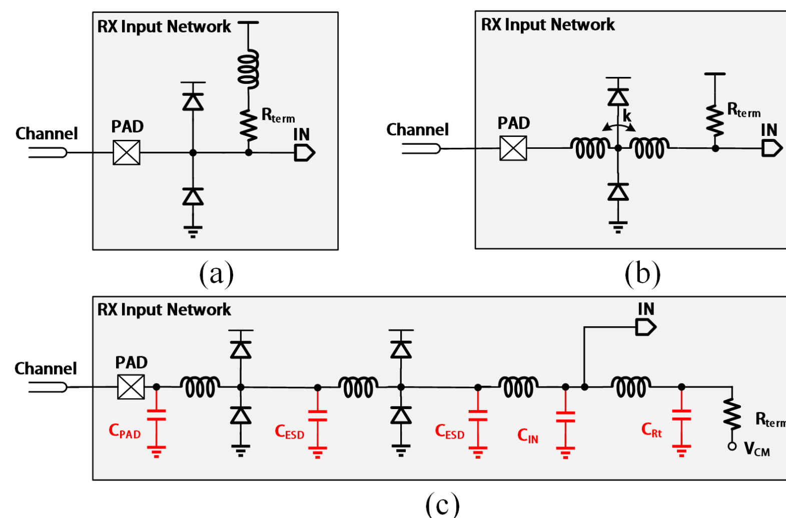

Figure 2. Impedance matching networks for SerDes receivers. (**a**) Inductive peaking. (**b**) T-coil peaking. (**c**) LC-π network.

This paper is organized as follows. Section 2 shows analysis and design details of the LC-π matching network. Simulation results are presented in Section 3, and Section 4 draws the conclusion.

2. LC-π Matching Network Design

2.1. Modeling of the Parasitic Capacitance and Inductance

During the packaging process of a chip, bonding wires are used to connect the *PAD* inside the chip to *PCB* boards, as shown in Figure 3, which introduces additional parasitic. The PAD adds a parasitic capacitance to GND. To minimize the parasitic capacitance, a total of only 3 metal layers are used for the *PAD* in our design, including the top AP layer, and M9 and M8 layers, with an area of 56 µm × 68 µm. The extraction of parasitic capacitance of *PAD* can be performed using the Calibre tool from Cadence during post-layout simulation or by using an electromagnetic field simulation tool like EMX to obtain accurate results.

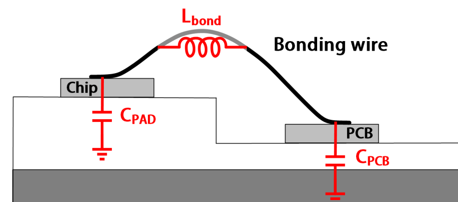

Figure 3. Structure of wire bonding in the chip packaging.

In comparison, accurate modeling of the bonding wire is much more difficult due to process constraints. Because the shape and length of the bonding wire can not be precisely controlled. However, the characteristics of the bonding wire still exhibit an inductance. As stated in [18]. This inductance has a much higher Q value than the planar spiral inductor implemented in CMOS technology, because the parasitic resistance and capacitance are smaller. Therefore, in our design, the bonding wire is modeled as an ideal inductor of about 200pH according to the data given by foundry and design experience. This will not affect the simulation accuracy, but simplifies the design. To characterize the fluctuation of the bonding wire inductance, we set the range of the inductance value to be 150–250 pH, and our goal is to ensure that the bandwidth of the matching network can still meet the requirements when the bonding wire inductance value fluctuates within this range.

Finally, when the bonding wire is connected to the *PCB* board, there will also be parasitic capacitance at the connection point. However, the difference is that the traces on the *PCB* can be accurately designed. Therefore, to some extent, it can be considered that this parasitic capacitance can be flexibly adjusted.

The packaging structure of the entire chip is modeled as shown in Figure 4, where C_{PCB} represents the parasitic capacitance on the *PCB*, which can be considered adjustable; L_{bond} represents the parasitic inductance of the bonding wire with a value fluctuating from 150 pH to 250 pH; C_{PAD} represents the parasitic capacitance of the *PAD* inside the chip, which is extracted by post-layout simulation or electromagnetic field simulation tools.

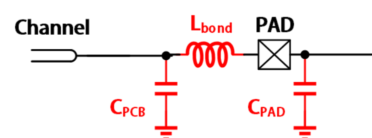

Figure 4. Model of the chip packaging.

2.2. Analysis and Selection of the Structure of LC-π Matching Networks

In previous articles, the effect of parasitic inductance is often neglected. Under such conditions, this inductor would be considered as part of the channel of the SerDes transceiver, simplifying the design of the matching network but degrading the attenuation characteristics of the channel. Because the loss introduced by chip packaging is also considered as part of the channel loss, thus increasing requirements for equalization circuits, as shown in Figure 5.

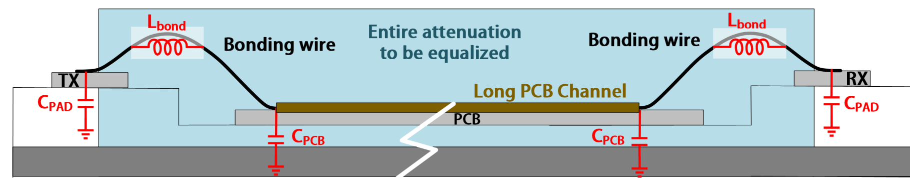

Figure 5. The channel to be equalized for SerDes transceiver.

Ignoring the parasitic inductance of the bonding wire, we first consider the impact of parasitic capacitance, which is the dominant cause of bandwidth limitation and impedance mismatch. For a SerDes receiver, the parasitic capacitance and termination resistance form a first-order RC low-pass filter with one pole [16], as shown in Figure 6. The transfer function can be represented as Formula (1), and the pole can be expressed as Formula (2):

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{SC_{total}}//R_{term}}{\frac{1}{SC_{total}}//R_{term} + R_S} \tag{1}$$

$$pole = \frac{1}{(R_S||R_{term})C_{total}} \tag{2}$$

where the transmission line impedance R_s and the termination resistance R_{term} are generally matched to be 50 Ω and the total parasitic capacitance at the input port of the SerDes receiver is C_{total}.

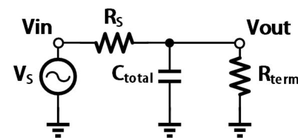

Figure 6. Small-signal model of the input port of SerDes receiver.

In order to eliminate the effects of parasitic capacitance, LC-π matching networks are commonly designed in the following forms: one method is similar to distributed *ESD* [19–21], or called artificial transmission line. This approach is applicable when the parasitic capacitance of the *ESD* device dominates. As shown in Figure 7, by dividing large *ESD* devices into smaller ones equally and separating them with inductors, an artificial transmission line can be implemented, thus increasing the bandwidth. In addition, another optional structure divides the capacitances too, but not into equal sizes. Instead, it is designed as an LC low-pass filter [22]. In the following article, the two design options are compared and the second option tends to demonstrate better performance.

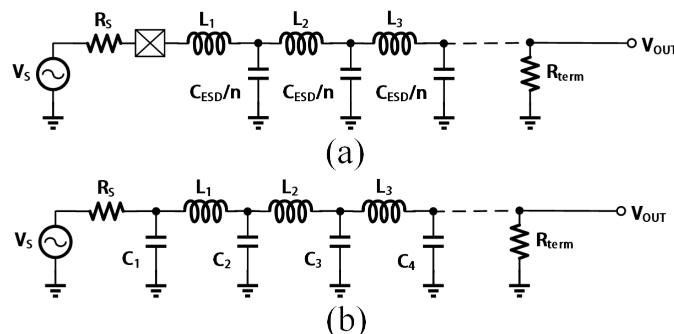

Figure 7. Two LC-π matching networks. (**a**) Artificial transmission line. (**b**) LC low-pass filter.

For a SerDes receiver, assuming that there is a total of 400 fF of parasitic capacitance at the input port, according to the design parameters of the artificial transmission line, we can divide the parasitic capacitance equally and add inductors based on the characteristic

impedance of the transmission line, as shown in Table 1. While the other LC-π network is designed as a low-pass filter by making a reasonable distribution of the parasitic capacitance according to the design parameters of the Chebyshev I filter. As shown in Figure 8, when both are designed to be of the same order, Chebyshev I low-pass filter demonstrates better return loss characteristics.

Table 1. LC values for LC-π matching networks.

	C_1	L_1	C_2	L_2	C_3	L_3	C_4
Chebyshev I	72 fF	216 pH	128 fF	239 pH	128 fF	216 pH	72 fF
Artificial t-line	100 fF	250 pH	100 fF	250 pH	100 fF	250 pH	100 fF

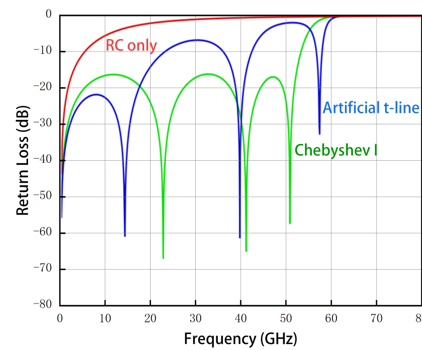

Figure 8. Return loss response of RC-only input port, artificial transmission line and Chebyshev I low-pass filter.

In addition to Chebyshev I filters, Table 2 lists LC values of different 7th-order low-pass filters with the same AC bandwidth of 30 GHz. The return loss, amplitude, and group delay responses are shown in Figure 9.

Table 2. LC values of different structures of LC low-pass filters.

	C_1	L_1	C_2	L_2	C_3	L_3	C_4
Bessel	46 fF	141 pH	261 fF	313 pH	78 fF	113 pH	15 fF
Butterworth	47 fF	331 pH	191 fF	531 pH	191 fF	331 pH	47 fF
Chebyshev I (0.01 dB ripple)	84 fF	369 pH	186 fF	433 pH	186 fF	369 pH	84 fF
Chebyshev I (0.1 dB ripple)	125 fF	377 pH	223 fF	417 pH	223 fF	377 pH	125 fF

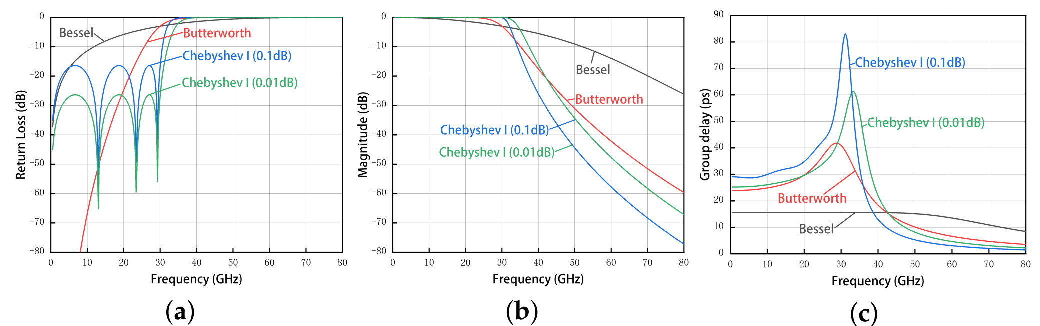

Figure 9. Responses of LC low-pass filters. (**a**) Return loss. (**b**) Magnitude. (**c**) Group delay.

It can be seen that the Butterworth filter has the flattest amplitude response [23–26], which ensures that the magnitude of all frequency components in the signal are not distorted. The Bessel filter has the slowest attenuation of amplitude and the smallest group delay variation. This means that the Bessel filter minimizes the attenuation of the signal and ensures that the phase relations between different frequencies of wideband signals are not distorted while passing through the Bessel filter, which are both beneficial for wideband

signal transmission. Therefore, the Bessel filter has optimal time-domain performance and can achieve the best eye diagram [27,28]. However, the Bessel filter has the minimum total capacitance, which means it can only absorb the smallest parasitic capacitance. So, it is difficult to be apply in circuits with large parasitic capacitance. In comparison, the Chebyshev I filter has ripples in pass-band and has the steepest cut-off characteristic. But if we limit the ripple in the pass-band to an acceptable range, with the same bandwidth, Chebyshev I filter tends to have the largest capacitance values. The ability to absorb parasitic capacitance is exactly what we need in the broadband matching network. This makes the Chebyshev I filter more suitable for broadband impedance matching design.

Besides the performance differences between different types of the filters, difficulty of implementation and robustness of the matching network should also be considered. For the artificial transmission line matching network, parasitic capacitance is divided into equal parts, which is often limited in implementation because parasitic capacitance of other devices is not so easy to be split as *ESD* devices. The implementation of LC low-pass filter matching networks faces the same challenge. To solve this problem, Ref. [16] provided a solution. By distributing the parasitic capacitance of each device based on the LC low-pass filter parameters, we can try to implement an ideal low-pass filter as much as possible. However, such a design is sometimes difficult to implement, too. In addition, the designs above did not take the bonding wire inductance into account. The bonding wire is an additional inductor that can be considered as a part of the matching network. This can reduce the design pressure faced by the equalizers because it does not need to equalize the parasitic of the chip package. But the issue to be faced is that the inductance variation is quite large, which affects the robustness of the matching network.

2.3. LC-π Matching Network Considering the Bonding Wire Inductance with Better Robustness

Due to the implement difficulties, we cannot design the matching network to be exactly the same as the aforementioned structure, but the analysis above provides design guidance for us. From the analysis above, we can draw the following conclusions: Butterworth filters have the most flat frequency response, Bessel filters can achieve the best output eye diagram, and Chebyshev I filters are the most suitable for broadband impedance matching. Therefore, we can design the matching network based on the parameters of the Chebyshev I filters initially to achieve maximum capacitance absorption capability. Then, we can adjust the parameters of the matching network to optimize its frequency response and group delay for the best time-domain performance.

Firstly, Chebyshev I filters represent the maximum matching bandwidth that can be achieved, so we need to approach it as closely as possible. Now, take a look at the structure of Chebyshev I filters. Table 3 gives the design parameters of Chebyshev I filters with different bandwidth. With the same order, all of the capacitances monotonically decrease as the bandwidth increases. Therefore, it is assumed that the largest parasitic capacitance in the circuit limits the maximum bandwidth that the matching network can achieve. In addition, for Chebyshev I filters, the capacitance is symmetrically distributed in pairs, and the capacitance on both sides is the smallest while the capacitance in the middle is the largest. As we can see, $C_1 = C_4 < C_2 = C_3$.

Table 3. LC values of Chebyshev I low-pass filters with different bandwidth.

Chebyshev I (0.1 dB Ripple)	C_1	L_1	C_2	L_2	C_3	L_3	C_4
15 GHz	46 fF	141 pH	261 fF	313 pH	78 fF	113 pH	15 fF
20 GHz	47 fF	331 pH	191 fF	531 pH	191 fF	331 pH	47 fF
25 GHz	84 fF	369 pH	186 fF	433 pH	186 fF	369 pH	84 fF
30 GHz	125 fF	377 pH	223 fF	417 pH	223 fF	377 pH	125 fF

Figure 10 shows the parasitic parameters at the input port of the SerDes receiver. The parasitic parameters of *PAD* and *ESD* are extracted based on Virtuoso post-layout

simulation from Cadence, and the parasitic inductance of the bonding wire is modeled as an ideal inductance fluctuating around 200 pH.

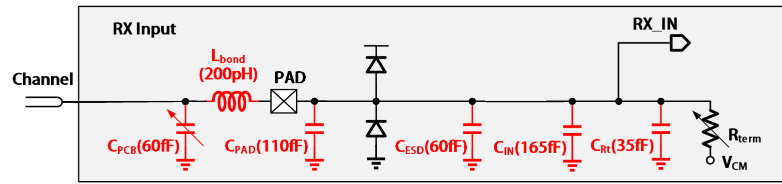

Figure 10. Parasitic parameters at the input port of the SerDes receiver.

When the total parasitic capacitance is fixed, as the order increases, the capacitance is divided into smaller parts. So the bandwidth of the matching network becomes larger. However, in our design, the input parasitic capacitance of the internal circuit is the largest and indivisible. This limits the achievable order. Therefore, we set the order of the matching network to 7, consisting of 3 inductors and 4 capacitors. According to the parameters of the Chebyshev I filter, we distribute the parasitic capacitance as shown in Figure 11.

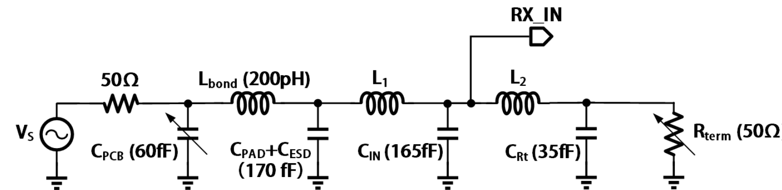

Figure 11. Parasitic capacitance distribution of the LC-π matching network.

Now there are two design freedoms of the LC-π matching network, including L_1 and L_2. Since the parasitic capacitance has been reasonably distributed, for a fixed L_{bond} value, the design of L_1 and L_2 can easily meet the required bandwidth. Thus, what we need to do is to find the least sensitive L_1, L_2 values to the change of L_{bond}. This process is accomplished through simulation and we ultimately chose L_1 to be 230 pH and L_2 to be 140 pH. We selected L_1 and L_2 to be the inductors provided in the PDK, and top metal M9 is used for their layout to minimize parasitic resistance. In the pre-layout simulation process, the Formula (3) can be used to calculate the inductance for octagonal inductors [29]:

$$L = \frac{1}{2}\mu n^2 \frac{(d_{in} + d_{out})}{2} \times 1.07 \times (\ln \frac{2.29}{\rho} + 0.19\rho^2) \tag{3}$$

where μ represents the vacuum permeability of 4×10^{-7} H/m, n represents the number of turns, d_{in} and d_{out} represent the inner and outer diameters of the inductor and ρ is defined as the filling factor of the inductor given by Formula (4):

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{4}$$

However, the PDK provides more accurate values. In the post-layout simulation, we will use electromagnetic field simulation tools to obtain more precise simulation results.

C_{PCB} can be controlled by the PCB designer, while R_t is often designed as an adjustable resistance array. Therefore, both of them can be considered as adjustable, which adds flexibility to the matching network. Next, we will demonstrate the benefits of utilizing these two flexibilities. Figure 12 shows the simulation result. It depicts that S11 will deteriorate at some frequencies when L_{bond} changes from 150 pH to 250 pH, but can be optimized if we adjust the values of C_{PCB} or R_t.

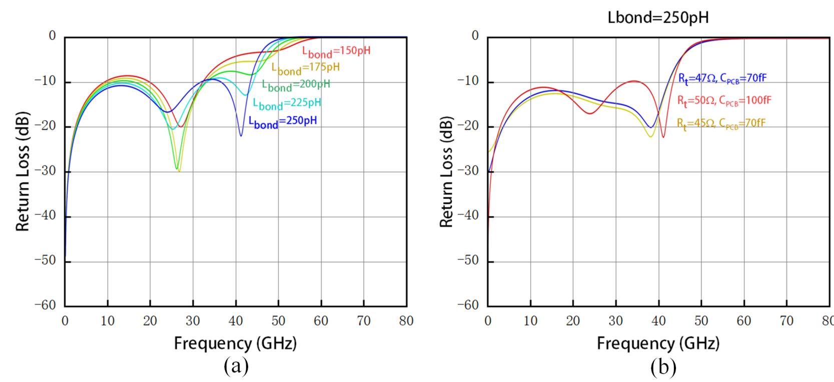

Figure 12. (**a**) Return loss responses with L_{bond} changing from 150 pH to 250 pH. (**b**) Return loss responses with different values of C_{PCB} and R_t.

However, it is worth mentioning that the adjustment of R_t should be probable, because it will change the gain of the matching network, as shown in Figure 13. If R_t decreases, the overall gain of the matching network will be reduced. This means that the swing of the signal received on C_{IN} will decrease, thus the height of the eye diagram will be reduced, so we should avoid setting R_t as too small.

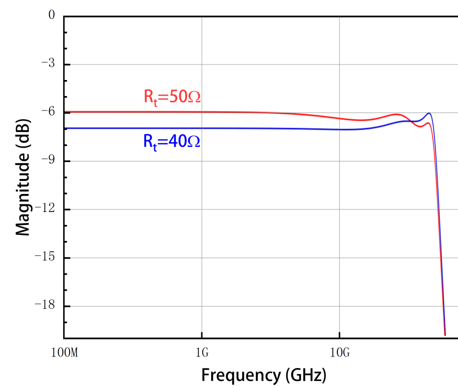

Figure 13. Magnitude responses of different R_t values.

Finally, in addition to optimizing the return loss, other characteristics of the matching network also need to be optimized. As considered in the design of the LC-π low-pass filter, the amplitude response of the matching network should be as flat as possible, and the group delay variations should be small in order to obtain the best eye diagram.

2.4. The Layout Design under Electromagnetic Field Simulation

The design of the layout should be carefully considered by electromagnetic field simulation [30]. Figure 14 shows the layout of the matching network, the signal on the *PCB* board will reach the *PAD* in chip through the bonding wire. Then, it comes to the *ESD* device, and connects to L_1 through a section of metal wire. Between L_1 and L_2 is the internal circuit of the receiver, while the other end of L_2 is connected to the R_t arrays. Next, the main parasitic effects in the layout will be analyzed.

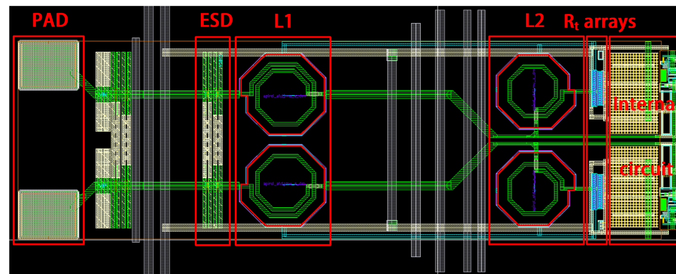

Figure 14. Layout of the LC-π matching network.

Due to the overall layout design of the SerDes receiver, there is a long distance between the *PAD* to L_1 and L_1 to L_2. These two metal wires are different from the wires of the internal circuits. As shown in Figure 15, wires in the internal layout are very dense, so there are only parasitic capacitors between adjacent wires and from wires to GND. Because the electromagnetic field generated by the internal metal wires will only form parallel plate capacitors with adjacent metal wires and GND. If there are no other metal wires around or very few wires, the electromagnetic field generated by the metal wires cannot form parallel plate capacitors. Instead, such a structure resembles a microstrip transmission line, and therefore, both parasitic inductance and parasitic capacitance exist. Based on our subsequent analysis, they will exhibit characteristics similar to inductors. So it is imprecise to extract only the parasitic capacitance of the layout [31].

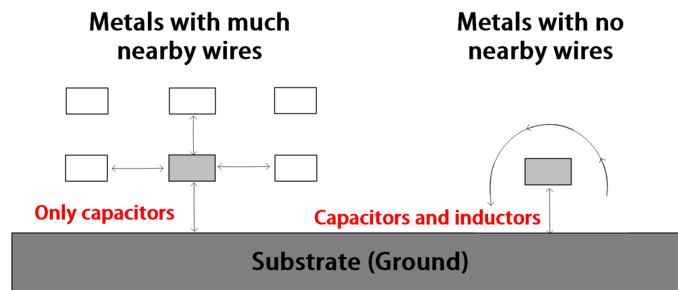

Figure 15. The characteristics of metal wires in different environments.

Figure 16 shows the electromagnetic field simulation results of a 300 µm × 9 µm M9 path by EMX. To better simulate the environment in the layout, we added ground wires and dummy metals around. The inductance is about 220 pH and Q in 20, which is close to the Q of a spiral inductor with the same inductance in PDK as shown in Figure 16. But their self-resonant frequency differs. This is because their parasitic capacitance is different. Overall, within the operating frequency range of this circuit, such lines in the layout should be treated as inductors in our design.

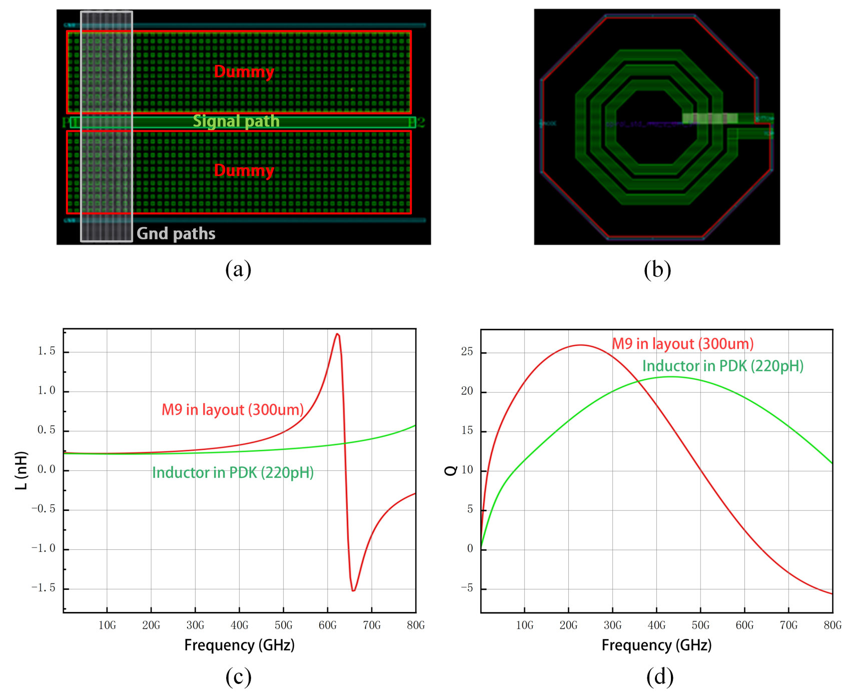

Figure 16. (**a**) A 300 µm × 9 µm M9 path. (**b**) A spiral inductor with the same inductance value in PDK. (**c**) L of the M9 path and the inductor in PDK. (**d**) Q of the M9 path and the inductor in PDK.

To investigate the influence of ground paths on the signal path, we compared the electromagnetic field simulation results of the M9 paths with different numbers of ground paths. Similar to the shielded ground in spiral inductors [32], these ground paths do not affect the inductance at low frequency, but increase the parasitic capacitance. The increase in parasitic capacitance is reflected as the decrease in the self-resonant frequency of the inductor, as shown in Figure 17.

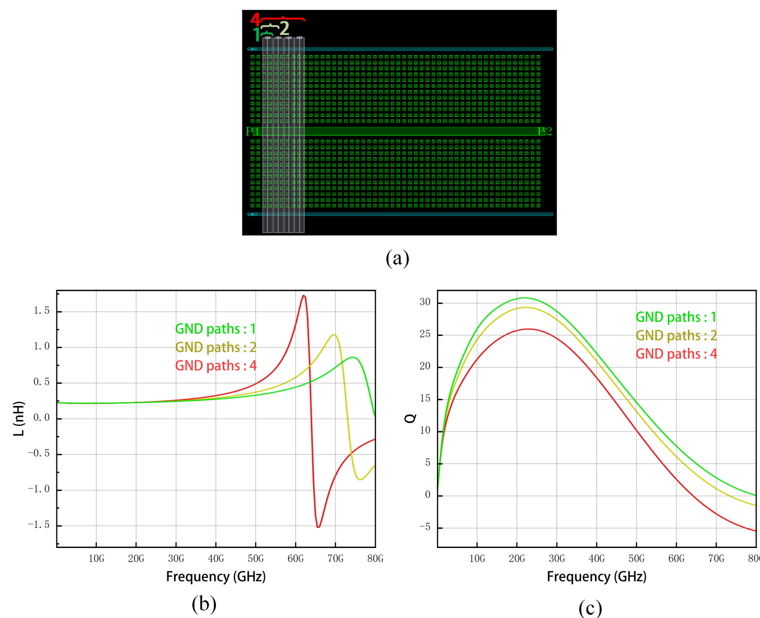

Figure 17. (**a**) Layout of the M9 path. (**b**) L of the M9 path with different numbers of ground paths. (**c**) Q of the M9 line with different numbers of ground paths.

After the layout design, dummy metals are added in blank areas for metal density requirements. As shown in Figure 18, we compared the influence of dummy metals by

electromagnetic field simulation. It shows that dummy metals can be neglected for design convenience without affecting the accuracy seriously [33]. Because the simulation results did not show significant changes after adding dummy metals, but the large number of dummy metals severely reduced the simulation speed.

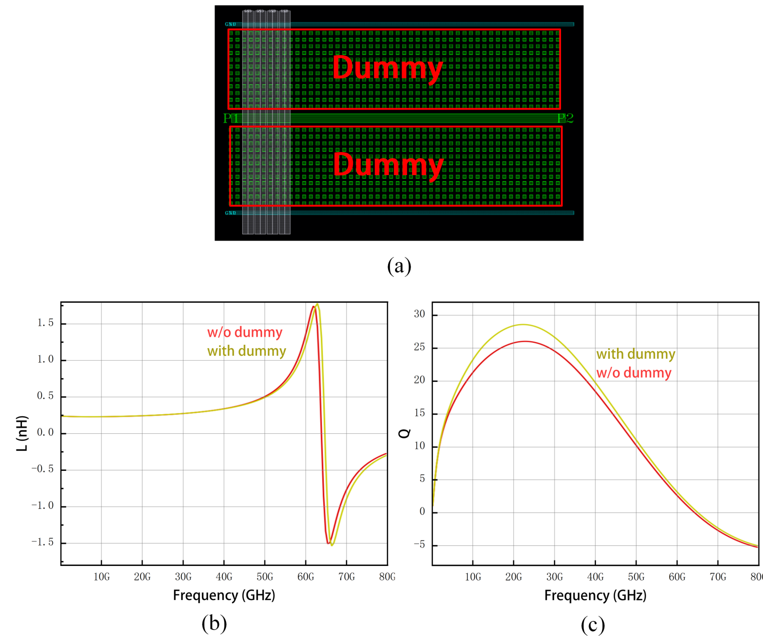

Figure 18. (**a**) Layout of the M9 path. (**b**) L of the M9 path with and without dummy metals. (**c**) Q of the M9 path with and without dummy metals.

When the final signal is connected to the internal circuit by a long metal wire, it could also lead to excessively long traces, thus adding parasitic inductance. By designing the distance between two differential signal path to be relatively close, the parasitic inductance will be greatly reduced. As shown in Figure 19, the differential signal produce negative mutual inductance, which reduces the parasitic inductance of each path.

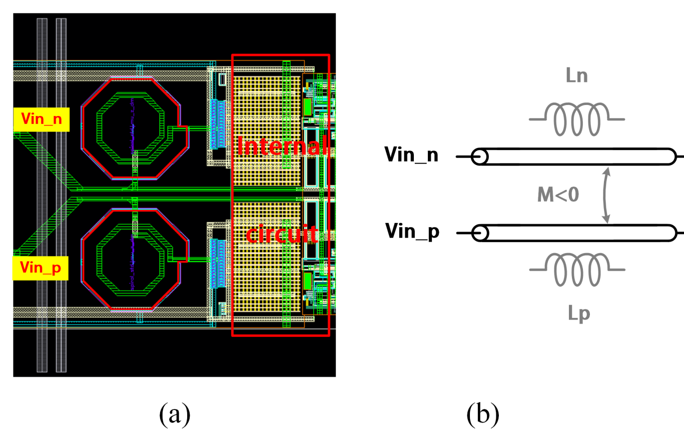

Figure 19. (**a**) Layout of the signal path to internal circuit. (**b**) Negative mutual between differential paths to reduce the parasitic inductance.

The values of L_1 and L_2 are then re-optimized based on the electromagnetic simulation results. In the electromagnetic simulation, we can block the area of L_1 and L_2 in the layout and extracted the s-parameter of the remaining part, as shown in Figure 20. This makes it easier to change the parameters of L_1 and L_2 externally while maintaining simulation accuracy.

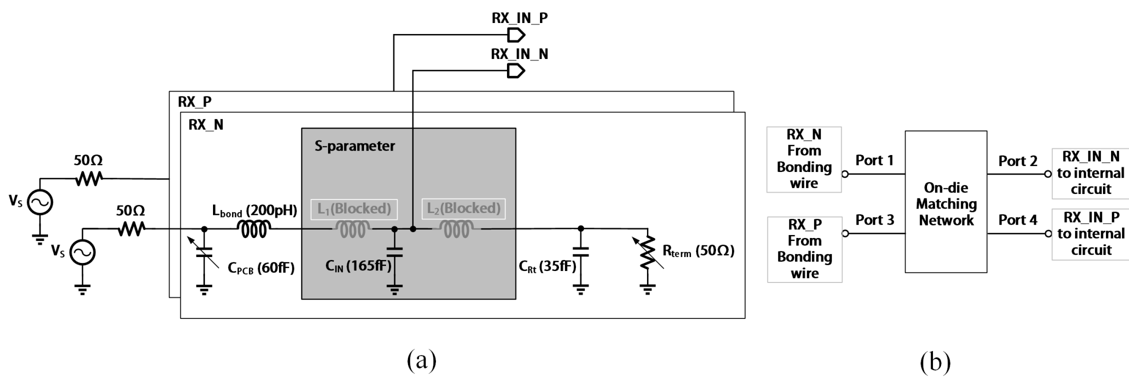

Figure 20. (**a**) S-parameter extraction method of the layout. (**b**) Return loss testing of the matching network.

It is worth noting that we used the coupling effects between differential signal paths to reduce the parasitic inductance, so differential characteristics of the return loss should be considered. The calculation for SDD_{11} is as Formula (5):

$$SDD_{11} = (S_{11} - S_{13} + S_{33} - S_{31})/2 \quad (5)$$

After iterative design based on electromagnetic field simulation results, we chose L_1 = 140 pH and L_2 = 150 pH for the best bandwidth and robustness performance.

3. Post-Layout Simulations Results

The proposed LC-π matching network was implemented in a 28 nm CMOS process with a total area of 580 µm × 220 µm (= 0.128 mm^2, without *PAD*). To ensure simulation accuracy, the simulation results were obtained by electromagnetic simulation of the entire matching network layout. Figure 21 shows the amplitude response and S11 results of the matching network at L_{bond} = 200 pH with default values of C_{PCB} and R_t. The 3 dB bandwidth of the matching network is 42 GHz, and the −10 dB bandwidth of S11 is 23 GHz.

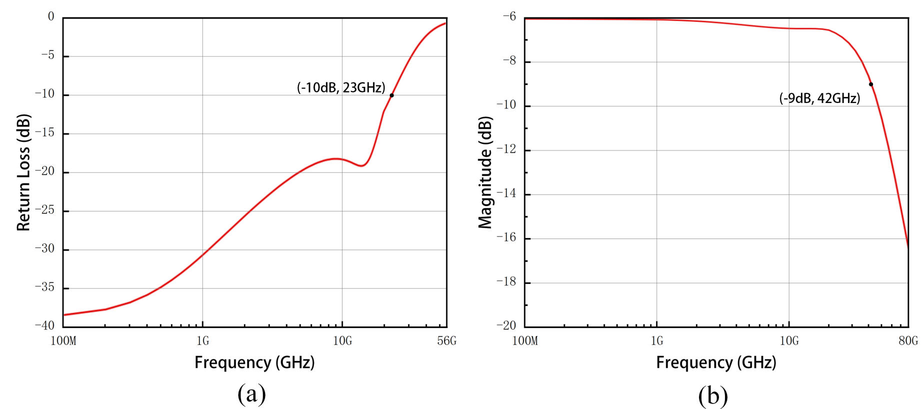

Figure 21. Response of the LC-π matching network with default values of C_{PCB} and R_t. (**a**) Return loss. (**b**) Magnitude.

As L_{bond} variates from 150 pH to 250 pH, we can obtain the best matching network by optimized values of C_{PCB} and R_t, listed in Table 4. These values were obtained through parameter sweeps to maximize the bandwidth of the matching network. Figure 22 shows the optimized results of different L_{bond} values about their amplitude response and S11 results and Figure 23 shows the eye diagrams. It depicts that the matching network can tolerate L_{bond} variation from 150 pH to 250 pH and always meets the transmission requirements of CEI-112G-XSR-PAM4 Extra Short Reach Interface. In addition, the time-domain simulation results also exhibit clear eye diagrams.

Table 4. Optimized values of C_{PCB} and R_t for different L_{bond} values.

L_{bond}	C_{PCB}	C_{Rt}
150 pH	50 fF	50 Ω
175 pH	80 fF	48 Ω
200 pH	60 fF	46 Ω
225 pH	70 fF	49 Ω
250 pH	80 fF	47 Ω

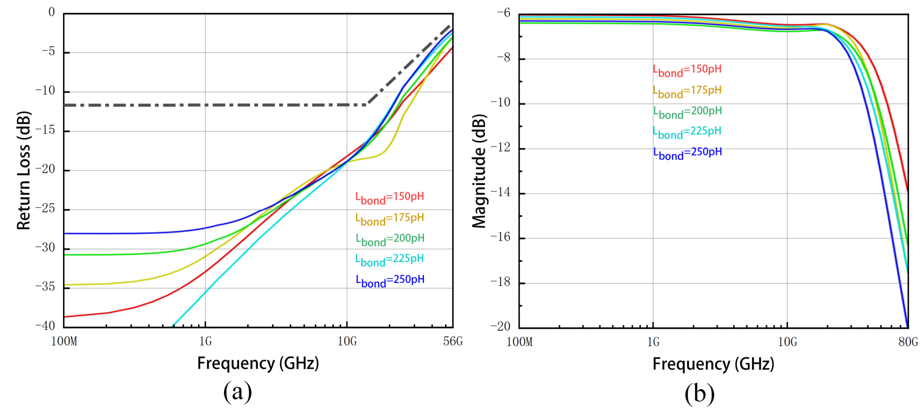

Figure 22. Optimized responses of different L_{bond} values. (**a**) Return loss. (**b**) Magnitude.

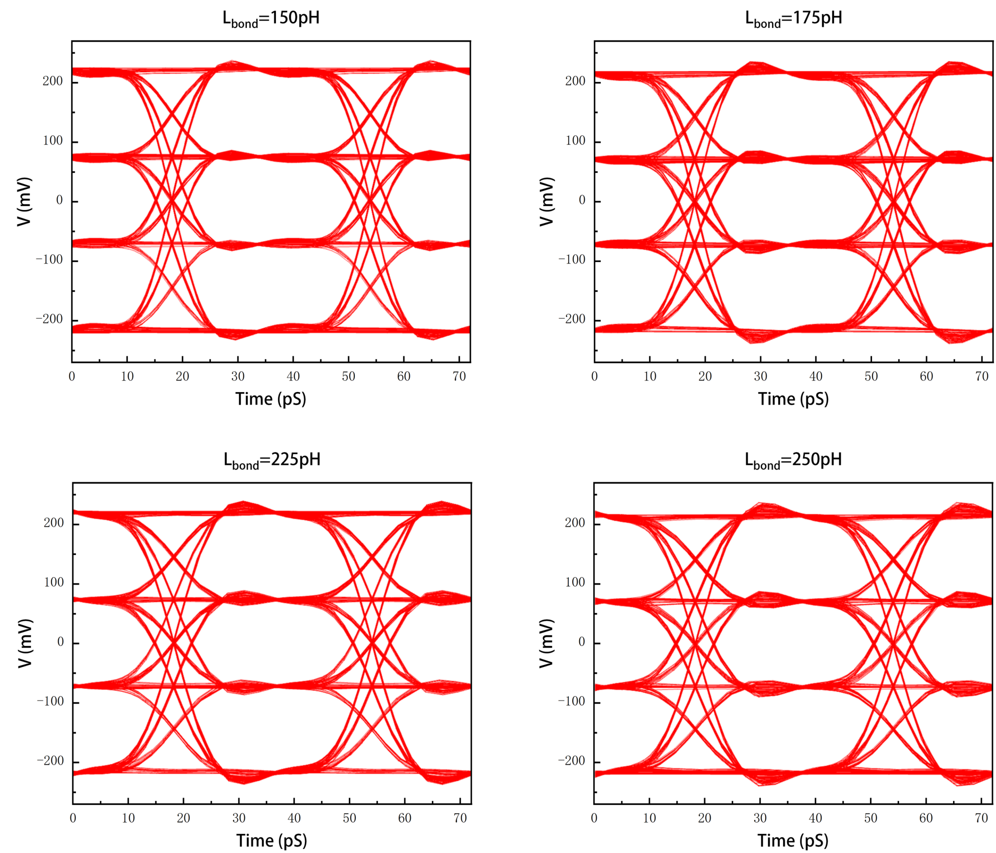

Figure 23. Eye diagrams of optimized LC-π matching networks with different L_{bond} values.

Table 5 provides a comparison between this work and some published broadband matching networks for SerDes transceiver. It can be confirmed that the LC-π matching network achieves higher data rates compared to other broadband matching techniques. Moreover, in our design, incorporating the parasitic inductance of the bonding wires as

part of the LC-π matching network extends the achievable bandwidth and reduces the design pressure of the equalization circuit.

Table 5. Comparison between this work and some published broadband matching networks for SerDes transceiver.

	This Work	[9]	[14]	[16]	[6]
Technology	28 nm	40 nm	16 nm	65 nm	10 nm
Data Rate [Gb/s]	112	56	40–64	50–64	224
Signaling	PAM4	NRZ/PAM4	NRZ	NRZ	PAM4
Matching Network	LC-π	Inductive Peaking	T-coil	LC-π	LC-π
Number of inductors	2 + 1 [1]	1	1 [2]	4	4
Area [mm^2]	0.128	-	-	-	-
Bonding Wire Consideration	Yes	No	No	No	No

[1] Two on-chip inductors and one bonding wire inductor. [2] Two coupled inductors behave as one tapped inductor.

4. Conclusions

We presented the analysis, design details, and simulation results of an impedance matching network designed for a 112 Gb/s PAM4 receiver using an LC-π structure. The proposed LC-π network designed the bonding wire as a part of the matching network, which reduced the design pressure on the equalizer, as there will be no need to compensate for the loss of the chip package. To avoid robustness issues caused by the fluctuation of the bonding wire inductance, the matching network is designed to be adjustable by the capacitance on *PCB* and the terminal resistance. We analyzed the parasitics in the layout and the influence of nearby and dummy metals and obtained reliable simulation results through electromagnetic field simulation. This matching network is designed with a 28 nm CMOS process. Simulation results show that with bonding wire inductance changing from 150 pH to 250 pH, it can always meet CEI-112G-XSR-PAM4 Extra Short Reach Interface requirements. In addition, the time-domain simulation results also exhibited clear eye diagrams.

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