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Advanced Thermal Control Using Chip Cooling Laminate Chip (CCLC) with Finite Element Method for System-in-Package (SiP) Technology

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Abstract: This paper introduces a novel approach to address thermal management challenges in system-in-package (SiP) technology, which is a significant concern in various advanced technologies. The main objective is to assess the electrical and thermal performance of the SiP model by utilizing Chip Cooling Laminate Chip (CCLC) technology. To achieve this, we employed finite element method (FEM) analysis using COMSOL Multiphysics® and MATLAB® to compare the results of electrical and thermal SiP models with and without CCLC technology. The numerical simulations revealed that, as opposed to the traditional model, the temperature variation decreased significantly with a uniform temperature distribution when employing the CCLC technology. Additionally, the thermal conduction performance of the packaging system using CCLC demonstrated remarkable reliability and resolution with cost-effective micro-devices, particularly in micro-medicine applications. The analysis of the electrical and thermal models reported a maximum error between them of 1.15 °C.

Keywords: chip cooling laminate chip (CCLC); finite element method (FEM); system-in-package (SiP)

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1. Introduction

Currently, it is feasible to manufacture more than 100 million transistors on a single semiconductor die, and the cost per transistor is continuously decreasing. Additionally, the semiconductor industry is now generating an annual output of transistors that equals or surpasses the cumulative total of transistors produced in all previous years [1,2]. However, the primary challenge today is not about how many transistors can be incorporated on a single chip; instead, it is about how to integrate a wide range of diverse technologies in a predictable and cost-effective manner. This is where System-in-Package (SiP), an extension of the System-on-Chip (SoC) concept, offers a solution by overcoming significant integration obstacles while allowing for optimization of individual chip technologies [3–5]. By preserving the on-chip electrical environment, SiP offers better performance with lower cost compared to SoC. As a result, it is essential to perceive SiP (System-in-Package) as a substantially integrated circuit rather than merely a downsized circuit board.

As integrated circuit (IC) fabrication technology continues to advance and the feature size approaches 90 nm, there is a growing divergence between dynamic random access memory (DRAM) technology and logic technology, despite both being based on complementary metal oxide semiconductor (CMOS) technology [6]. The utilization of embedded DRAM is hindered by its high fabrication complexity and low yield, making it an impractical and cost-ineffective solution [7,8]. An alternative solution is memory/logic integration based on SiP technology. In contrast to the System-on-Chip (SoC) approach,

which requires compromises in chip fabrication technologies, the System-in-Package (SiP) approach maximizes the potential of integrated circuit (IC) technology. It achieves this by seamlessly integrating conventional application-specific integrated circuits (ASIC) and memory technologies by using existing ICs that have been individually optimized. This approach allows for the integration of memory and logic at a reduced cost and smaller form factor while maintaining comparable performance to that of SoC designs.

System-in-package (SiP) technology entails the integration of multiple chips on a commonly used 2D or 3D substrate, creating a compact system. It offers an excellent solution for combining diverse manufacturing technologies and integrating multiple devices when meeting all requirements on a single die becomes challenging or expensive. However, as packing densities increase, effectively managing heat dissipation between SiP chips and addressing the self-heating of individual chips becomes vital. This is crucial due to the adverse effects high temperatures can have on performance and reliability [9–12]. Therefore, researchers and electronic developers have turned their attention to thermal management problems in SiP implementations.

The prevalent method for constructing SiPs is through stacked chips, which eliminates the need for additional chip layout design processes. However, this stacked construction poses challenges when seeking superior heat efficiency compared to traditional designs due to its lower heat conductivity. Advancements have been made in SiP technology to tackle this limitation. In a CCLC module, a thin film serves as a substrate, wiring resource, and decoupling capacitor for the power source. The chips are soldered to both sides of the laminate, which allows heat dissipation through the top and bottom of the package. Moreover, CCLC provides better electrical and thermal performance compared to Chip-on-Chip (CoC) technology [13,14].

The proposed SiP model with CCLC technology was modeled with the COMSOL tool. COMSOL Multiphysics® is a modular finite element numerical computation tool allowing modeling of a wide variety of multi-physics phenomena to characterize a real problem. It represents a design tool as well, thanks to the ability to manage complex 2D and 3D geometries and to the different physical modules in COMSOL Multiphysics®, among are fluid mechanics, heat transfer, electricity, electromagnetism, chemistry, structural mechanics, etc. It is possible to combine several physical phenomena in the same numerical simulation, which is one of the strong points of this tool.

Thermal management of SiPs is a crucial aspect of the design and manufacture of these advanced electronic packages [15–18]. Efficient thermal dissipation, optimized thermal design, use of suitable thermal materials, accurate thermal simulations, and, if necessary, advanced cooling systems are all important elements of SiP thermal management to ensure stable and reliable performance.

The CCLC method is a new technology used in SiP and reflects several aspects, such as efficiency, precision, and integration; it has a number of advantages:

(i) Improved heat dissipation: the CCLC method provides more efficient heat dissipation compared to traditional cooling methods. It uses a thin film to transfer the heat generated by the components, allowing for more efficient heat dissipation and better temperature control.
(ii) Hot Spot Reduction: the CCLC method helps to reduce hot spots, which are high-temperature areas on the SiP. By directly cooling the chips and effectively removing the generated heat, it helps to maintain more consistent temperatures throughout the SiP, thereby reducing the risk of overheating and thermal stress.
(iii) Improved power density: SiPs combine multiple components and features into a single package, leading to increased power density. The CCLC method effectively manages this high power density by rapidly removing heat generated by the components, helping to maintain reliable performance and avoiding heat-related problems.
(iv) Design Flexibility: CCLC technology provides greater design flexibility for SiPs. Because heat dissipation is managed by a cooling system, designers can have more

freedom in arranging components and tracks without being limited to the strict thermal constraints of traditional cooling methods.

(v) Size and Weight Reduction: by enabling better heat dissipation, the CCLC method can reduce the need for heat sinks and other cooling devices, which helps reduce the overall size and weight of the SiP. This is particularly beneficial for applications where space and weight are critical factors, such as portable devices or compact embedded systems.

The CCLC method offers improved thermal dissipation, reduces hot spots, handles high power density well, allows greater design flexibility, and reduces the size and weight of SiPs. These advantages make it a promising technology for applications requiring efficient thermal management and high performance.

In the field of microelectronics, the issue of thermal control and management is widely acknowledged. While significant efforts and efficient models have been proposed for reducing the negative impact of self-heating on circuit operation in SoC, there is currently no effective solution proposed for SiPs [19,20]. Furthermore, heat removal remains a challenging problem for SiP designers. In [20], several techniques for the thermal management of electronic devices were presented. However, these techniques mainly focus on developing solutions suitable for steady-state operations. In addition, according to [21] SoCs are increasingly used in applications involving time-varying workloads. This is partly due to the detailed thermal management solutions proposed to ensure their performance and reliability [22–24].

The objective of designers is to integrate memory and logic in mixed-signal and digital applications as well as to integrate passive components with active circuitry in the final system-in-package (SiP). To ensure optimal performance, temperature monitoring is crucial throughout the operation of the SiP. Unfortunately, merging any of these technologies can compromise each of them and increase the complexity of thermal management. This negatively impacts the time-to-market of new products, especially memory cells, which would cost more to manufacture with integrated dynamic random access memory (DRAM). By combining several levels of memory in a stack, a multi-layer memory combination can be realized, as shown in Figure 1 below.

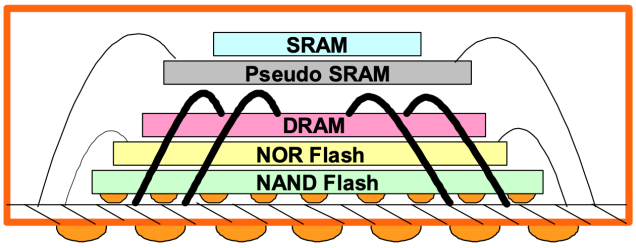

Figure 1. Multiple memories stacking in SiP.

Several technologies have been proposed for the creation of system-in-package (SiP) modules, with the stacked-chip SiP technology the most commonly employed. This method eliminates the need for any additional design processes during chip design, making it a popular choice in SiP development. However, it has a number of limitations. For example, the bonding wires used in this technology have lower electrical properties, including high parasitic inductance. Additionally, the stacked structure leads to subpar thermal heat conductivity. Therefore, achieving improved electrical or thermal performance is challenging compared to traditional designs. To overcome these issues, Chip-on-Chip SiP technology (CoC) has been proposed in multiple studies [25,26].

CoC has introduced an innovative module called FPGA/DRAM SiP designed to enhance memory access by combining a high-capacity FPGA and multi-bank DRAM within a single package. This integration is facilitated through solder bumping and flip-chip assembly techniques, enabling the incorporation of diverse chips with reduced interconnection lengths and increased IO densities. However, an important limitation of CoC is that it

can only be utilized when the substrate chip has sufficient size to accommodate all other chips. To address this issue, CCLC technology was introduced in [27,28]. CCLC technology employs a thin film laminate that serves multiple functions as a package substrate, wiring resource, and decoupling capacitor for the power source. The chips are solder-bumped on both sides of the laminate, enabling heat dissipation from both the top and bottom of the package. Consequently, CCLC technology delivers superior electrical and thermal performance compared to CoC solutions.

Our contributions in this paper are as follows: (1) we analyze the thermal process in SiP with and without CCLC technology using the finite element method (FEM) in COMSOL Multiphysics®; (2) we study the electrical performance of the resulting SiP with MATLAB®; and (3) we conduct a comparison study between the electrical and thermal models presented in this paper in order to prove their performance advantages over conventional SiP technologies.

This article proposes an innovative method to manage heat in system-in-package (SiP) technology. This is a critical design concern in many advanced technologies.

The remainder of the paper is organized as follows. In Section 2, we present the electrical performance analysis of the proposed CCLC-based SiP. In Section 3, the thermal performance of the CCLC-based SiP is examined by developing a thermal model and simulating it using COMSOL Multiphysics®. Finally, Section 4 concludes the paper with our closing remarks.

2. Electrical Performance Analysis of CCLC-Based SiP

2.1. CCLC Technology

The focus of this paper is on the concept of a complex material package, which operates under the assumption that heat transfer primarily transpires through heat conduction between individual dies. The dissipated heat generated by power is directed along a thermal path, enabling the efficient flow of energy within the system. While the development of thermal paths has been widely explored in diverse industries, such as air cooling and water cooling, IC (integrated circuit) packaging poses distinctive challenges due to its compact size, high power distribution, dense wiring, and limited accessibility. Therefore, this study proposes a schematic design that can address the specific requirements of a multi-chip module (MCM) by ensuring more effective and accurate thermal management.

The objective of this study is to propose a thermoconductive path that connects two arrays. This path incorporates a thermally conductive material that is joined to the support structure through ribbons along the flat and thin edges. The backing material plays a crucial role in efficiently conducting thermal energy away from the housing. This research explores two types of components: a thread connection, and a hybrid configuration combining thread and flip-chip connections. Figure 2 illustrates the schematic of a Chip Cooling Laminate Chip (CCLC) solution demonstrating the implementation of multiple layers of stacked chip packages.

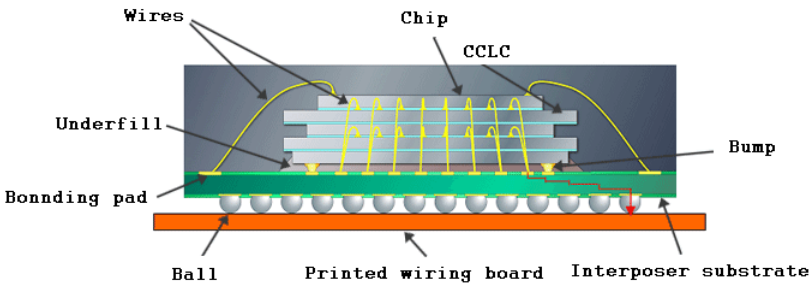

Figure 2. Layers of stacked chips.

Industry is interested in the SiP configuration due to its advantages in terms of component integration, improved performance, reduced power consumption, cost reduction,

and design flexibility. SiP offers an efficient approach to meet the increasing demands for more compact, powerful, and energy-efficient electronic systems.

Figure 3 depicts a thermal conduction layer sample comprising a thin film or foil with high thermal conductivity of 384.1 W/m·K.

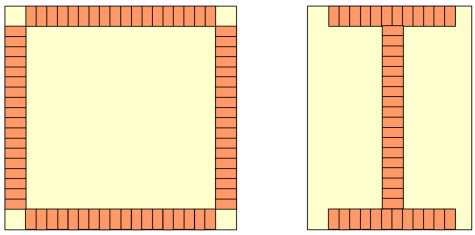

Figure 3. CCLC technology sample model.

In the CCLC technology module, the laminate is part of the packaging shown in Figure 2, while the upper and lower chips consist of a flip-chip mounted on the laminate. The decoupling capacitors are integrated, resulting in a better power-to-ground structure in comparison with the CoC architecture. Among the features of the CCLC package are:

- Maximum off-chip delay;
- Signal round-trip time < rise time (500 ps);
- Inter-chip skew < board skew (500 ps);
- No termination resistor required;
- Smaller buffer size and minimized ESD protection.

When logic and memory chips are assembled with the CLC, they are electrically considered CCLCs, and are on the same chip electrically even if they are physically manufactured on different chips.

The substrate takes the shape depicted in the illustration, with the dies securely bonded to the central frame and irregularly shaped bands that conform to the electrical bond's unique contours. A conductive heat pattern is applied to the substrate, facilitating swift dissipation of the heat produced by the dies. The efficient dissipation of heat minimizes the thermal stress experienced by both the bonding and die layers, leading to a notable reduction in issues such as layer delamination, die failure, electrical connection failure, and other potential defects.

In addition to resolving the thermal conductivity issue, this approach entails a more intricate and multi-step chip bonding and stacking process, resulting in a greater stacking thickness due to the larger package size resulting from the thermal conduction liner. Despite these drawbacks, the technique's effectiveness in dissipating heat and reducing temperature strain makes it advantageous. This is particularly true in light of the growing demand for greater reliability and more stringent temperature monitoring [29].

The presented plan involves incorporating a thermal dissipation element; its focus is not on establishing a specific thermal conductivity pattern, however. The reasoning behind this is informed by the proposed approach depicted in Figure 4.

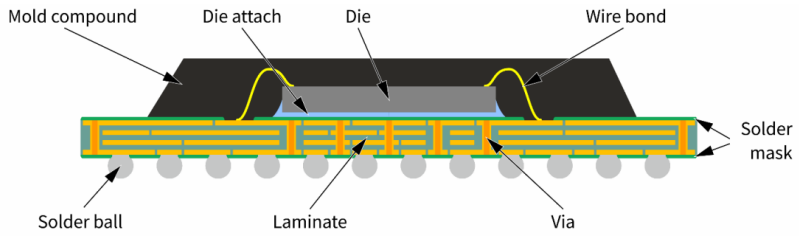

Figure 4. Integration of the laminated chip technology.

The use of laminated chip technology offers significant packaging advantages for MCMs that consist solely of chips.

Figure 5 shows an example of an integration module that can help in understanding Equations (1) through (6) in the next section.

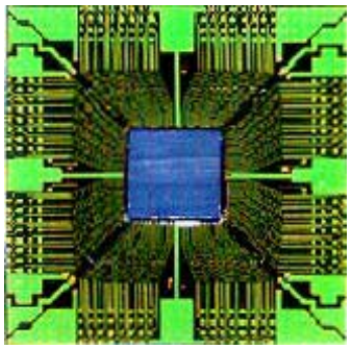

Figure 5. The integration module implemented by CCLC technology.

This tighter integration provides more memory access bandwidth than onboard graphics memory while requiring little overhead.

2.2. Modeling and RLC Equivalent Circuit

In this section, our objective is to analyze the electrical characteristics of the SiP based on CCLC technology. We accomplish this by modeling the circuit depicted in Figure 3 to evaluate the SiP's performance. By approximating the resistances (R), inductances (L), and capacitances (C) of the rerouted metal and solder bumps, we obtain an equivalent circuit. The pad primarily serves as a capacitive load for the output driver. We can easily calculate the capacitance of the pad as a load for the output driver using the approximate Formula (1) mentioned in [30]:

$$C_{pad} = \varepsilon_{ox} \left[1.15 \frac{A_{pad}}{H} + 1.4 \left(\frac{T}{H}\right)^{0.222} P_{pad} \right] \quad (1)$$

The variables used in the equation are as follows: A_{pad} represents the area of the bonding pad, P_{pad} represents the perimeter of the bonding pad, H represents the height of the bonding pad with respect to the conductive silicon substrate, and T represents the thickness of the metallization layer on the bonding pad.

The reason that the coupling capacitance for rerouting wires can be disregarded is due to the typically spacious gaps between them. Therefore, the wire capacitance can be calculated using the formula described in [30]:

$$C_{reroute} = \varepsilon_{ox} \left[\frac{W}{1.15H} + 2.8 \left(\frac{T}{H}\right)^{0.222} \right] \times W_{reroute} \quad (2)$$

The length of the rerouting wire, denoted as $W_{reroute}$, can be calculated using an equation that considers the width of the wire (W), the height of the rerouting layer above the conductive silicon substrate (H), and the thickness of the rerouting material (T).

Assuming the center of the chip as the origin, the chip has dimensions $M \times N$, and the solder pitch size is P. If we denote the location of the solder as (x, y) and it is positioned in the upper-right quarter of the chip, we can proceed with the calculations. In such a case, we can determine the length of the wire using the following Formula (3):

$$W_{reroute} = min \left(\frac{M}{2} - x, \frac{N}{2} - y \right) + \alpha P \quad (3)$$

where α is a parameter dependent on the chip geometry. To make estimating the equivalent resistance more straightforward, we make the assumption that the rerouting interconnects can be treated as a single metal line. This is a reasonable assumption, as rerouting typically

involves either no change or only one change of the routing layer as long as there are sufficient routing resources available.

$$R_{reroute} = \rho \frac{W_{reroute}}{W \times T} \tag{4}$$

The equation involves the use of several variables. The variable ρ represents the resistivity of the metal line, while W represents the width of the interconnect and T represents the thickness of the metal layer. Additionally, we can model the solder as a cylindrical conductor. To estimate its resistance, we can employ the following Formula (5):

$$R_{solder} = \rho_{solder} \frac{4H_{solder}}{\pi D^2}. \tag{5}$$

To calculate the resistance of the solder, Formula (5) considers the resistivity of the solder material, denoted as ρ_{solder}, along with the solder's height H_{solder} and diameter D. These parameters are used to estimate the resistance value. The capacity of the weld joint can be calculated from Equation (1) and deduced as follows:

$$C_{solder} = \varepsilon_{laminate} \left[1.15 \frac{\pi D^2}{4H_{sl}} + 1.4 \left(\frac{H_{solder}}{H_{sl}} \right)^{0.222} \pi D \right]. \tag{6}$$

In addition, each solder bump underneath contributes approximately 0.5 nH inductance [31]. Therefore, we have the equivalent RLC listed in Table 1.

Table 1. The values of RLC in the equivalent circuit of the CCLC technology.

	R (Ohms)	L (nH)	C (pF)
Pad	1.28	0.5	0.362
Wire	2.98	0.5	0.377
Solder	3.46	0.5	0.0317

By adopting chip stacking the need for extra rerouting layers is eliminated, resulting in cost savings and reduced design complexity. However, the introduction of bond wires in the stacked configuration leads to significant inductance, which imposes limitations on its application in the high-frequency domain. In our analysis, we model the bond wire as a copper line with a diameter of 25 µm and length of 3 mm.

The equivalent circuits of the I/O path with and without CCLC are shown in Figure 6.

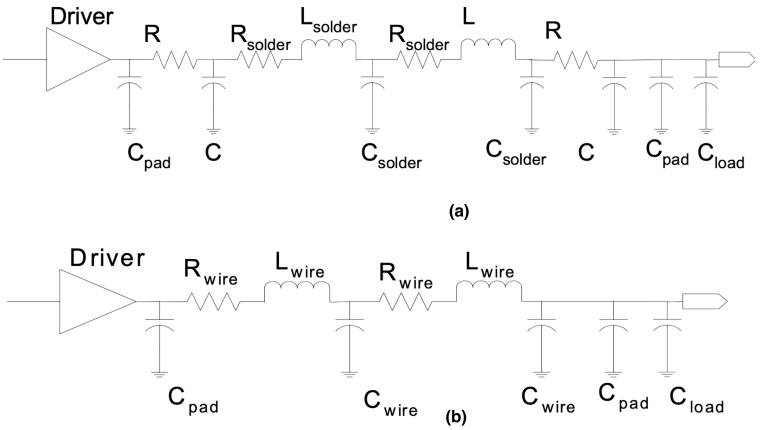

Figure 6. RLC equivalent circuit for (**a**) with CCLC technology and (**b**) without CCLC technology.

The Simulink model based on the RLC circuit uses Equations from (1)–(6) to describe the circuit's behavior. The steps for building and simulating a Simulink model for an RLC circuit are as follows:

1. Model construction: in Simulink, we used function blocks to represent RLC circuit components such as the resistors, inductors, and capacitors and used lines to represent electrical connections.
2. Component parameterization: we specified the values of RLC circuit components such as the resistors, inductors, and capacitors as shown in Table 1. These parameters were configured in the corresponding blocks of the Simulink model.
3. Adding signal sources: a signal source was added to power the RLC circuit.
4. Simulation: the simulation was run after building and configuring the Simulink model of the RLC circuit. Simulink uses the appropriate mathematical equations to solve the behavior of the RLC circuit as a function of the defined parameters, signal sources, and initial conditions.
5. Analyzing the results: after the simulation, we analyzed the results shown in Figure 6 to understand the behavior of the RLC circuit.

The obtained thermal results are presented in the next section covering the RLC circuit analysis.

2.3. Result of the Simulation of RLC Equivalent Circuit

We simulated the above circuits (Figure 6) using MATLAB®. The objective was to analyze the thermal performance of the CCLC technology using the equivalent RLC circuits. Figure 7 illustrates the results of the thermal simulation.

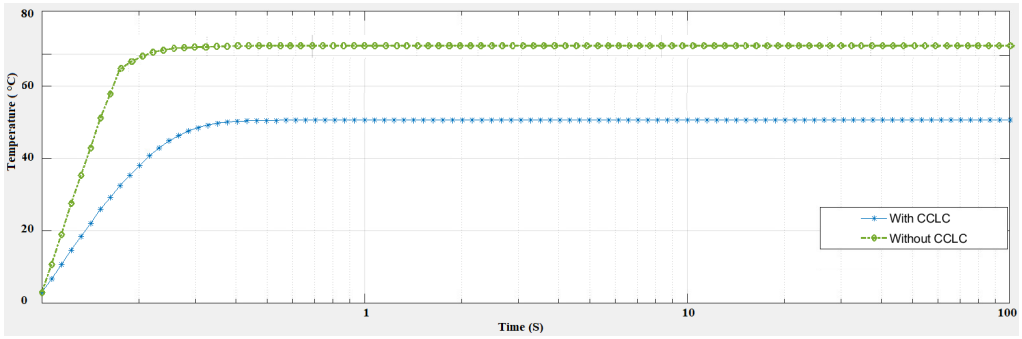

Figure 7. Maximum temperature generated with and without CCLC technology.

After analysis of the results reported in Figure 7, the maximum value of the temperature without CCLC technology was 71.85 °C and the maximum value with CCLC technology was 43.85 °C. Thus, we can deduce that the use of CCLC technology allows the global temperature to be reduced, which aids in the thermal management of SiPs.

The temperature can evolve in different ways depending on many factors, such as the thermal properties of the CCLC technology and the heat sources presented by the RLC circuit. Among the reasons that the temperature can be stable over less than a second and continue to rise after 20 s are:

1. The RLC circuit quickly reaches a state of thermal equilibrium with its surroundings, and the temperature can stabilize in less than a second. This can happen when the R, L, and C components rapidly exchange heat with their surroundings and reach a balanced temperature.
2. When the RLC circuit is subjected to continuous heat sources, the temperature may continue to rise even after 20 s. In this case, the constant heat input outweighs the heat loss, resulting in a continuous rise in temperature.
3. The values of the RLC equivalent circuit shown in Table 1 can influence heat propagation and thermal response, leading to rapid stabilization followed by a continuous rise in temperature.

In order to validate our thermal model, in the next section we present temperature simulations carried out in COMSOL Multiphysics® based on the finite element method and compare them to the maximum temperature values obtained with the MATLAB® tool.

3. Heat Analysis of SiPs Based on CCLC

As mentioned above, a series of numerical models were simulated in COMSOL Multiphysics® using FEM [32–34]. Figures 8 and 9 depict these numerical models, while Figures 10 and 11 show the temperature distribution results obtained from the simulations. In the traditional die-layered approach, there exists an adhesive layer and an electrical conductivity layer positioned between the two dies. However, the thermal conductivity of this layer is often disregarded due to its narrowness and the focus on its electrical conductance within the bonding lane [35,36]. However, the junction layer, despite its narrowness, possesses significant heat conductivity [37,38], making it one of the crucial factors affecting heat distribution. Table 2 lists the parameters used in the model.

Table 2. The measurable attributes of important materials present in the simulated SiP in terms of their physical properties.

	Substrate	**Dies**	**Conductivity**
Materials	Ceramic	Si	Copper
Depth (um)	1000	100	50
Surface Size (mm^2)	30×30	10×10	10×10
Thermal Conduction (W/m·K)	1.49	0.75	390
Thermal Capability (J/Kg·K)	877.96	834.61	390
Thermal Expand Modules (K^{-1})	1.08×10^{-5}	9×10^{-6}	2.4×10^{-4}
Ratio of Poisson (NA)	0.22	0.23	0.37

In the illustrated model (Figure 8), the top surface temperature of each die is considered separately, with values of 5, 10, and 10 Watts for both the upward and downward directions. The bottom surface of the substrate is assumed to have a temperature of 25 °C. This configuration involves stacked dies bonded together with a glue layer, represented by the blue region, while the array of chips deposited on the substrate is depicted in silver. The model depicted in Figure 8 showcases the Chip Cooling Laminate Chip (CCLC) arrangement simulated using the COMSOL tool.

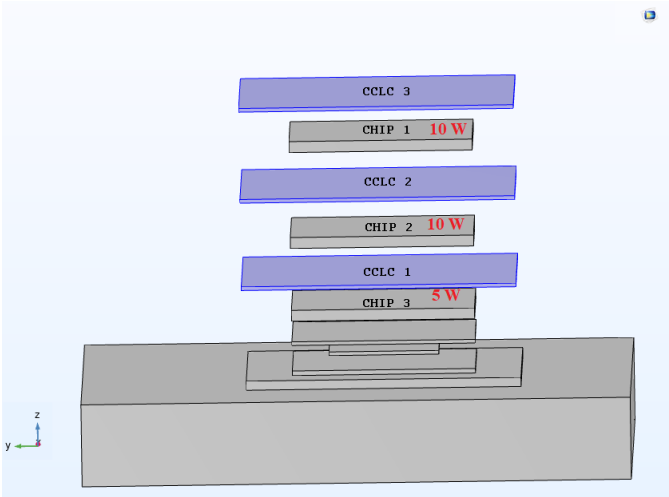

Figure 8. CCLC technology modeled with COMSOL.

Heat transfer solvers play a crucial role in predicting the temperature of circuits and systems. These software programs are equipped with heat transfer codes that help to identify any issues with compliance. The results generated from the heat transfer analysis can provide a visualization of the temperature distribution and detect whether there are any instances in which the operational limits are exceeded, especially in system-in-package (SiP) setups. The heat transfer results obtained from the simulations enable designers to

assess the effectiveness of the current design and determine whether optimization is necessary. By employing numerical solvers, various thermomechanical phenomena, including temperature distribution, the average temperature of heated surfaces, and pressure drop effects, can be analyzed.

In order to confirm that the thermal results obtained are stable, we can run simulations with a normal triangle mesh and a denser triangle mesh. Appropriate meshing is essential to obtain a stable and robust solution, as in the case of the normal triangles used in Figure 12 to represent the geometry. Figure 12 depicts the denser triangle mesh geometry of the CCLC concept studied and modeled using COMSOL Multiphysics®.

Results obtained from the denser triangle mesh can be easier to interpret, as they provide a more detailed representation of the thermal phenomenon under study. This can lead to a better understanding of local characteristics and fixed boundary conditions.

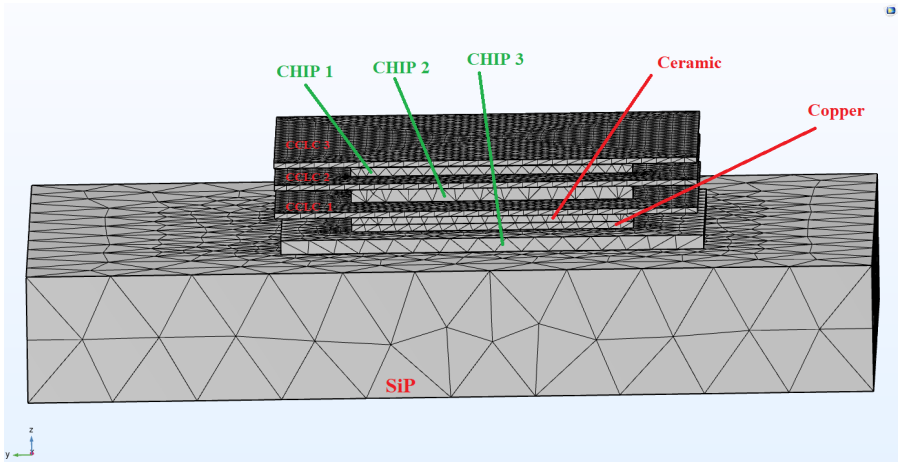

Figure 9. Normal triangle mesh geometry of the model studied in COMSOL Multiphysics®.

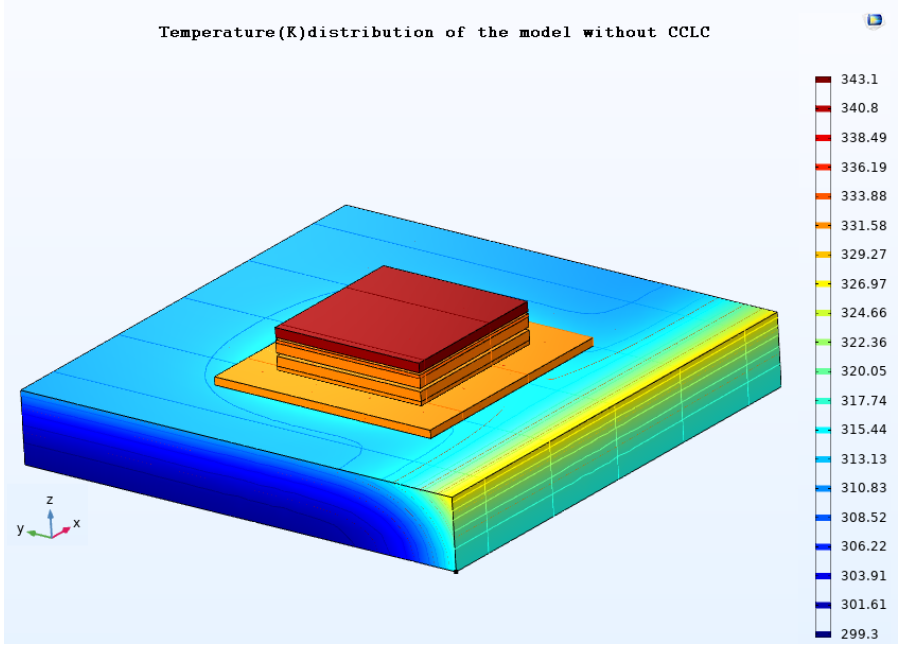

Figure 10. Model thermal results without CCLC.

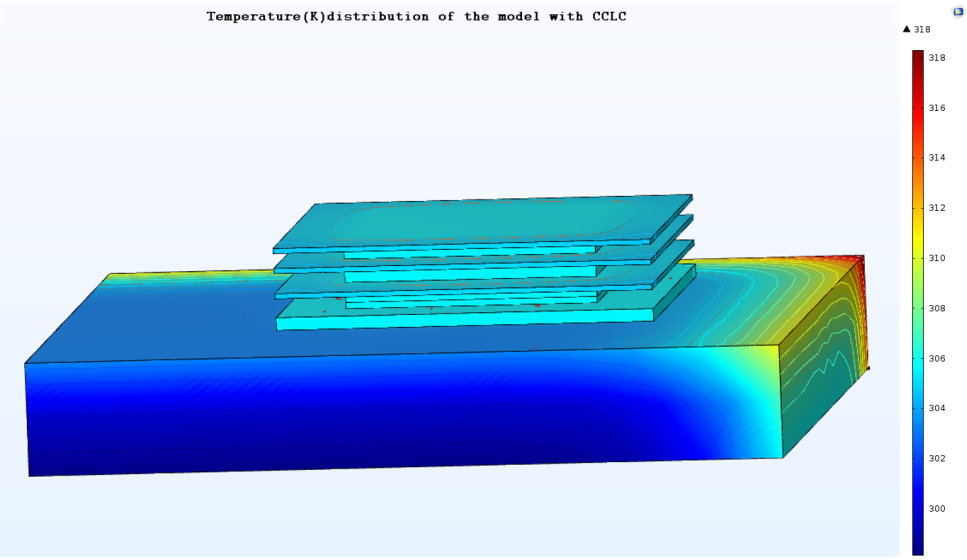

Figure 11. Model results with CCLC.

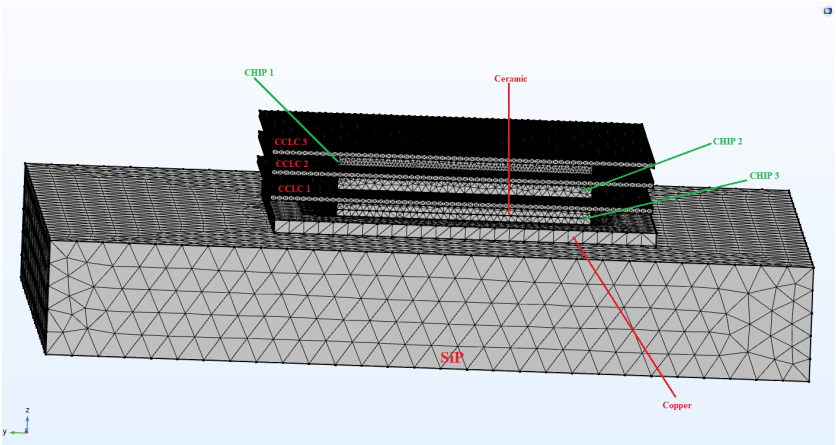

Figure 12. Denser triangle geometry of the model studied in COMSOL Multiphysics®.

In our study, we used the COMSOL Multiphysics® tool to generate heat maps for models with and without CCLC technology. Initially, we assumed an even temperature distribution over the entire structure with a denser triangle mesh and a base temperature of 25 °C (298.15 K) at ground level. Figure 13 shows the temperature results obtained from the model without CCLC.

After initial modeling of the system using COMSOL Multiphysics®, we carried out an in-depth analysis of the heat distribution resulting from the three heat sources in the absence of CCLC technology. This analysis revealed a maximum temperature of 72.85 °C (346.19 K) inside the system using the denser triangle mesh type. We can run simulations with a normal triangle mesh. Figure 9 depicts the normal triangle mesh geometry of the CCLC concept studied and modeled using COMSOL Multiphysics®.

We employed two methods in modeling our CCLC using COMSOL: Computational Fluid Dynamics (CFD) and Finite Element Method (FEM). The evaluation of thermal performance in electronic systems often relies on simulation techniques supported by specialized preprocessing and postprocessing tools. Finite Element Method (FEM) solvers are extensively utilized for heat transfer analysis [39–41]. Figure 10 depicts the temperature outcomes obtained from the model without CCLC.

Following the initial modeling of the system using COMSOL Multiphysics®, we conducted a thorough analysis of the heat distribution resulting from the three heat sources

in the absence of CCLC technology. This analysis revealed a maximum temperature of 70 °C (343.15 K) inside the system using the normal triangle mesh type.

We observe that the thermal results obtained using both normal triangles and denser triangles are stable, with a very low error rate of around 0.9%. Thus, neither types of mesh can lead to numerical instabilities such as solution non-convergence. According to these comparison results, our thermal simulations can be continued using either of the two mesh types while keeping the normal mesh type for all future results.

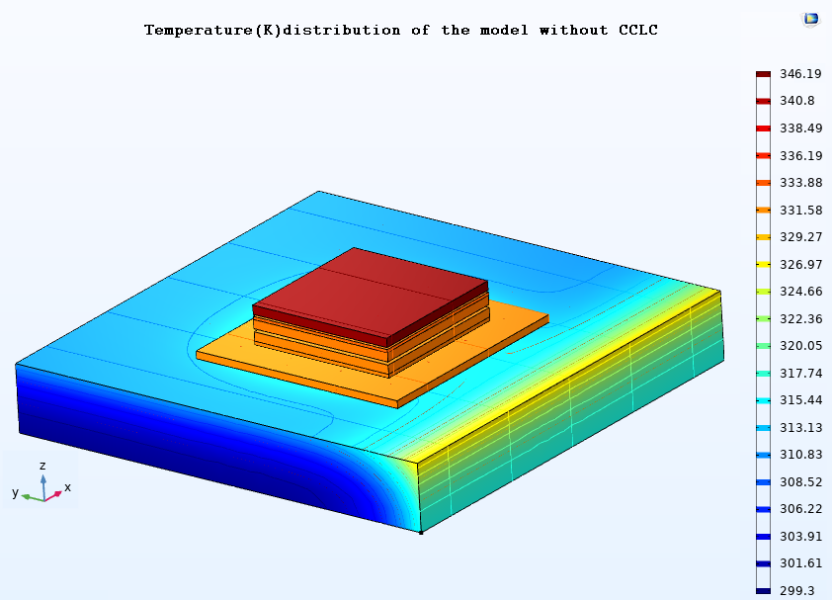

Figure 13. Model thermal results without CCLC.

In a thermal model, inhomogeneity refers to the presence of spatial and temporal variations in thermal properties in SiP. This means that thermal characteristics such as temperature, thermal conductivity, and heat capacity are not uniform throughout the system. It is important to account for inhomogeneity in this thermal model in order to obtain accurate and realistic predictions. Without accounting for these variations the model results may be biased and not match the experimental observations and actual behaviors of the SiP system under study.

The presence of a maximum temperature in the corner of the base plate can be attributed to several factors. Possible explanations include:

- If the plate is subjected to heat flow from an electronic component, the heat dissipation may not be uniform across the entire surface of the plate; the corners of the plate may have lower heat dissipation due to less heat conduction to the environment than other more exposed areas. This can result in heat building up in the corners and higher temperatures.
- Here, the corners of the plate are affected by boundary conditions of 25 °C, which favors a temperature increase; for example, if the corners are insulated or partially insulated, they can retain heat and reach higher temperatures than other parts of the plate.
- Natural convection can play a role in the distribution of heat through the plate. Weaker natural convection effects can result in heat buildup and peak temperatures.

Figure 11 shows a visual presentation of the model's heat map of, offering a comprehensive depiction of the temperature distribution. The heat map highlights a maximum temperature of 45 °C (318.15 K), providing valuable insight into the overall thermal behavior of the system.

Figure 11 presents a cross-sectional view of the temperature distribution, illustrating a symmetrical split. This split indicates a reduction in temperature within the network,

with the highest temperature level of approximately 70 °C decreasing to 45 °C. This result suggests that the thermal conductivity strips are able to effectively transfer heat to the carrier, thereby reducing thermal resistivity between the films and minimizing temperature centralization.

To mitigate hot spots in the corners of the SiP it is important to consider heat dissipation in the early design stages. This can include proper component selection and layout, creating efficient heat dissipation paths, optimizing airflow around the SiP, and using materials with high thermal conductivity. A combination of several of these approaches is recommended to achieve a significant reduction in hot spots in the corners of the SiP. However, it is important to consider cost, space, and performance constraints when implementing these solutions, as increasing the heat sink area in the corners by using larger heat sinks or adding additional cooling fins is generally not a solution favored by industry. Figure 14 showcases the transient temperature distribution on the examined chips, comparing the scenarios with and without CCLC technology.

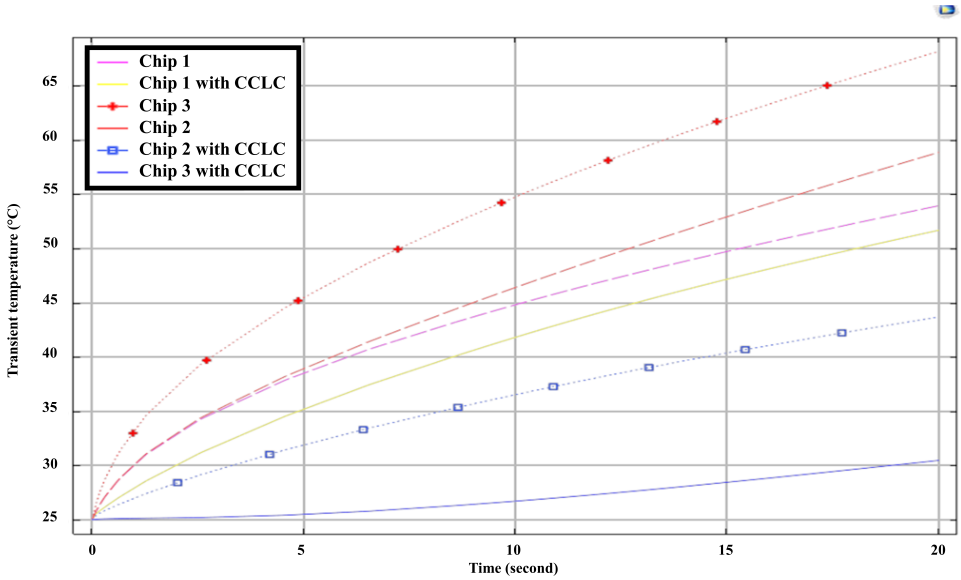

Figure 14. Thermal transient distribution on chips with and without CCLC.

Figure 14 presents compelling evidence supporting the advantages of employing CCLC technology. It demonstrates the effectiveness of CCLC as a thermal barrier, which significantly enhances the area available for heat diffusion within the carrier. As a result, heat is distributed more evenly throughout the system and temperatures remain below 45 °C, enabling electronic devices to function effectively under such conditions.

The system temperature can be effectively reduced by utilizing metal-based materials as a replacement for the substrate in high-powered dies. Additionally, substituting the carrier with metallic-based or silicon materials that offer superior heat conductivity can further contribute to decreasing the substrate temperature.

To verify the effectiveness of our approach, we provide a comprehensive comparison between the results of the electrical performance analysis of a CCLC-based SiP, as discussed in Section 2, and the thermal results of the same SiP configuration presented in Section 3. Table 3 summarizes the comparison results.

Table 3. Comparison between electrical and thermal analysis results of CCLC-based SiP.

	Without CCLC Technology	**With CCLC Technology**
Electrical analysis (°C)	71.85	43.85
Thermal analysis (°C)	70	45
Error (°C)	1.85	1.15

The electrical and thermal evaluations of SiPs without CCLC technology exhibit satisfactory concurrence, demonstrating a maximum deviation of 1.85 °C. For SiPs with CCLC technology the agreement between the electrical and thermal analysis was even better, with a minimum error of 1.15 °C.

In order to validate our methodology, we present a comprehensive comparison with relevant literature and quantify the rate of overheating error in our SiP module. This error occurs when our module reaches a dangerously high temperature that can damage or destroy it. In certain cases this may be due to cooling system failure or equipment overload.

Table 4 outlines how the proposed CCLC system compares to similar works.

Table 4. Analysis of the performance of the CCLC system in comparison to similar studies.

References	Proposed	[42]	[43]
Method	CCLC [a]	BGA [b]	LTI [c]
Temperature (°C)	71.85	100	105.50
Error (°C)	1.15	2.16	3.09

[a] Chip Cooling Laminate Chip (CCLC). [b] Ball Grid Array (BGA). [c] Linear Time-Invariant (LTI).

We analyzed the thermal performance of the CCLC-based SiP module using COMSOL commercial software. We tried to compare the error rate for each technique for both BGA and LTI.

Table 4 showcases the increased efficiency achieved through the implementation of the CCLC-based approach proposed in this study. We have compared these results with the methods presented in [42,43].

These findings indicate that our proposed model holds significant promise, particularly in terms of temperature reduction, which constitutes the novel contribution of this research. This enhanced performance represents a noteworthy solution considering the lack of dependable methods available to assess and mitigate temperature levels in many SiPs.

4. Conclusions

In this paper, we introduce a novel thermal management approach for system-in-package (SiP) technology. Our research demonstrates the effectiveness of CCLC technology in facilitating the rapid dispersion of thermal heat. This method represents a significant advance over conventional thermal dispersion models by strategically managing the paths of thermal conductivity. Based on the electrical and thermal model analysis, the maximum temperatures in the arrays are reduced to their minimum with a maximum error of 1.15 °C. Additionally, this study presents an approach that can be applied to chip-on-chip (CoC) packaging, particularly in scenarios where there is a significant increase in the power of one or two chips. In our future work, we plan to implement this method in microchannel/microjet heat sinks to develop our first realistic SiP circuit.

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