electronics

MDPI

Article

A Fully Integrated 0.6 Gbps Data Communication System for Inductive-Based Digital Isolator with 0.8 ns Propagation Delay and 10^{-15} BER

Isa Altoobaji [1,*], Ahmad Hassan [1], Mohamed Ali [1], Morteza Nabavi [1], Yves Audet [1] and Ahmed Lakhssassi [2]

[1] Electrical Engineering Department, Polytechnique Montréal, Quebec, QC H3T 1J4, Canada; ahmad.hassan@polymtl.ca (A.H.); mohamed.ali@polymtl.ca (M.A.); morteza.nabavi@polymtl.ca (M.N.); yves.audet@polymtl.ca (Y.A.)

[2] Department of Engineering and Computer Science, Université du Québec en Outaouais, Gatineau, QC J8X 3X7, Canada; ahmed.lakhssassi@uqo.ca

* Correspondence: isa.altoobaji@polymtl.ca

Abstract: Digital isolators are implemented to protect low-voltage electronics and ensure human safety during high-voltage surge events. In this work, we present the design of an inductive-based digital isolation system that can sustain up to 1 kV_{rms} breakdown voltage. The proposed system is designed using the pulse polarity modulation scheme and fabricated in a 0.35 µm CMOS. Two identical dies are bounded within the IC package, with one die housing the transmitter (Tx) and the isolation transformer, while the other die contains the receiver (Rx). Two different customized designs between three metal layers are implemented to form the isolation element. The transformer's secondary coil is constructed in metal-1, while the primary coil is formed in metal-2 and metal-3 for comparing the system functionality, isolation capability, and propagation delay. The functionality has been verified by measurements for an operating frequency of 300 MHz with a 2.6 ns propagation delay and an energy consumption of 8.15 × 10^3 pJ/bit at 1 Mbps. The chip was tested under extreme temperatures and achieved a maximum measured common mode transient immunity (CMTI) of 500 V/µs. Jitter has been examined to ensure fast transmission at a bit error rate (BER) of 10^{-15} with a total jitter (TJ) of 188.18 ps.

Keywords: breakdown voltage; digital isolator; inductive isolation; integrated transformer; industrial applications; system-on-chip applications; gate driver; pulse polarity modulation

check for updates

Citation: Altoobaji, I.; Hassan, A.; Ali, M.; Nabavi, M.; Audet, Y.; Lakhssassi, A. A Fully Integrated 0.6 Gbps Data Communication System for Inductive-Based Digital Isolator with 0.8 ns Propagation Delay and 10^{-15} BER. *Electronics* **2023**, *12*, 3336. https://doi.org/10.3390/electronics12153336

Academic Editor: Costas Psychalinos

Received: 9 July 2023
Revised: 26 July 2023
Accepted: 2 August 2023
Published: 4 August 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Sensor Interfaces are key elements in industrial applications as they provide dedicated power levels for various actuators, sensors, and read-back links within the system. To ensure reliable circuit operations, power management systems require control levels configuration for their data communication channels in terms of human safety and circuitry protection [1,2]. One main requirement to afford optimum performance is to have an isolation system that enables digital signal transmission while eliminating dangerous effects on low-voltage system electronics caused by the high-voltage domain. Typically, in high-voltage applications, isolation barrier breakdown can not only cause potential hazards to end users but also may cause damage to low-voltage control circuits affecting the system functionality. For example, if the isolation barrier failure mode occurs in the AC motor drive system, either the damage is limited to the die with the isolation capacitor or to the gate driver die [3].

Digital isolation techniques are in the broad area of data communication systems for modern sensor interfaces. They are widely used in different applications, including medical equipment, network interfaces, and automotive industrial systems. The purpose of the isolation barrier is to eliminate voltage spikes and unwanted ground loops that may exist

between high-voltage and low-voltage circuit domains [4]. This is achieved by establishing two separate ground references for the transmitter (Tx) and receiver (Rx) circuits, allowing safe communication between different voltage levels. Additionally, it is mandatory in many industrial applications to maintain the required protection level against multiple noise sources, such as lightning strikes, while ensuring the correct functionality at the targeted signal transfer speed.

The coupling methods to perform the digital isolation are based mainly on three types: optocouplers, capacitors, and transformers. Digital isolators based on optocouplers were the very first conventional way in data communication systems that exploit light to transfer data in the near-infrared band. The main advantages of optocouplers are a high isolation breakdown and immunity to electromagnetic interference (EMI). On the other hand, they suffer from high power consumption (30 mA at 40 Mbps) [5], which causes lifetime degradation. Moreover, optocouplers are not compatible with the CMOS process since they are fabricated in gallium arsenide (GaAs), and discrete chips are required for multiple isolation channels [6,7].

Capacitive isolators are implemented in silicon dioxide (SiO_2) technology which has a dielectric strength of up to 500 V/µm [8,9]. As a result, an isolation voltage of 1.5 kV_{rms} can be achieved within a 3 µm SiO_2 thickness between metal-1 and metal-6 in a 0.18 µm CMOS process [10]. Compared to optocouplers, capacitive isolators can be integrated with the CMOS process and have lower power consumption [11–13]. In addition, capacitive techniques are well-suited for high-speed data transfer due to their higher EMI. However, because of the fast ground shift (in hundreds of kV/µs) between the two circuit domains, capacitive techniques have lower common mode transient immunity (CMTI) [14–16]. This common mode current, which is proportional to the capacitor size, may corrupt data transfer and increase the bit error rate (BER).

To achieve higher data rates, more isolation voltage, and improve the CMTI, the inductive-based isolation method is adopted. Inductive methods use polyimide, with a field strength of 250 V/µm before breakdown, as the insulation material between coils to transfer data and power through magnetic coupling. Polyimide outperforms SiO_2 by having a lower parasitic capacitance of the isolation barrier at the expense of added fabrication cost [17–24]. This method supports high data rates of 0.5 Gbps [25], provides an excellent CMTI (650 kV/µs) [26], and offers a great isolation voltage of 7.5 kV_{rms} [27]. In addition to data transmission [28,29], isolated DC-DC converters use transformers for power transfer because of their high-quality factor compared to capacitive coupling, which usually requires off-chip elements to construct subharmonic resonant peak efficiency [30–33].

Figure 1 shows the typical block diagram of an inductive-based digital isolation system for industrial sensor interfaces. Transceiver blocks are implemented on the low-voltage and high-voltage sides, each with their respective supply and ground rails: $VDD_L/VDD_H/VDD_1/VDD_2/VDD_3$ and $GND_L/GND_1/GND_2/GND_3$. Two differential signals are transmitted from the microcontroller logic unit (MLU) on the low-voltage side to the gate driver on the high-voltage side, while the read-back signal is transmitted from the off-chip load through the analog-to-digital converter (ADC) on the high-voltage side to MLU. To ensure a fully isolated environment, the system incorporates an isolated DC-DC converter that takes the input voltage source from the low-voltage side and generates required voltage levels in the high-voltage domain. A fully integrated digital isolation system attempts to combine the communication links into a single compact die to further minimize power consumption and reduce fabrication costs.

This design utilizes edge-based modulation [34] due to its lower power consumption compared to on-off-keying (OOK) architecture [35,36], which uses a single chip area at the cost of higher power consumption during the logic high state of the signal modulation process. A set/reset architecture with a dual transformer is an example of edge-based communication with a high isolation rating. It, however, occupies twice the transformer area compared to single transformer architectures. Another example is the pulse count

method [19,20], where the chip area and the power consumption stand in an acceptable range. When compared to the single-pulse method, the power is 1.5 times higher, the propagation delay is longer, and it operates at lower data rates since it requires more time to evaluate the pulse count.

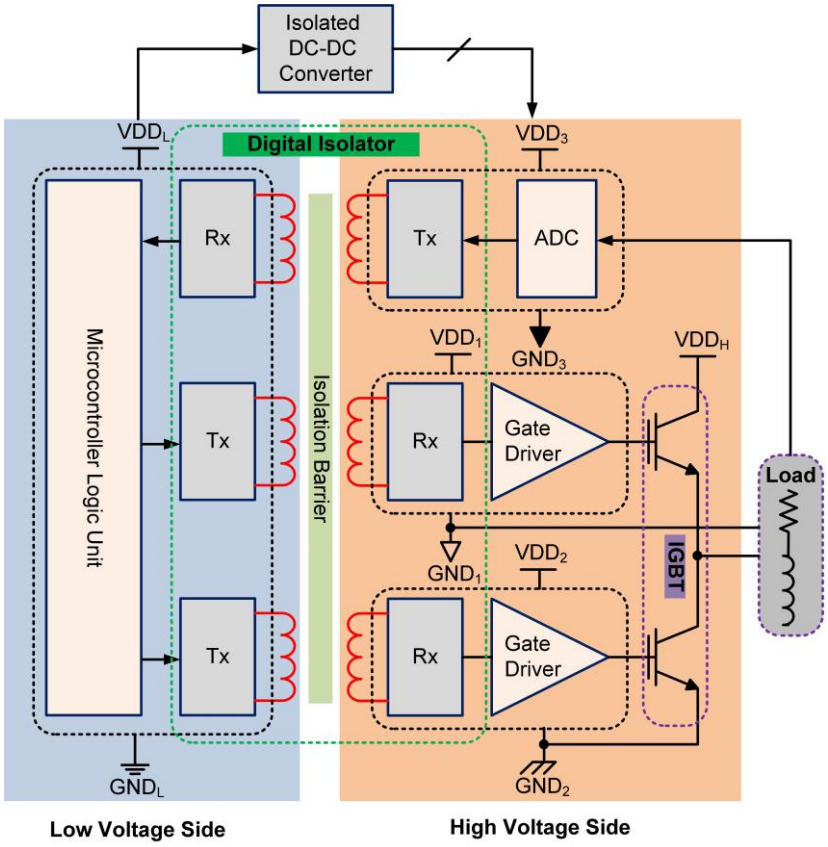


Figure 1. Inductive-based digital isolation system for industrial sensor interfaces.

Although the currently available maximum achievable data rate is sufficient for the current applications, future demands are expected to require higher data rates, lower latency, and lower BER. To the best of our knowledge, the maximum speed achieved with the minimum propagation delay for fully integrated inductive digital isolators in a 0.18 µm CMOS is 0.5 Gbps and 3.6 ns, respectively. Moreover, to operate at higher speeds, two transformers are utilized, which increases the fabrication cost [25]. This work proposes high data rates, reduced delay, and a low BER fully integrated inductive digital isolation system based on the pulse polarity modulation scheme in a high-voltage 0.35 µm CMOS process. The rest of this paper is organized as follows: design and implementation of the inductive-based digital isolation system are given in Section 2. Measurement results are presented in Section 3. Discussion and comparison with prior state-of-the-art are illustrated in Section 4, and final conclusions are drawn in Section 5.

2. Inductive-Based Digital Isolation System

The transceiver circuit of the implemented system utilizes the pulse polarity modulation scheme, which has the advantages of a compact circuit area, low power consumption, and high data rates. The presented scheme generates short pulses (in GHz sub-band) from the input digital signal for logic state transmission. The basic principle of GHz sub-band generation is demonstrated by the resulting CMOS inverter's harmonic overtones. When a sinusoidal input signal with a frequency of half the bandwidth of the CMOS process is applied under a VDD/2 bias condition, the output waveform is enhanced to a square shape

with a fast slew rate. The Tx can then modulate these overtones and transmit them to the Rx using a small on-chip isolation transformer area.

2.1. Tx Design

Figure 2 shows the circuit diagram, including the operation waveforms of the Tx side of the digital isolator system supporting single channel one direction (half duplex) data communication. The MLU input digital signal is processed through the Tx subcircuit stages and transmitted to the Rx side through inductive coupling. The Tx circuit consists of two differential parts: a negative pulse generator and a positive pulse generator, for shaping the negative pulses and positive impulses, respectively. Each of these branches consists of a pulse detector, cascaded inverters, a current limiter, and driver transistors.

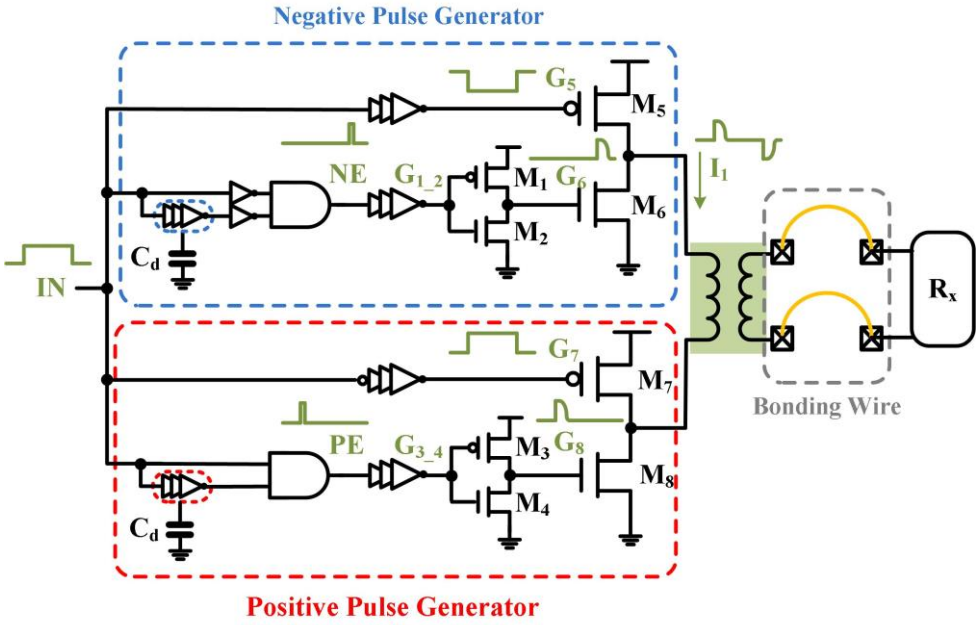


Figure 2. Transmitter (Tx) circuit diagram including the operation waveforms.

The pulse detector is the first circuit of the Tx chain, and it is responsible for detecting the positive and negative edges of the input digital signal "IN." The sizing of the transistors is designed so that it generates a 2 ns pulse width signal, negative edge (NE) or positive edge (PE), to accommodate the desired system bandwidth. The current limiting inverter controls the current passing through the large-sized driving transistors (M_5, M_6, M_7, and M_8) by shaping the generated pulse from the edge detector to have a sharp rise and a lower falling slope. This is achieved by increasing the current of M_1/M_3 and decreasing the current of M_2/M_4, i.e., the high change of the current with respect to time, the sharper the edge of the signal and vice versa. During the high-to-low transition of IN, the G_6 signal is determined and activates the driver transistor M_6. Then, the cascade-connected inverters output (G_5) at the upper circuit branch triggers the driving transistor M_5. This operation is repeated for the transmission of IN from low to high, which corresponds to the lower part of the Tx.

2.2. Transformer Design

We performed two case studies to investigate the isolation capability of the technology at different separation distances between the coils. The voltage at the secondary side of the transformer is formed by differentiating the current I_1 generated in the primary coil at the Tx side and can be controlled by proper magnetic coupling between the two coils. Since the design kit does not include inductor or transformer models, we customized the coils on two different metal layers separated by the inter-metal dielectric material. Among other configurations, such as tapped or interleaved, we chose the stacked structure due to its

highest self-inductance and coupling efficiency. Figure 3a illustrates the lateral parameters of the square spiral coil with a number of turns n = 3 and a number of sides N = 4. The coil width is denoted by w, while s is the spacing between the adjacent turns, and inner and outer diameters are d_{in} and d_{out}, respectively. Square spirals are chosen among other alternative geometries due to their layout simplicity. Also, they have the smallest effective area compared to hexagonal, circular, and octagonal shapes. Figure 3b shows the two versions of the on-chip transformer implemented on the three metal layers of a CMOS process. Higher isolation can be achieved between metal-1 and metal-3 due to the larger insulation material thickness. Our objective is to examine the effect of changing the isolation distance on the performance of the data communication link for the isolation system.

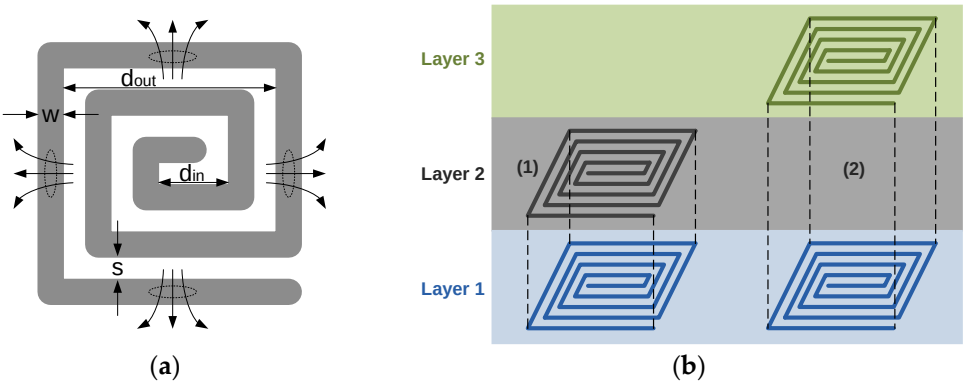


Figure 3. (**a**) Square spiral coil layout [28]; (**b**) the coil implementation on three metal layers of a CMOS process [28].

The isolation transformer is modeled by a non-ideal equivalent circuit consisting of an inductance, parasitic resistance, substrate resistance, and parasitic capacitances. The equivalent circuit of the non-ideal transformer formed by two π models for the primary and secondary coils is shown in Figure 4. The series inductances, resistances, and parallel capacitances are defined by [37]

$$L_s = \frac{2\mu n^2 d_{avg}}{\pi}\left[ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2\right], \quad (1)$$

$$R_s = \frac{\rho l}{\delta w\left(1 - e^{-\frac{t}{\delta}}\right)}, \quad (2)$$

and

$$C_{ox} = C_{ov} = 0.5\frac{\varepsilon_{ox}}{t_{ox}} lw, \quad (3)$$

respectively. The magnetic permeability is denoted by μ, d_{in} is the average diameter of turns, ρ is the fill ratio, δ refers to the skin depth, and t represents the thickness of the metal. ε_{ox} is the oxide permittivity, t_{ox} is the oxide thickness, and the coil length is represented by l. The substrate coupling elements, R_{si} and C_{si}, can be ignored by considering the pattern ground shield effect. Finally, the mutual inductance is related to the coupling coefficient k and the primary/secondary inductances L_{sp}/L_{ss} as [37]

$$M = k\sqrt{L_{sp}\, L_{ss}}\,. \quad (4)$$

The typical range of mutual inductance for the stacked spiral configuration is between 0.3 and 0.9, with the highest coupling coefficient being used in this design to ensure the correct functionality of the digital isolator system. In addition, the proper matching of the transformer's inductance value should be considered to avoid distortion of the detected voltage pulse at the secondary side. The detected voltage pulse has been simulated at

different inductance values, where a typical value of 10 nH has been selected based on the desired amplitude and pulse width at the Rx. Then, on-chip spiral coils of the transformer parameters are designed from the obtained inductance value.

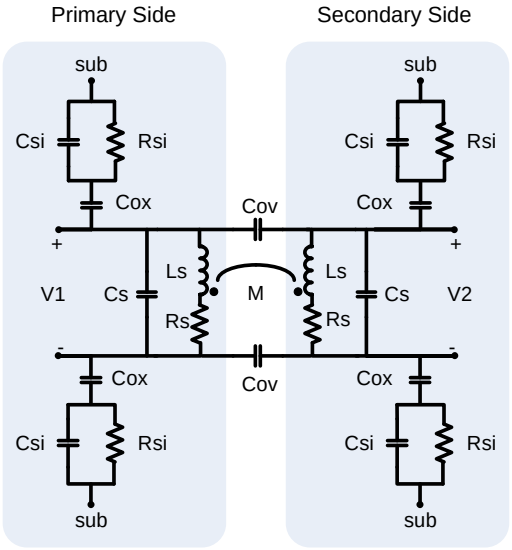


Figure 4. Non-ideal transformer equivalent circuit model [28].

2.3. Rx Design

The Rx circuit consists of a high pass filter (HPF), peak/bottom levels hold, a differential amplifier, and a hysteresis comparator. Figure 5 presents the schematic of the Rx with its operation waveforms. The isolation transformer's secondary side is connected to the Rx front side using two bond wires between the corresponding pads.

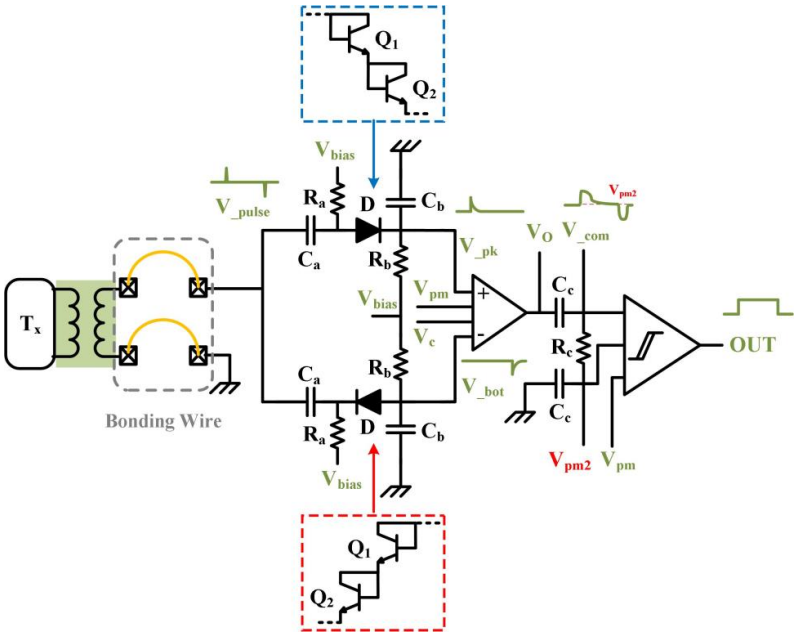


Figure 5. Circuit diagram of the implemented receiver (Rx) and the operation waveforms.

The received signal ($V_{\_pulse}$) with a frequency of 3–5 GHz is first filtered from low-frequency noise components caused by common mode transients (CMT) using the HPF. The diode circuit is formed by implementing two series diode connected BJTs adopted to detect positive and negative impulses according to the V_{bias} threshold applied between its

terminals through resistances R_a and R_b. The capacitor C_b helps widen the detected pulses to a 10 MHz frequency so that they can be handled by the differential amplifier.

The single-stage amplifier design compares both inputs, $V_{\_pk}$ and $V_{\_bot,}$ with the reference voltage V_c [38,39], as shown in Figure 6. The reference current of the differential amplifier is settled by a Cascode current mirror, where the latter is referenced by the V_{pm}-biased external current source. This amplification stage is designed to further reject the magnitude of the slow swing pulses that exceed the threshold voltage of the diodes. The purpose of capacitive coupling elements (R_c and C_c) at the amplifier output V_O is to establish the DC level of the comparator input $V_{\_com}$ at V_{pm2}.

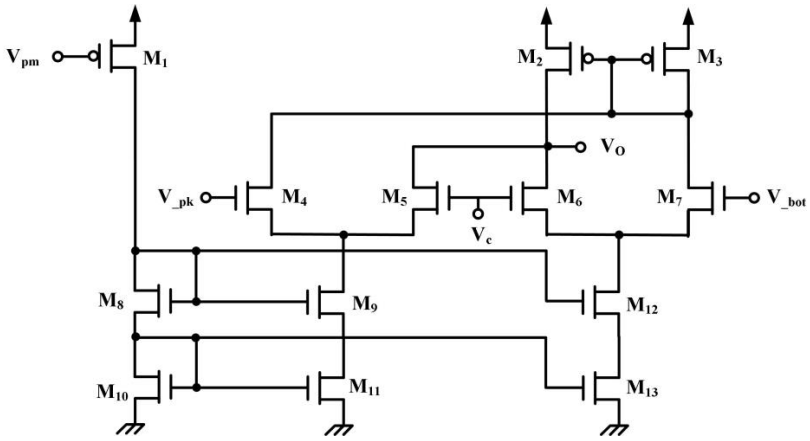


Figure 6. Schematic of the differential amplifier.

The last block of the Rx is the hysteresis comparator, which consists of three stages: a differential input pair, a decision stage, and an output buffer [40]. Figure 7 shows the circuit of the hysteresis comparator. The cross-coupled differential stage transistors provide positive feedback to the decision stage inputs and control the switching point of the comparator. The tail current of the differential stage is adjusted by the current mirror biased at V_{pm}. Thus, if the comparator's differential input signal exceeds/falls down this threshold level (i.e., positive/negative peak voltage), the output signal OUT switches to logic 1/0.

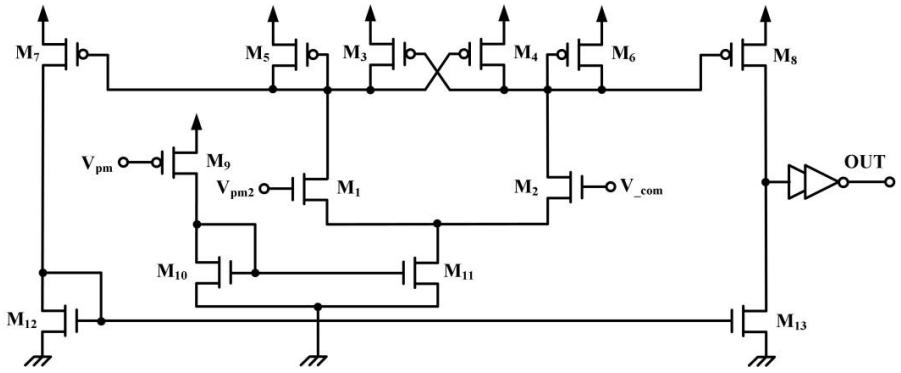


Figure 7. Schematic of the hysteresis comparator.

2.4. Common Mode Noise Analysis

One important characteristic of digital isolators is the system's ability to reject CMT pulses while maintaining error-free transmission at the desired data rate. The common mode voltage refers to the voltage difference between the Tx ground and the Rx ground. The common mode voltage is related to the rapid switching of the integrated gate bipolar transistor (IGBT) at the high voltage side, which propagates through the overlapping capacitance of transformer coils (C_{ov}) and affects the Rx-detected signal level. Consequently,

the Rx signal $V_{\_pulse}$ will follow similar rise/fall transitions of the common mode pulse in the range of hundreds of kV/µs range. The unwanted slew rate added to $V_{\_pulse}$ can lead to false detection at the Rx side and hence miss-determining the correct logic level at the final system output. Since the common mode component of $V_{\_pulse}$ is with a frequency less than the actual modulation frequency ($f_{cm} < f_{mod}$), the amount of this noise can be further reduced by the HPF, the first element of the Rx circuit. The differential architecture of the Rx helps further improve the common mode rejection of the overall implemented system. Figure 8 illustrates the block diagram of the digital isolator under CMTI simulation. A high voltage pulse V_{cmti} = 550 V with a rising/falling time of 2.5 ns which corresponds to a CMTI of 220 kV/µs is being injected between the Tx ground (GND_{Tx}) and the Rx ground (GND_{Rx}).

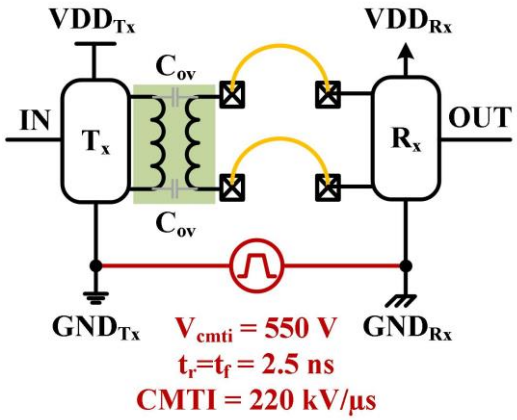


Figure 8. Block diagram of the digital isolator under common mode transient immunity (CMTI) simulation.

The system's response to the CMT pulse is demonstrated in Figure 9. The input digital signal at the Tx with a frequency of 10 MHz is modulated and transmitted to the Rx input through the isolation transformer. The second waveform is the 42 MHz high-voltage pulse between the Tx and Rx grounds (V_{cmti} = 220 kV/µs). In typical scenarios, the high-voltage pulse combinations are applied at multiple IN rising/falling edges, i.e., during different surge events: rising, high amplitude, falling, and low amplitude. Although the applied surge added additional top/bottom peaks on the comparator input $V_{\_com}$, the final Rx output OUT is successfully recovered. This is because the unwanted peaks fall above/below the threshold level of the comparator within a small duration. The total system propagation delay from the Tx input to the Rx output during the surge event is 28 ns.

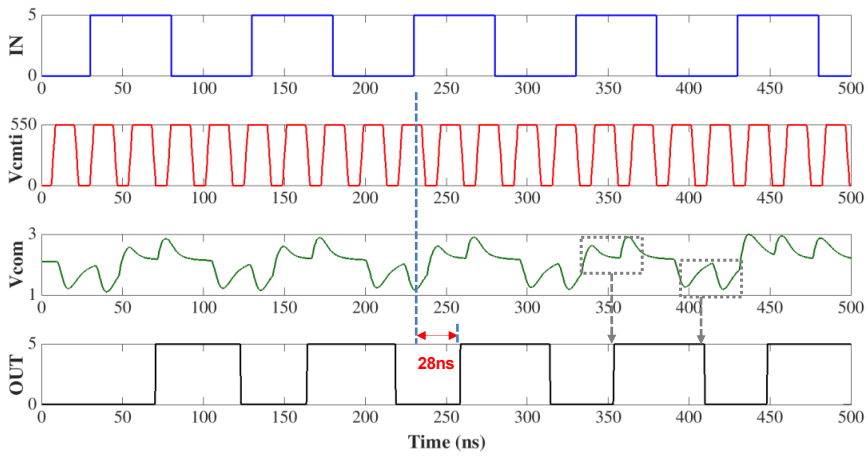


Figure 9. System functionality simulation showing the digital isolator's signal flow in the presence of a common mode transients (CMT) pulse.

3. Measurement Results

The experimental test bench setup for the fabricated inductive-based digital isolator system is shown in Figure 10a. One power supply is used for supplying the printed circuit board (PCB) domain A_1/domain A_2 and domain B (Figure 10b), while the other power supply is employed to generate reference voltages for the Rx circuit. The continuous input digital signal is supplied to the system's Tx input using a 0.4/0.68 Gbps pulse/pattern generator which is then recovered at the Rx output analyzed on an Agilent 13 GHz Infiniium digital signal analyzer through the 12 GHz active probes adopted for their noise immunity performance. The input and output signals are simultaneously displayed on the oscilloscope for the propagation delay measurement. The 1:1 isolation transformer is used to assign a floating ground to the Tx side's equipment. The bottom layer of our custom PCB prototype is divided into three isolated domains, each one assigned to separate supply rail terminals. Pairs of surface-mounted ceramic capacitors (0.1 µm and 10 µm) are placed close to package pins to filter out power supply noise. The zoomed view of the two-layer PCB with 80 mm × 70 mm dimensions is also shown in Figure 10b. The HALFCUBE temperature chamber is used to measure the system functionality over a wide range of temperature variations (Figure 10c).

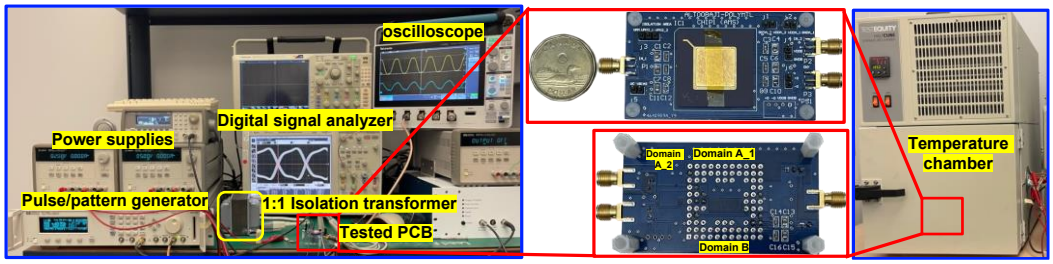


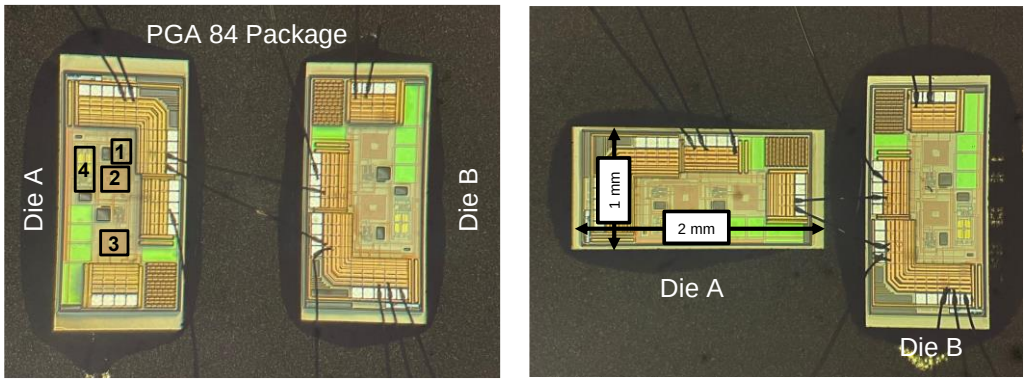
Figure 10. Experimental measurements: (**a**) testbench setup with the equipment to measure the performance of the fabricated digital isolator chip; (**b**) front and bottom view of PCB prototype; (**c**) temperature chamber.

The implemented inductive-based digital isolator system is fabricated in a 5 V 0.35 µm CMOS process. The total area for each die is 2 mm^2, and the two dies are assembled and bounded inside an 84-pins PGA package (Figure 11). Die A, which houses the Tx and the on-chip transformer, is powered from the domain A supply, while die B (which contains the Rx circuit) is driven from the domain B supply rails. The Tx and isolation transformers occupy a silicon area of 142 µm × 126 µm and 224 µm × 224 µm, respectively, while the Rx block consumes an active area of 7.3 × 10^4 $µm^2$. The coil width of the transformer is 6 µm, and the spacing is 2 µm. Two bonding arrangements were implemented to test the system functionality according to two customized coil designs for the isolation transformer: Figure 11a metal-1 to metal-3, and Figure 11b metal-1 to metal-2.

3.1. System Functionality

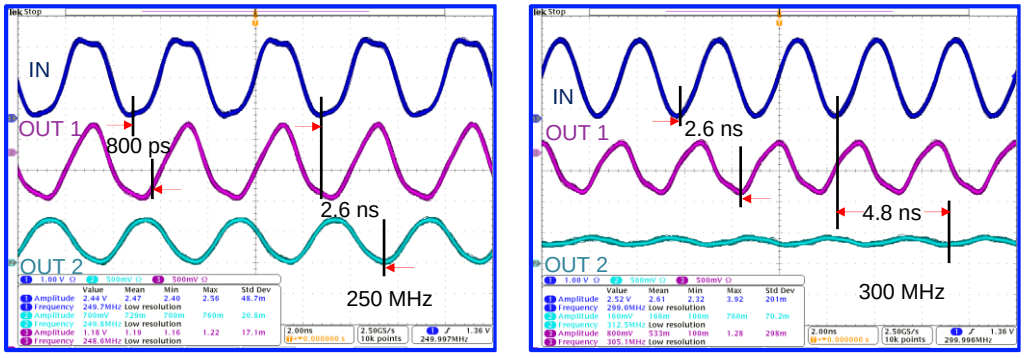
Isolated solutions for protocols such as USB3 and HMDI require data rates in the range of Gbps. Moreover, isolated high-speed clocks and data links for industrial sensor interfaces operate at the same range. For this purpose, we have performed the system measurements at high frequencies. Figure 12 demonstrates the input-output waveforms of the fabricated inductive-based digital isolation system at (a) 250 MHz and (b) 300 MHz frequencies. We have compared the input with outputs from both systems based on the two fabricated customized transformers. OUT1 is related to the system using the metal1-metal2 transformer, while the system's output denoted by OUT2 utilizing the metal1-metal3 transformer is denoted by OUT2. The measured typical propagation delay from the generated Tx input IN and the recovered Rx output OUT1 is 800 ps at both rising and falling edges for 250 MHz, as shown in Figure 12a. Compared to OUT1, the propagation delay is increased to 3.25 times, and the amplitude is reduced by 59% for

OUT2 at 250 MHz. This is because the separation between the coils maximizes the isolation voltage at the cost of reducing the energy of the detected signal at the Rx input. Figure 12b shows the measured outputs at 300 MHz, where the propagation delay for OUT1 and OUT2 is increased from 2.6 ns to 4.8 ns, respectively. Despite the increased propagation delay, the achieved results support fast transmission for high data rate applications.



(**a**) (**b**)

Figure 11. (**a**) Chip micrograph of the integrated digital isolation system in a high-voltage 0.35 µm CMOS process: (1) transmitter, (2) metal1-metal3 transformer, (3) metal1-metal2 transformer, (4) receiver; (**b**) Another implementation of the digital isolation system.



(**a**) (**b**)

Figure 12. (**a**) Experimental measurement of the digital isolation system input-output functionality at 250 MHz; (**b**) Measured input-output waveforms at 300 MHz.

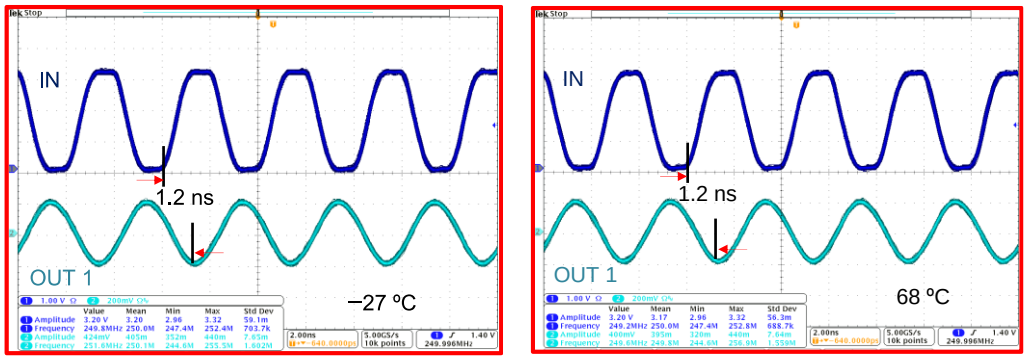
3.2. Temperature Variations

To ensure the system functionality at extreme conditions, we performed the measurement under different temperatures. Figure 13 demonstrates the effect of temperature variations on the system functionality at −27 °C (Figure 13a) and 68 °C (Figure 13b). The digital isolator system is tested under the operational frequency of 250 MHz. The PCB is placed inside the chamber, and the temperature is gradually varied to monitor the waveform on the oscilloscope. The variation rate of the propagation delay from its typical value of 800 ps at room temperature is 9.7 ps/°C, for temperature variations from 27 °C and 68 °C, as shown in Figure 13b. Therefore, the propagation delay is insensitive to temperature variations.

3.3. Common Mode Rejection

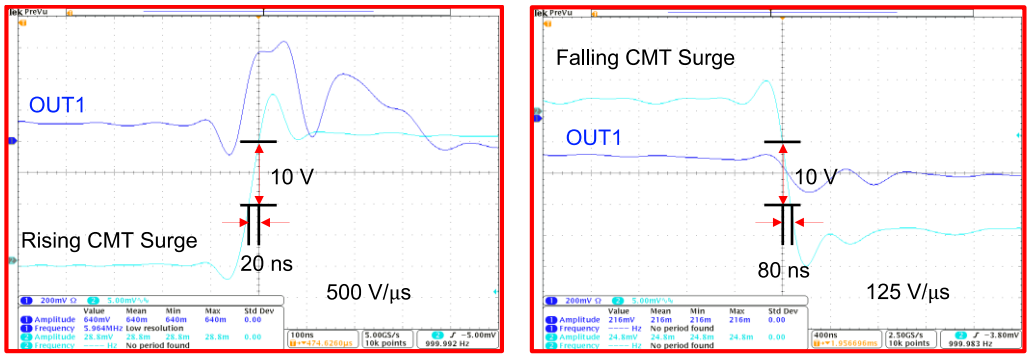
Figure 14 shows the digital isolation system output in the presence of CMT noise. The high-voltage pulser is equipped with a 1:1000 divider to monitor the generated pulse on the oscilloscope. The system's output response to the rising CMT surge is shown in Figure 14a, where a slew rate of 500 V/µs is observed at an amplitude of 28 V during a 100 ns duration. The output glitch of 500 mV at the start of the surge is observed. The

system's output during the falling CMT surge demonstrated in Figure 14b shows only a 200 mV shift due to the slower transient slope of 80 ns. The difference in slope measurement between the rising and falling CMT noise is due to the accuracy of the high-voltage pulser device. Although the simulation results demonstrate a CMTI of 220 kV/µs, higher CMTI could not be achieved due to the slow rise/fall times of the high-voltage pulser device (25 ns), which is limited to 125 V/µs at the falling CMT surge.



(**a**) (**b**)

Figure 13. (**a**) Measured continuous oscilloscope waveforms of the overall digital isolation system input-output functionality at 250 MHz and −27 °C; (**b**) Measured waveforms at 250 MHz and 68 °C.



(**a**) (**b**)

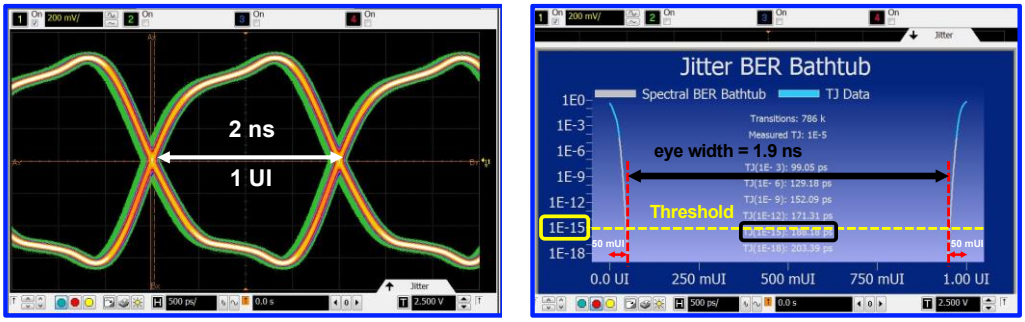
Figure 14. (**a**) Measured system output signal in the presence of CMT pulse at the rising edge surge (500 V/µs); (**b**) system output at the falling CMT surge (125 V/µs).

3.4. Jitter Analysis

Jitter is a critical parameter characterizing high-speed data communication systems, as it can cause errors in transmitting bits, leading to incorrect estimation at the receiving end and increasing BER. Jitter can be caused by a system, data transmission, or random noise. Figure 15a shows the real-time eye diagram of the system output OUT at the Rx end captured at a 0.5 Gbps input digital signal. The Eye width indicates a clear opening of 1.9 ns mean-value. The measured total jitter (TJ) value at both edges of the eye is 100 ps, composed of the early/late transition deviations from the ideal time location. The BER bathtub curve of the eye diagram is shown in Figure 15b. Each symmetrical Gaussian tail is made of two segments: the measured section (in blue) and the extrapolated section (in gray). The digital isolator system achieved the lowest BER of $10^{-15,}$ which is computed by intersecting the effective eye width with the bathtub curve. The accumulated jitter is the main cause of bit errors that occurs below the threshold line. TJ of the system is the difference between the unit interval (UI) and the eye width, which is 188.18 ps.

Typically, TJ is composed of deterministic jitter (DJ) and random jitter (RJ). DJ is further categorized into data-dependent jitter (DDJ) and periodic jitter (PJ). RJ is related to thermal noise, shot noise, and pink noise. Figure 16a shows DDJ versus bit, where the first two bits of the generated stream are zoomed. The negative jitter value at the falling edge of the

first bit (−10.9 ps) indicates that the transition arrived earlier than it should have, while for the second bit, the transition arrived later, resulting in increased transmission errors in the system. Figure 16b illustrates the extracted composite jitter histogram, showing the distribution of three types of jitters present in the system: TJ, RJ/PJ, and DDJ. The amount of RJ/PJ is evaluated by subtracting DDJ from TJ, which is 166.38 ps or 83.19 ps at each peak. By computing the peak frequencies of inter-symbol-interference (ISI) and duty cycle distortion (DCD) using a digital signal analyzer time interval error (TIE) algorithm, DDJ can be eliminated.



(**a**) (**b**)

Figure 15. (**a**) Measured real-time eye diagram of the fabricated inductive digital isolator chip output at 0.5 Gbps; (**b**) corresponding jitter bit error rate (BER) bathtub over one unit interval (UI) window.

(**a**) (**b**)

Figure 16. (**a**) Data-dependent jitter (DDJ) vs. bit (first 2 bits zoomed); (**b**) composite jitter histogram showing the distribution of jitter in the system.

4. Discussion

A performance summary and comparison of this work with other fabricated state-of-the-art from the literature are given in Table 1. In this comparison table, we have included both capacitive and inductive-based isolation systems. Yun et al. [27] achieved the highest isolation voltage rating of 7.5 kV_{rms} within 30 µm thick polyimide using an on-chip transformer implemented in a 5 V 0.18 µm CMOS, however, at the cost of higher energy consumption. The capacitive isolator implemented in a 1.8 V 0.5 µm process has the lowest energy of 99 pJ/b [12]. The work of Kaeriyama et al. [23] stands out among the others, with the smallest effective area using the pulse polarity scheme. Within the works presented in Table 1, our design achieved the maximum speed of 0.6 Gbps and a 0.8 ns minimum propagation delay for metal1-meta2 transformer implementation utilizing pulse polarity modulation implemented in a high-voltage 5 V 0.35 µm CMOS process. The presented results show the effect of increasing the separation distance between coils, where it increases the isolation voltage from 0.5 kV_{rms} to 1 kV_{rms}. However, this comes with a trade-off of reduced speed and increased propagation delay to 0.5 Gbps and 2.6 ns, respectively.

Table 1. Performance comparison and summary with other prior works.

Ref.	Process (µm)	Iso. Element	Area ($\times 10^4$ µm^2)	Scheme	Max. VDD (V)	Iso. Rating (kV_{rms})	Max. CMTI (kV/µs)	Max. Speed (Gbps)	Delay (ns)	Energy @ 1 Mbps (pJ/b)
[9]	0.35	Cap.	-	Pulse	5	2.28 [b]	-	0.5	2	1200
[12]	0.5	Cap.	60 [a]	Pulse	1.8	-	-	0.26	15	99
[13]	0.4	Cap.	37.5	Pulse	3.3	2.3	-	0.1	10	363 [d]
[23]	0.5	Ind.	11.98	Pulse	5	2.5	35	0.25	5.5	8000
[25]	0.18	Ind.	12.26	Pulse	5	1	130 [c]	0.5	3.2	5800
[26]	0.25	Ind.	71.25 [a]	OOK	5	3.34	650	0.08	15.5	9500
[27]	0.18	Ind.	-	OOK	5	7.5	200	0.2	11	14,000
This work @ M1-M2 coils	**0.35**	**Ind.**	**75.36**	**Pulse**	**5**	**0.5** [b]	**0.5**	**0.6**	**0.8**	**8150**
This work @ M1-M3 coils						**1** [b]		**0.5**	**2.6**	

[a] estimated from chip micrograph, [b] calculation, [c] simulation, [d] at 50 Mbps.

5. Conclusions

An inductive-based digital isolator implementation was discussed in this paper. The system is suitable for the on-chip integration of multiple high-speed clocks and data links between MLU and the gate driver in industrial sensor interfaces. The utilized pulse polarity modulation scheme, as well as the metal1-metal2 transformer structure, allows the design to achieve a higher speed and a minimum propagation delay of 0.6 Gbps and 800 ps, respectively. Moreover, the designed system using the metal1-metal3 transformer has a maximum isolation voltage of 1 kV_{rms} at the expense of a slight reduction in the transmission speed and an approximately three-fold increase in the propagation delay. The tested chip can operate at temperature variations between −27 °C and 68 °C. Correct system functionality under the presence of CMT of 500 V/µs was verified by measurement. The system has a minimum BER of 10^{-15} with a TJ of 188.18 ps.

Author Contributions: Methodology, I.A.; Software, I.A. and M.N.; Validation, Y.A. and A.L.; Investigation, I.A. and M.A.; Resources, A.H.; Writing—original draft, I.A.; Writing—review & editing, A.H., M.A., M.N. and Y.A.; Visualization, A.L.; Supervision, A.H., M.A. and Y.A.; Funding acquisition, Y.A. All authors have read and agreed to the published version of the manuscript.

Funding: The authors would like to thank the Natural Sciences and Engineering Council of Canada (NSERC), Mathematics of Information Technology and Complex Systems (MITACS), and Canadian Microsystems Corporation (CMC) for financial support and technology access.

Data Availability Statement: Data is unavailable due to privacy restrictions.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Ali, M.; Hassan, A.; Honarparvar, M.; Nabavi, M.; Audet, Y.; Sawan, M.; Savaria, Y. A versatile SoC/SiP sensor interface for industrial applications: Implementation challenges. *IEEE Access* **2022**, *10*, 24540–24555. [CrossRef]
2. Stecher, M.; Jensen, N.; Denison, M.; Rudolf, R.; Strzalkoswi, B.; Muenzer, M.N.; Lorenz, L. Key technologies for system-integration in the automotive and Industrial Applications. *IEEE Trans. Power Electron.* **2005**, *20*, 537–549. [CrossRef]
3. Kamath, A.; Neeraj, B.; Kannan, S. *Understanding Failure Modes in Isolators*; Texas Instruments Incorporated: Dallas, TX, USA, 2018.
4. Ragonese, E.; Palmisano, G.; Parisi, A.; Spina, N. Highly Integrated Galvanically Isolated Systems for Data/Power Transfer. In Proceedings of the 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genoa, Italy, 27–29 November 2019; pp. 518–521.
5. Mazumder, S.K.; Sarkar, T. Optically activated gate control for power electronics. *IEEE Trans. Power Electron.* **2011**, *26*, 2863–2886. [CrossRef]
6. *SFH6747T*; High Speed Optocoupler. Vishay Semiconductor: Malvern, PA, USA, 2004.
7. Mallia, S.S.; Ns, S.; Adinarayana, S.K.; Aniruddhan, S. A self powered 50-Mb/s OOK transmitter for optoisolator LED emulation. *IEEE J. Solid-State Circuits* **2017**, *52*, 678–687. [CrossRef]
8. Krone, A.; Tuttle, T.; Scott, J.; Hein, J.; Dupuis, T.; Sooch, N. A CMOS direct access arrangement using digital capacitive isolation. In Proceedings of the 2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177), San Francisco, CA, USA, 7 February 2001; pp. 300–301. [CrossRef]

9. Altoobaji, I.; Ali, M.; Hassan, A.; Audet, Y.; Lakhssassi, A. A High Speed Fully Integrated Capacitive Digital Isolation System in 0.35 µm CMOS for Industrial Sensor Interfaces. In Proceedings of the 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), Toulon, France, 13–16 June 2021; pp. 1–4. [CrossRef]
10. Shi, G.; Yan, R.; Xi, J.; He, L.; Ding, W.; Pan, W.; Liu, Z.; Yang, F.; Chen, D. A Compact 6 ns Propagation Delay 200 Mbps 100 kV/um CMR Capacitively Coupled Direction Configurable 4-Channel Digital Isolator in Standard CMOS. In Proceedings of the 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Bordeaux, France, 9–12 December 2018; pp. 721–724.
11. Mahalingam, P.; Guiling, D.; Lee, S. Manufacturing challenges and method of fabrication of on-chip capacitive digital isolators. In Proceedings of the 2007 International Symposium on Semiconductor Manufacturing, Santa Clara, CA, USA, 15–17 October 2007; pp. 1–4.
12. Moghe, Y.; Terry, A.; Luzon, D. Monolithic 1.8V–3.3V dual-channel 640Mbps digital isolator in 0.5µm SOS. In Proceedings of the 2012 IEEE International SOI Conference (SOI), Napa, CA, USA, 1–4 October 2012; pp. 1–2. [CrossRef]
13. Akiyama, N.; Kojima, Y.; Nemoto, M.; Yukutake, S.; Iwasaki, T.; Amishiro, M.; Kanekawa, N.; Watanabe, A.; Takeuchi, Y. A high-voltage monolithic isolator for a communication network interface. *IEEE Trans. Electron Devices* **2002**, *49*, 895–901. [CrossRef]
14. Culurciello, E.; Pouliquen, P.O.; Andreou, A.G.; Strohben, K.; Jaskulek, S. Monolithic digital galvanic isolation buffer fabricated on silicon on sapphire CMOS. *Electron. Lett.* **2005**, *41*, 526–528. [CrossRef]
15. von Daak, M.; Hille, P.; Silber, D. Isolated capacitively coupled MOS driver circuit with bidirectional signal transfer. In Proceedings of the PESC 98 Record, 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196), Fukuoka, Japan, 22–22 May 1998; pp. 1208–1213. [CrossRef]
16. Hashimoto, T.; Yuyama, Y.; Amishiro, M.; Nemoto, M.; Yukutake, S.; Kojima, Y.; Kanekawa, N.; Takeuchi, Y.; Watanebe, A. 4-kV 100-Mbps monolithic isolator on SOI with multi-trench isolation for wideband network. In Proceedings of the 2009 21st International Symposium on Power Semiconductor Devices & IC's, Barcelona, Spain, 14–18 June 2009; pp. 49–52. [CrossRef]
17. Munzer, M.; Ademmer, W.; Strzalkowski, B.; Kaschani, K.T. Insulated signal transfer in a half bridge driver IC based on coreless transformer technology. In Proceedings of the The Fifth International Conference on Power Electronics and Drive Systems, 2003. PEDS 2003, Singapore, Singapore, 17–20 November 2003; pp. 93–96. [CrossRef]
18. Münzer, M.; Ademmer, W.; Strzalkowski, B.; Kaschani, K.T. Coreless transformer, a new technology for half bridge driver ICs. In Proceedings of the PCIM, Nuremberg, Germany, 20–22 May 2003.
19. Chen, B.; Wynne, J.; Kliger, R. High speed digital isolators using microscale on-chip transformers. *Elektron. Mag.* **2003**, *15*, 1–6.
20. Chen, B. Isolated half-bridge gate driver with integrated high-side supply. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 3615–3618. [CrossRef]
21. Krishnapura, N.; Bhat, A.N.; Mukherjee, S.; Shrivastava, K.A.; Bonu, M. Maximizing the data rate of an inductively coupled chip-to-chip link by resetting the channel state variables. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 3531–3543. [CrossRef]
22. Timothe, S.; Nicolas, R.; Jean-Christophe, C.; Jean-Daniel, A. Design and characterization of a signal insulation coreless transformer integrated in a CMOS gate driver chip. In Proceedings of the 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, USA, 23–26 May 2011; pp. 360–363. [CrossRef]
23. Kaeriyama, S.; Uchida, S.; Furumiya, M.; Okada, M.; Maeda, T.; Mizuno, M. A 2.5 kV isolation 35 kV/us CMR 250 Mbps digital isolator in standard CMOS with a small transformer driving technique. *IEEE J. Solid-State Circuits* **2012**, *47*, 435–443. [CrossRef]
24. Uchida, S.; Kaeriyama, S.; Nagase, H.; Takeda, K.; Nakashiba, Y.; Maeda, T.; Ishihara, K. A face-to-face chip stacking 7 kV RMS digital isolator for automotive and industrial motor drive applications. In Proceedings of the 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Waikoloa, HI, USA, 15–19 June 2014; pp. 442–445. [CrossRef]
25. Kagaya, T.; Miyazaki, K.; Takamiya, M.; Sakurai, T. A 500-Mbps Digital Isolator Circuits using Counter-Pulse Immune Receiver Scheme for Power Electronics. In Proceedings of the 2019 International Conference on IC Design and Technology (ICICDT), Suzhou, China, 17–19 June 2019; pp. 1–4.
26. Javid, M.; Ptacek, K.; Burton, R.; Kitchen, J. A 650 kV/µs Common-Mode Resilient CMOS Galvanically Isolated Communication System. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 587–598. [CrossRef]
27. Yun, R.; Sun, J.; Gaalaas, E.; Chen, B. A transformer-based digital isolator with 20kVPK surge capability and >200 kV/µS Common Mode Transient Immunity. In Proceedings of the 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, USA, 15–17 June 2016; pp. 1–2. [CrossRef]
28. Altoobaji, I.; Ali, M.; Hassan, A.; Nabavi, M.; Audet, Y.; Lakhssassi, A. A Fully Integrated On-Chip Inductive Digital Isolator: Design Investigation and Simulation. In Proceedings of the 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, 9–12 August 2020; pp. 868–871.
29. Sankaran, S.; Kramer, B.; Howard, G.; Sutton, B.; Walberg, R.; Khanolkar, V.; Payne, R.; Morgan, M. An efficient and resilient ultra-high speed galvanic data isolator leveraging broad-band multi resonant tank electro-magnetic coupling. In Proceedings of the 2015 Symposium on VLSI Circuits (VLSI Circuits), Kyoto, Japan, 17–19 June 2015; pp. C210–C211. [CrossRef]
30. Chen, L.; Sankman, J.; Mukhopadhyay, R.; Morgan, M.; Ma, D.B. 25.1 A 50.7% peak efficiency subharmonic resonant isolated capacitive power transfer system with 62 mW output power for low-power industrial sensor interfaces. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 428–429. [CrossRef]
31. Ragonese, E.; Spina, N.; Castorina, A.; Lombardo, P.; Greco, N.; Parisi, A.; Palmisano, G. A Fully Integrated Galvanically Isolated DC-DC Converter with Data Communication. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2018**, *65*, 1432–1441. [CrossRef]

32. Mukherjee, S.; Bhat, A.N.; Shrivastava, K.A.; Bonu, M.; Sutton, B.; Gopinathan, V.; Thiagarajan, G.; Patki, A.; Malakar, J.; Krishnapura, N. 25.4 A 500 Mb/s 200 pJ/b die-to-die bidirectional link with 24 kV surge isolation and 50 kV/µs CMR using resonant inductive coupling in 0.18µm CMOS. In Proceedings of the 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 5–9 February 2017; pp. 434–435.
33. Ishihara, H.; Onizuka, K. 18.8 A Fully-Generic-Process Galvanic Isolator for Gate Driver with 123 mW 23% Power Transfer and Full-Triplex 21/14/0.5 Mb/s Bidirectional Communication Utilizing Reference-Free Dual-Modulation FSK. In Proceedings of the 2020 IEEE International Solid- State Circuits Conference—(ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 300–302. [CrossRef]
34. *ISO72x Single Channel High-Speed Digital Isolators, Data Sheet, Rev. L*; Texas Instruments: Dallas, TX, USA, 2015.
35. *ISO7841x High-Performance, 8000-Vpk Reinforced Quad-Channel Digital Isolator, SLLSEM3G*; Texas Instruments: Dallas, TX, USA, 2014.
36. *ADuM110N, 3.0 kV RMS Digital Isolator*; Analog Devices: Norwood, MA, USA, 2019.
37. Mohan, S.S.; Yue, C.P.; del Mar Hershenson, M.; Wong, S.S.; Lee, T.H. Modeling and characterization of on-chip transformers. International Electron Devices Meeting 1998. In Proceedings of the International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), San Francisco, CA, USA, 6–9 December 1998; pp. 531–534.
38. Razavi, B. *Design of Analog CMOS Integrated Circuits*; McGraw-Hill: New York, NY, USA, 2001.
39. Sackinger, E.; Guggenbuhl, W. A versatile building block: The CMOS differential difference amplifier. *IEEE J. Solid-State Circuits* **1987**, *22*, 287–294. [CrossRef]
40. Baker, R.J. *CMOS Circuit Design, Layout, and Simulation*, 3rd ed.; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2010.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.