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Generalization of Split DC Link Voltages Behavior in Three-Phase-Level Converters Operating with Arbitrary Power Factor with Restricted Zero-Sequence Component

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Abstract: This article examines the impact of a power factor on the behavior of partial DC link voltages in three-phase three-level AC/DC (or DC/AC) converters operating without additional balancing hardware. We consider the case in which the controller utilizes a bandwidth-restricted (DC in steady state) zero-sequence component to achieve average partial DC link voltage equalization since the injection of high-order zero-sequence components is impossible or forbidden. An assessment of partial split DC-link capacitor voltage behavior (particularly that of ripple magnitudes and phases) is necessary for, e.g., minimizing the values of DC link capacitances and selecting reference voltage values. Previous studies assessed the abovementioned behavior analytically for operation under a unity power factor based on third-harmonic-dominated split partial voltages' ripple nature. However, it is shown here that deviation from the unity power factor introduces additional (to the third harmonic) non-negligible harmonic content, increasing partial voltage ripple magnitudes and shifting their phase (relative to the mains voltages). As a result, the third-harmonic-only assumption is no longer valid, and it is then nearly impossible to derive corresponding analytical expressions. Consequently, a numerical approach is used in this work to derive a generalized expression of normalized ripple energy as a function of the power factor, which can then easily be utilized for assessments of split DC link voltage behaviors for certain DC link capacitances and reference voltages. Simulations and experimental results validate the proposed methodology applied to a 10 kVA T-type converter prototype.

Keywords: three-phase three-level converters; split DC link; capacitance; power factor

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1. Introduction

With the increasing demand for high-power AC/DC and DC/AC converters in modern energy systems, the use of controlled multilevel converters is becoming more common [1]. Multilevel converters offer several advantages over traditional two-level converters, including improved efficiency, reduced dv/dt, and lower total harmonic distortion of the output voltage [2]. Common topologies of multilevel converters include cascaded H-bridge, flying capacitor and neutral point clamped [3].

Multilevel converters play a significant role in dual-stage power conversion systems that use an intermediate DC voltage link [4–9]. In such systems, the DC link is usually implemented using a single capacitor in the case of two-level conversion or multiple split capacitors in the case of multi-level conversion [10,11]. This arrangement provides power decoupling between phases, and allows for independent control of AC/DC and DC/AC converters using different methods of pulse width modulation (PWM) [12–18]. The size, weight and cost of the DC-link capacitor depend on the DC link voltage reference value and power conversion system rating [19]. In addition, capacitors' limited lifetime affects the overall system reliability [20]. Hence, it is desirable to reduce both DC link voltage reference and capacitance values [21–23].

Among the various topologies, three-phase AC/DC and three-phase DC/AC converters have emerged as a viable choice for power ratings ranging from 10 kVA to 100 kVA and have found widespread use in industrial applications [24]. The efficiency, reliability and quality of output waveforms in three-level converters are significantly affected by the PWM method employed [25]. In carrier-based PWM, the main distinction between PWM methods lies in the injection of a zero-sequence voltage to balance the DC link split capacitance voltages [26]. While other dedicated hardware solutions exist for split capacitance balancing [27,28], they lead to increase in system cost and physical size. Alternatively, various methods of zero-sequence injection have been proposed over the years, with the aim of balancing the average values or the instantaneous values of the split DC link voltages [29–33]. This paper addresses the group of cases in which the harmonic content of the zero-sequence component is limited to the DC constituent only (due to, e.g., four-wire converter implementation or strict leakage current restraint). Such a limitation leads to a significant steady-state voltage ripple across split DC link capacitors, requiring the careful selection of both capacitance values and corresponding voltage set points. Previous studies evaluated these fluctuations using complex and non-analytical neutral point expressions [34,35]. Another study proposed a methodology based on instantaneous split DC coupling forces, which allows for an analytical and intuitive quantification of corresponding voltage fluctuations [36]. However, these methodologies were developed for the unity power factor only and do not account for arbitrary power factor operation.

While this paper mainly focuses on low-frequency oscillations and the influence of the power factor, frequency-related components are omitted for brevity in the present discussion and can be found in [35,37]. It is found that, under balanced operation on the AC side with any power factor, total DC link voltage remains free of low-frequency oscillations. However, split DC-link capacitors absorb power components at the triple fundamental frequency of a magnitude equivalent to one-sixth the load power affected by the power factor, resulting in out-of-phase voltage fluctuations. Reference [38] asserts that the power factor does not impact the split link capacitor ripple voltages. However, this article presents analytical expressions that contradict this claim, demonstrating that the power factor does influence the harmonic content of the capacitor voltages. Particular emphasis is placed on the third harmonic, which is the most dominant component in the evaluation. The specialized expressions are validated through simulations and experiments, providing comprehensive insights into the effect of the power factor on the behavior of the capacitor voltages. Consequently, the selection of DC link capacitors and voltage set points must consider the expected magnitudes of the AC-side phase voltages, the power factor, as well as the voltage and current ratings of the split DC link capacitors. In [39], the authors demonstrated a method to minimize the capacitance values of split DC capacitors in three-phase three-level converters, but the analysis was restricted to a unity power factor scenario. However, when the power factor deviates from unity, the above-presented analysis becomes invalid, necessitating the results presented in this paper to extend the findings in [39]. The present study is essential in providing insights and solutions for cases where the power factor is different from unity, thereby complementing and broadening the applicability of the results in [39].

The results of the proposed split DC link capacitor voltage evaluation can serve as a baseline for the evaluation of advanced high-order zero-sequence injection algorithms aiming to reduce low-frequency neutral voltage fluctuations and minimize the utilization of split DC link capacitors. The validity of the presented findings is strongly supported by simulations and experiments.

2. Steady-State Operation of a Generalized Three-Phase Three-Level AC/DC Converter

Figure 1 presents a typical three-phase dual-stage AC-DC power conversion system, comprising a three-level AC/DC (or DC/AC) converter, a DC link, and a DC/DC converter. It is important to emphasize that the direction of energy flow can be either from the AC side

(R, S, T terminals) to the DC side (W, Z terminals) or vice versa, i.e., the "Load" signifies a power source when the energy flows from the DC side to AC side. In the case of three-level conversion, the DC link is formed by three terminals (X, O, Y). During balanced operation, AC-side steady-state quantities (all discussed signals are subsequently averaged over a switching cycle) are given by

$$\begin{aligned} \vec{v}_{RST}(t) &= \begin{pmatrix} v_{RN}(t) \\ v_{SN}(t) \\ v_{TN}(t) \end{pmatrix} = V_M \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \theta) \\ \sin(\omega t + \theta) \end{pmatrix} \\ \vec{i}_{RST}(t, \varphi) &= \begin{pmatrix} i_R(t, \varphi) \\ i_S(t, \varphi) \\ i_T(t, \varphi) \end{pmatrix} = I_M \begin{pmatrix} \sin(\omega t - \varphi) \\ \sin(\omega t - \theta - \varphi) \\ \sin(\omega t + \theta - \varphi) \end{pmatrix} \end{aligned} \tag{1}$$

with $\theta = 2\pi/3$, V_M and I_M representing voltage and current magnitudes, respectively, ω symbolizing base frequency, and φ denoting an arbitrary phase.

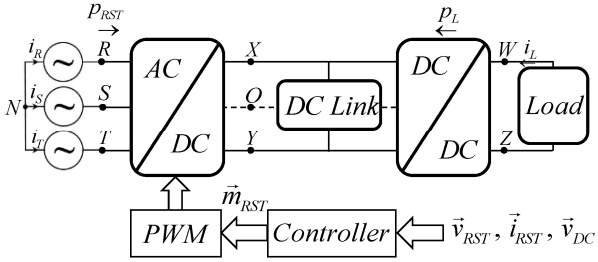


Figure 1. Generalized dual-stage AC-DC power conversion system.

AC-side voltage is attained by applying pulse-width modulation signals of the form [29]

$$\vec{m}_{RST}(t) = \begin{pmatrix} m_R(t) \\ m_S(t) \\ m_T(t) \end{pmatrix} \approx M(t) \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \theta) \\ \sin(\omega t + \theta) \end{pmatrix} + m_0(t) \tag{2}$$

created by the controller shown in Figure 1, with

$$\vec{v}_{DC}(t, \varphi) = \begin{pmatrix} v_{XO}(t, \varphi) \\ v_{YO}(t, \varphi) \end{pmatrix} \tag{3}$$

and $M(t)$, $m_0(t)$ denoting modulation index and zero-sequence component, respectively. It is considered in this paper that $m_0(t)$ contains the DC component only in steady state (allowing for an average values equalization of split DC link voltages), while in other designs it may contain both DC and high-order AC components (allowing for the equalization of split DC link voltages' instantaneous values). It should be emphasized that $m_0(t)$ may also be supplied by additional hardware-based equalization circuits [27,28].

Considering (1), the instantaneous AC-side phase power vector is given by

$$\vec{p}_{RST}(t, \varphi) = \begin{pmatrix} p_R(t, \varphi) \\ p_S(t, \varphi) \\ p_T(t, \varphi) \end{pmatrix} = \begin{pmatrix} v_{RN}(t) i_R(t, \varphi) \\ v_{SN}(t) i_S(t, \varphi) \\ v_{TN}(t) i_T(t, \varphi) \end{pmatrix} = \frac{S}{3} \begin{pmatrix} \cos\varphi - \cos 2\left(\omega t - \frac{\varphi}{2}\right) \\ \cos\varphi - \cos 2\left(\omega t - \frac{\varphi}{2} - \theta\right) \\ \cos\varphi - \cos 2\left(\omega t - \frac{\varphi}{2} + \theta\right) \end{pmatrix}, \quad S = 3\frac{V_M I_M}{2}. \tag{4}$$

Hence, total instantaneous AC-side power is ripple-free, given by

$$p_{RST}(t, \varphi) = p_R(t, \varphi) + p_S(t, \varphi) + p_S(t, \varphi) = S\cos\varphi = P_{RST}. \tag{5}$$

On the other hand, assuming load-side voltage and current are governed by

$$v_{WZ}(t) = V_L, \quad i_L(t) = I_L, \tag{6}$$

the corresponding steady-state instantaneous power is also constant, given by

$$p_L(t) = v_{WZ}(t)i_L(t) = V_L I_L = P_L. \tag{7}$$

Consequently, instantaneous system power balance (neglecting the conversion losses and energy stored in AC-side L, LC or LCL type filters [37,40] cf. Figure 2) is given by

$$P_{RST} = S\cos\varphi = V_L I_L = P_L, \tag{8}$$

indicating that the instantaneous low-frequency power flow into the DC link in Figure 1 is zero. Considering the AC/DC converter belonging to generalized three-level three-phase topology shown in Figure 2, two split capacitors, C_{DC1} and C_{DC2}, form the DC link. According to the above, $p_{DC} = p_{DC1} + p_{DC2} = P_{RST} + P_L = 0$; hence, v_{DC} is low-frequency-ripple-free without implying zero p_{DC1}, p_{DC2} and low-frequency-ripple-free v_{DC1}, v_{DC2}, as shown next. Note that the line connecting the middle point of DC link with that of the load middle point in Figure 1 is virtual and may be non-existent in reality. It is only used to demonstrate that the power element p_L may be split into two halves [41].

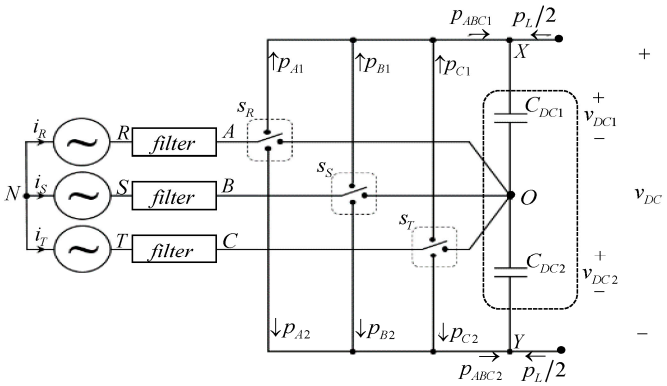


Figure 2. Three-level three-phase power conversion topology.

Since grid AC-side voltages $\vec{v}_{RST}$ and currents $\vec{i}_{RST}$ in Figure 2 cannot contain zero-sequence components (even for nonzero m_0), corresponding power vectors are given by (4). On the other hand, converter-imposed AC-side voltages $\vec{v}_{ABC} = \begin{pmatrix} v_{AN} & v_{BN} & v_{CN} \end{pmatrix}^T$ would contain DC components in case the corresponding modulation signals are DC-shifted,

$$\vec{v}_{ABC}(t) = \begin{pmatrix} v_{AN}(t) \\ v_{BN}(t) \\ v_{CN}(t) \end{pmatrix} \approx v_0(t) + V_M \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \theta) \\ \sin(\omega t + \theta) \end{pmatrix} \tag{9}$$

with v_0 denoting the shift imposed by m_0. Consequently, (cf. Figure 2)

$$\begin{aligned} \vec{p}_{A1B1C1}(t,\varphi) &= \begin{cases} \begin{pmatrix} v_{AN}(t)i_R(t,\varphi) \\ v_{BN}(t)i_S(t,\varphi) \\ v_{CN}(t)i_T(t,\varphi) \end{pmatrix}, & \vec{i}_{ABC}(t) > 0 \\ 0, & \vec{i}_{ABC} < 0 \end{cases} = \begin{pmatrix} p_{A1}(t,\varphi) + \frac{P_0}{3} \\ p_{B1}(t,\varphi) + \frac{P_0}{3} \\ p_{C1}(t,\varphi) + \frac{P_0}{3} \end{pmatrix} \\ \vec{p}_{A2B2C2}(t,\varphi) &= \begin{cases} 0, & \vec{i}_{ABC}(t) > 0 \\ \begin{pmatrix} v_{AN}(t)i_R(t,\varphi) \\ v_{BN}(t)i_S(t,\varphi) \\ v_{CN}(t)i_T(t,\varphi) \end{pmatrix}, & \vec{i}_{ABC} < 0 \end{cases} = \begin{pmatrix} p_{A2}(t,\varphi) - \frac{P_0}{3} \\ p_{B2}(t,\varphi) - \frac{P_0}{3} \\ p_{C2}(t,\varphi) - \frac{P_0}{3} \end{pmatrix} \end{aligned} \tag{10}$$

with $P_0/3$ denoting DC power component imposed by m_0. Therefore, the low-frequency partial power components exchanged between the AC side of the converter and the DC

link of the converter (again, without considering conversion losses and energy stored in AC-side filters) can be expressed as

$$\begin{aligned} p_{ABC1}(t,\varphi) &= p_{A1}(t,\varphi) + p_{B1}(t,\varphi) + p_{C1}(t,\varphi) \approx \tfrac{P_L}{2} - \Delta p_L + P_0 + p_{AC}(t,\varphi) \\ p_{ABC2}(t,\varphi) &= p_{A2}(t,\varphi) + p_{B2}(t,\varphi) + p_{C2}(t,\varphi) \approx \tfrac{P_L}{2} + \Delta p_L - P_0 - p_{AC}(t,\varphi) \end{aligned} \tag{11}$$

with p_{AC} denoting the zero-average pulsating power component and Δp_L representing load power mismatch. Note that P_0 may be either positive, negative or zero, compensating for instantaneous energy shortages in one or both split DC link capacitors. Obviously, instantaneous system power balance (8) is sustained with $P_0 = \Delta p_L$ and partial low-frequency DC link power components are given in steady state by

$$\begin{aligned} p_{DC1}(t,\varphi) &= v_{DC1}(t,\varphi) C_{DC1} \tfrac{dv_{DC1}(t,\varphi)}{dt} \approx p_{AC}(t,\varphi) \\ p_{DC2}(t,\varphi) &= v_{DC2}(t,\varphi) C_{DC2} \tfrac{dv_{DC2}(t,\varphi)}{dt} \approx -p_{AC}(t,\varphi) \end{aligned}. \tag{12}$$

In the case where partial capacitor voltages v_{DC1} and v_{DC2} are regulated to set points given by V^*_{DC1} and V^*_{DC2}, respectively, the corresponding instantaneous low-frequency energies e_{DC1} and e_{DC2} and steady-state voltages are

$$\begin{aligned} e_{DC1}(t,\varphi) &\approx \tfrac{C_{DC1}}{2}\left(V^*_{DC1}\right)^2 + \underbrace{\int p_{AC}(t,\varphi)dt}_{e_{AC}(t,\varphi)} = \tfrac{C_{DC1}}{2} v^2_{DC1}(t,\varphi) \\ e_{DC2}(t,\varphi) &\approx \tfrac{C_{DC2}}{2}\left(V^*_{DC2}\right)^2 - \underbrace{\int p_{AC}(t,\varphi)dt}_{e_{AC}(t,\varphi)} = \tfrac{C_{DC2}}{2} v^2_{DC2}(t,\varphi) \\ &\Downarrow \\ v_{DC1}(t,\varphi) &= V^*_{DC1}\sqrt{1 + \tfrac{2}{C_{DC1}\left(V^*_{DC1}\right)^2}\int p_{AC}(t,\varphi)dt} = V^*_{DC1}\sqrt{1 + \tfrac{2}{C_{DC1}\left(V^*_{DC1}\right)^2} e_{AC}(t,\varphi)} \\ v_{DC2}(t,\varphi) &= V^*_{DC2}\sqrt{1 - \tfrac{2}{C_{DC2}\left(V^*_{DC2}\right)^2}\int p_{AC}(t,\varphi)dt} = V^*_{DC2}\sqrt{1 - \tfrac{2}{C_{DC2}\left(V^*_{DC2}\right)^2} e_{AC}(t,\varphi)}, \end{aligned} \tag{13}$$

respectively. Typically,

$$V^*_{DC1} = V^*_{DC2} = 0.5V^*_{DC}, \quad C_{DC1} = C_{DC2} = C_{DC} \tag{14}$$

are employed, with V^*_{DC} denoting overall DC link voltage reference value, so that

$$\begin{aligned} &v_{DC1,2}(t,\varphi) = \\ 0.5V^*_{DC}\sqrt{1 \pm \tfrac{2}{\left(0.5V^*_{DC}\right)^2 C_{DC}} e_{AC}(t,\varphi)} &\approx 0.5V^*_{DC} \pm \underbrace{\frac{1}{0.5V^*_{DC}C_{DC}} e_{AC}(t,\varphi)}_{\Delta v_{DC}(t)}, \quad \tfrac{2\max\limits_{t,\varphi}|e_{AC}(t,\varphi)|}{\left(0.5V^*_{DC}\right)^2 C_{DC}} << 1 \end{aligned} \tag{15}$$

i.e., split capacitor voltages contain DC components as well as the nonzero opposite-phase AC voltage ripples. The approximation in (15) is valid in practical systems where the AC ripple magnitude is much lower than the DC component [42]. As a result, each instantaneous partial DC link capacitor's voltage is bounded by

$$0.5V^*_{DC} - \frac{E_{AC}(\varphi)}{0.5V^*_{DC}C_{DC}} < v_{DC1,2}(t,\varphi) < 0.5V^*_{DC} + \frac{E_{AC}(\varphi)}{0.5V^*_{DC}C_{DC}}, \tag{16}$$

with

$$E_{AC}(\varphi) = \max_t |e_{AC}(t,\varphi)|. \tag{17}$$

3. Steady-State Generalization and Evaluation of Pulsating Components

In order to generalize the discussion, consider normalized quantities given by

$$\begin{aligned}\vec{v}^{\,pu}_{RST}(t) &= \begin{pmatrix} v^{pu}_R(t) \\ v^{pu}_S(t) \\ v^{pu}_T(t) \end{pmatrix} = \frac{\vec{v}_{RST}(t)}{0.5V^*_{DC}} = \frac{V_M}{0.5V^*_{DC}} \begin{pmatrix} \sin(\omega t) \\ \sin(\omega t - \theta) \\ \sin(\omega t + \theta) \end{pmatrix}, \\ \vec{p}^{\,pu}_{RST}(t,\varphi) &= \begin{pmatrix} p^{pu}_R(t) \\ p^{pu}_S(t) \\ p^{pu}_T(t) \end{pmatrix} = \frac{\vec{p}_{RST}(t,\varphi)}{3S} = \frac{1}{3} \begin{pmatrix} \cos\varphi - \cos 2\left(\omega t - \frac{\varphi}{2}\right) \\ \cos\varphi - \cos 2\left(\omega t - \frac{\varphi}{2} - \theta\right) \\ \cos\varphi - \cos 2\left(\omega t - \frac{\varphi}{2} + \theta\right) \end{pmatrix}\end{aligned} \tag{18}$$

so that

$$p^{pu}_{RST}(t,\varphi) = \frac{p_{RST}(t,\varphi)}{S} = \frac{p_L}{S} = p^{pu}_L = \cos\varphi. \tag{19}$$

Likewise, assuming $P_0 = \Delta p_L$, there is

$$\begin{aligned}\vec{p}^{\,pu}_{A1B1C1}(t,\varphi) &= \begin{pmatrix} p^{pu}_{A1}(t,\varphi) \\ p^{pu}_{B1}(t,\varphi) \\ p^{pu}_{C1}(t,\varphi) \end{pmatrix} = \frac{1}{5} \begin{cases} \begin{pmatrix} v_{AN}(t) i_R(t,\varphi) \\ v_{BN}(t) i_S(t,\varphi) \\ v_{CN}(t) i_T(t,\varphi) \end{pmatrix}, & \vec{i}_{ABC}(t) > 0 \\ 0, & \vec{i}_{ABC} < 0 \end{cases}, \\ \vec{p}^{\,pu}_{A2B2C2}(t,\varphi) &= \begin{pmatrix} p^{pu}_{A2}(t,\varphi) \\ p^{pu}_{B2}(t,\varphi) \\ p^{pu}_{C2}(t,\varphi) \end{pmatrix} = \frac{1}{5} \begin{cases} 0, & \vec{i}_{ABC}(t) > 0 \\ \begin{pmatrix} v_{AN}(t) i_R(t,\varphi) \\ v_{BN}(t) i_S(t,\varphi) \\ v_{CN}(t) i_T(t,\varphi) \end{pmatrix}, & \vec{i}_{ABC} < 0 \end{cases}\end{aligned} \tag{20}$$

so that

$$\begin{aligned} p^{pu}_{ABC1}(t,\varphi) &= \frac{p_{ABC1}(t,\varphi)}{S} = p^{pu}_{A1}(t,\varphi) + p^{pu}_{B1}(t,\varphi) + p^{pu}_{C1}(t,\varphi) \\ &\approx \frac{\cos\varphi}{2} + \frac{p_{AC}(t,\varphi)}{S} = \frac{p^{pu}_L}{2} + p^{pu}_{AC}(t,\varphi) \\ p^{pu}_{ABC2}(t,\varphi) &= \frac{p_{ABC2}(t,\varphi)}{S} = p^{pu}_{A2}(t,\varphi) + p^{pu}_{B2}(t,\varphi) + p^{pu}_{C2}(t,\varphi) \\ &\approx \frac{\cos\varphi}{2} - \frac{p_{AC}(t,\varphi)}{S} = \frac{p^{pu}_L}{2} - p^{pu}_{AC}(t,\varphi) \end{aligned}. \tag{21}$$

Lastly, normalized pulsating energy swing magnitude is obtained as

$$E^{pu}_{AC}(\varphi) = \frac{E_{AC}(\varphi)}{S} = \frac{1}{S}\max_t |e_{AC}(t,\varphi)| = \max_t \left| e^{pu}_{AC}(t,\varphi) \right| = \max_t \left| \int p^{pu}_{AC}(t,\varphi) \right|. \tag{22}$$

Figure 3 illustrates the resulting normalized waveforms, with Figure 3a–c corresponding to individual phase voltages, currents and instantaneous power components as well as total AC-side power (cf. 18), (19)). Figure 3d presents normalized partial DC-side power components cf. (20) (upper ones only are shown for brevity), each possessing average value of $p^{pu}_{RST}/6 = \cos\varphi/6$. The corresponding total upper partial DC-side power cf. (21) is depicted in Figure 3e, possessing an average value of $p^{pu}_{RST}/2 = \cos\varphi/2$. Subtracting the average value from the total upper partial DC-side power yields a normalized partial pulsating power component p^{pu}_{AC}, shown in Figure 3f. Lastly, the normalized pulsating energy component e^{pu}_{AC} obtained by integrating p^{pu}_{AC} is depicted in Figure 3g with normalizing pulsating energy swing magnitude shown in the same subplot.

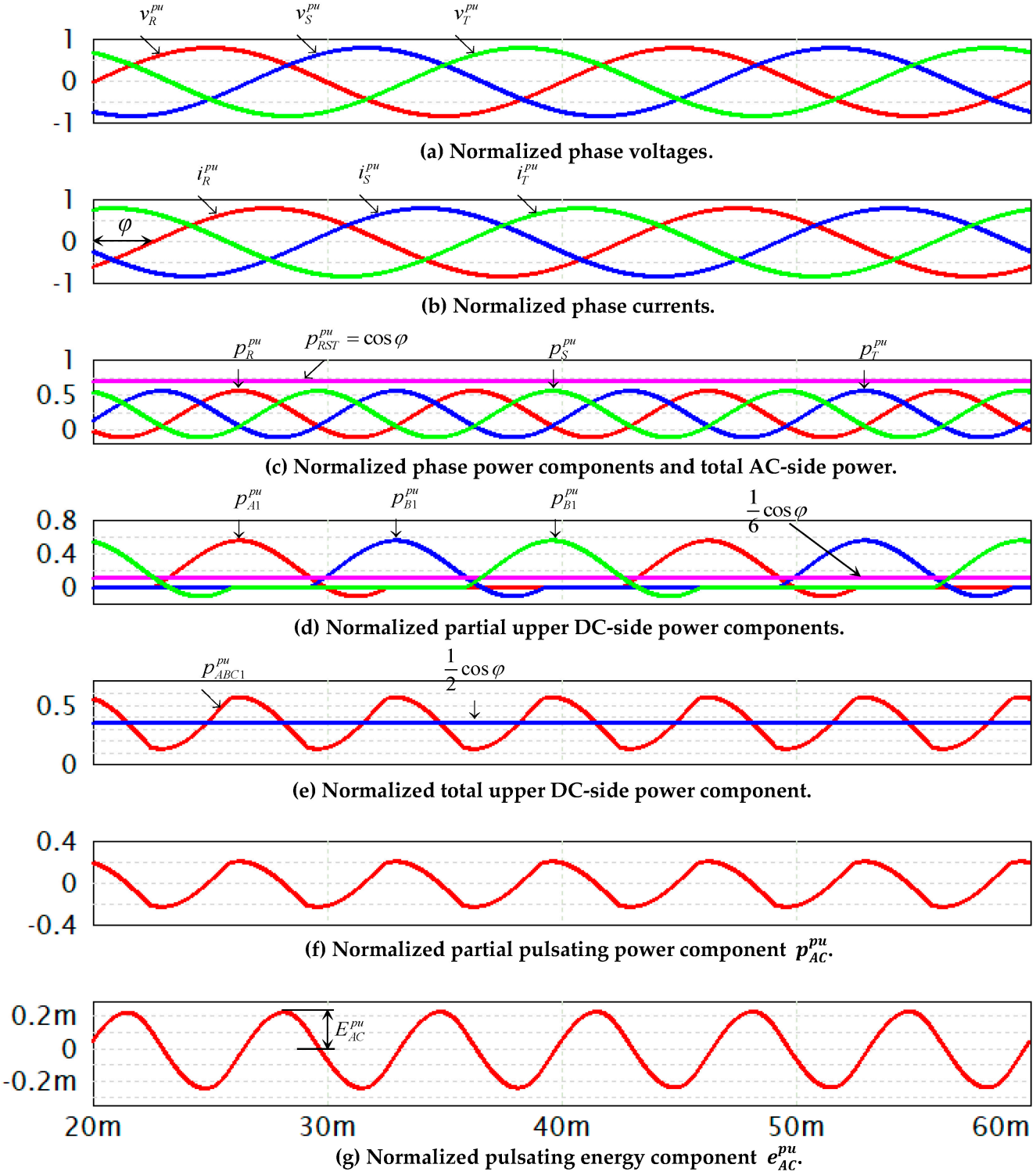


Figure 3. Generalized normalized operational waveforms.

In order to demonstrate the operating power factor's influence on partial power components, Figure 4 depicts the spectra (excluding the DC component) of normalized partial upper DC-side powers p_{A1}^{pu}, p_{B1}^{pu}, p_{C1}^{pu} for different values of φ.

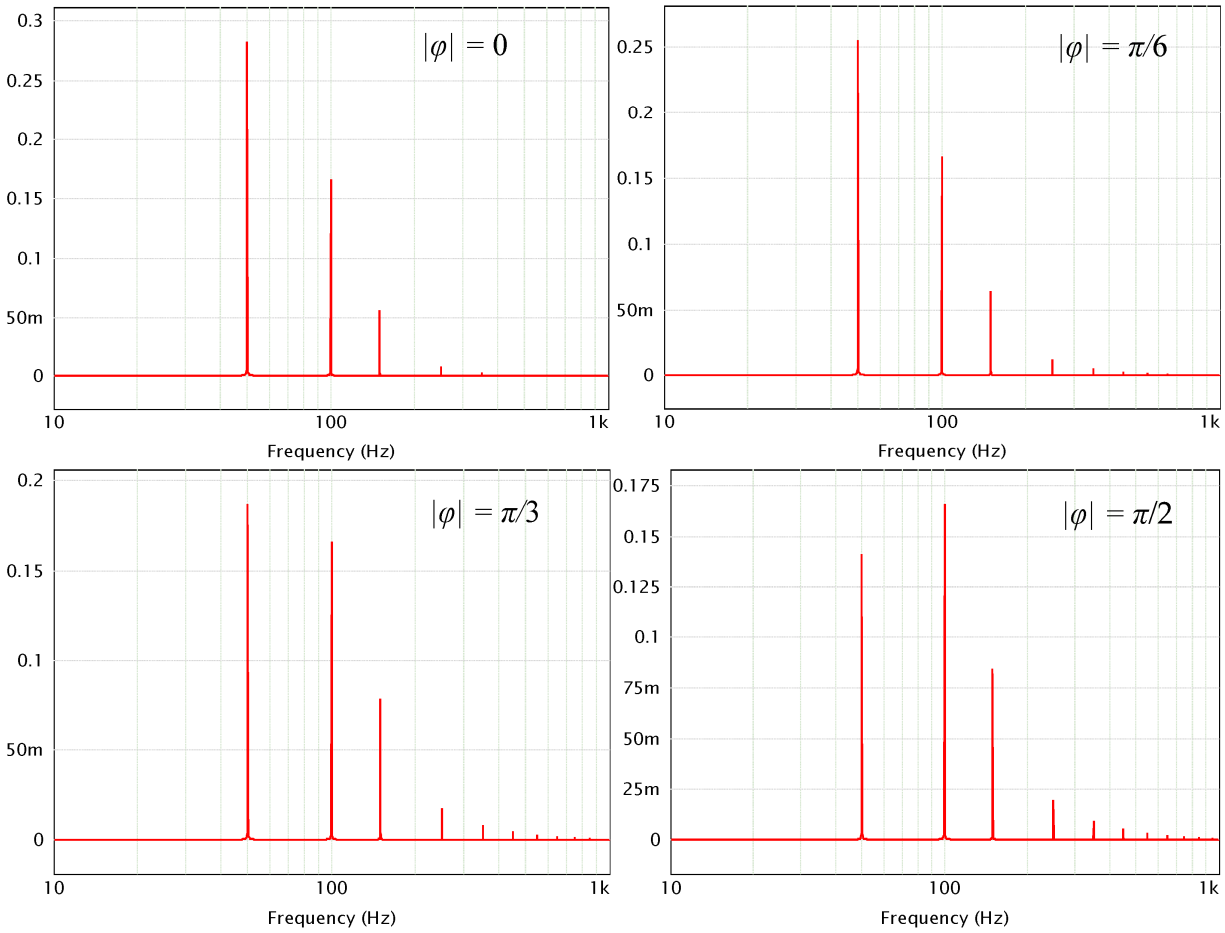


Figure 4. AC component spectra of normalized partial DC-side powers p^{pu}_{A1}, p^{pu}_{B1}, p^{pu}_{C1}.

It is well-evident that operating power factor considerably influences the harmonic content of normalized partial DC-side powers. It is interesting to note that, upon a decrease in power factor, the first harmonic magnitude reduces while the rest of the harmonic magnitudes inrease. As shown in [36,39] (and evident from Figure 4), normalized partial upper DC-side power components p^{pu}_{A1}, p^{pu}_{B1}, p^{pu}_{C1} are given by

$$\begin{aligned} p^{pu}_{A1}(t,\varphi) &= \tfrac{\cos\varphi}{6} + P^{pu}_2(\varphi)\sin(2\omega t + \alpha_2(\varphi)) + \sum_{n=1,\ldots odd}^{\infty} P^{pu}_n(\varphi)\sin(n\omega t + \alpha_n(\varphi)) \\ p^{pu}_{B1}(t,\varphi) &= p^{pu}_{A1}(t - \tfrac{2\pi}{3\omega},\varphi) \\ p^{pu}_{C1}(t,\varphi) &= p^{pu}_{A1}(t + \tfrac{2\pi}{3\omega},\varphi) \end{aligned} \tag{23}$$

Consequently, cf. (21),

$$p^{pu}_{AC}(t) = 3\sum_{n=3k}^{\infty} P^{pu}_n(\varphi)\sin(n\omega t + \alpha_n(\varphi)), \quad k = odd \tag{24}$$

with corresponding spectra depicted in Figure 5 for different values of φ.

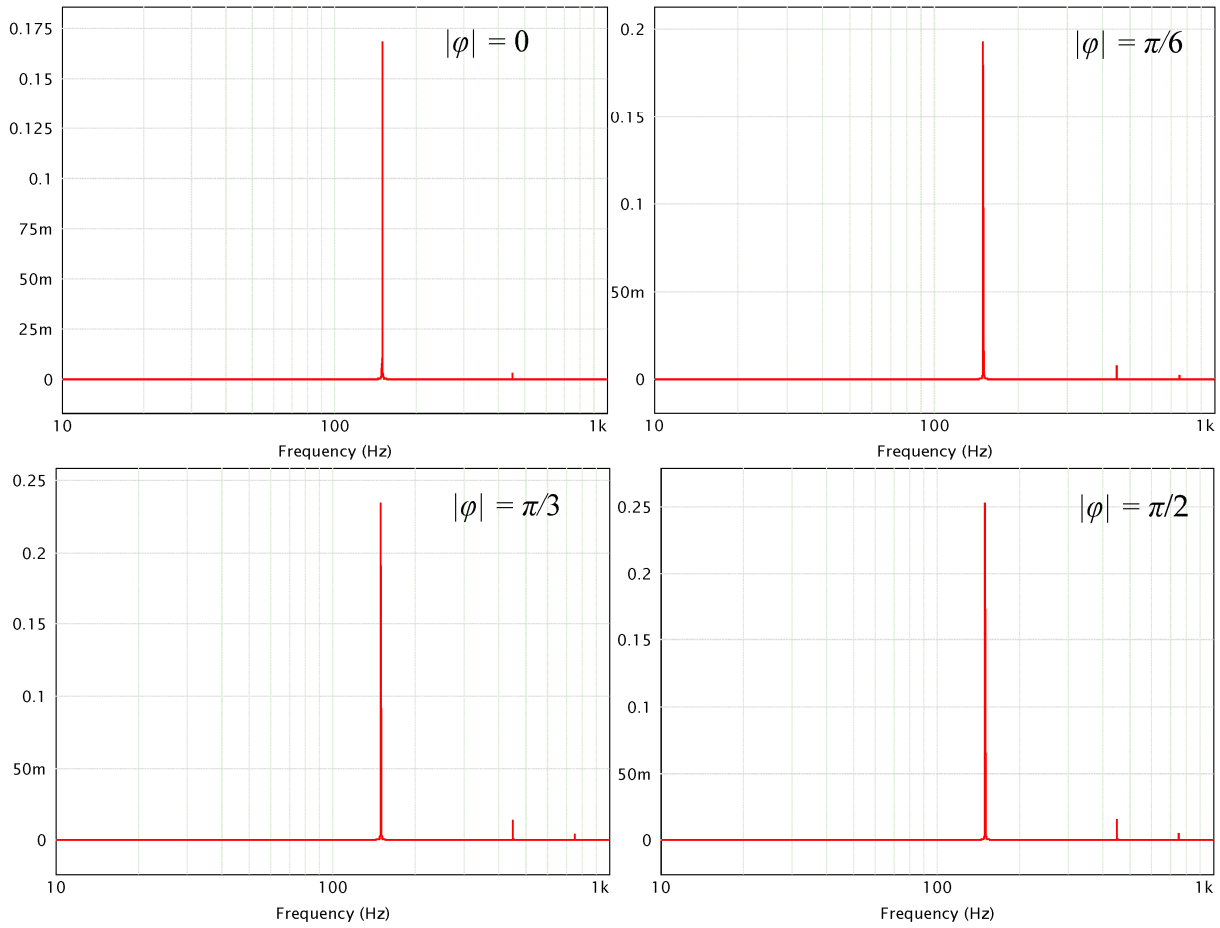


Figure 5. Spectra of normalized partial pulsating power component p_{AC}^{pu}.

It is again evident that operating power factor significantly influences the harmonic content of the normalized partial pulsating power component p_{AC}^{pu}. Moreover, it is obvious that the third harmonic dominates the spectra. Consequently, (24) may be approximated as

$$p_{AC}^{pu}(t) \cong 3P_3^{pu}(\varphi)\sin(3\omega t + \alpha_3(\varphi)). \tag{25}$$

Integrating (27) yields

$$e_{AC}^{pu}(t,\varphi) = \int p_{AC}^{pu}(t,\varphi)dt = -\frac{3P_3^{pu}(\varphi)}{3\omega}\cos(3\omega t + \alpha_3(\varphi)) \tag{26}$$

so that normalized pulsating energy swing magnitude is obtained as (cf. (22))

$$E_{AC}^{pu}(\varphi) = \frac{P_3^{pu}(\varphi)}{\omega}. \tag{27}$$

Combining this with (15), the partial DC link voltage ripple component is given by

$$\Delta v_{DC}(t,\varphi) = \frac{1}{0.5V_{DC}^{*}C_{DC}}e_{AC}(t,\varphi) = -\Delta V(\varphi)\cos(3\omega t + \alpha_3(\varphi)) \tag{28}$$

with

$$\Delta V(\varphi) = \frac{S}{0.5V_{DC}^{*}C_{DC}}E_{AC}^{pu}(\varphi). \tag{29}$$

Contrary to the statement in [38], it turns out that the power factor influences both the amplitude ΔV and the phase α_3 of the partial DC link voltage ripple component. It is important to emphasize that the normalized pulsating energy swing magnitude (27) and the phase α_3 are generalized quantities that are valid for a given mains frequency ω, irrespective of system rated power, partial DC link capacitance values and corresponding voltage set points. Unfortunately, it is nearly impossible to obtain an analytical expression for both quantities. Consequently, multiple numerical simulations are carried out for different operating power factor values under 50 Hz mains frequency to evaluate the two parameters. Subsequently, polynomial approximations were derived based on the results, as shown in Figure 6. The following generalized expressions are obtained:

$$\begin{aligned} E_{AC}^{pu}(\varphi) &\approx \left(-84.46|\cos\varphi|^4 + 116.3|\cos\varphi|^3 - 124.1|\cos\varphi|^2 + 9.197|\cos\varphi| + 265.1\right) \cdot 10^{-6}\left[\tfrac{J}{VA}\right] \\ \alpha_3(\varphi) &\approx \left(-308.1|\cos\varphi|^4 + 410.7|\cos\varphi|^3 - 196.7|\cos\varphi|^2 + 9.883|\cos\varphi| + 86.87\right) \cdot \tfrac{2\pi}{360^\circ}[rad] \end{aligned} \tag{30}$$

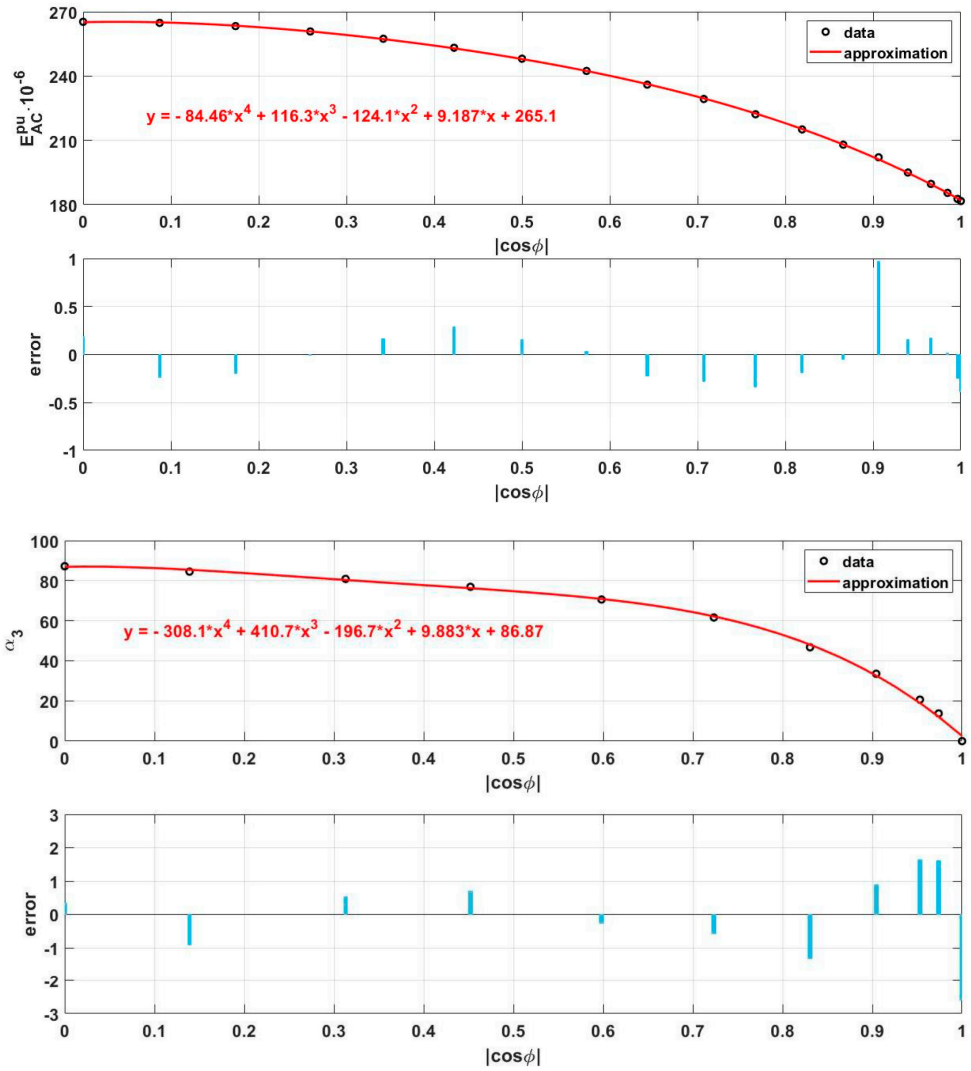


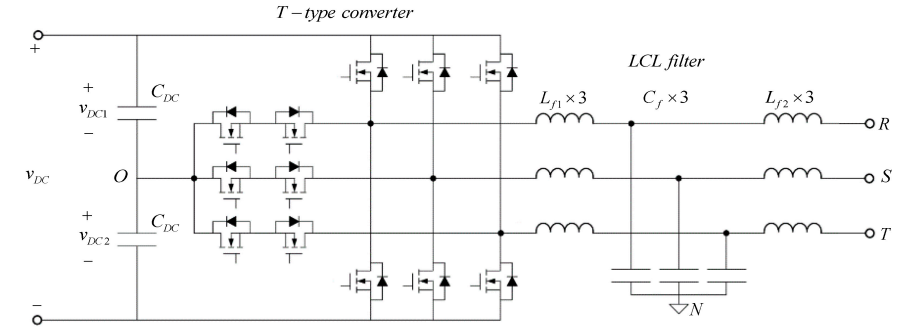
Figure 6. Magnitude (**top**) and phase (**bottom**) of pulsating energy component versus cosφ.

The obtained numerical expressions can be readily adapted to any system through a straightforward calculation of the DC link voltage ripple amplitude cf. (29). The inherent generality and adaptability of the expression makes it applicable across various systems, facilitating efficient evaluations and comparisons in different practical scenarios. It is important to note that, in case of operation under 60 Hz mains frequency, the first polynomial

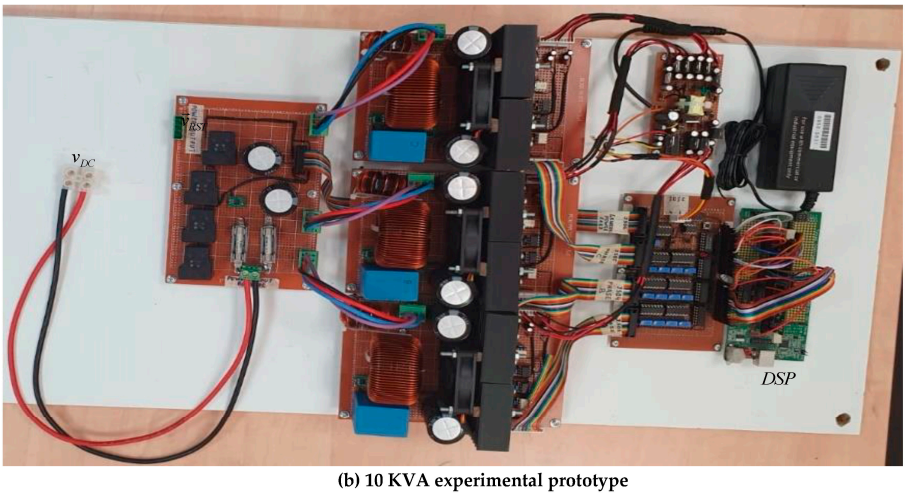
in (30) (magnitude) should be multiplied by 5/6 due to the frequency dependence in (27) while the second one (phase) should be left unchanged.

4. Validation

In order to validate the proposed methodology, a 10 kVA LCL-filter-based, three-phase, three-level, T-type converter, as shown in Figure 7a is employed. A corresponding experimental prototype, based on design guidelines given in [41], is shown in Figure 7b. The converter was operated at 50 kHz switching frequency using the Texas Instruments TMS320F28335 DSP [43]. The power stage was supplied from an 800 V DC power source and connected to a three-phase balanced load. Partial DC link capacitances of 440 μF, possessing equivalent series resistances (ESR) of 0.5 Ohm, were used [44]. Pulse-width modulation signals (2) with M = 325/400 were applied to operate the power stage in a semi-open-loop, feeding the load with a balanced three-phase 50 Hz, 400 V supply. The value of $m_0(t)$ was generated in closed-loop fashion, as shown in Figure 8, where NF_{150} represents a 150 Hz-tuned notch filter aiming to remove the triple-mains-frequency ripple, with K_0 denoting a constant gain [38]. Three experiments were performed under the rated loading, operating with different power factors, accompanied by matching PSIM software simulations. Corresponding results are shown in Figures 9–11 (only one phase current and voltage are shown experimentally, due to four-channel oscilloscope usage, along with partial DC link voltage ripples).



(a) Power stage circuitry



(b) 10 KVA experimental prototype

Figure 7. T-type three-phase three-level power converter.

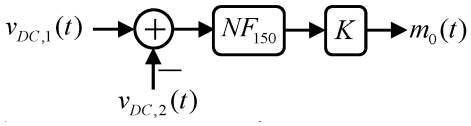


Figure 8. Generation of zero-sequence component $m_0(t)$.

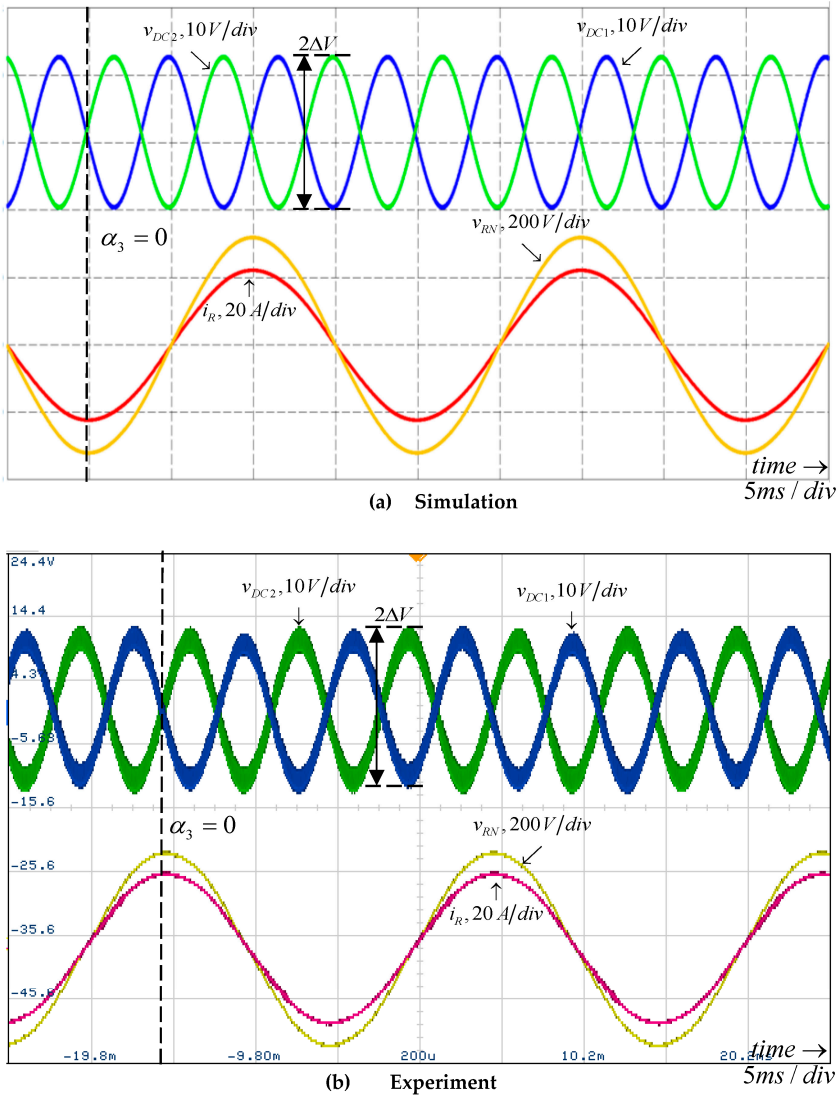


Figure 9. Results under rating loading with cosφ = 1.

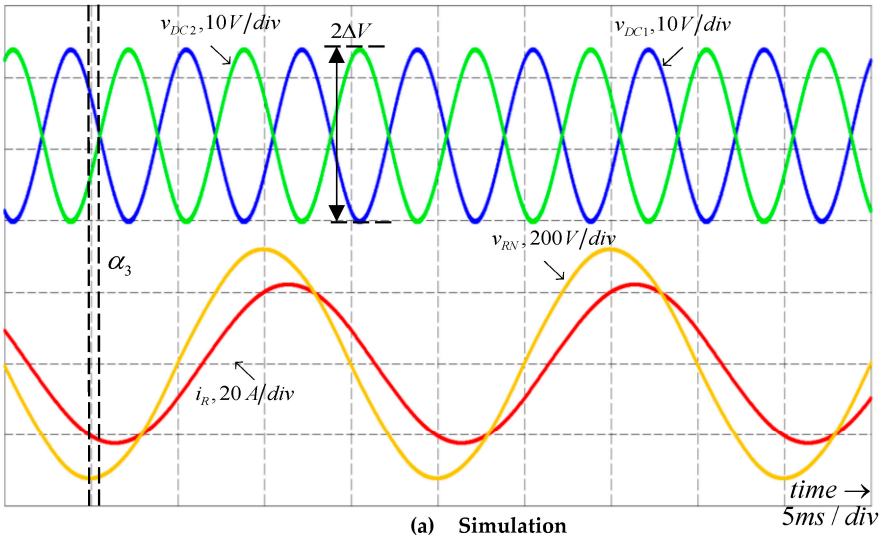


Figure 10. *Cont.*

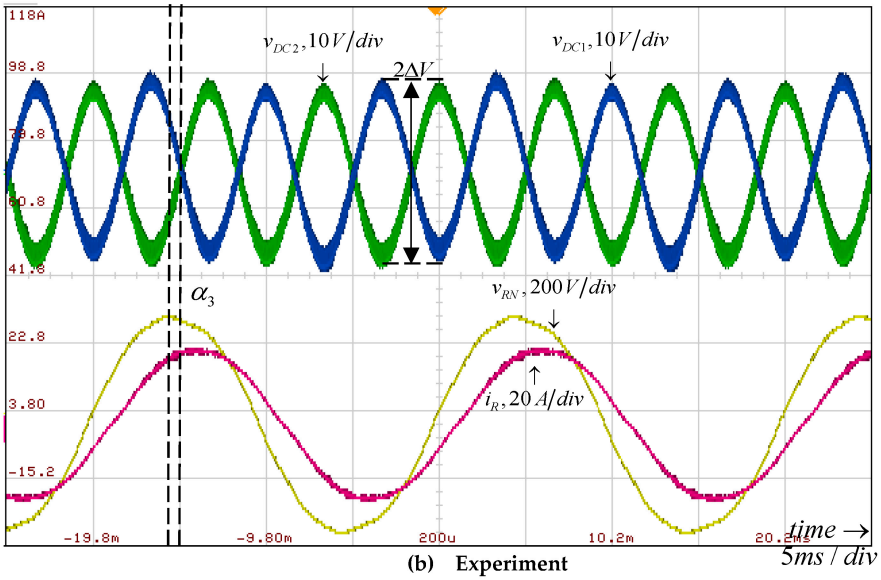


Figure 10. Results under rating loading with cosφ = 0.9.

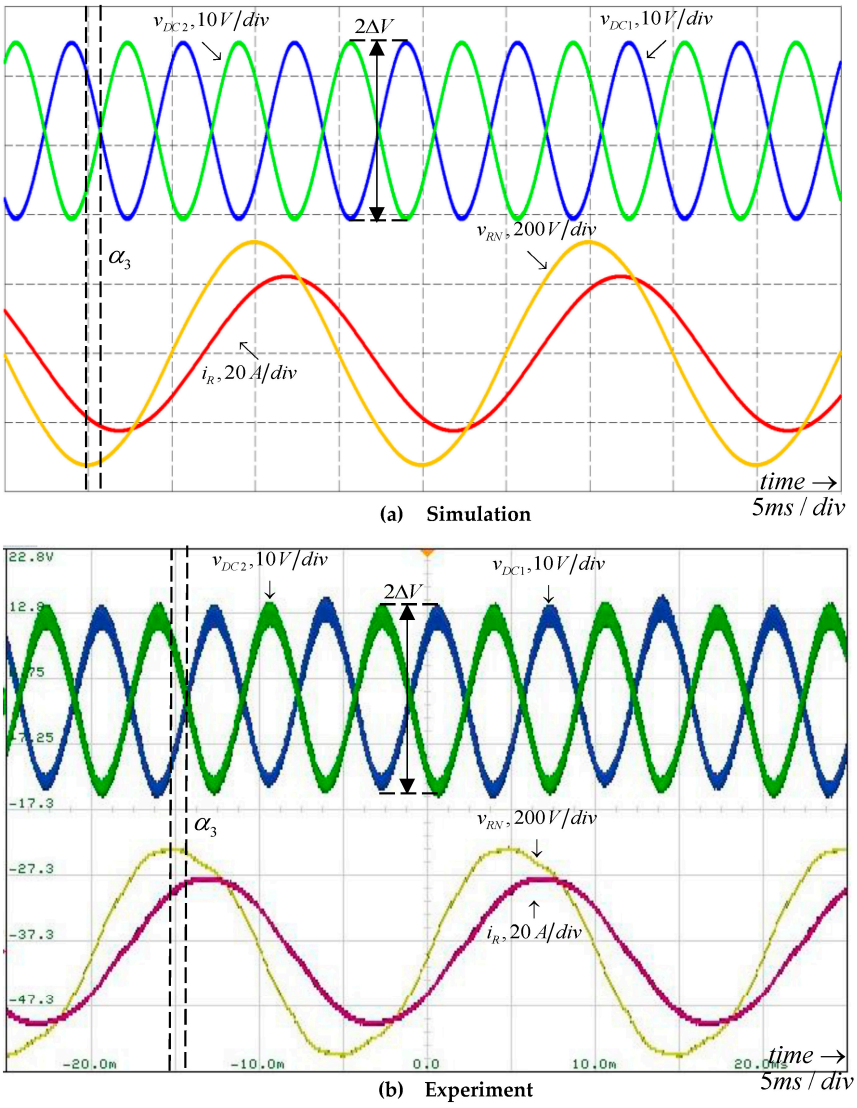


Figure 11. Results under rating loading with cosφ = 0.83.

Figure 12 presents a comparison between the simulations, experimental results and corresponding analytical predictions. A near-perfect match between simulation results and analytical predictions is obvious, supporting the presented methodology. On the other hand, some deviations are visible between experiments and simulations/analytical predictions. These may be explained by voltage drops across capacitor ESRs, which were neglected in simulations and during theoretical modeling. In order to support this assumption, the ESR of electrolytic capacitors was included in simulations. Corresponding results are shown in Figure 12 as "Simulation (ESR)". It is evident that the modified simulation model outcomes accurately coincide with the experimental results, supporting the above assumption.

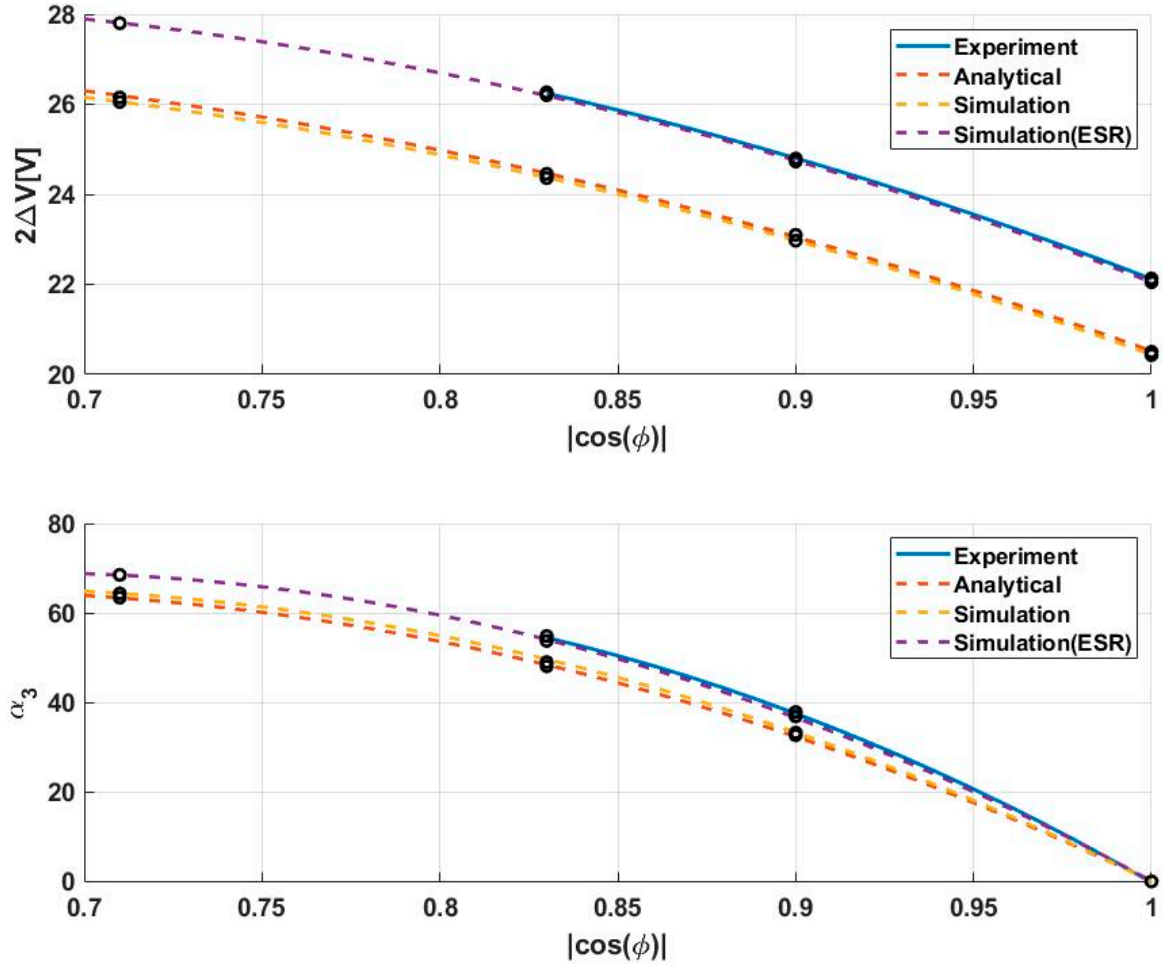


Figure 12. Comparison between simulations, experimental results and corresponding analytical predictions.

5. Conclusions

The article presents an evaluation of the impact of power factor on the ripple voltage of split DC link capacitors in three-phase three-level converters. The results indicate that deviations from the unity power factor leads to an increase in the amplitude of harmonic content and a phase shift. Due to the fact that the non-unity power factor gives rise to rich harmonic content, analytical expression derivations are non-feasible. As a result, a numerical analysis was carried out to obtain generalized relations of normalized pulsating energy magnitude and phase with the operating power factor. The obtained numerical expressions can be readily adapted to any system through a straightforward calculation of partial DC link voltages' ripple amplitude and phase. Simulations and experiments carried out by applying the proposed methodology to a 10 kVA T-type converter successfully validated the revealed findings.

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References

1. Bose, B.K. Multi-Level Converters. *Electronics* **2015**, *4*, 582–585. [CrossRef]
2. Franquelo, L.G.; Leonand, J.; Rodriguez, J. The age of multilevel converters arrives. *IEEE Ind. Electron. Mag.* **2008**, *2*, 28–39. [CrossRef]
3. Rodriguez, J.; Lai, J.-S.; Peng, F.Z. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
4. Norões, M.; Jacobina, C.B.; Carlos, G.A. A new three-phase ac–dc–ac multilevel converter based on cascaded three-leg converters. *IEEE Trans. Ind. Appl.* **2017**, *53*, 2210–2221.
5. Zhou, D.; Zhao, J.; Li, Y. Model-predictive control scheme of five-leg ac–dc–ac converter-fed induction motor drive. *IEEE Trans. Ind. Electron.* **2016**, *63*, 4517–4526. [CrossRef]
6. Lima, M.; Cursino, B.J.; Rocha, N.; Santos, E.C. Ac–dc–ac three-phase converter based on three three-leg converters connected in series. *IEEE Trans. Ind. Appl.* **2016**, *52*, 3171–3181.
7. Filho, S.; Cipriano, O.; de Almeida, B.R.; Souza, D.; Neto, T.R.F. High-frequency isolated AC–DC–AC interleaved converter for power quality applications. *IEEE Trans. Ind. Appl.* **2018**, *54*, 4594–4602. [CrossRef]
8. Norões, M.; Jacobina, C.B.; Freitas, N.B.; Queiroz, A.; Silva, E.R.C. Three-phase four-wire ac–dc–ac multilevel topologies obtained from an interconnection of three-leg converters. *IEEE Trans. Ind. Appl.* **2018**, *54*, 4728–4738.
9. Norões, M.; Jacobina, C.B.; Freitas, N.B.; Vitorino, M.A. Investigation of three-phase ac–dc–ac multilevel nine-leg converter. *IEEE Trans. Ind. Appl.* **2016**, *52*, 4156–4169.
10. Kaufhold, E.; Meyer, J.; Schegner, P. Measurement-based identification of DC-link capacitance of single-phase power electronic devices for grey-box modelling. *IEEE Trans. Power Electron.* **2021**, *37*, 454–4552.
11. Khalil, A.; Ahmed, G.; Lee, D.C. DC-link capacitance estimation in AC/DC/AC PWM converters using voltage injection. *IEEE Trans. Ind. Appl.* **2008**, *44*, 1631–1637. [CrossRef]
12. Divan, D.; Habetler, T.; Lipo, T. PWM techniques for voltage source inverters. *Proc. PESC* **1990**.
13. Laszlo, H.; Kumar, M.; Jovanović, M.M. Performance comparison of three-step and six-step PWM in average-current-controlled three-phase six-switch boost PFC rectifier. *IEEE Trans. Power. Electron.* **2016**, *31*, 7264–7272.
14. Strajnikov, P.; Kuperman, A. Guidelines for voltage controller coefficients design to attain prescribed grid current THD and DC-link voltage undershoot values in power factor correction front ends. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 6523–6533. [CrossRef]
15. Xiong, X.; Zhang, Y.; Wang, J.; Du, H. An improved model predictive control scheme for the PWM rectifier-inverter system based on power-balancing mechanism. *IEEE Trans. Ind. Electron.* **2016**, *63*, 5197–5208.
16. Sahraoui, K.; Gaoui, B. Reconfigurable control of PWM AC-DC-DC converter without redundancy leg supplying an ac motor drive. *Period. Polytech. Electr. Eng. Comp. Sci.* **2021**, *65*, 74–81. [CrossRef]
17. Lu, Y.; Zhao, Z.; Lu, T.; Yang, S.; Zou, G. An improved DC-link voltage fast control scheme for a PWM rectifier-inverter system. *IEEE Trans. Ind. Appl.* **2014**, *50*, 462–473.
18. Iqbal, A.; Lewicki, A.; Morawiec, M. Pulse-Width Modulation of Power Electronic DC–AC Converter. In *High Performance Control of AC Drives with MATLAB®/Simulink*, 2nd ed.; Wiley: Hoboken, NJ, USA, 2021.
19. Pu, X.-S.; Nguyen, T.H.; Lee, D.-C.; Lee, K.-B.; Kim, J.-M. Fault diagnosis of DC-link capacitors in three-phase AC/DC PWM converters by online estimation of equivalent series resistance. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4118–4127. [CrossRef]
20. Pu, X.-S.; Nguyen, T.H.; Lee, D.-C.; Lee, S.-G. Identification of DC-link capacitance for single-phase AC/DC PWM converters. *J. Pow. Electron.* **2010**, *10*, 270–276. [CrossRef]
21. Hur, N.; Jung, J.; Nam, K. A fast dynamic DC-link power-balancing scheme for a PWM converter-inverter system. *IEEE Trans. Ind. Electron.* **2001**, *48*, 794–803.
22. Gu, B.-G.; Nam, K. A DC-link capacitor minimization method through direct capacitor current control. *IEEE Trans. Ind. Appl.* **2006**, *42*, 573–581.
23. Malesani, L.; Rossetto, L.; Tenti, P.; Tomasin, P. AC/DC/AC PWM converter with reduced energy storage in the DC link. *IEEE Trans. Ind. Appl.* **1995**, *31*, 287–292. [CrossRef]

24. Stecca, M.; Soeiro, T.B.; Elizondo, L.R.; Bauer, P.; Palensky, P. Comparison of two and three-level DC-AC converters for a 100 kW battery energy storage system. In Proceedings of the 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), Delft, The Netherlands, 17–19 June 2020; pp. 677–682.
25. Novak, M.; Sangwongwanich, A.; Blaabjerg, F. Online optimization of zero-sequence voltage injection of PWM strategy for 3L-NPC converters. In Proceedings of the 2022 International Power Electronics Conference (IPEC-Himeji 2022-ECCE Asia), Himeji, Japan, 15–19 May 2022; pp. 2405–2411.
26. Sangwongwanich, A.; Novak, M.; Sangwongwanich, S.; Blaabjerg, F. Reliability of DC-link capacitors in three-level NPC inverters under different PWM methods. In Proceedings of the 2022 IEEE Applied Power Electronics Conference and Exposition (APEC), Houston, TX, USA, 20–24 March 2022; pp. 1804–1811.
27. In, H.-C.; Kim, S.-M.; Lee, K.-B. Design and control of small DC-link capacitor-based three-level inverter with neutral-point voltage balancing. *Energies* **2018**, *11*, 1435. [CrossRef]
28. Zielinski, C.; Stefanczak, B.; Jedrus, K. Phase-independent reactive power compensation based on four-wire power converter in the presence of angular asymmetry between voltage vectors. *Energies* **2022**, *15*, 497. [CrossRef]
29. Cao, D.P.; Song, W.X.; Xi, H.; Chen, G.C.; Chen, C. Research on zero-sequence signal of space-vector modulation for three-level neutral-point-clamped inverter based on vector diagram partition. In Proceedings of the 2009 IEEE 6th International Power Electronics and Motion Control Conference, Wuhan, China, 17–20 May 2009; pp. 1435–1439.
30. Helle, L.; Munk-Nielsen, S.; Enjeti, P. Generalized discontinuous DC-link balancing modulation strategy for three-level inverters. In Proceedings of the Power Conversion Conference-Osaka 2002 (Cat. No.02TH8579), Osaka, Japan, 2–5 April 2002; pp. 359–366.
31. Song, Q.; Liu, W.; Yu, Q.; Xie, X.; Wang, Z. A neutral-point potential balancing algorithm for three-level NPC inverters using analytically injected zero-sequence voltage. *Proc. IEEE. Appl. Pow. Electron. Conf.* **2003**, *1*, 228–233.
32. Pou, J.; Zaragoza, J.; Rodriguez, P.; Ceballos, S.; Sala, V.M.; Burgos, R.P.; Boroyevich, D. Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point. *IEEE Trans. Ind. Electron.* **2007**, *54*, 2288–2294. [CrossRef]
33. Alemi; Jeung, Y.-C.; Lee, D.-C. DC-link capacitance minimization in T-type three-level AC/DC/AC PWM converters. *IEEE Trans. Ind. Electron.* **2015**, *62*, 1382–1391.
34. JPou; Pindado, R.; Boroyevich, D.; Rodriguez, P. Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. *IEEE Trans. Ind. Electron.* **2005**, *52*, 1582–1588. [CrossRef]
35. Gopalakrishnan, K.S.; Janakiraman, S.; Das, S.; Narayanan, G. Analytical evaluation of DC capacitor RMS current and voltage ripple in neutral-point clamped inverters. *Sadhana* **2017**, *42*, 827–839. [CrossRef]
36. Siton, Y.; Sitbon, M.; Aaron, I.; Lineykin, S.; Baimel, D.; Kuperman, A. On the minimum value of split DC link capacitances in three-phase three-level grid-connected converters operating with unity power factor with limited zero-sequence Injection. *Electronics* **2023**, *12*, 1994. [CrossRef]
37. Orfanoudakis, G.I.; Sharkh, M.A.Y.S.M. Analysis of dc-link capacitor current in three-level neutral point clamped and cascaded H-bridge inverters. *IET Power Electron.* **2013**, *6*, 1376–1389. [CrossRef]
38. Siton, Y.; Yuhimenko, V.; Baimel, D.; Kuperman, A. Baseline for split DC-link design in three-phase three-level converters operating with unity power factor based on low-frequency partial voltage oscillations. *Machines* **2022**, *10*, 722. [CrossRef]
39. Kui-Jun, L. Analytical modeling of neutral point current in T-type three-level PWM converter. *Energies* **2020**, *13*, 1324.
40. Beres, R.N.; Wang, X.; Liserre, M.; Blaabjerg, F.; Bak, C.L. A review of passive power filters for three-phase grid-connected voltage-source converters. *IEEE J. Emerg. Sel. Top. Pow. Electron.* **2016**, *4*, 54–69. [CrossRef]
41. Singer, S.; Erickson, R.W. Power-source element and its properties. *IEE Proc. Circ. Dev. Syst.* **1994**, *141*, 220–226. [CrossRef]
42. Mellinkovsky, M.; Yuhimenko, V.; Zhong, Q.C.; Peretz, M.M.; Kuperman, A. Active DC link capacitance reduction in grid-connected power conversion systems by direct voltage regulation. *IEEE Access* **2018**, *6*, 18163–18173. [CrossRef]
43. Available online: https://www.ti.com/lit/ug/tidue53f/tidue53f.pdf (accessed on 21 September 2023).
44. Available online: https://product.tdk.com/system/files/dam/doc/product/capacitor/aluminum-electrolytic/snap-in/data_sheet/20/30/db/aec/b43643.pdf (accessed on 21 September 2023).