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A Wideband and Low Reference Spur PLL with Clock Feedthrough Suppressed and Low Current Mismatch Charge Pump and Symmetrical CML Divider

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Abstract: This paper presents the design and performance analysis of a wideband charge-pump phase-locked loop (CPPLL) characterized by low reference spur and low phase noise. The proposed CPPLL, operating as a wideband phase-locked loop (PLL) with a reference frequency of 100 MHz, achieves a wide tuning range of 40% from 2.0 GHz to 3.0 GHz. A clock feedthrough suppressed charge pump with additional bias current branches is used to reduce the PLL's loop reference spur. The 4-stage current mode logic (CML) divide-by-2/3 circuit is utilized in the frequency divider to achieve high-speed frequency division. The circuit of an AND gate and latch in the 2/3 divider adopts a full differential symmetric structure to minimize the phase error of high-frequency differential signals. The voltage-controlled oscillator (VCO) is designed to provide a wide tuning range while optimizing the trade-off between the phase noise and power consumption. The fabricated PLL is implemented using a 0.13 µm CMOS process. Experimental measurements reveal a reference spur of −74.39 dBc at an oscillation frequency of 2.4 GHz. Moreover, the CPPLL achieves phase noise of −102.55 dBc/Hz@100 kHz and −127.15 dBc/Hz@1 MHz, while consuming 33.6 mW under a 1.2 V supply voltage. The integrated root-mean-square (rms) jitter, measured from 10 kHz to 10 MHz, is 340.99 fs, and the figure-of-merit (FoM) is −234.08 dB at a carrier frequency of 2.4 GHz, highlighting the potential of the proposed PLL for integrated circuit applications.

Keywords: phase-locked loop (PLL); voltage-controlled oscillator (VCO); clock feedthrough; current mismatch; charge pump; current-mode logic (CML)

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1. Introduction

The phase-locked loop (PLL) is a ubiquitous component in wireless communication systems. It is responsible for generating the desired frequency signal for frequency down-conversion and up-conversion. With the increasing demand for high-speed and wideband communication systems, the design of PLLs with improved performance metrics has become crucial.

The performance concerning the reference spur is crucial for PLLs, as an inadequate reference spur can result in significant inter-channel crosstalk. Previous research in the field has primarily focused on enhancing various aspects of PLL performance, including phase noise, spur suppression, settling time, and tuning range [1,2].

In essence, the reference spur is caused by the non-idealities of the charge pump circuit as well as the phase and frequency detector (PFD) circuit. Ideally, in the locked state, the static phase error between the input reference clock and the output signal of the divider should be zero because of the infinite DC loop gain [3–7].

However, to maintain a constant control voltage, the static phase error is not zero due to the presence of non-idealities. These non-idealities are primarily introduced by the charge pump, which includes factors such as current mismatch, current leakage, switching time error between PMOS and NMOS transistors, and so on.

When the non-idealities are converted to the current mismatch in the charge pump [8], the current mismatch can result in ripples in the tuning voltage of the voltage-controlled oscillator (VCO). Consequently, the modulated oscillation frequency of the VCO degrades the spectral quality of the output signal [9–12]. In order to improve the signal quality, various techniques have been proposed to directly improve the current matching of the charge pump [13] or apply analog [14,15] or digital [16–19] calibration to achieve it.

In addition to the charge pump, the frequency divider plays a vital role in achieving high-speed frequency division while maintaining signal integrity. While various techniques have been introduced to improve the tank-based injection-locked type, the current mode logic (CML) type is widely recognized for its superior division bandwidth [20–26].

In this paper, we present a detailed design of a wideband PLL featuring low reference spur and low phase noise. The proposed wideband PLL is implemented using a 130 nm CMOS process. The structure of the paper is organized as follows: In Section 2, the PLL architecture and its constituent modules are discussed. Section 3 introduces the design of the clock feedthrough suppressed charge pump with additional bias current branches, the VCO with a wide tuning range, and the symmetrical CML divider, respectively. Section 4 presents the experimental results obtained from the proposed PLL. Finally, Section 5 concludes the paper by summarizing the key results and implications of the research.

2. PLL Architecture

Figure 1 illustrates the block diagram of the proposed wide-tuning PLL. It comprises essential components, such as a phase and frequency detector (PFD), a charge pump, a third-order loop filter, a VCO , and a divider.

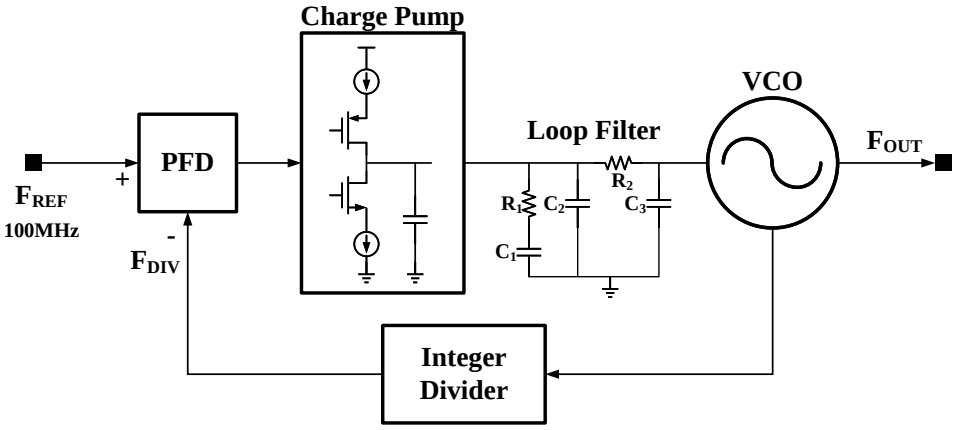


Figure 1. Block diagram of the proposed PLL.

The charge pump in the PLL is crucial to achieve low current mismatch. By minimizing the discrepancies between current sources, the low current mismatch charge pump effectively reduces random phase modulation, thereby enhancing the overall phase noise performance of the PLL.

To improve the charging and discharging speed, the charge pump utilizes a source-switched structure. Furthermore, to reduce the current mismatch in the charge pump, we employ a source-switched charge pump with additional bias current branches. These branches finely adjust the charging and discharging transistor currents, compensating for process, voltage, and temperature (PVT) variations. In addition, a rail-to-rail operational trans-conductance amplifier (OTA) is employed to enhance the accuracy of the current replication. This design choice ensures improved current replication accuracy, resulting in low output voltage ripple and enhanced phase noise performance.

The VCO is designed to provide a wide frequency tuning range while optimizing the trade-off between phase noise and power consumption. By employing tail resistors, the VCO allows for fine adjustment of the phase noise characteristics, ensuring optimal performance across the desired frequency range. The VCO is specifically designed to oscillate within the frequency range of 1.9 GHz to 3.1 GHz. It is composed of a pair of cross-coupled NMOS transistors and an LC tank. To accommodate variations in PVT, a 7-bit switched capacitor array (SCA) is employed, ensuring that the frequency tuning range meets the design specifications.

To achieve the desired frequency tuning range of 2 to 3 GHz with a reference frequency of 100 MHz, a significant frequency division ratio of approximately 30 is required. To meet this requirement, a 4-stage divide-by-2/3 circuit is employed to achieve high-speed frequency division and maintain signal integrity. The proposed divider is specifically designed to provide a frequency division ratio ranging from 16 to 31, effectively fulfilling the specified criteria. The divide-by-2/3 circuit employs CML AND gates and latches to enhance the high-frequency operation speed.

The open-loop transfer function of a conventional charge pump PLL is expressed as follows:

$$H_o(s) = \frac{I_{CP}K_{VCO}}{2\pi Ns} Z_{LF}(s) \tag{1}$$

where I_{CP} represents the current value when the charge pump is charged or discharged, K_{VCO} is the tuning gain of the *VCO*, N is the frequency division ratio, and $Z_{LF}(s)$ represents the characteristic impedance of the loop filter.

A PFD, a charge pump, and a divider are the main contributors to the in-band noise of a PLL. The noise transfer function of the PFD and the charge pump can be expressed as follows:

$$H_i(s) = \frac{NH_o(s)}{1 + H_o(s)} \cdot \frac{2\pi}{I_{CP}}. \tag{2}$$

In order to reduce the contribution of the PFD and the charge pump to the output noise of the PLL, it is necessary to increase the output current of the charge pump appropriately.

Additionally, the noise transfer function of the reference clock and the divider can be represented as follows:

$$H_d(s) = \frac{NH_o(s)}{1 + H_o(s)}. \tag{3}$$

According to Formula (3), for the constant noise of the reference clock and the divider, its contribution to the output noise of the PLL is basically constant when the frequency division ratio is determined.

The *VCO* plays a significant role in the out-of-band noise of the PLL. The noise transfer function of the *VCO* is expressed as follows:

$$H_n(s) = \frac{1}{1 + H_o(s)}. \tag{4}$$

The phase noise spectrum (S_Φ) of the *VCO* is proportional to the square of K_{VCO}. It can be mathematically represented as follows:

$$S_\Phi \propto \frac{1}{Q_{tank}^2} (\frac{K_{VCO}}{2\Delta\omega})^2. \tag{5}$$

where Q_{tank} is the quality factor of the *VCO*'s LC tank. In order to achieve low phase noise in the *VCO*, it is essential to ensure that the K_{VCO} is not excessively large.

Referring to Formulas (1) and (4) , if K_{VCO} is certain, I_{CP} needs to be large in order to minimize the contribution of the *VCO* noise to the output noise of the PLL. This is similar to the case of the charge pump, where increasing I_{CP} helps reduce the impact of the charge pump noise on the output of the PLL.

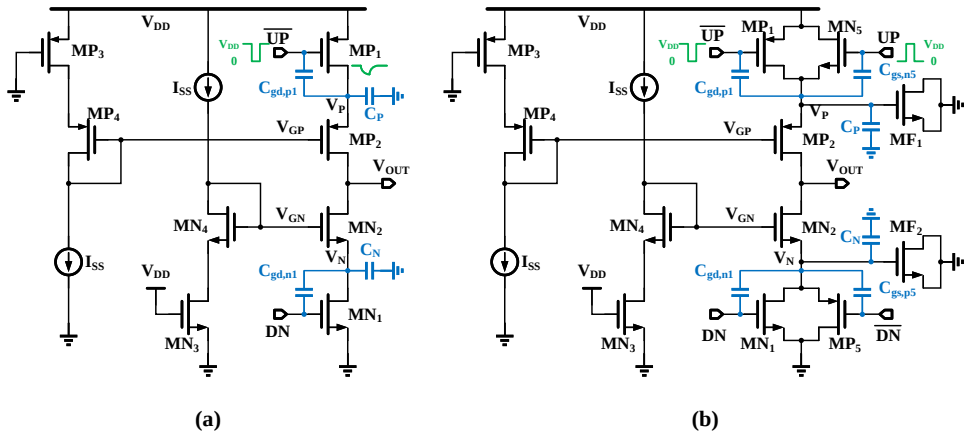
3. Circuit Design

3.1. Clock Feedthrough Suppressed and Low Current Mismatch Charge Pump

The charge pump is a critical component in the proposed PLL design. It is responsible for generating the required voltage levels to control the loop dynamics. But in fact, there are many non-ideal factors in charge pumps, among which, current mismatch, clock feedthrough, charge sharing, and charge injection lead to non-idealities of the reference spur of PLL.

Among them, the clock feedthrough is caused by the gate–drain capacitor of the switched transistor, which leads to the high-frequency components being fed to the loop filter through this parasitic capacitor, thus leading to the deterioration of the PLL's reference spurs. In order to reduce the influence of the clock feedthrough, it is a better choice to adopt the source-switched charge pump.

To mitigate the impact of the clock feedthrough, utilizing the conventional source-switched charge pump is proved to be a favorable option, as illustrated in Figure 2a. The source-switched charge pump can reduce the output voltage ripple compared to other charge pump architectures. By dynamically switching between current sources, it effectively mitigates the impact of switching transients and ripple noise. As a result, the output voltage exhibits improved smoothness and stability. In Figure 2a, MP_2 and MN_2 operate as current sources, and MP_1 and MN_1 operate as switches. Additionally, the switched transistors placed close to the power and ground improve the charging and discharging speed.



(a) (b)

Figure 2. (**a**) Conventional source-switched charge pump. (**b**) Improved conventional source-switched charge pump.

Indeed, along with its advantages, the source-switched structure also leads to negative effects resulting from the current mismatch. Their saturation currents in accordance with the channel length modulation effect can be expressed as

$$I_{UP} = \frac{1}{2}\mu_p C_{ox}(\frac{W}{L})_{P2}(V_P - V_{GP} - V_{tp})^2(1 + \lambda_p|V_{OUT} - V_P|) \quad (6)$$

$$I_{DN} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})_{N2}(V_{GN} - V_N - V_{tn})^2(1 + \lambda_n|V_{OUT} - V_N|). \quad (7)$$

The clock signals are fed to the nodes V_P and V_N through $C_{gd,p1}$ and $C_{gd,n1}$, which are the gate–drain capacitors of MP_1 and MN_1, respectively, so that the node voltages of V_P and V_N change. When the voltages of nodes V_P and V_N change, I_{UP} and I_{DN} will change, which will lead to non-ideal factors. Assuming the equivalent capacitors of nodes V_P and V_N to the ground are represented as C_P and C_N, respectively, we note that the voltage variation at node V_P due to clock feedthrough is given by $V_{DD}\ C_{gd,p1}/(C_{gd,p1}+C_P)$.

In order to reduce the influence of the clock feedthrough on nodes V_P and V_N, MP_1 and MN_1 are replaced by transmission gates, and MOS transistors with a filtering function

are added at V_P and V_N to further reduce the influence of non-ideal factors, as shown in Figure 2b. The differential signals *UP* and $\overline{UP}$, as well as *DN* and $\overline{DN}$, undergo cancellation of the feedthrough signals upon passing through the transmission gates. Since $C_{gd,p1}$ and $C_{gs,n5}$ are generally not equal, a net amount of change appears at V_P given by V_{DD} ($C_{gd,p1}$ − $C_{gs,n5}$)/($C_{gd,p1}$ + $C_{gs,n5}$ + C_P). Moreover, due to the low-voltage operation of the charge pump, the transmission gate dimensions are increased to mitigate voltage drops. This enlargement of transmission gate dimensions, however, leads to larger parasitic capacitances within the transmission gates, facilitating favorable clock feedthrough conditions. Hence, it becomes imperative to further suppress the clock feedthrough at nodes V_P and V_N. To address this challenge while considering design simplification, we adopted the utilization of NMOS transistors, MF_1 and MF_2, as a filtering mechanism. NMOS transistors were introduced at nodes V_P and V_N, as depicted in Figure 2b, exploiting their inherent parasitic capacitances (C_{gs} and C_{gd}) to facilitate the filtering process. It is noteworthy that the introduction of the filtering NMOS transistors is specific to the source-switched charge pump.

Figure 3 illustrates the impact of filtering NMOS transistors of different dimensions on the filtering effectiveness at the V_P node. It is evident that, in the absence of filtering NMOS transistors, the voltage variation at node V_P due to clock feedthrough with the transmission gate is less affected by clock feedthrough than without the transmission gate. Upon the integration of filtering NMOS transistors, an increase in the size of the filtering NMOS transistors MF_1 results in a more pronounced attenuation of feedthrough. However, with the increase in the capacitance of the filtering NMOS, the charging and discharging speeds of the current slows down, which leads to the unequal current copied by the current mirror and the current mismatch. Optimal results are achieved when the area of the filtering NMOS transistor is compromised with the filtering effect. Specifically, as can be seen from Figure 3, when the area of the filtering NMOS transistor is twice that of MP_1, the trade-off between the charging and discharging speeds of the current and the filtering effect is good for achieving the desired feedthrough suppression. Another function of the filtering NMOS transistor is to reduce the voltage transients at the source terminal during feedthrough, as well as to mitigate the potential impact of signal coupling onto the gate terminal of the current mirror.

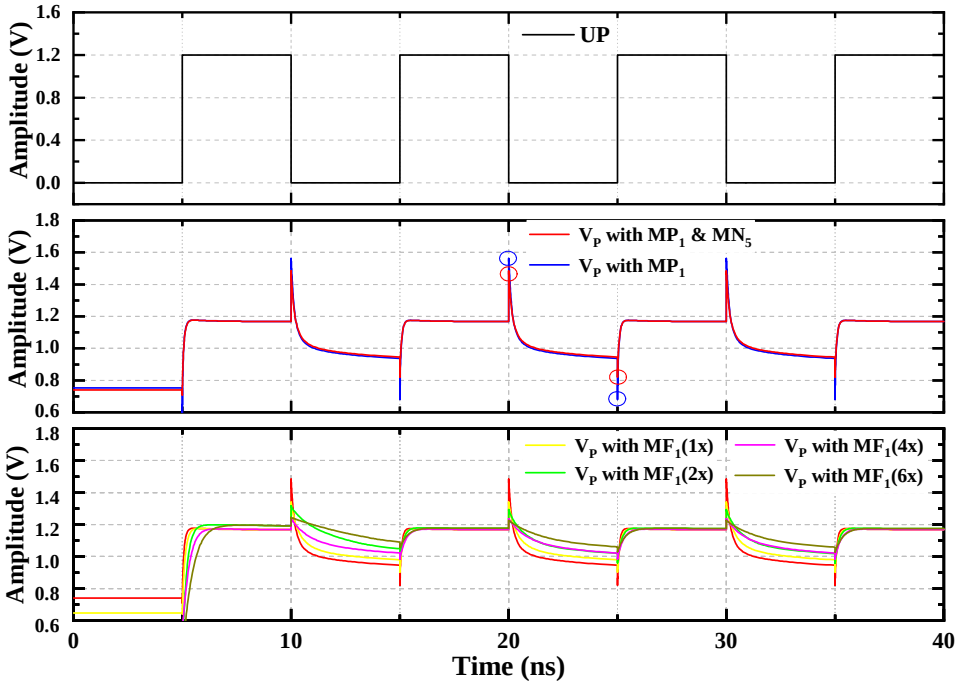


Figure 3. Simulation of the clock feedthrough effect.

The current mismatch is one of the key factors contributing to the reference spur in the PLL. The amount of the reference spur is approximately calculated as [27]

$$P_{spur}(dBc) = 20log(\frac{\Delta\phi}{\sqrt{2}} \cdot \frac{N \cdot BW}{f_{ref}}) - 20log(\frac{f_{ref}}{f_p}) \quad (8)$$

where N is the frequency division ratio, BW is the PLL bandwidth, and f_p is the frequency of the pole in the loop filter. $\Delta\phi$ refers to the phase error. The major phase error contributors are the leakage currents, the current mismatch of the charge pump, and the switching time mismatch between the up and down current pulses. The analytic expression of the phase error is

$$\Delta\phi = \Delta\phi_{leakage} + \Delta\phi_{current} + \Delta\phi_{time} = 2\pi \cdot (\frac{I_{leakage}}{I_{CP}} + \frac{\Delta I}{I_{CP}} \cdot \frac{T_{switch}}{T_{ref}} + \frac{\Delta T \cdot T_{switch}}{T_{ref}^2}) \quad (9)$$

where $I_{leakage}$ is the leakage current, I_{CP} is the current of the charge pump, T_{switch} is the frequency of reference clock, and ΔT, ΔI are the time and current mismatch, respectively.

Formulae (8) and (9) show that the reference spur P_{spur} is positively correlated with the current mismatch ΔI of the charge pump, which means that the reference spur can be scaled down by decreasing the current mismatch of the charge pump.

In order to effectively constrain the current mismatch within a limited range, additional bias current branches, namely $I_{N,offset}$ and $I_{P,offset}$, introduced parallel to P_1 and N_1 in the charge pump to finely adjust the currents of both the pump-up and pump-down current mirrors. Figure 4 illustrates the proposed circuit configuration for the charge pump.

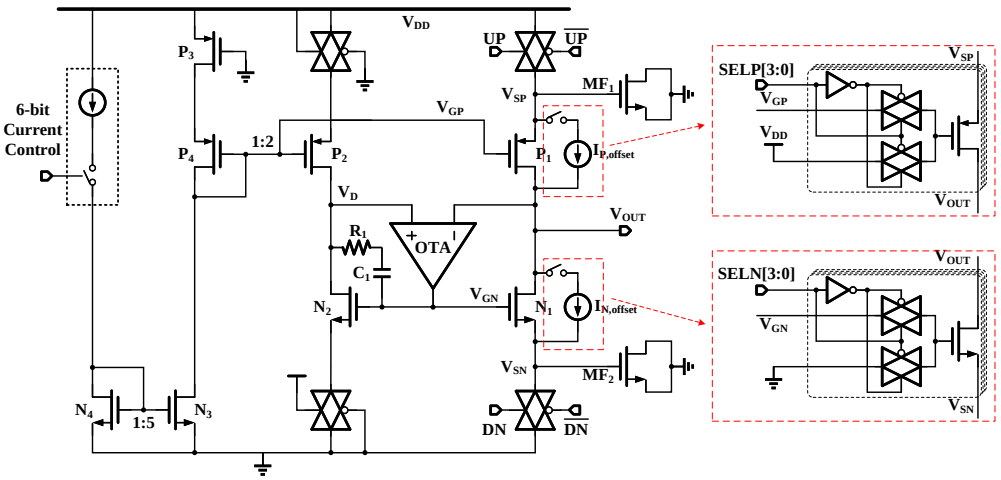


Figure 4. Schematic of the proposed source-switched charge pump.

Due to the presence of the operational transconductance amplifier (OTA), the voltage at V_{OUT} is equivalent to the voltage at V_D. However, the existence of the transmission gates prevents the source voltages of P_1/P_2 and N_1/N_2, which act as current mirrors, from being exactly equal. According to Formulae (6) and (7), a mismatch in currents occurs between the transistors P_1 and N_1. Additionally, process deviations in MOS transistors contribute to pump-up and pump-down current mismatch.

To further mitigate the impact of the current mismatch-induced reference spur, the current compensation branches are introduced into the circuit, as depicted in Figure 4. When the switches are connected to the ground or the power supply, the compensation branches remain closed and do not participate in current compensation. However, when the switches are connected to the gate terminals of the parallel MOS transistors, the compensation branches become active, aiding in current compensation. Notably, the compensation branches' minimum compensating current should not be excessively large, thus a minimum current of 2 µA is set with 4-bit compensation current branches.

Figure 5 illustrates the current mismatch effect under different process corners and temperatures. As observed from the graph, compensating through the bypass branch effectively limits the mismatch to below 0.1% across various process corners.

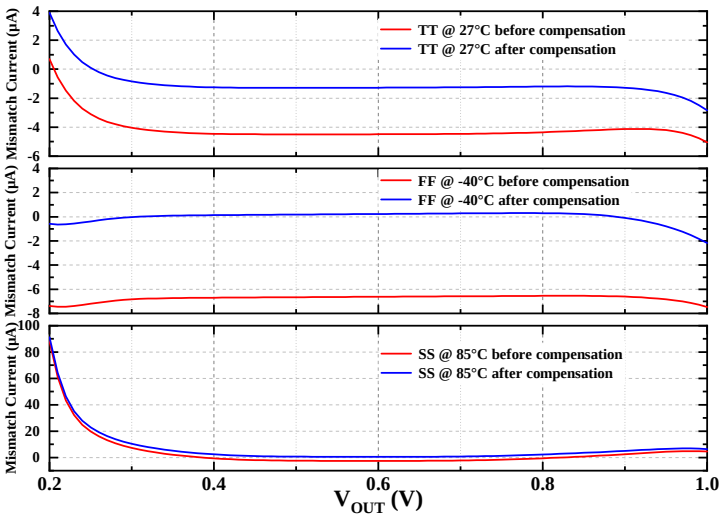


Figure 5. Simulated mismatch currents under different process corners and temperatures.

After designing the charge pump, it is necessary to conduct a linearity simulation for the cascade of the PFD and the charge pump. By changing the time error ΔT between the rising edge of the reference clock and the rising edge of the output of the loop feedback clock, the average output current of the charge pump can be viewed, as shown in Figure 6. As can be seen from the figure, when the time error ΔT is greater than zero, the average output current of the charge pump is positive, indicating that it is in a charging state at this time. When the time error ΔT is less than zero, the average output current of the charge pump is negative, indicating that it is in a discharging state at this time. However, with the increase of the time error ΔT, the average output current of the charge pump increases. When ΔT exceeds an integer multiple of the period of the reference clock, the average output current of the charge pump will change approximately periodically. When the rising edge of the reference clock coincides with the rising edge of the loop feedback clock, that is, ΔT is zero, the average output current of the charge pump is the mismatch current. After the charge pump is compensated, the average output current drops from 1.76 μA to 0.71 μA, which shows that the current mismatch between the charging current and the discharging current is 0.71 μA when the PLL is locked.

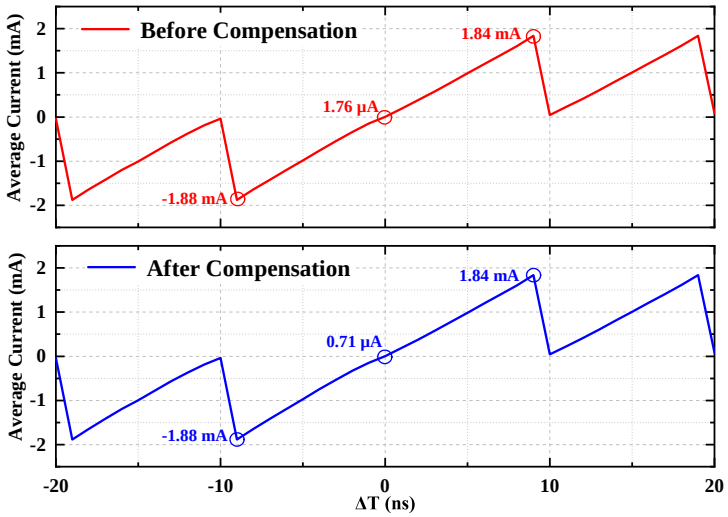


Figure 6. Linearity simulation for the cascade of PFD and charge pump.

3.2. Wide-Tuning Range VCO

Figure 7 illustrates the schematic of a cross-coupled LC-VCO. The proposed VCO employs a differential topology consisting of NMOS transistors, which generate negative resistance to compensate for losses in the LC tank. To achieve current control, resistor-switched is utilized instead of a current mirror, as it contributes less flicker noise.

The current of the proposed VCO can be adjusted within a range of 0.5 mA to 15.5 mA, with a step size of 0.5 mA, utilizing a 6-bit resistor bank. For frequency tuning, the VCO incorporates a 7-bit binary-weighted metal–insulator–metal (MIM) capacitor bank for coarse tuning and varactors for fine-tuning. The designed VCO offers a tuning range from 1.9 GHz to 3.1 GHz. To characterize the VCO's performance, an average gain (K_{VCO}) of 50 MHz/V is targeted, ensuring suitable frequency modulation capabilities.

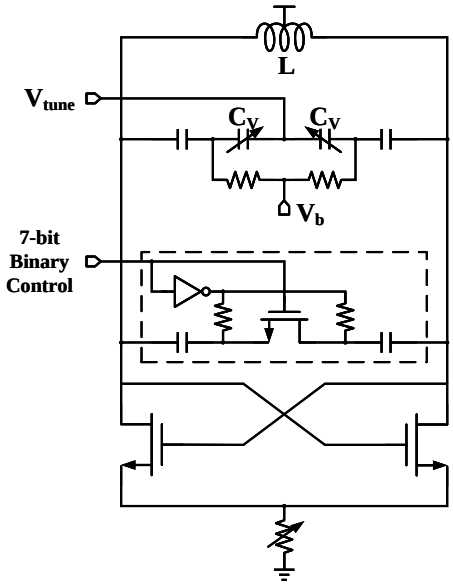


Figure 7. Schematic of the proposed VCO.

3.3. Symmetrical CML Divider

CML dividers utilize differential voltage signaling, which offers several advantages. Firstly, differential signaling helps in rejecting noise, leading to improved signal integrity. Additionally, the differential nature of CML circuits enables seamless integration with other differential circuits present in the system, promoting compatibility and ease of design.

Moreover, CML dividers are capable of operating at high frequencies, making them suitable for applications that require the rapid division of clock signals or frequency synthesis. This attribute enhances their versatility and applicability in various systems.

The total frequency division ratio achieved by the cascade of multi-stage divide-by-2/3 circuits is calculated as 2^N to $2^{N+1} - 1$, where 'N' represents the number of stages.

Figure 8 presents the block diagram of the proposed frequency divider utilized in this design. The frequency divider employs a four-stage cascade structure of divide-by-2/3 circuits, enabling a frequency division ratio ranging from 16 to 31. To further enhance the performance of the frequency divider, retiming technology is implemented.

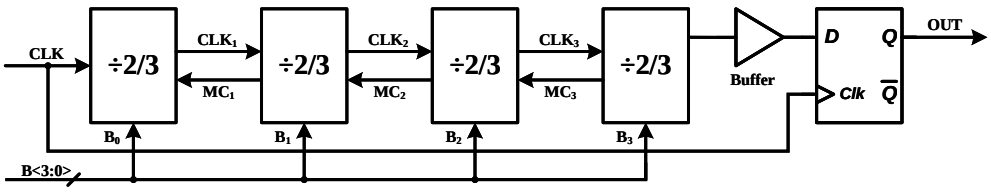


Figure 8. Block diagram of the proposed frequency divider.

The divide-by-2/3 circuit is depicted in Figure 9, and the circuit of the CML latch is depicted in Figure 10a. Due to the differential input and output nature of the CML divider, there exists a heightened requirement for circuit symmetry. In Figure 9, with the exception of the input terminals of AND2 and Latch2, which accommodate control signal B, the input terminals of the remaining AND gates and latches are driven by clock signals. In cases where input signals are not propelled by buffer elements, the conventional topology illustrated in Figure 10b may result in disparate differential input impedances within the AND gate. This incongruence in impedance is undesirable within a fully differential structure.

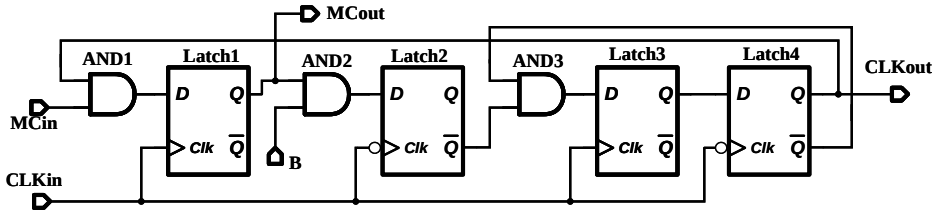


Figure 9. Block diagram of the divide-by-2/3 circuit.

In response to this concern, an improved topology, as depicted in Figure 10c, has been devised. In this enhanced configuration, input signals A and B exhibit symmetric conditions, thus facilitating a more symmetrical design for the entire 2/3 divider. This symmetric arrangement is conducive to a more balanced design of the overall 2/3 divider, which is especially advantageous within the context of the CML divider's imperative for heightened circuit symmetry.

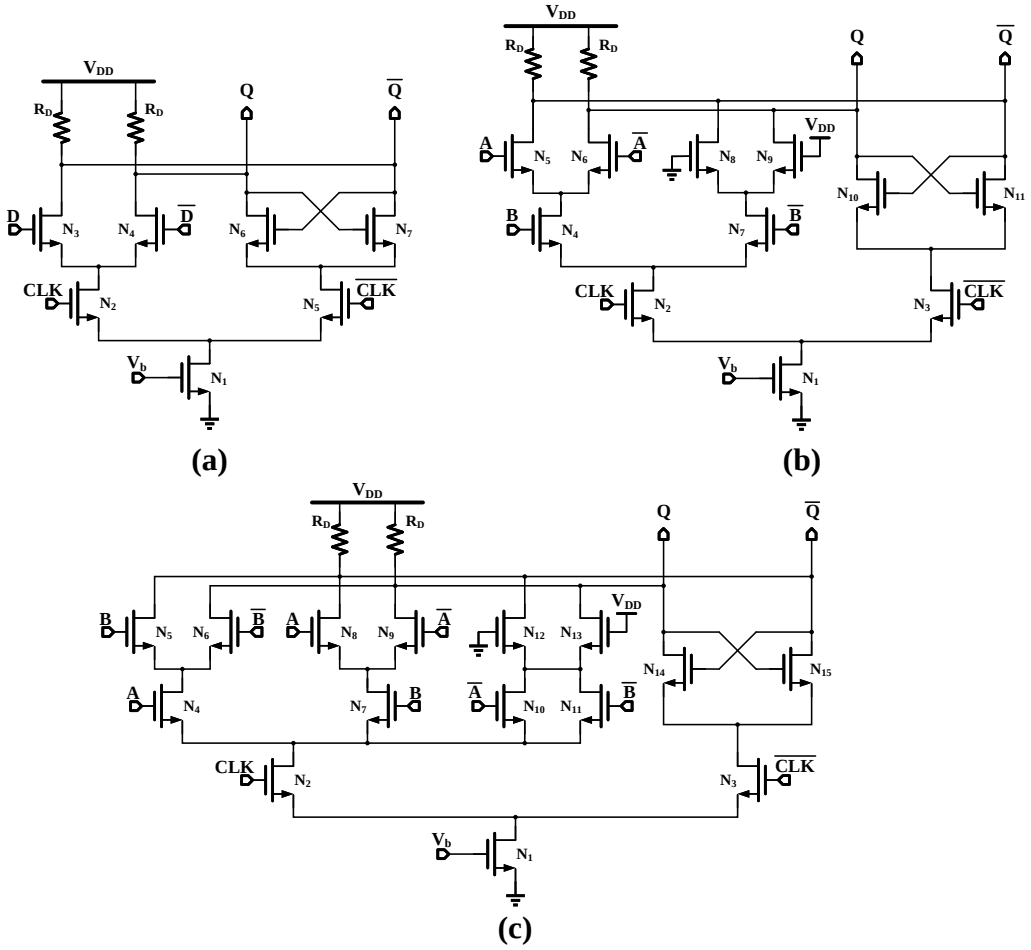


Figure 10. (**a**) Schematic of the CML latch. (**b**) Conventional topology of CML AND gate and latch. (**c**) Proposed topology of the CML symmetrical AND gate and latch.

CML circuits offer speed advantages due to two key properties. Firstly, they employ moderate voltage swings, which helps in achieving faster operation. Secondly, only NMOS devices are used in the data and clock paths, further enhancing the speed performance.

The output swing of the latch can be adjusted by varying the resistance value of R_D, allowing for control of the static output bias voltage. This adjustment helps optimize the performance and characteristics of the CML latch circuit.

If the transistors switch completely, the single-ended output voltage swing of Output Q and Output $\overline{Q}$ can be expressed as

$$V_{pp} = I_{SS}R_D \tag{10}$$

where V_{pp} is the maximum single-ended output voltage swing of Output Q and Output $\overline{Q}$. I_{SS} is the average tail current and R_D is the load resistance.

The output common mode (CM) level of Output Q and Output $\overline{Q}$ is given by:

$$V_{CM} = V_{DD} - (I_{SS}R_D)/2. \tag{11}$$

To increase the maximum operating frequency of the divider, the current of the CML latch can be increased, but this may result in a reduction in the output swing and the driving ability of the latch becomes weak.

4. Measurement Results

The designed PLL is fabricated in a 130 nm CMOS technology process. The control code voltages, the frequency tuning voltage, and the DC supply are wire-bonded to a printed circuit board (PCB). The chip micrograph of the fabricated PLL is shown in Figure 11.

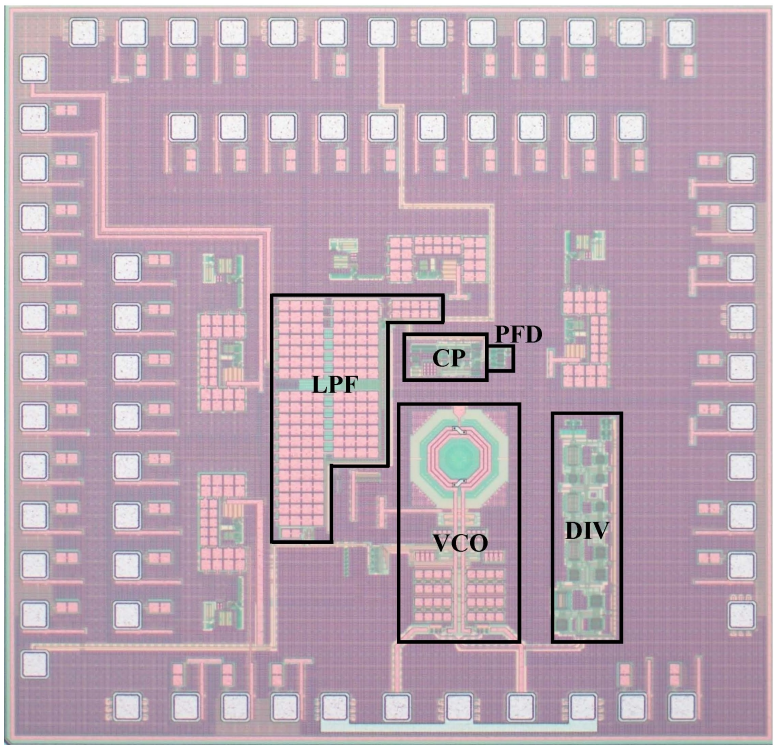


Figure 11. Chip micrograph of the proposed PLL.

A PXA signal analyzer (Agilent N9030A, Agilent Technologies, Santa Clara, CA, USA) is used to measure the proposed PLL. During the test, the operating current of the VCO is set to 11.5 mA, and the branch current of the charge pump is set to 2 mA. At these settings, Figures 12 and 13 show the output spectrum and the phase noise of the proposed PLL at a carrier frequency of 2.4 GHz, respectively. The reference spur of the

PLL is −74.39 dBc below the carrier as shown in Figure 12. The measured phase noise of the PLL is −102.55 dBc/Hz@100kHz and −127.15 dBc/Hz@1MHz as displayed in Figure 13. The total power consumption of the proposed PLL is 33.6 mW from a 1.2 V supply. Among the components, the charge pump consumes 5.5 mA, the VCO core draws 11.4 mA from a 1.2 V supply voltage, and the divider dissipates 12.8 mA. In terms of jitter performance, the measured rms jitter integrated from 10 kHz to 10 MHz at a carrier frequency of 2.4 GHz is 340.99 fs. Additionally, the figure-of-merit (FoM) at the same carrier frequency is −234.08 dB.

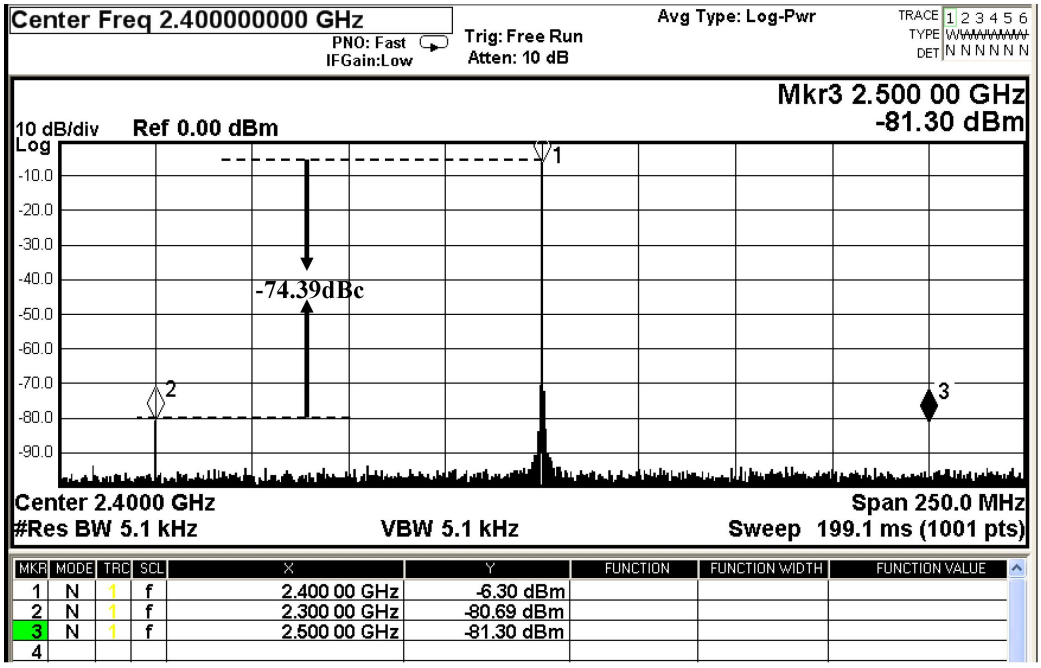


Figure 12. Output spectrum of the proposed PLL at a 2.4 GHz carrier frequency.

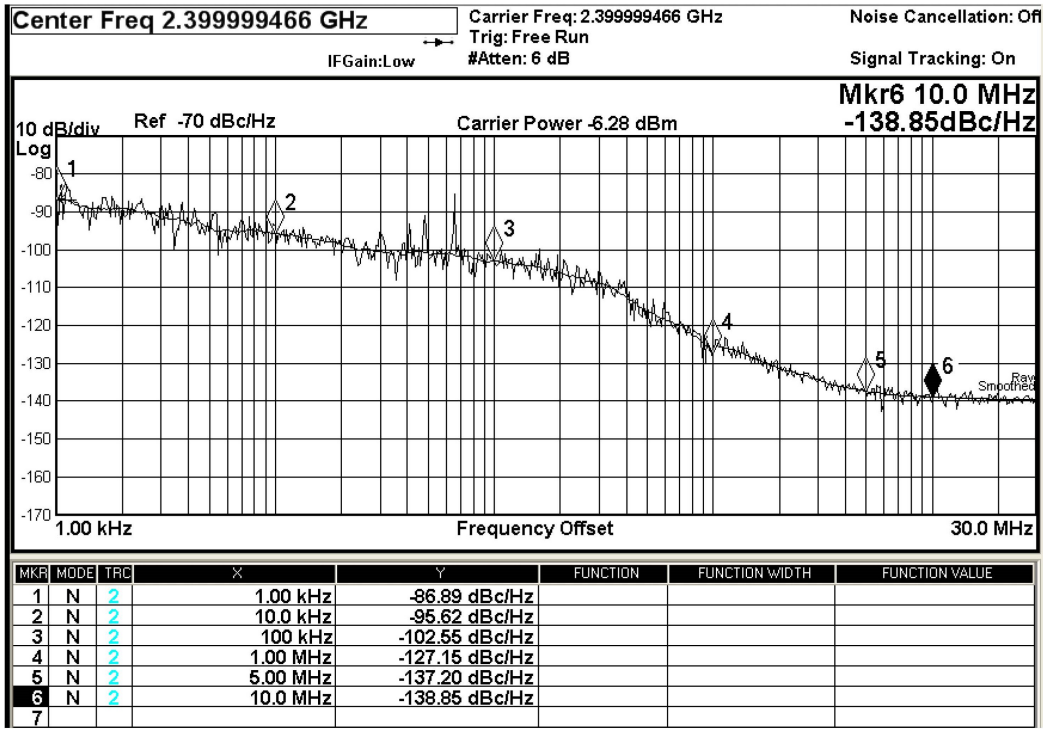


Figure 13. Phase noise of the PLL at a 2.4 GHz carrier frequency.

Table 1 summarizes a comprehensive comparison of the performance between the proposed PLL and other PLLs reported in previous studies. The phase noise performance of the proposed PLL stands out significantly in comparison to the reported PLLs. In addition, the proposed wideband PLL achieves a tuning range of 40%, which is only narrower than that of [28]. The FoM of the proposed PLL is comparable to that of other works. However, it is worth noting that their reference spur is worse than the proposed PLL's reference spur of −74.39 dBc.

Table 1. Performance comparison with the state of the pulished PLLs.

Reference		**This Work**	**ISSCC'19 [28]**	**ISSCC'15 [29]**	**ISSCC'14 [30]**	**JSSC'13 [31]**	**JSSC'12 [32]**
Technology (nm)		**130**	10	45	40	65	130
Supply (V)		**1.2**	0.9	1	N/A	1.2	N/A
Oscillator Topology		**LC**	Ring	Ring	LC	LC	LC
Reference freq. (MHz)		**100**	100	22.6	26	40	60
Output freq. (GHz) /freq. Range (GHz)		**2.4 /(2.0–3.0)**	3.2 /(0.5–5.0)	2.4 /(2.0–3.0)	3.883 /(3.276–3.883)	3.61 /(3.0–4.0)	2.438 / N/A
Tuning Range (%)		**40**	164	40	17	28.6	N/A
Phase Noise (dBc/Hz)	@100 kHz	**−102.55**	N/A	−109.18	−105.49	−103.62	−102.27
	@1 MHz	**−127.15**	N/A	−113.78	−123.06	−103.79	−99.63
RMS jitter (fs)		**340.99 (10 k–10 M)**	1870 (100 k–100 M)	970 (1 k–200 M)	300 (1 k–10 M)	972.9 (3 k–30 M)	1092.6 (10 k–10 M)
FoM (dB) *		**−234.08**	−233	−234.1	−242	−235.1	−229.41
Reference Spur (dBc)		**−74.39**	−57	−65	N/A	−71	−54.7

*: FoM = 20log(J_{rms}/1 s) + 10log(P_{DC}/1 mW).

5. Conclusions

We presented a comprehensive design of a wideband PLL with low reference spur and low phase noise. The charge pump employs a source-switched charge pump with additional bias current branches to minimize current mismatch, resulting in improved phase noise performance. The utilization of the 4-stage CML divide-by-2/3 circuit in the frequency divider enables high-speed frequency division without the limitations of narrowband resonator structures. The VCO design, incorporating a wide tuning range and adjustable tail resistor, optimizes the trade-off between phase noise and power consumption. The measured results demonstrate a frequency tuning range from 2.0 GHz to 3.0 GHz, with a remarkable tuning range of 40%. Notably, the PLL exhibits a reference spur of −74.39 dBc and a FoM of −234.08 dB at a carrier frequency of 2.4 GHz. The achieved performance levels and the significant advancements in phase noise and reference spur make the proposed wideband PLL a promising solution for high-speed wireless communication systems. The low phase noise and low reference spur characteristics enable stable and accurate frequency synthesis, contributing to improved data transmission and reception in future wireless communication applications.

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