

A Reliability-Enhanced Differential Sensing Amplifier for Hybrid CMOS/MTJ Logic Circuits

Chengzhi Wang ¹, Tianqi Yang ², Min Han ^{3,*} and Dongsheng Wang ^{1,*}¹ National Innovation Institute of Defense Technology, Academy of Military Sciences, Beijing 100091, China² Beijing Aerohydrodynamic Research Center, Beijing 100020, China³ Institute of Systems Engineering, Academy of Military Sciences, Beijing 100091, China

* Correspondence: hanminchina@163.com (M.H.); wdsh2011@gmail.com (D.W.)

Abstract: Recently, hybrid logic circuits based on magnetic tunnel junctions (MTJs) have been widely investigated to realize zero standby power. However, such hybrid CMOS/MTJ logic circuits suffer from a severe sensing reliability due to the limited tunnel magnetoresistance ratio ($TMR \leq 150\%$) of the MTJ and the large process variation in the deep sub-micrometer technology node. In this paper, a novel differential sensing amplifier (DSA) is proposed, in which two PMOS transistors are added to connect the discharging branches and evaluation branches. Owing to the positive feedback realized by these two added PMOS transistors, it can achieve a large sensing margin. By using an industrial CMOS 40 nm design kit and a physics-based MTJ compact model, hybrid CMOS/MTJ simulations have been performed to demonstrate its functionality and evaluate its performance. Simulation results show that it can achieve a smaller sensing error rate of 9% in comparison with the previously proposed DSAs with a TMR ratio of 100% and process variation of 10%, while maintaining almost the same sensing delay of 74.5 ps and sensing energy of 1.92 fJ/bit.

Keywords: hybrid logic circuits; magnetic tunnel junction; differential sensing amplifier; sensing margin



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1. Introduction

As the technology node continuously scales down, CMOS-based logic circuits suffer from high standby power consumption induced by the increasing leakage current. To address this issue, many new nanodevices and structures have been presented recently to realize zero standby power [1–3]. Among them, the MTJ is preferable, because of its high speed, long data retention, nearly infinite endurance, great scalability and good compatibility with CMOS process technology, in comparison with other eNVM devices [4–6]. Figure 1a illustrates the structure of an MTJ device composed of two ferromagnetic (FM) layers (e.g., CoFeB) separated by one oxide barrier layer (e.g., MgO). Generally, the magnetization direction of the FM layer (which is called a free layer) is fixed; the magnetization direction of the other FM layer (which is called the pinning layer) can be reversed. Depending on the relative magnetization orientation of these two FM layers, i.e., parallel (P) or anti-parallel (AP), each MTJ device can exhibit two stable resistance states, i.e., R_P or R_{AP} , which are used to represent binary logic information ‘0’ and ‘1’, respectively, as shown in Figure 1b. Using the MTJs as the non-volatile storage elements, several non-volatile logic circuits, such as magnetic flip-flop [7–9], magnetic look-up table [10–12], magnetic full-adder [13–15] and ternary content-addressable memory [16–18], have been proposed.

One critical issue in these hybrid CMOS/MTJ logic circuits is to correctly sense the information stored in the MTJ [19–23]. So far, various DSAs have been proposed, in which two MTJs with opposite resistance states are employed to represent one bit. For example, the pre-charge sensing amplifier (PCSA) circuit [24], as shown in Figure 2a, can achieve high sensing reliability (10–5 at 90 nm), small sensing delay (~125 ps) and low sensing energy (~1 fJ/bit). However, as the CMOS technology shrinks below 45 nm, the sensing

reliability gets worse and worse (e.g., 79% at 40 nm) due to the increased process variation. To overcome this issue, a separated PCSA (SPCSA) [25] is proposed as shown in Figure 2b, which can improve the sensing reliability (82% at 40 nm) while retaining high sensing speed and low sensing energy dissipation. However, its sensing margin is still limited due to the small TMR ratio of the MTJ. To improve the sensing margin, a reliability-enhanced SPCSA (RESPCSA) [26] is proposed as shown in Figure 2c, which can further improve the sensing reliability (84% at 40 nm). However, it is still not sufficient for reliable logic circuits. This paper proposes a novel differential sensing amplifier based on the RESPCSA, in which two PMOS transistors are added to connect the discharging branches and evaluation branches. By using the positive feedback of two PMOS transistors, the proposed DSA is envisioned to obtain a large sensing margin, thereby achieving high sensing reliability.

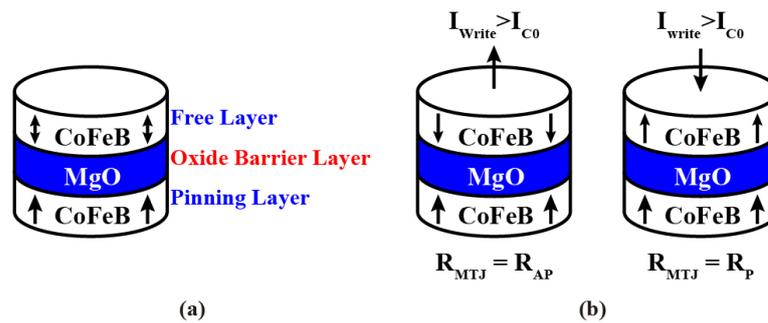


Figure 1. (a) Structure schematic of Magnetic Tunnel Junction (MTJ). (b) Spin Transfer Torque (STT) writing mechanism.

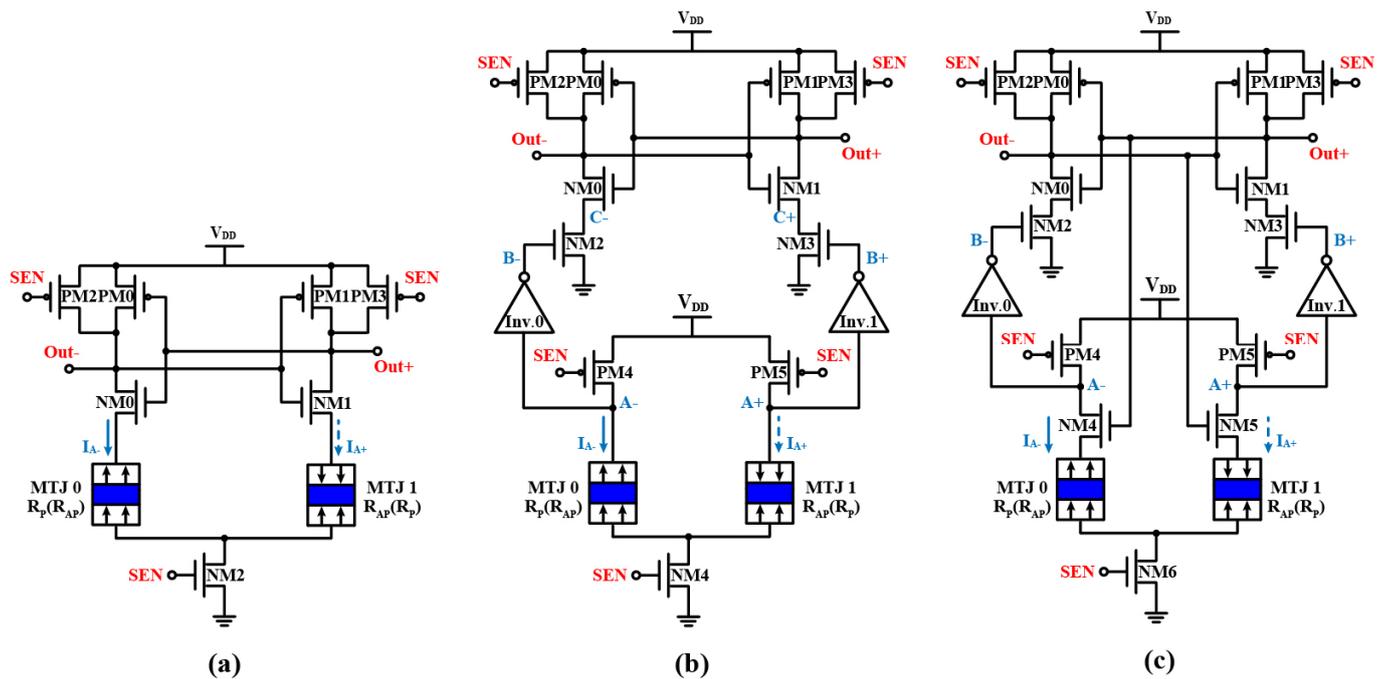


Figure 2. Schematics of (a) PCSA [24] (b) SPCSA [25] and (c) RESPCSA [26].

The remainder of this paper is organized as follows. Section 2 describes the proposed novel differential sensing amplifier and its operation. Section 3 demonstrates its functionality and evaluates its performance. Finally, Section 4 concludes this paper.

2. Proposed Reliability-Enhanced Differential Sensing Amplifier Circuit

Figure 3 shows the proposed reliability-enhanced differential sensing amplifier (REDSA) circuit. Similar to the previous RESPCSA, the proposed REDSA also includes three operation phases, i.e., pre-charging phase, discharging phase and evaluation phase, depending on the control signal “SEN”. From the perspective of the circuit configuration, the main difference is that two PMOS transistors PM4 and PM5 are added to connect the discharging branches and evaluation branches. As a result, two positive feedback loops can be formed and a large sensing margin can be achieved, which will be demonstrated in Section 3. The sensing operation is described as follows.

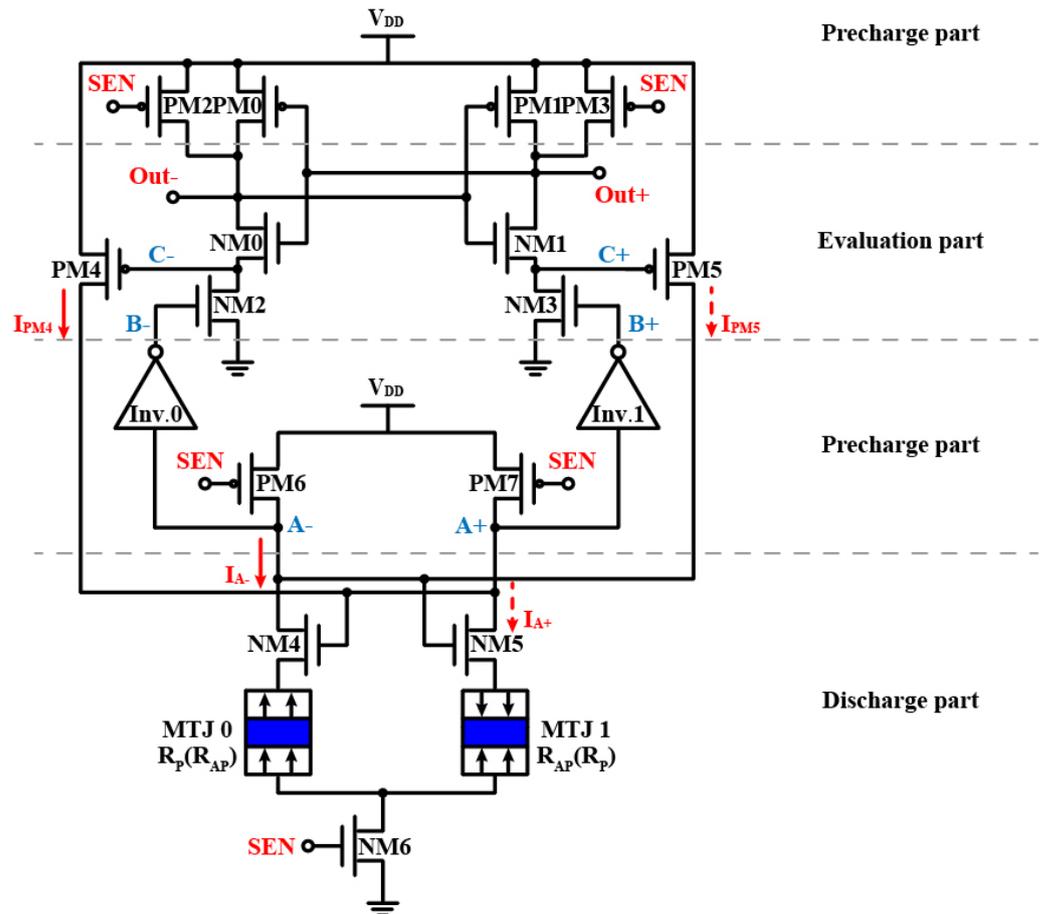


Figure 3. Schematic of the proposed sensing amplifier.

When the “SEN” is set to ‘0’, the proposed REDSA enters the pre-charging phase. PM2–PM3 and PM6–PM7 turn on and the NMOS transistor NM6 is in the off state. As a result, the nodes A (A+ and A-), C (C+ and C-) and Out (Out+ and Out-) are charged to V_{DD} . When the “SEN” goes to ‘1’, the proposed REDSA goes into the discharging phase. NM6 turns on, and both the nodes A+ and A- begin to discharge, but with different speeds due to the resistance difference between their individual discharging branches, resulting in a voltage difference (ΔV_A) between them. Then, the ΔV_A can be inversely amplified by both the inverter 0 (Inv.0) and Inv.1, which enables the nodes Out+ and Out- to discharge with different speeds as well as the nodes C+ and C-, leading to a voltage difference ΔV_{Out} and a voltage difference ΔV_C . The voltage difference ΔV_C can in turn enlarge the ΔV_A thanks to the positive feedback of PM4 and PM5. Once one of the nodes Out+ and Out- becomes less than the threshold voltage of the cross-coupled inverters (composed of PM0–NM0 and PM1–NM1), the proposed REDSA enters into the evaluation phase. Finally, one of the nodes Out+ and Out- will continue discharging to GND, while the other will eventually charge to V_{DD} . For example, when MTJ0 is in a high resistance (R_{AP}) state and MTJ1 in a

low resistance (R_p) state, the node Out+ will be discharged to GND and the node Out- will be charged to V_{DD} and vice versa.

3. Functional Verification

By using a physics-based MTJ compact model [27–30] and an industrial CMOS 40 nm design kit, hybrid CMOS/MTJ simulations have been performed to demonstrate its functionality and evaluate its performance. The key parameters of the compact MTJ model are listed in Table 1.

Table 1. The Key Parameters of the MTJ in Simulations.

Parameter	Description	Default Value
t_{ox}	Oxide barrier thickness	0.85 nm
t_f	Free layer height	1.3 nm
Area	MTJ surface	$40^2 \times \pi/4 \text{ nm}^2$
V	Volume of free layer	$\text{Area} \times t_f$
R.A	Resistance \times Area product	$5.0 \Omega \cdot \mu\text{m}^2$
TMR(0)	the TMR ratio with zero V_{bias}	100%
ΔTMR	the TMR ratio variation	3%
Δt_{sl}	Variation of free thickness	3%
Δt_{ox}	Variation of oxide barrier thickness	3%

Figure 4a shows the transient simulation waveforms of the proposed REDSA, where the MTJ0 is in a low resistance state and the MTJ1 in a high resistance state. As seen, during the pre-charging phase (“SEN” = 0 V), the nodes (A+, A-) and (Out+, Out-) are charged to V_{DD} . When the “SEN” rises to ‘1’, they enter the discharging phase, and the nodes A+ and A- begin to discharge but with different speeds, resulting in a voltage difference ΔV_A . Owing to the positive feedback of the two added PMOS transistors, the ΔV_A is enlarged after the point M1 (or M2). Then, this enlarged ΔV_A is amplified, inducing a large voltage difference ΔV_{Out} . As a result, the node Out- firstly becomes less than the threshold of the cross-coupled inverters. Then, the proposed REDSA enters into the evaluation phase, the node Out- continues discharging after the point M10 and the Out+ is charged after the point M9. As seen, the proposed REDSA can achieve a large sensing margin of 732.6 mV (the voltage difference between the points M9 and M10) and a small sensing delay of 74.5 ps (taken from the points M0 to M11). Since the sensing delay is less 75 ps, it can work with a high clock frequency, up to 6.7 GHz. Figure 4b confirms that there is no static current during the sensing operation, only dynamic charging and discharging current. The total power per bit sensing operation of the proposed REDSA is about 1.92 fJ.

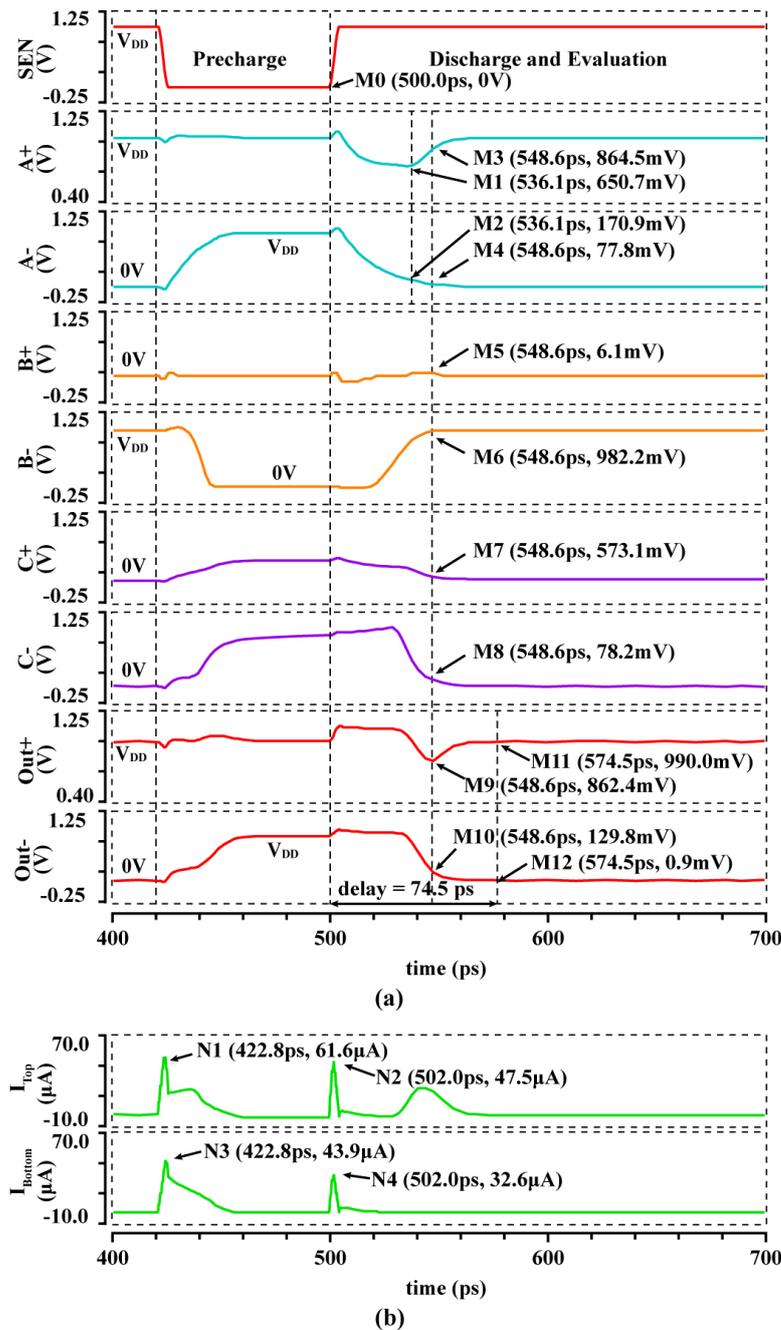


Figure 4. (a) Transient voltage simulation waveforms of the proposed REDSA. (b) Currents that flow through the proposed REDSA.

4. Performance Analysis and Comparison

4.1. Reliability Analysis and Comparative Discussion

Firstly, this paper investigates the sensing margin of the proposed REDSA with respect to different supply voltages. As shown in Figure 5a, with the increase of the supply voltage, its sensing margin can be improved. Compared to the previous RESPCSA in [17], the proposed REDSA can achieve a very larger sensing margin, even with a small supply voltage. For example, the sensing margin can reach 696 mV when the supply voltage is 0.8 V, while it is only about 280 mV for the RESPCSA. The influence of the TMR ratio on the sensing margin is also investigated, as shown in Figure 5b. As seen, the sensing margin increases with the increase of the TMR ratio. However, even with a small TMR ratio of 50%,

the sensing margin of the proposed REDSA can reach up to 632 mV, which is much larger than that of the RESPCSA.

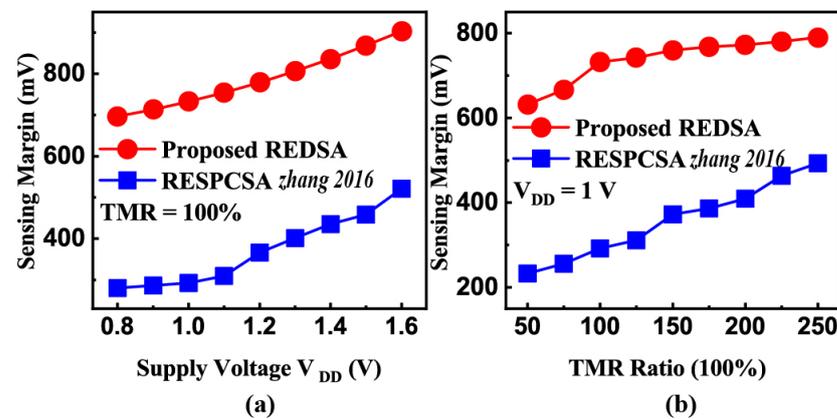


Figure 5. Comparison of the sensing margin of the proposed REDSA and the RESPCSA with respect to different supply voltages (a) and TMR ratios (b) [17].

To evaluate the sensing reliability of the proposed REDSA quantitatively, Monte Carlo statistical simulations (1000 runs per case) have been performed with consideration of the 1σ probability distributions of the CMOS transistors fixed by the CMOS process manufacturer and the 3% process variations of MTJ, including TMR ratio, free layer thickness and oxide barrier thickness. Figure 6a shows the impact of the device variation on the sensing error rate (SER), where the TMR ratio is 100%. As seen, the proposed REDSA exhibits a greater tolerance to device variation in comparison with the RESPCSA. Additionally, the SER with respect to the TMR ratio is evaluated, as shown in Figure 6b. As seen, the proposed REDSA can provide a much higher sensing reliability in comparison to the RESPCSA when the TMR ratio is less than 150%.

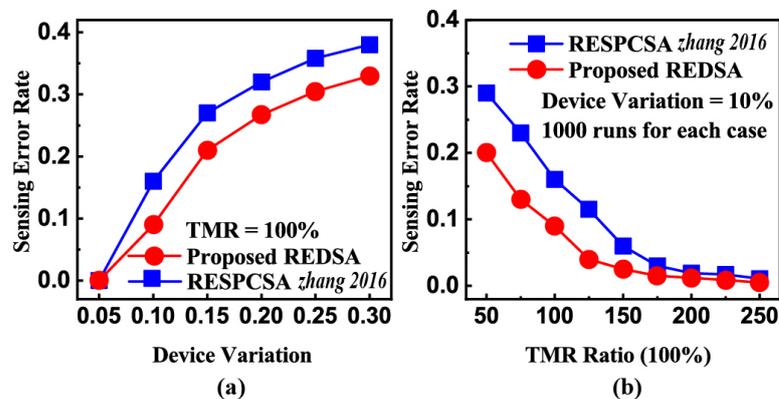


Figure 6. Comparison of the sensing error rate of proposed REDSA and the RESPCSA with respect to different device variation (a) and TMR ratios (b) [17].

4.2. Layout of the Proposed REDSA

A hybrid CMOS/MTJ process can be used to fabricate MTJs as they can be embedded above CMOS circuits. As shown in Figure 7a, the MTJ device can be fabricated between the third metal level (M3) and the fourth metal level (M4) using a 3D back-end integration process. Figure 7b shows the standard cell for one logic bit, which is composed of two complementary MTJs. The MTJ bottom electrode connects to the third metal level (M3) and the MTJ top electrode connects to the fourth metal level (M4). Figure 7c shows the layout of the proposed REDSA, which is drawn with the 40 nm layout design rules. The effective area of the proposed REDSA is about $16.48 \mu\text{m}^2$.

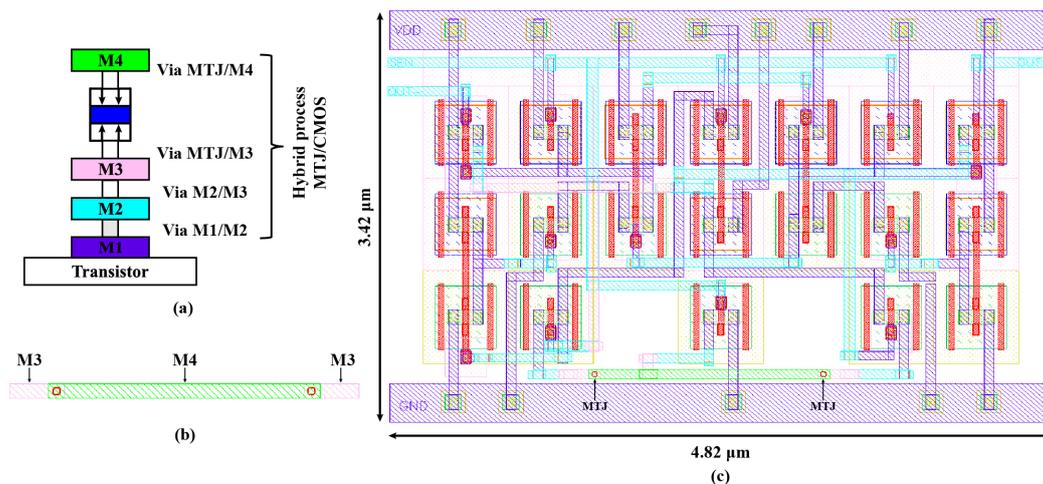


Figure 7. (a) The MTJ nano-pillar is implemented above the CMOS logic circuit with a 3D back-end integration process between the third metal level (M3) and the fourth metal level (M4). (b) The standard cell for one logic bit, which is composed of two complementary MTJs. (c) Layout of the proposed REDSA, where the two MTJs in the layout are marked out in the figure.

4.3. Performance Comparison

Table 2 summarizes the performance comparison of the proposed REDSA and the previous DSAs. As seen, compared to the previous DSAs, the proposed REDSA can achieve a smaller sensing error rate, while retaining almost the same sensing delay of 74.5 ps and sensing energy of 1.92 fJ per bit. Although the main drawback of the proposed REDSA is its relatively larger area, multiple non-volatile memory cells can share one sensing amplifier by using multi-context hybrid CMOS/MTJ logic circuits [31,32].

Table 2. Performance comparison with TMR Ratio of 100% and Process Variation of 10%.

Parameter	PCSA [15]	SPCSA [16]	RESPCSA [17]	This Work
Technology (nm)	40	40	40	40
# of Transistor	7	15	17	19
Latency(ps/bit)	49.1	56.4	66.8	74.5
Sensing Error Rate	0.21	0.18	0.16	0.09
Sensing Energy (fJ/bit)	0.847	1.68	1.83	1.92

5. Conclusions

In this paper, a novel reliability-enhanced differential sensing amplifier with a large sensing margin is proposed to realize high reliability. Hybrid CMOS/MTJ simulation results show that it can achieve a smaller sensing error rate of 9% than that of the previous differential sensing amplifiers, while retaining almost the same sensing delay of 74.5 ps and sensing energy of 1.92 fJ/bit. The proposed REDSA will assist in the design of low-power and high-reliability nonvolatile SRAMs in battery operated sensor nodes and Internet of Things (IoT) applications.

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