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Relative Jitter Measurement Methodology and Comparison of Clocking Resources Jitter in Artix 7 FPGA

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Abstract: Phase jitter is one of the crucial factors in modern digital electronics, determining the reliability of a design. This paper presents a novel approach to designing a jitter comparison system and methodology for FPGA chips using a Tapped Delay Line (TDL)—commonly used to implement a Time-to-Digital Converter (TDC). The design and its revision utilizing latches replacing some of the flip-flops are presented and discussed, with potential further improvements. A minimal temperature influence is verified and presented. The methodology of automated relative jitter measurements is discussed. Multiple different FPGA clock signal path configurations are measured, and the results are presented. The influence of clock routing is identified as critical when MMCM or PLL modules are omitted. It is demonstrated that with careful resource and routing allocation, the clock signal's jitter performance does not have to be deteriorated by the absence of jitter filtering blocks. The proposed technique was implemented and verified and relative jitter performance was measured in the AMD/Xilinx Artix 7 35T FPGA platform.

Keywords: field-programmable gate array (FPGA); tapped delay line (TDL); relative jitter comparison; clocking resources; latch

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1. Introduction

Jitter performance is an important aspect of modern digital electronics—especially microprocessors, field programmable gate arrays (FPGAs), and application-specific integrated circuit (ASIC) devices. However, only a few papers address the aspect of internal FPGA jitter specifically [1–4]. The measurement methodology of these publications involved the use of external equipment. For this reason, a different methodology was developed which utilizes only FPGA resources and allows for comparison of the influence of the jitter generated by different elements. Only an external test clock signal is required. While the presented methodology might not be as precise as other approaches, it gives a rough estimate of the jitter level and allows for a relative comparison of the influence of different FPGA resources on the phase noise.

Several jitter measurement techniques based on FPGAs have already been published. The "Follow Me" method [5] utilizes a Digital Clock Manager (DCM) module [6] to track the slow clock edge movements. However, this method is mainly applicable to low-frequency jitter measurements.

The second technique utilizes a Time-to-Digital Converter (TDC) approach [7]. In contrast to [5], this method is applicable for high-frequency jitter measurements. However, in order to minimize the interpolation error, it requires a significant amount of FPGA resources for multiple phase-shifted counters.

Another technique is based on the measurement of the probability density function (PDF) of the edge distribution over one unit interval (UI) [8]. It utilizes two identical D-type flip-flops clocked by two separated clock signals, sampling the measured signal.

The number of clock cycles during which the output values of the sampling flip-flops are different from each other is counted. Combined with the phase shift of both sampling clock signals, it allows for the measurement of the edge distribution probability density function.

The aforementioned approaches focus on the absolute jitter measurement. However, in certain cases where a fixed and limited set of components is available, information about the relative jitter level obtained using different components may be sufficient. This is the case of FPGA chips with sets of resources used for clock signal propagation.

The presented jitter comparison technique combines the PDF of the edge distribution concept [8] with a tapped delay line (TDL) often used in TDC applications [7,9]. Some resource placement is manually chosen (in contrast to default automatic placement) to minimize the measurement errors between compared signals. The design is used to compare the jitter level of multiple configurations of input clock signal—including standard fabric instead of dedicated clocking resources.

This paper is organized as follows. Section 2 presents the architecture of the relative jitter measurement system. Section 3 describes the methodology of data acquisition and analysis. The reference measurements and initial concept verification are described in Section 4 The results are presented in Section 5. The paper ends with conclusions.

2. Design Architecture

A commercially available Digilent Arty A7-35T [10] development board was selected as a target device for implementation, verification, and measurements. The platform uses an AMD/Xilinx Artix 7 35T FPGA—specifically the XC7A35TICSG324-1L FPGA chip. This modern FPGA family is designed in a 28 nm process [11] and is a relevant example of currently available FPGA technologies.

2.1. Initial Concept

The relative jitter measuring system is based on the dual TDL-based phase difference detector architecture [12]. The main part of the system consists of two symmetrical TDLs implemented as carry chains in the FPGAs. The output of each tap is connected to a synchronizer consisting of two consecutive flip-flops, synchronizing the delayed signal to a system clock domain. The stored values are mutually compared using an array of XOR gates connected to the synchronizers' outputs, as shown in Figure 1. The registered TDLs' taps effectively create a temporary snapshot of an input signal being transmitted through the delay line. As a result, the output vector of the XOR gates is equivalent to the input signal misalignment during a given period of the system clock—assuming the transition of the input signal is captured in both TDLs in a given sample. The outputs of the XOR gates create a vector of differences between both snapshots of the captured input signals in both TDLs. The differences vector is updated every system clock cycle, thus enabling a continuous comparison of the input signals.

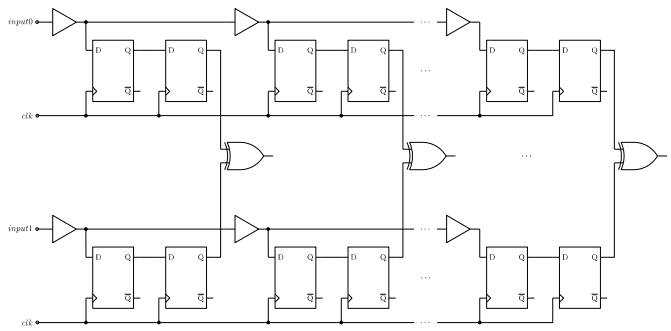


Figure 1. TDL-based phase difference detector architecture diagram.

Tapped delay lines are often implemented in FPGAs using carry chains. This approach is common in TDC designs, e.g., in [9,13–15]. In contrast to other FPGA resources (i.e., lookup tables or LUTs), carry logic uses dedicated carry multiplexers (that can be used as

delays) and can be cascaded to form a wider chain [16] in a Configurable Logic Block (CLB) without the use of generic switching fabric. Additionally, each carry multiplexer can be connected to a storage element (configured as a D-type flip-flop or level-sensitive latch) in the same CLB slice (in 7 Series FPGAs each CLB element contains a pair of slices [16]). In Figure 2, a single slice block diagram is depicted, with carry logic highlighted. For these reasons, CARRY4 primitives [17], implementing carry chain, were instantiated in the design.

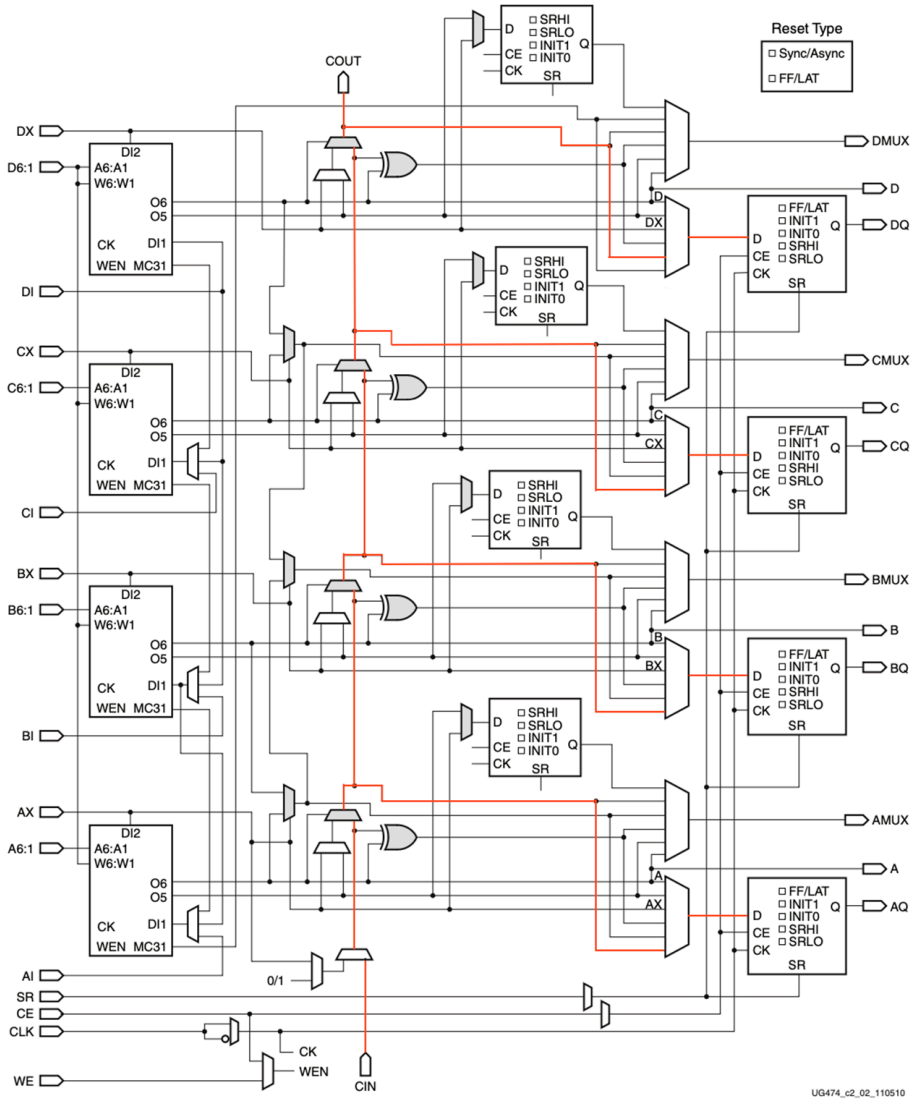


Figure 2. Diagram of SLICEM [16], with carry logic path and connections to storage elements highlighted.

The placement was manually selected so that both TDL delays match (across all taps) and the system clock source to each corresponding flip-flop delay is matched. All of the aforementioned delay requirements have been precisely matched for all four process corners reported by Xilinx Vivado (with 1 ps precision)—despite the graphically displayed differences in the device view. Until the very last interconnects to the flip-flops in the slices, the system clock signal is transmitted using the same path, as depicted in Figure 3. These results suggest that selected logic cells and their interconnects are the closest implementation of two mirrored and symmetrical TDLs that it is possible to achieve in this FPGA chip. A simplified diagram of the selected Artix 7 FPGA's clock regions, resources, clock-capable pins, and TDL placement is depicted in Figure 4.

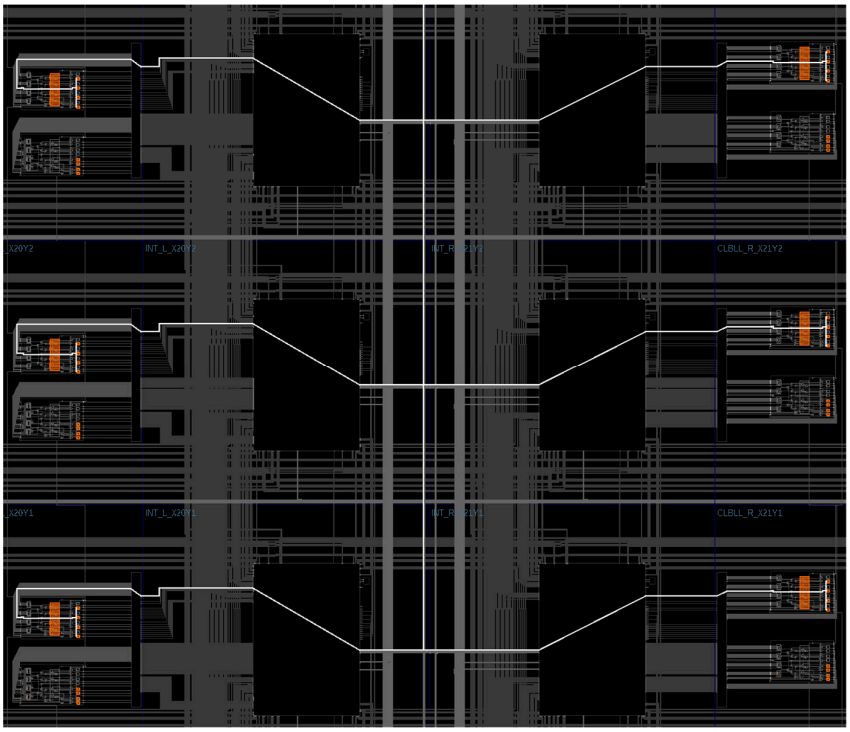


Figure 3. Selected section of an implemented device view illustrating the system clock to TDL flip-flops connection. The orange elements are parts of the TDLs.

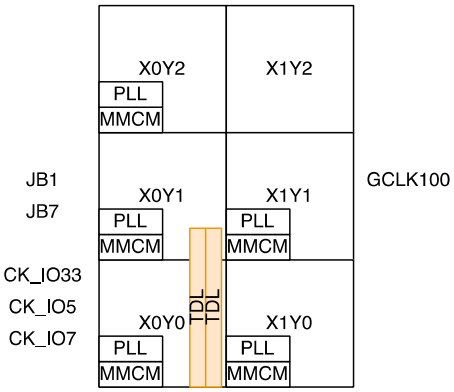


Figure 4. Simplified block diagram of the selected FPGA clocking resources and TDL placement in AMD/Xilinx Artix 7 35T FPGA.

The symmetrical delays from the system clock source to TDL flip-flops ensure that the input signals are captured at the same time, with minimal to no impact from system clock jitter, process, supply voltage, or temperature variations.

The TDLs are connected to the transition detection circuit described in [12]. Once a transition is captured in both TDLs, the XOR-ed difference of the two TDL vectors is stored in a block RAM [18]. The memory can be read and written from a PC to which a FPGA board (in this case Digilent Arty A7-35T [10]) is connected via a USB cable. For this purpose, a combination of AXI Block RAM Controller [19] and JTAG to AXI Master [20] IP blocks has been implemented. This solution enables a block memory access via a Tcl console in a Xilinx Vivado development environment. To avoid additional complexity, all submodules operate in the same system clock domain. The block diagram is depicted in Figure 5.

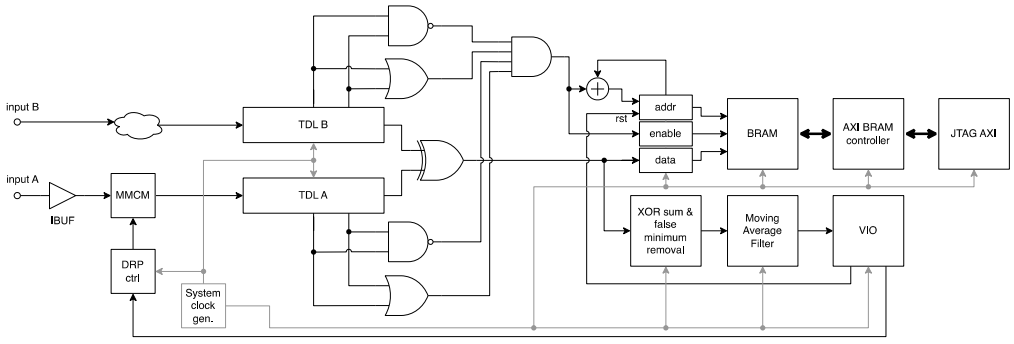


Figure 5. Simplified block diagram of data acquisition system.

The maximum configurable width of the AXI bus in the JTAG to AXI Master IP block is 64 bits [20]. The dual port block RAM, with one port set to the data width of 64 bits, can be configured to the maximum data width of 256 bits on the second port [18]. For this reason and to avoid additional complexity, 256 taps was set as the length of both TDLs. The length of 256 taps has later proven to be a sufficient value, which does not limit the operation of the measurement acquisition.

In parallel, the XOR-ed difference of the two TDL vectors is summed and filtered. In order to mitigate the issue of improper TDL lengths compared to the input signal frequency [12], additional logic has been added (named "false minimum removal" in Figure 5). The filter input is set to a maximum value (representing phase misalignment), if:

- No transition is detected in both TDLs for a certain amount of time;
- Multiple transitions are detected in the XORed difference of the two TDL vectors—as depicted in Figure 6.

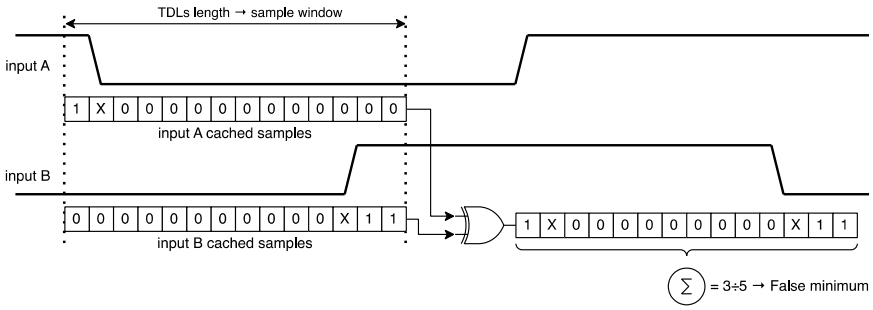


Figure 6. Example waveform of the captured input signals resulting in a false minimum detection. All registers are in the same clock domain.

The stream of XOR-ed differences is filtered using a moving average filter (MA filter). The moving average filter is a common smoothing method; it is a time-domain finite impulse response filter. It is quite simple in design as well as in implementation. The most significant parameter that needs to be determined when the MA filter is used is the filter length. Compared to other types of filters, it has the sharpest step response [21].

The filtered value is redirected to the Virtual Input/Output [22] IP block along with the current block memory address. This module enables access to selected signals in the FPGA design from a PC to which the FPGA board is connected, without the need for additional ports.

The Virtual Input/Output block also controls the DRP (Dynamic Reconfiguration Port) controller module. This module is based on the Xilinx Application Note [23] and a reference design. It is responsible for configuring the Mixed-Mode Clock Management (MMCM—an advanced PLL module with programmable phase shift) that is always placed on one of the input signal paths—as depicted in Figure 5. The MMCM is always configured to replicate the input signal frequency to the output signal frequency. The DRP controller is used only

to selectively phase shift the signal prior to the TDL input. This is also the reason why the MMCM is always present on one of the input signals paths. This is further discussed in Section 3.

The design uses minimal resources. Table 1 presents the post-implementation resource utilization. The only resource used significantly is BRAM. Block memory is used only to store samples for later readout via JTAG to the AXI Master block. Therefore, a high utilization of this resource was intentional and can be reduced at the expense of larger number of memory readout operations.

Table 1. Total resource utilization of the implemented design.

Resource	Utilization	Available	Utilization %
LUT	3116	20,800	14.98%
LUTRAM	372	9600	3.88%
FF	4442	41,600	10.68%
BRAM	44	50	88%
DSP	0	90	0%

3. Measurement Methodology

The measurement acquisition is automated using Tcl scripting and utilizing JTAG to the AXI Master and Virtual Input/Output (VIO) blocks depicted in Figure 5. The acquisition procedure takes seven steps, with the first three steps skipped for the design verification measurements presented in Sections 4.1 and 4.2:

1. Set the MMCM phase shift value (from 0 to 255) via the VIO and restart the MMCM;
2. Read 16 average measurements (MA filter output values) via the VIO and calculate the final average for the currently selected MMCM phase shift value;
3. After repeating the first and second step for all 256 phase shifts, set the MMCM phase shift equal to the value corresponding to the least average measurement acquired in Step 2;
4. After resetting the BRAM via the VIO, wait for memory to fill up with data;
5. Read the FPGA die temperature using a temperature sensor in the FPGA XADC (system monitor) [24];
6. Read the BRAM data to the connected PC via the JTAG to the AXI Master;
7. Repeat steps four through six fifty times and merge the acquired data and temperatures to two CSV files.

The BRAM block contains 2048 256-bit words. Therefore, the total number of raw samples for each measurement equals 102,400.

Afterward, the raw measurements are processed on a PC. The probability density function (PDF) can be obtained by counting the number of '1s' (the equivalents of the differences between two channels) in each 256-bit word and summing the number of occurrences of each value of the counted number of differences.

The input signals were generated using a Si5351 clock generator. Its maximum output jitter equals 100 ps peak-to-peak [25]. To reduce jitter, two outputs of the generator were programmed in the integer mode at 23.4375—both using the same internal phase-locked loop (PLL). During verification and measurements, each tested channel pin was directly connected to a separate output of the generator– with no additional intermediary such as a tee connector (which could negatively impact signal integrity and amplitude). The system clock frequency was set to 50 MHz and was generated from an on-board oscillator.

The initial verification involved the same signal sent to both TDLs' inputs. The reported delays from each FPGA input pin to the corresponding TDL input have been matched (with 1 ps precision). Similarly to the connection of the system clock to the TDLs' flip-flops depicted in Figure 3, the measured signal is transmitted using the same paths until the very last interconnects before the final slices. The delay from the MMCM OUTPUT0 port to each TDL input is the same with 1 ps precision. The signal was transmitted directly

to the TDLs' inputs—with no additional global buffers (BUFG) placed in the path. Such buffers are often added automatically by the tool; therefore, this action had to be manually prevented using design constraints. Theoretically, the global buffer has a rather negative influence [26] or no influence on the signal phase noise. Therefore, no additional buffer and a common clock region were selected. The described auto comparison is considered a reference result for further analysis of the results.

3.1. Calculation of Absolute Jitter

Calculating the absolute or period jitter values [27] based on the obtained differences vector for the presented design is theoretically possible, but difficult. It would require taking into account several effects:

- The CARRY4 primitive delays reported by Xilinx Vivado are the same for all elements used for TDL implementation, but differ depending on the PVT corner—as depicted in Table 2;
- The reported delays for each CARRY4 primitive are non-monotonic—as depicted in Table 2;
- The interconnect delays between the consecutive CARRY4 elements reported by Xilinx Vivado are 0 (with 1 ps precision) for interconnects in a single clock region, and non-zero for interconnects across clock regions;
- While the paths from the system clock source to the corresponding TDL flip-flops are symmetrical (as described in Section 2.1), the delays for each flip-flop pair are different and non-monotonic—as depicted in Tables S1 and S2 in the Supplementary Materials;
- The setup and hold time violations (resulting in storage elements metastability) are inherent to the TDL architecture, which is an additional source of Gaussian jitter [28] that would need to be subtracted from the raw measurement. This effect is further discussed in Section 4.1.

Table 2. Delays of CARRY4 element reported by Xilinx Vivado for four PVT corners.

CARRY4 Input	CARRY4 Output	FAST_MAX Corner	FAST_MIN Corner	SLOW_MAX Corner	SLOW_MIN Corner
CYINIT	CO0	206 ps	165 ps	536 ps	432 ps
CYINIT	CO1	180 ps	144 ps	494 ps	398 ps
CYINIT	CO2	210 ps	169 ps	592 ps	477 ps
CYINIT	CO3	215 ps	173 ps	580 ps	467 ps
CIN	CO0	100 ps	76 ps	271 ps	206 ps
CIN	CO1	56 ps	45 ps	157 ps	127 ps
CIN	CO2	81 ps	65 ps	228 ps	184 ps
CIN	CO3	49 ps	39 ps	114 ps	92 ps

The implications of these effects include counting the exact positions of the detected differences in each vector and calculating the ranges of timing differences for each PVT corner individually. As neither the input-to-output delays of the CARRY4 element, nor the delays from the system clock source to the flip-flop pairs are monotonic, the series of '1' bits in the raw results can be interrupted by one or several '0' bits. The temporary value of absolute jitter would need to be calculated for each of more than 100,000 raw samples individually for each measurement, resulting in a need for a significant amount of computing resources.

Taking into account the above considerations, the purpose of the described design is the measurement of relative jitter that enables multiple configurations to be compared. As a result, the most suitable configuration can be selected for a given application and system constraints.

3.2. Relative Entropy Calculation

As the task of obtaining the most valuable absolute jitter calculation was deemed impractical considering limited data on internal Xilinx resources, the comparison of the relative jitter became one of the most important objectives of the described research. The Kullback–Leibler divergence [29], also known as a relative entropy, is one of the most recognized measures to compare two probability distributions. It is a nonnegative function with the following formula:

$$D_{KL}(P||Q) = \sum_{x \in \chi} P(x) log\left(\frac{P(x)}{Q(x)}\right) \quad (1)$$

where:
$D_{KL}(P||Q)$: relative entropy;
χ: sample space;
P, Q: probability distributions.

The results of the Kullback–Leibler divergence calculation for multiple clocking resource configurations are presented in Section 5. It is worth noting that for meaningful results, the compared distributions need to have the same sample space. Moreover, non-zero values of Q distribution are required for proper division. To fulfill these requirements, the shorter distribution was padded with a non-zero guard value, which was very small with respect to the main lobe. All zero positions in P and Q distributions were also replaced with the guard value.

4. Reference Measurements and Initial Concept Revision

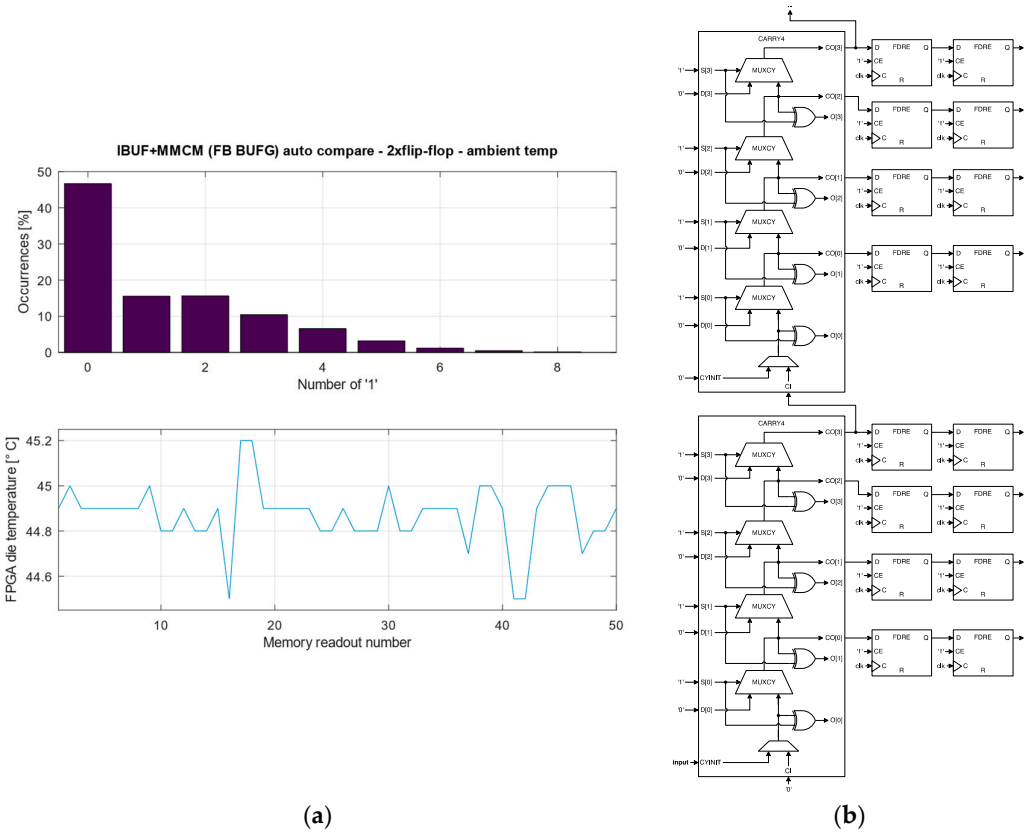
4.1. Design Verification

To verify the presented design, both TDLs' inputs were connected to the same signal source, i.e., the output of the same MMCM primitive [17]. The MMCM block, the clock-capable input pin, and the first taps of TDLs were placed in the X0Y0 clock region, as depicted in Figure 4. Apart from the MMCM feedback loop, no global clock buffers (BUFG) [17] were used. Due to the placement of the TDLs, until the very last interconnects before the first CARRY4 input, the MMCM output signal is transmitted using the same path—similar to the system clock signal paths shown in Figure 3. The reported delay from the MMCM output to each carry chain input is the same for both TDLs.

In the ideal case, the measured differences between the captured signals would be equal to zero 100% of the time. However, the measurements show that only <50% of the captured samples contained zero differences. The exact statistics and distribution are presented in Figure 7a and Table 3. The details of the measurement methodology are described in Section 3.

Table 3. Distribution of the number of detected differences at ambient temperature for two different TDLs' configurations.

Number of '1s'	2x Flip-Flop Configuration	Latch + Flip-Flop Configuration
0	46.682%	59.646%
1	15.561%	20.775%
2	15.658%	14.968%
3	10.456%	4.194%
4	6.604%	0.415%
5	3.192%	0.001%
6	1.188%	0.000%
7	0.502%	0.000%
8	0.158%	0.000%
9	0.000%	0.000%



(**a**) (**b**)

Figure 7. Measured number of differences using TDLs with 2x flip-flop configuration at ambient temperature: (**a**) measurement results; (**b**) simplified schematic diagram of the corresponding implemented TDL.

The difference between the ideal theoretical results and the data actually obtained is partially caused by the metastability of the asynchronous flip-flops in the TDLs (presented in Figure 1). Metastability is an unavoidable phenomenon that might cause state uncertainty in a bistable circuit and variations in its propagation delay. State uncertainty is nondeterministic and depends on the circuit's sensitivity to the initial condition near the metastable point. It is known that the initial condition is disturbed by thermal noise processes, thus the flip-flop's operation near the metastable point ensures state randomness [30]. For this reason, the outputs of two corresponding flip-flops from different TDLs are random during input signal transitions. The minimum setup and hold times of CLB flip-flops equal 110 and 220 ps, respectively, ref. [31] and the CARRY4 element delays can be significantly lower than 100 ps (depending on ports and process corner—as depicted in Table 2). As a result, in the absolute worst case, up to 7 flip-flops input signals from CARRY4 outputs can violate the setup timing condition, and up to 18 can violate the hold timing condition—as depicted in Table 4. The timing violations can result in metastability and a greater number of differences between stored TDLs' words than expected.

Another reason for the difference between the ideal theoretical results and the data actually obtained is non-ideal symmetry between the two TDLs. The FPGAs are not designed for this purpose. As a result, the complementary TDLs' elements (both carry multiplexers and storage elements) as well as the interconnects differ in timing performance.

After examination of the CARRY4 elements' timing performance reported by the Vivado tool, it turned out the delays are different for CYINIT and CIN inputs—as shown in Table 2. However, Vivado reports the same delays for each CARRY4 element used. As a result, the design was modified so that the first CARRY4 element was used only as a pass-through to the whole carry chain—with no outputs connected to storage elements. This ensures the same delays for each CARRY4 element in chain.

Table 4. Cumulative delays of cascaded CARRY4 elements in FAST_MIN process corner (reported interconnect delay between CARRY4 elements in the same clock region equals 0 ps).

CARRY4 Element Index	CARRY4 Element Output	Accumulated Delay	Setup Time Violation	Hold Time Violation
0	CO0	76 ps	✔	✔
	CO1	45 ps	✔	✔
	CO2	65 ps	✔	✔
	CO3	39 ps	✔	✔
1	CO0	115 ps	✘	✔
	CO1	84 ps	✔	✔
	CO2	104 ps	✔	✔
	CO3	78 ps	✔	✔
2	CO0	154 ps	✘	✔
	CO1	123 ps	✘	✔
	CO2	143 ps	✘	✔
	CO3	117 ps	✘	✔
3	CO0	193 ps	✘	✔
	CO1	162 ps	✘	✔
	CO2	182 ps	✘	✔
	CO3	156 ps	✘	✔
4	CO0	232 ps	✘	✘
	CO1	201 ps	✘	✔
	CO2	221 ps	✘	✘
	CO3	195 ps	✘	✔

To mitigate the aforementioned issues, for each delay line tap the first flip-flop in the synchronizer chain has been replaced with a latch—using the LDCE primitive [17]. Latches are known to have better timing performance compared to flip-flops [32,33]. In contrast to flip-flops, a latch register is transparent for a portion of the clock period and stores the input on the clock edge that causes the latch to become opaque. Flip-flops are edge sensitive, and latches are level sensitive [34]. An example of sample acquisition waveform is depicted in Figure 8.

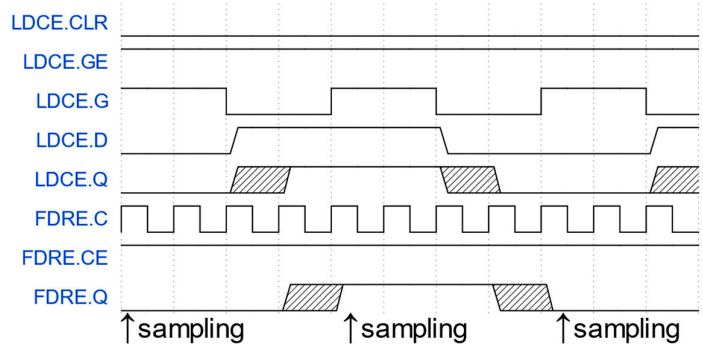
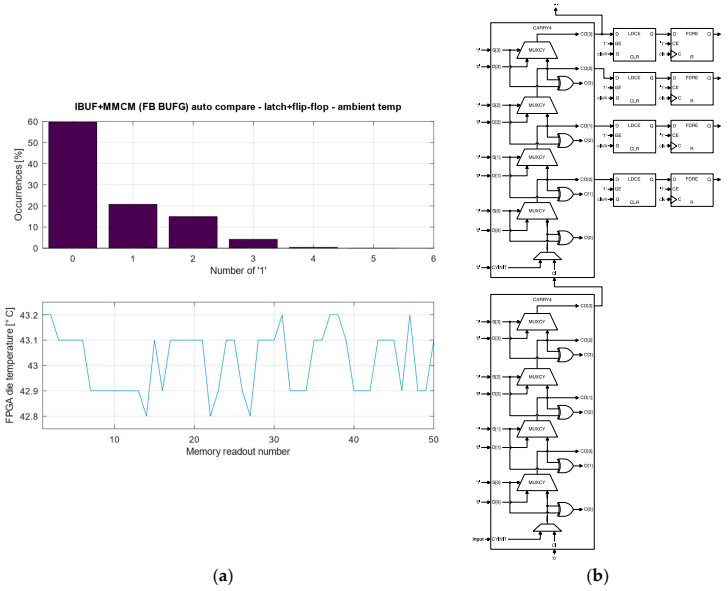


Figure 8. Example waveform of latch+flip-flop pair sample acquisition.

Similarly to the initial two flip-flop approach, the latch+flip-flop configuration has been verified using the auto comparison described previously. The measurements have

shown a significant increase in the 0 difference detection number, by over 10 percentage points. The exact statistics and distribution are presented in Figure 9a and Table 3.



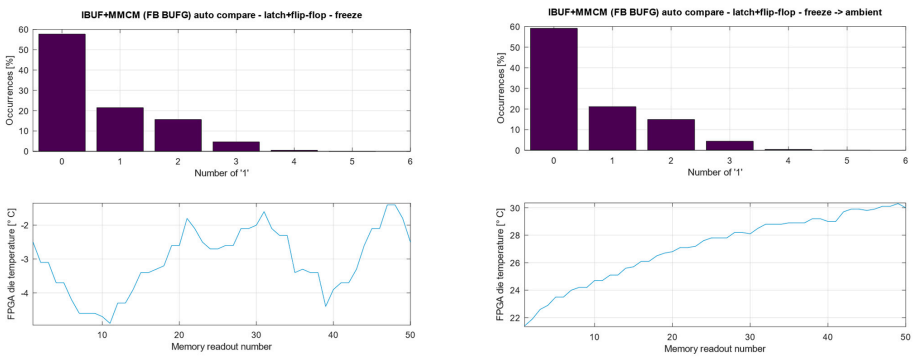
(**a**) (**b**)

Figure 9. Measured number of differences using TDLs with latch+flip-flop configuration at ambient temperature: (**a**) measurement results; (**b**) simplified schematic diagram of the corresponding implemented TDL.

4.2. Temperature Influence

The delay time of a carry chain is sensitive to the manufacturing process, supply voltage, and operating temperature (PVT), thus the measurement precision and accuracy could deteriorate due to voltage and temperature variation [35]. Like time generators, the absolute phase comparators are sensitive to process, voltage, and temperature (PVT) variations. On the contrary, the relative time generators and comparators are robust to PVT. However, the relative methods are hampered by path or element mismatches [36].

The operation of the design has been also verified at temperatures below 0 °C. The distributions of detection numbers are presented in Figure 10 and Table 5. The observed temperature influence is minimal. The final deviation from the ideal theoretical distribution is most probably mainly caused by the metastability and element mismatch. Theoretically, using LVT transistors in the TDLs' latches could further improve the results, as low threshold voltage transistors are known to have lower delay compared to SVT and HVT [37]. The implementation of a dedicated ASIC chip and verification might be an interesting topic for future research.



(**a**) (**b**)

Figure 10. Measured number of differences using TDLs with latch+flip-flop configuration at temperatures ranging (**a**) from −4.9 °C to −1.4 °C; (**b**) from 21.4 °C to 30.3 °C.

Table 5. Distribution of the number of the detected differences using TDLs lath+flip-flop configuration with 2 CARRY4 CO outputs used, at different temperatures.

Number of '1s'	Ambient Temperature <42.8 °C; 43.2 °C>	Freezing Temperature <−4.9 °C; −1.4 °C>	Heating Up from Freezing Temperature <21.4 °C; 30.3 °C>
0	59.646%	57.697%	59.130%
1	20.775%	21.491%	21.155%
2	14.968%	15.648%	14.910%
3	4.194%	4.640%	4.397%
4	0.415%	0.510%	0.406%
5	0.001%	0.0137%	0.001%
6	0.000%	0.000%	0.000%

Apart from the number of zero detected differences (the first bar in Figures 7, 9 and 10), the number of bars (the horizontal axis range of each bar chart in this paper is always equivalent to the last non-zero result) and overall results distribution are equally important.

5. Results

All FPGA chips contain several types of I/O pins. One of their attributes is being a clock-capable pin or not. The clock-capable pins can access either a single or multiple clock region and the global clock tree, as well as other CMTs above and below in the same column [38] using clock resources. The non-clock-capable pins are not directly connected to clock resources and to be utilized as clock signal inputs, they need to be routed using general routing matrices. Both kinds of pins were compared in multiple configurations of the input clock signal. During all measurements, signals with the same frequency (generated in the same PLL in the Si5351 generator) were separately connected to the input pins.

The results are divided into five groups:

- Involving a common input pin and a single common clock region for TDLs and both compared signal sources;
- Involving a common input pin and a separate clock region for TDLs with a reference signal source and a second clock region for a compared signal source;
- Involving a separate input pin and a single common clock region for TDLs and both compared signal sources;
- Involving a separate input pin (in common I/O bank) and a separate clock region for TDLs with a ref. signal source and second clock region for a compared signal source;
- Involving a separate input pin (in different I/O bank) and a separate clock region for TDLs with a ref. signal source and second clock region for a compared signal source.

All detailed results are presented in Tables S3–S9 in the Supplementary Materials.

5.1. Common Input Pin and Single Common Clock Region

The TDLs are placed in the X0Y0 clock region—as depicted in Figure 4. Therefore, the common clock region comparisons involve only resources located in the X0Y0 clock region (e.g., MMCM, PLL, input buffers (IBUF)) and between the contiguous clock regions (e.g., global buffers (BUFG)). The input pin used for these tests is clock-capable T14 (named CK_IO5 in Arty A7 board). Table 6 presents the schematic diagrams and the measurement results at ambient temperature of multiple connection configurations involving a common input pin and a single common clock region. Table S3 presents the detailed results—both absolute and percentage numbers.

Table 6. Measurements results and diagrams for configurations with common input pin and common clock region.

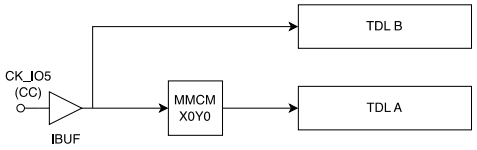
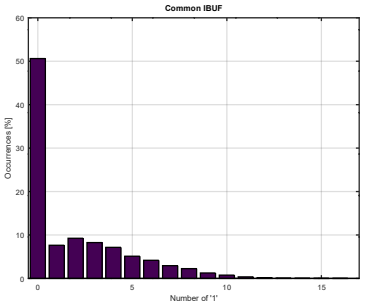
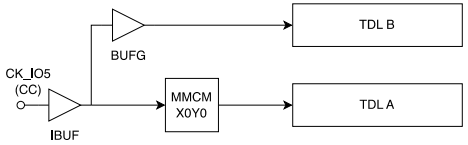
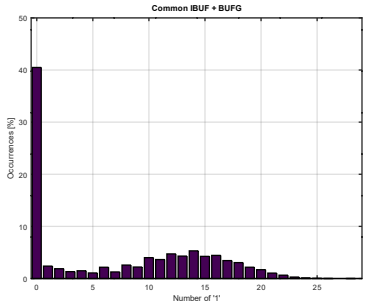
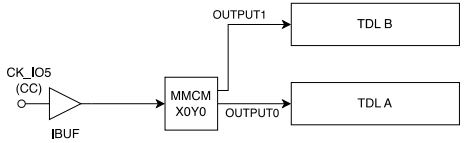
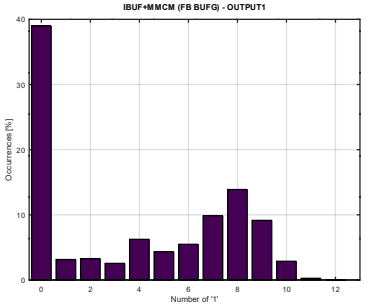
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.1.1	Common IBUF	 • Maximum number of the detected differences: 16. • The most common number of the detected differences is 0 (50.614% occurrences).	
5.1.2	Common IBUF + BUFG	 • Maximum number of the detected differences: 28. • The most common number of the detected differences is 0 (40.490% occurrences).	
5.1.3	Separate MMCM output	 • Maximum number of the detected differences: 12. • The most common number of the detected differences is 0 (38.984% occurrences).	

Table 6. *Cont.*

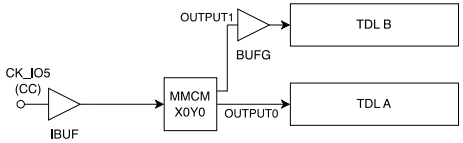
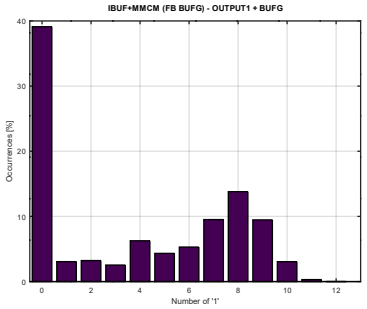
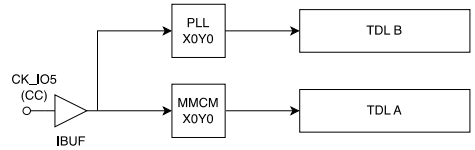
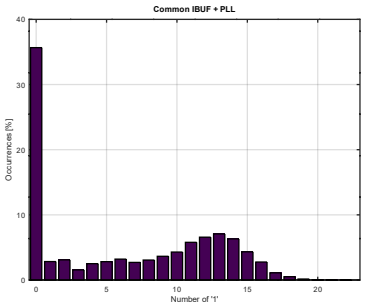
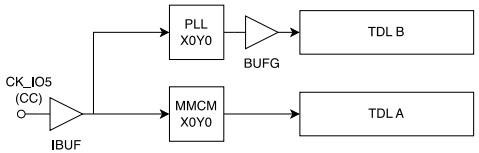
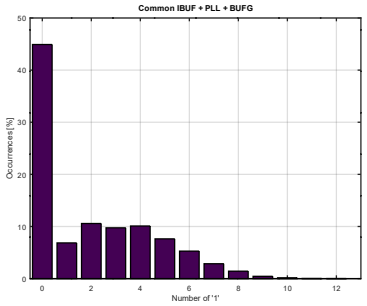
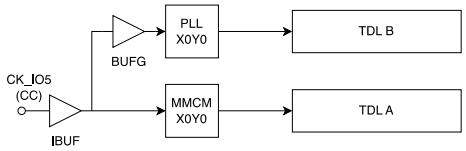
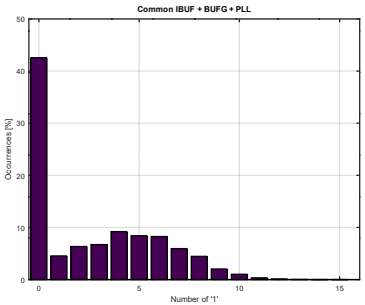
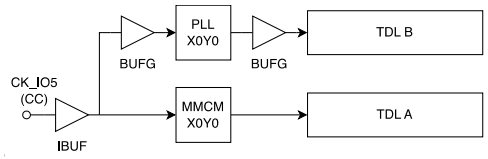
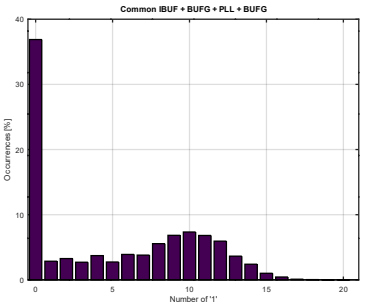
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.1.4	Separate MMCM output + BUFG	 • Maximum number of the detected differences: 12. • The most common number of the detected differences is 0 (39.118% occurrences).	
5.1.5	Common IBUF + same clock region PLL	 • Maximum number of the detected differences: 22. • The most common number of the detected differences is 0 (35.665% occurrences).	
5.1.6	Common IBUF + same clock region PLL + BUFG	 • Maximum number of the detected differences: 12. • The most common number of the detected differences is 0 (44.912% occurrences).	

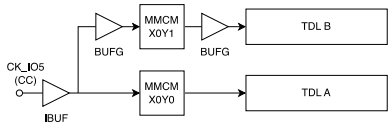
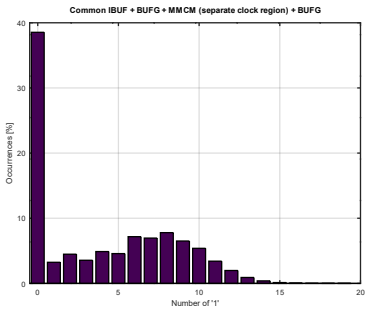
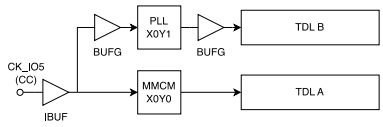
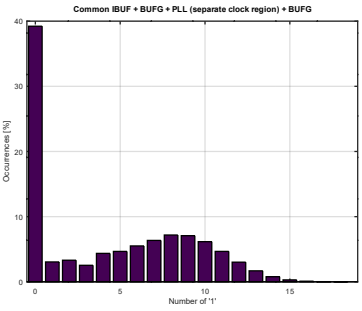
Table 6. *Cont.*

Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.1.7	Common IBUF + BUFG + same clock region PLL	 • Maximum number of the detected differences: 15. • The most common number of the detected differences is 0 (42.565% occurrences).	
5.1.8	Common IBUF + BUFG + same clock region PLL + BUFG	 • Maximum number of the detected differences: 20. • The most common number of the detected differences is 0 (36.882% occurrences).	

5.2. Common Input Pin and a Separate Clock Region

In contrast to the previous tests, the placement of the MMCM or PLL blocks in a different clock region can both positively and negatively impact the jitter level. For this test the X0Y1 clock region was selected. A smaller number of clock signals in the X0Y1 clock region can result in less noise in the measured traces. At the same time the clock region crossing might introduce additional jitter. Due to the FPGA architecture, the global buffers are required for transmitting the signal in and out of the contiguous clock regions. Table 7 presents the schematic diagrams and the measurements results at ambient temperature of multiple connection configurations involving a common input pin and a separate clock region. Table S4 presents the detailed results—both absolute and percentage numbers.

Table 7. Measurements results and diagrams for configurations with common input pin and a separate clock region.

Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.2.1	Common IBUF + BUFG + separate clock region MMCM + BUFG	 • Maximum number of the detected differences: 19. • The most common number of the detected differences is 0 (38.537% occurrences).	
5.2.2	Common IBUF + BUFG + separate clock region PLL + BUFG	 • Maximum number of the detected differences: 18. • The most common number of the detected differences is 0 (39.225% occurrences).	

5.3. Separate Input Pin in the Same Clock Region and a Single Common Clock Region

The TDLs are placed in the X0Y0 clock region—as depicted in Figure 4. Therefore, the common clock region comparisons involve only resources located in the X0Y0 clock region (e.g., MMCM, PLL, input buffers (IBUF)) and between the contiguous clock regions (e.g., global buffers (BUFG)). The input pins used for these tests are from the same X0Y0 clock region and the same I/O bank:

- Clock-capable T14 pin (named CK_IO5 in Arty A7 board),
- Clock-capable P15 pin (named CK_IO33 in Arty A7 board),
- Non-clock-capable T16 pin (named CK_IO7 in Arty A7 board).

Table 8 presents the schematic diagrams and the measurements results at ambient temperature of multiple connection configurations involving a common input pin and single common clock region. Tables S5 and S6 present the detailed results—both absolute and percentage numbers.

Table 8. Measurements results and diagrams for configurations with a separate input pin and a single common clock region.

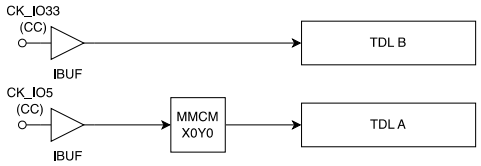
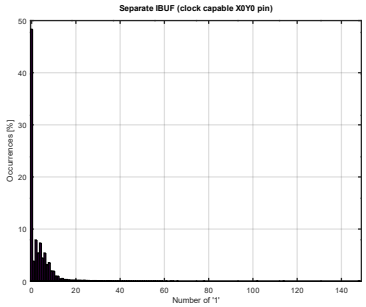
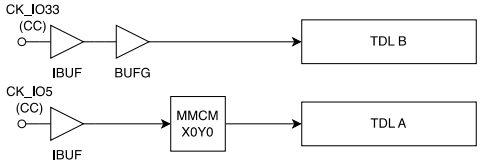
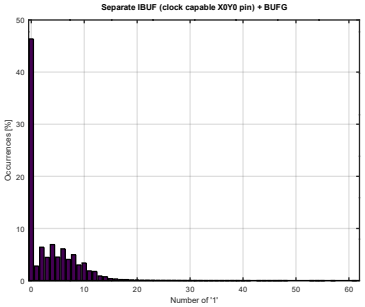
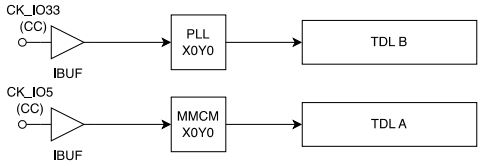
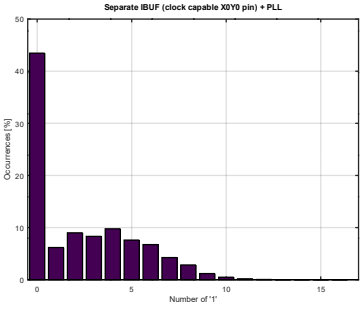
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.3.1	Separate IBUF (clock-capable pin in the same clock region)	 • Maximum number of the detected differences: 148. • The most common number of the detected differences is 0 (48.333% occurrences).	
5.3.2	Separate IBUF (clock-capable pin in the same clock region) + BUFG	 • Maximum number of the detected differences: 61. • The most common number of the detected differences is 0 (46.363% occurrences).	
5.3.3	Separate IBUF (clock-capable pin in the same clock region) + same clock region PLL	 • Maximum number of the detected differences: 16. • The most common number of the detected differences is 0 (43.463% occurrences).	

Table 8. *Cont.*

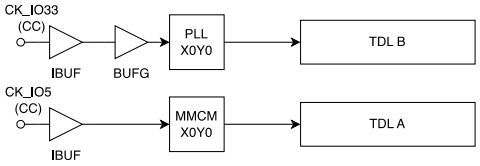
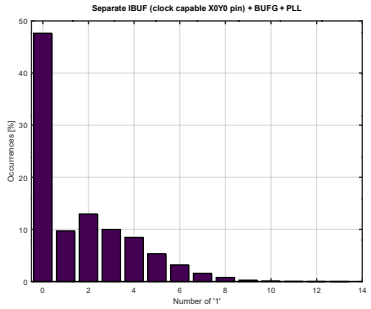
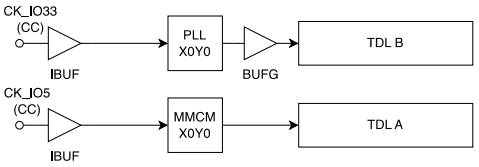
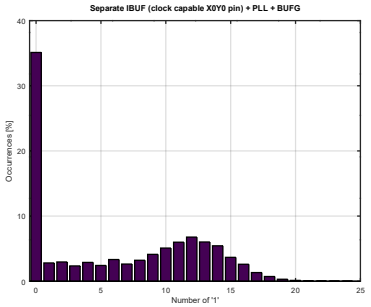
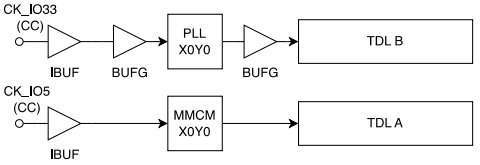
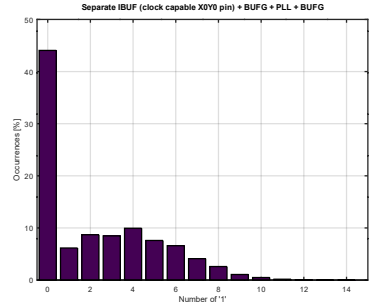
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.3.4	Separate IBUF (clock-capable pin in the same clock region) + BUFG + same clock region PLL	 • Maximum number of the detected differences: 13. • The most common number of the detected differences is 0 (47.636% occurrences).	
5.3.5	Separate IBUF (clock-capable pin in the same clock region) + same clock region PLL + BUFG	 • Maximum number of the detected differences: 24. • The most common number of the detected differences is 0 (35.111% occurrences).	
5.3.6	Separate IBUF (clock-capable pin in the same clock region) + BUFG + same clock region PLL + BUFG	 • Maximum number of the detected differences: 14. • The most common number of the detected differences is 0 (44.056% occurrences).	

Table 8. *Cont.*

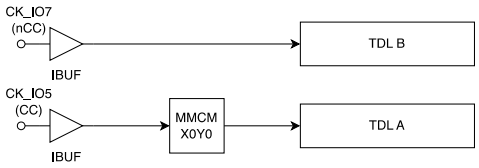
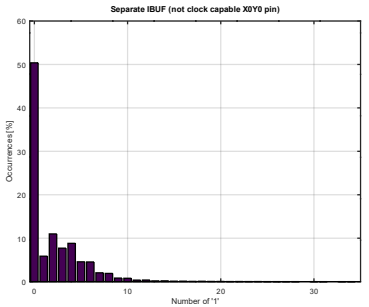
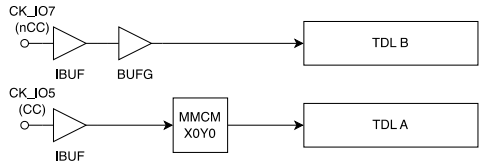
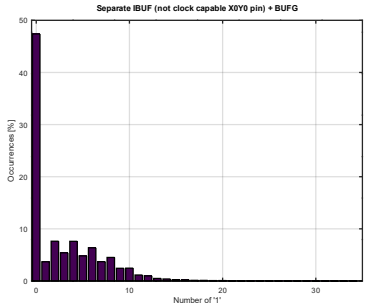
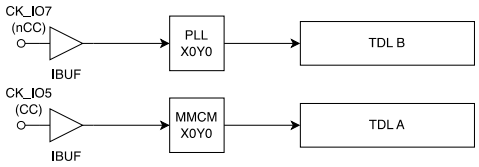
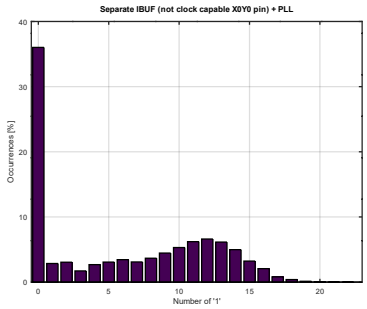
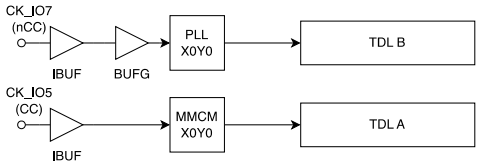
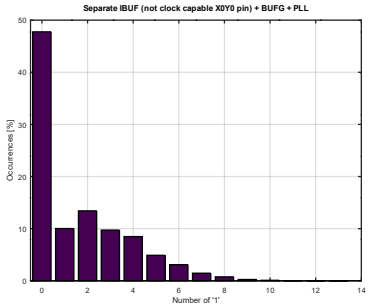
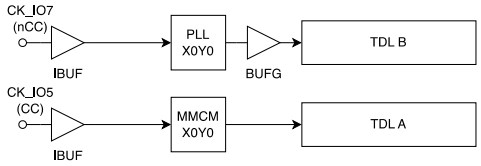
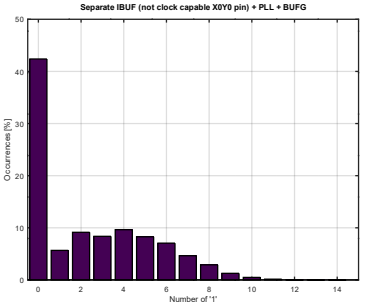
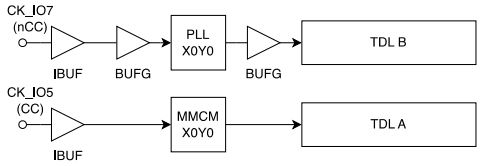
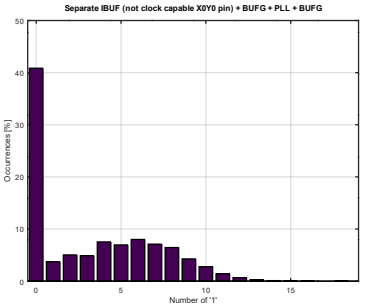
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.3.7	Separate IBUF (non-clock-capable pin in the same clock region)	 • Maximum number of the detected differences: 34. • The most common number of the detected differences is 0 (50.376% occurrences).	
5.3.8	Separate IBUF (non-clock-capable pin in the same clock region) + BUFG	 • Maximum number of the detected differences: 40. • The most common number of the detected differences is 0 (47.387% occurrences).	
5.3.9	Separate IBUF (non-clock-capable pin in the same clock region) + same clock region PLL	 • Maximum number of the detected differences: 22. • The most common number of the detected differences is 0 (36.021% occurrences).	

Table 8. *Cont.*

Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.3.10	Separate IBUF (non-clock-capable pin in the same clock region) + BUFG + same clock region PLL	 • Maximum number of the detected differences: 13. • The most common number of the detected differences is 0 (47.764% occurrences).	
5.3.11	Separate IBUF (non-clock-capable pin in the same clock region) + same clock region PLL + BUFG	 • Maximum number of the detected differences: 14. • The most common number of the detected differences is 0 (42.387% occurrences).	
5.3.12	Separate IBUF (non-clock-capable pin in the same clock region) + BUFG + same clock region PLL + BUFG	 • Maximum number of the detected differences: 18. • The most common number of the detected differences is 0 (40.851% occurrences).	

5.4. Separate Input Pin (in Common I/O Bank) and a Separate Clock Region

In contrast to the previous tests, the placement of the MMCM or PLL blocks in a different clock region can impact the jitter level either positively or negatively. For this test, the X0Y1 clock region was selected. The tested input signals are received through clock-capable and non-clock-capable pins in the X0Y0 clock region.

A lower number of clock signals in the X0Y1 clock region can result in less noise in the measured traces. At the same time the clock region crossing might introduce additional jitter. Due to the FPGA architecture, the global buffers are required for transmitting the signal in and out of the contiguous clock regions. Table 9 presents the schematic diagrams and the measurements results at ambient temperature of multiple connection configurations involving a common input pin and a separate clock region. Table S7 presents the detailed results—both absolute and percentage numbers.

Table 9. Measurement results and diagrams for configurations with a separate input pin (in common I/O bank) and a separate clock region.

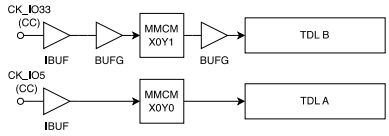
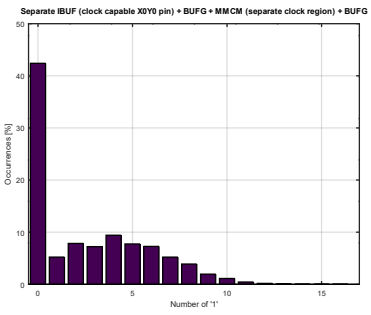
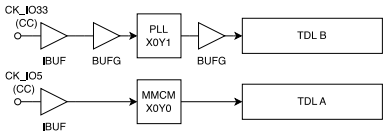
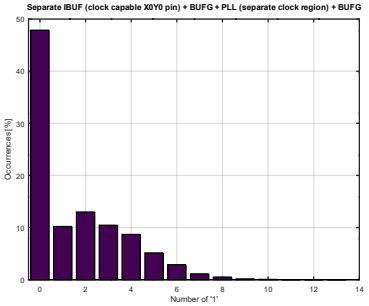
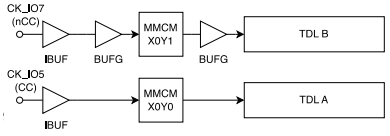
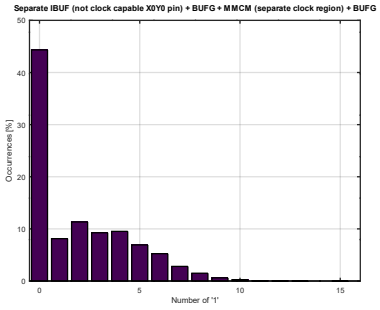
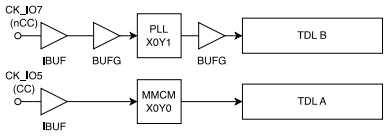
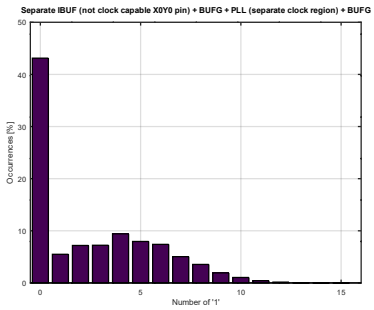
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.4.1	Separate IBUF (clock-capable pin in the same clock region) + BUFG + different clock region MMCM + BUFG	 • Maximum number of the detected differences: 16. • The most common number of the detected differences is 0 (42.397% occurrences).	
5.4.2	Separate IBUF (clock-capable pin in the same clock region) + BUFG + different clock region PLL + BUFG	 • Maximum number of the detected differences: 13. • The most common number of the detected differences is 0 (47.857% occurrences).	
5.4.3	Separate IBUF (non-clock-capable pin in the same clock region) + BUFG + different clock region MMCM + BUFG	 • Maximum number of the detected differences: 15. • The most common number of the detected differences is 0 (44.335% occurrences).	

Table 9. *Cont.*

Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.4.4	Separate IBUF (non-clock-capable pin in the same clock region) + BUFG + different clock region PLL + BUFG	 • Maximum number of the detected differences: 15. • The most common number of the detected differences is 0 (43.118% occurrences).	

5.5. Separate Input Pin (in Different I/O Bank) and a Separate Clock Region

The TDLs are placed in the X0Y0 clock region—as depicted in Figure 4. Separate clock region comparisons involve resources located in the X0Y1 clock region (e.g., MMCM, PLL, input buffers (IBUF)) and between the contiguous clock regions (e.g., global buffers (BUFG)). The input pins used for these tests are from a separate X0Y1 clock region and matching I/O bank:

- Clock-capable E15 pin (named JB1 in Arty A7 board),
- Non-clock-capable J17 pin (named JB7 in Arty A7 board).

Table 10 presents the schematic diagrams and the measurements results at ambient temperature of multiple connection configurations involving a common input pin and a separate clock region. Tables S8 and S9 present the detailed results—both absolute and percentage numbers.

Table 10. Measurements results and diagrams for configurations with a separate input pin (in different I/O bank) and a separate clock region.

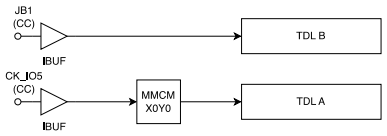
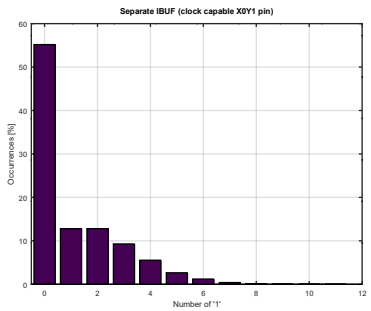
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.5.1	Separate IBUF (clock-capable pin in X0Y1 clock region)	 • Maximum number of the detected differences: 11. • The most common number of the detected differences is 0 (55.176% occurrences).	

Table 10. *Cont.*

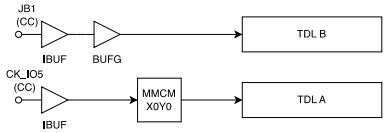
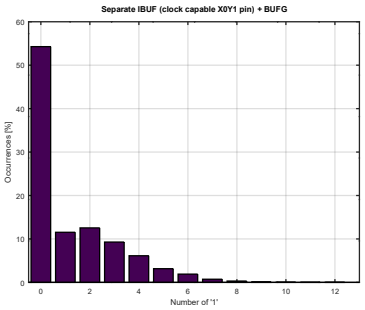
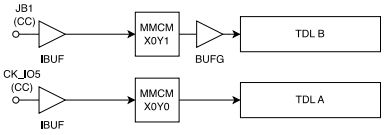
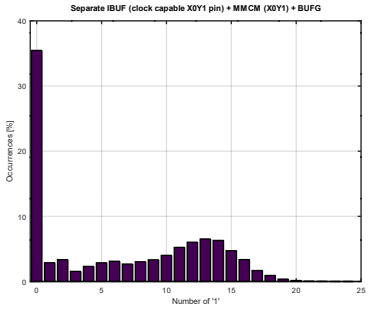
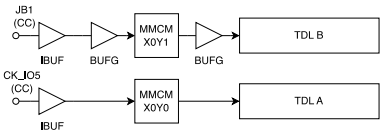
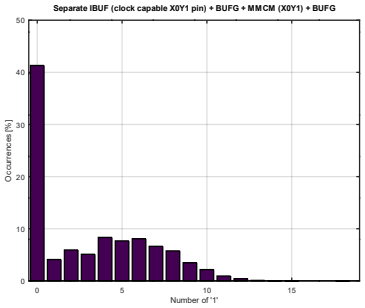
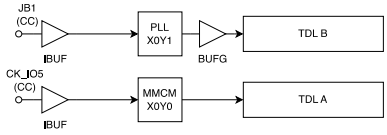
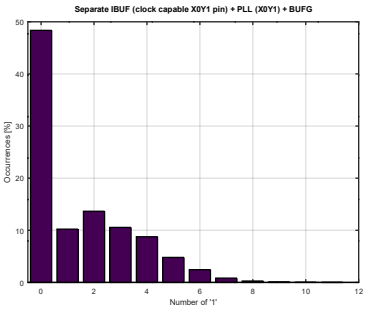
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.5.2	Separate IBUF (clock-capable pin in X0Y1 clock region) + BUFG	 • Maximum number of the detected differences: 12. • The most common number of the detected differences is 0 (54.273% occurrences).	
5.5.3	Separate IBUF (clock-capable pin in X0Y1 clock region) + X0Y1 clock region MMCM + BUFG	 • Maximum number of the detected differences: 24. • The most common number of the detected differences is 0 (35.465% occurrences).	
5.5.4	Separate IBUF (clock-capable pin in X0Y1 clock region) + BUFG + X0Y1 clock region MMCM + BUFG	 • Maximum number of the detected differences: 18. • The most common number of the detected differences is 0 (41.317% occurrences).	
5.5.5	Separate IBUF (clock-capable pin in X0Y1 clock region) + X0Y1 region PLL + BUFG	 • Maximum number of the detected differences: 11. • The most common number of the detected differences is 0 (48.355% occurrences).	

Table 10. *Cont.*

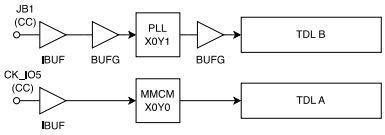
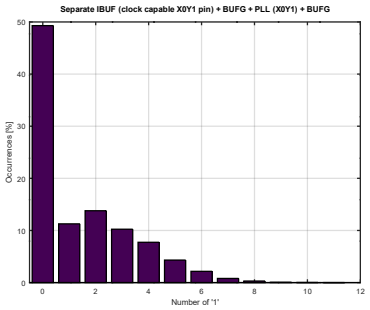
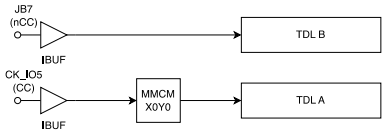
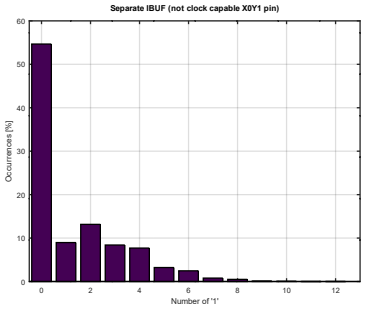
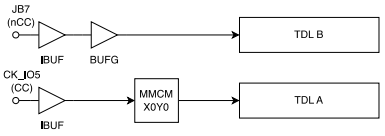
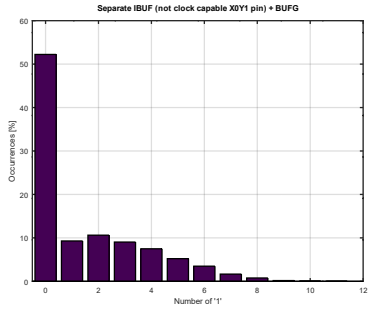
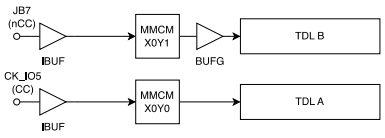
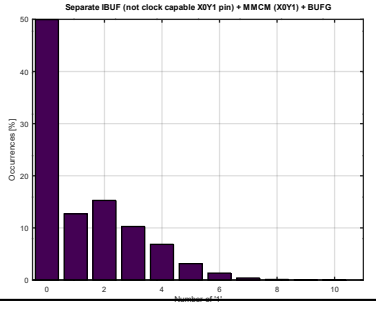
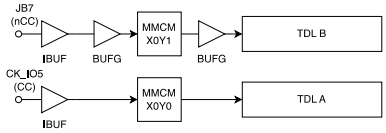
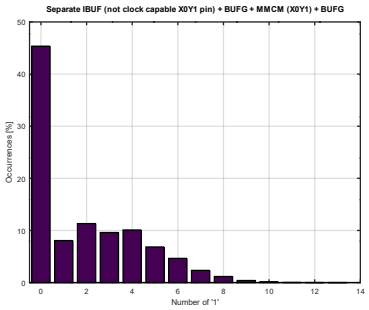
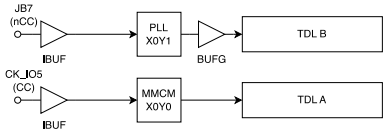
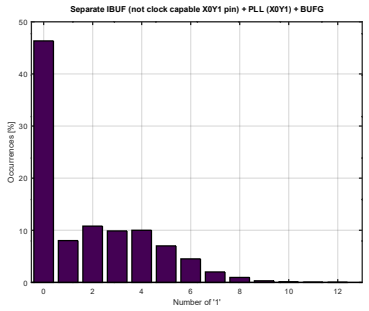
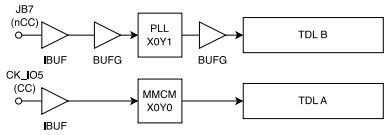
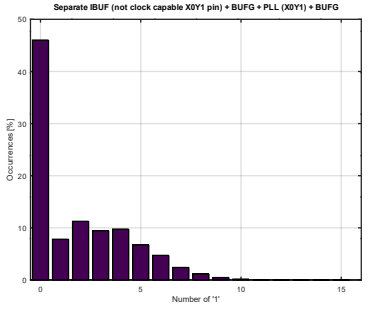
Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.5.6	Separate IBUF (clock-capable pin in X0Y1 clock region) + BUFG + X0Y1 clock region PLL + BUFG	 • Maximum number of the detected differences: 11. • The most common number of the detected differences is 0 (49.297% occurrences).	
5.5.7	Separate IBUF (non-clock-capable pin in X0Y1 clock region)	 • Maximum number of the detected differences: 12. • The most common number of the detected differences is 0 (54.666% occurrences).	
5.5.8	Separate IBUF (non-clock-capable pin in X0Y1 clock region) + BUFG	 • Maximum number of the detected differences: 11. • The most common number of the detected differences is 0 (52.228% occurrences).	
5.5.9	Separate IBUF (non-clock-capable pin in X0Y1 clock region) + X0Y1 clock region MMCM + BUFG	 • Maximum number of the detected differences: 10. • The most common number of the detected differences is 0 (49.954% occurrences).	

Table 10. *Cont.*

Config. Number	Config. Name	Schematic Diagram and Short Summary	Measurement Results at Ambient Temperature
5.5.10	Separate IBUF (non-clock-capable pin in X0Y1 clock region) + BUFG + X0Y1 clock region MMCM + BUFG	 • Maximum number of the detected differences: 13. • The most common number of the detected differences is 0 (45.351% occurrences).	
5.5.11	Separate IBUF (non-clock-capable pin in X0Y1 clock region) + X0Y1 clock region PLL + BUFG	 • Maximum number of the detected differences: 12. • The most common number of the detected differences is 0 (46.335% occurrences).	
5.5.12	Separate IBUF (non-clock-capable pin in X0Y1 clock region) + BUFG + X0Y1 clock region PLL + BUFG	 • Maximum number of the detected differences: 15. • The most common number of the detected differences is 0 (46.019% occurrences).	

5.6. Comparison of the Results

Table 11 presents the calculated values of relative entropy for each obtained measurement in ascending order. The $D_{KL}(P||Q)$ calculations were performed for two reference probability distributions Q:

- Ideal theoretical PDF of 100% zero differences detected;
- Empirical PDF of auto compared latch+flip-flop configuration, stated in Section 4.1.

It is worth noting that the calculated relative entropy for the reference measurements compared to the ideal theoretical distribution is the lowest of all obtained results. Also, the change in relative entropy at different temperatures is negligible. In comparison, the initial design (utilizing two consecutive flip-flops—presented on Figure 7) noticeably differs in relative entropy comparisons. The initial design deviates from the ideal theoretical PDF notably more than the design utilizing the latch+flip-flop approach.

Table 11. Calculated relative entropies for obtained measurements, with theoretical (ideal) and empirical reference.

Section/ Config. Number	Result Name	Relative Entropy (Ideal Ref.)	Relative Entropy (Empirical Ref.)
4.1	IBUF + MMCM auto compare—latch+flip-flop—ambient temp.	5.15235	0
4.2	IBUF + MMCM auto compare—latch+flip-flop—freeze -> ambient	5.22654	0.000155105
4.2	IBUF + MMCM auto compare—latch+flip-flop—freeze	5.4275	0.00167469
5.5.1	Sep. IBUF (CC X0Y1 pin)	5.40074	0.602199
4.1	IBUF + MMCM auto compare—2xflip-flop—ambient temp.	6.62013	0.732354
5.5.9	Sep. IBUF (nCC X0Y1 pin) + MMCM (X0Y1) + BUFG	6.13525	0.7401
5.5.2	Sep. IBUF (CC X0Y1 pin) + BUFG	5.45964	0.818643
5.5.7	Sep. IBUF (nCC X0Y1 pin)	5.37273	0.989554
5.5.6	Sep. IBUF (CC X0Y1 pin) + BUFG + PLL (X0Y1) + BUFG	6.14203	1.07626
5.5.5	Sep. IBUF (CC X0Y1 pin) + PLL (X0Y1) + BUFG	6.2609	1.22945
5.4.2	Sep. IBUF (CC X0Y0 pin) + BUFG + PLL (X0Y1) + BUFG	6.28831	1.37145
5.3.10	Sep. IBUF (nCC X0Y0 pin) + BUFG + PLL	6.27178	1.42141
5.5.8	Sep. IBUF (nCC X0Y1 pin) + BUFG	5.6276	1.47346
5.3.4	Sep. IBUF (CC X0Y0 pin) + BUFG + PLL	6.27908	1.50762
5.3.7	Sep. IBUF (nCC X0Y0 pin)	5.67175	1.98895
5.5.11	Sep. IBUF (nCC X0Y1 pin) + PLL (X0Y1) + BUFG	6.41065	2.04863
5.1.1	Com. IBUF	5.66629	2.05207
5.5.12	Sep. IBUF (nCC X0Y1 pin) + BUFG + PLL (X0Y1) + BUFG	6.42639	2.10493
5.5.10	Sep. IBUF (nCC X0Y1 pin) + BUFG + MMCM (X0Y1) + BUFG	6.53075	2.11106
5.4.3	Sep. IBUF (nCC X0Y0 pin) + BUFG + MMCM (X0Y1) + BUFG	6.63287	2.28577
5.1.6	Com. IBUF + PLL + BUFG	6.56871	2.40495
5.3.6	Sep. IBUF (CC X0Y0 pin) + BUFG + PLL + BUFG	6.58761	2.94546
5.3.1	Sep. IBUF (CC X0Y0 pin)	5.56103	2.98708
5.3.3	Sep. IBUF (CC X0Y0 pin) + PLL	6.66421	3.00739
5.3.11	Sep. IBUF (nCC X0Y0 pin) + PLL + BUFG	6.8134	3.20675
5.3.8	Sep. IBUF (nCC X0Y0 pin) + BUFG	5.84805	3.30594
5.4.4	Sep. IBUF (nCC X0Y0 pin) + BUFG + PLL (X0Y1) + BUFG	6.63702	3.48722
5.4.1	Sep. IBUF (CC X0Y0 pin) + BUFG + MMCM (X0Y1) + BUFG	6.73066	3.52268
5.3.2	Sep. IBUF (CC X0Y0 pin) + BUFG	5.86949	3.79135
5.1.7	Com. IBUF + BUFG + PLL	6.7178	3.89694
5.5.4	Sep. IBUF (CC X0Y1 pin) + BUFG + MMCM (X0Y1) + BUFG	6.80247	4.36376
5.3.12	Sep. IBUF (nCC X0Y0 pin) + BUFG + PLL + BUFG	6.8181	4.65398
5.2.2	Com. IBUF + BUFG + MMCM (X0Y1) + BUFG	7.02862	5.37672
5.2.2	Com. IBUF + BUFG + PLL (X0Y1) + BUFG	6.8868	5.59853
5.1.2	Com. IBUF + BUFG	6.34482	5.75471
5.1.4	IBUF + MMCM (FB BUFG)—OUTPUT1 + BUFG	7.24451	5.79941
5.1.3	IBUF + MMCM (FB BUFG)—OUTPUT1	7.26737	5.80405
5.1.8	Com. IBUF + BUFG + PLL + BUFG	7.12567	5.88812
5.3.9	Sep. IBUF (nCC X0Y0 pin) + PLL	7.12688	6.1222
5.3.5	Sep. IBUF (CC X0Y0 pin) + PLL + BUFG	7.20829	6.12283
5.5.3	Sep. IBUF (CC X0Y1 pin) + MMCM (X0Y1) + BUFG	7.15239	6.14977
5.1.5	Com. IBUF + PLL	7.17464	6.20072

From the results in Table 11 we can deduce that almost all results utilizing an input clock pin located in the X0Y1 clock region have a relatively low Kullback–Leibler divergence, regardless of the pin's clock capability. These results suggests that the signal routing and congestion of the neighboring resources has significant influence on the signal jitter. Even if these resources are not connected with the analyzed signal, their operation can greatly impact the jitter performance.

6. Conclusions

As expected, the worst results were obtained when any jitter filtering block (MMCM or PLL) was omitted. Particularly configuration 5.1.2 (Common IBUF + BUFG), configuration 5.3.1 (separate IBUF (clock-capable pin in the same clock region)), configuration 5.3.2 (Separate IBUF (clock-capable pin in the same clock region) + BUFG), configuration 5.3.7 (Separate IBUF (non-clock-capable pin in the same clock region)) and configuration 5.3.8 (Separate IBUF (non-clock-capable pin in the same clock region) + BUFG) present the widest spread of the number of the detected differences—over 25 differences were detected at least once. Both clock-capable and non-clock-capable input pins result in relatively high

jitter levels. However, regardless of the clock-capability of the input pin, the addition of a MMCM or PLL block significantly reduces the jitter level—which confirms the theoretical assumptions. Notably, the absolute worst results were obtained for separate clock-capable pin configurations rather than for non-clock-capable pin configurations. This suggests that for configurations with no MMCM or PLL blocks the clock signal routing is crucial for jitter level.

In every tested configuration omitting the usage of jitter filtering modules (MMCM or PLL), the addition of a global buffer clearly worsened the obtained results. Specifically, this can be observed by comparing the results:

- Common IBUF (configuration 5.1.1, relative entropy: 5.66629) vs. Common IBUF + BUFG (configuration 5.1.2, relative entropy: 5.75471);
- Separate clock-capable pin IBUF in X0Y0 region (configuration 5.3.1, relative entropy: 2.98708) vs. separate clock-capable pin IBUF in X0Y0 region + BUFG (configuration 5.3.2, relative entropy: 3.79135);
- Separate non-clock-capable pin IBUF in X0Y0 region (configuration 5.3.7, relative entropy: 1.98895) vs. separate non-clock-capable pin IBUF in X0Y0 region + BUFG (configuration 5.3.8, relative entropy: 3.30594);
- Separate clock-capable pin IBUF in X0Y1 region (configuration 5.5.1, relative entropy: 0.602199) vs. separate clock-capable pin IBUF in X0Y1 region + BUFG (configuration 5.5.2, relative entropy: 0.818643);
- Separate non-clock-capable pin IBUF in X0Y1 region (configuration 5.5.7, relative entropy: 0.989554) vs. separate non-clock-capable pin IBUF in X0Y1 region + BUFG (configuration 5.5.8, relative entropy: 1.47346).

In these cases, the additional global buffers effectively extended the traces required to route the design. As a result, routing the signal path closer and in longer segments to other clock signal paths (e.g., a system clock signal) with no jitter filtering modules causes interference from the aggressor signal. The results suggest that keeping the internal routing short and avoiding the usage of global buffers (BUFG) when these are not necessary, is beneficial in terms of jitter level. This conclusion coincides with the general intuitive understanding of FPGA design.

Surprisingly, the best results (the most similar to the reference—Figure 9) were obtained for a separate input pin in a different I/O bank and a separate clock region, regardless of the input pin type—configuration 5.5.1 (separate IBUF (clock-capable pin in X0Y1 clock region)), configuration 5.5.2 (separate IBUF (clock-capable pin in X0Y1 clock region) + BUFG), configuration 5.5.5 (separate IBUF (clock-capable pin in X0Y1 clock region) + X0Y1 region PLL + BUFG), configuration 5.5.6 (separate IBUF (clock-capable pin in X0Y1 clock region) + BUFG + X0Y1 clock region PLL + BUFG), configuration 5.5.7 (separate IBUF (non-clock-capable pin in X0Y1 clock region)), configuration 5.5.8 (separate IBUF (non-clock-capable pin in X0Y1 clock region) + BUFG), configuration 5.5.9 (separate IBUF (non-clock-capable pin in X0Y1 clock region) + X0Y1 clock region MMCM + BUFG), configuration 5.5.10 (separate IBUF (non-clock-capable pin in X0Y1 clock region) + BUFG + X0Y1 clock region MMCM + BUFG) and 5.5.11 (separate IBUF (non-clock-capable pin in X0Y1 clock region) + X0Y1 clock region PLL + BUFG). Particularly, the configurations omitting MMCM and PLL blocks. These results show that even non-clock-capable input pins can be successfully used as clock input with low jitter—even without jitter filtering. The most probable cause of these results is the usage of a very weakly utilized X0Y1 clock region. Hardly any resource was used in this part of the FPGA chip; therefore, the input signal was not interfered with by other signals. Considering that the usage of additional global buffers can slightly deteriorate the results, reaffirms this conclusion.

The conclusion that the jitter level is related to the resource utilization of a clock region with different and asynchronous clock signals is further justified by comparing the results of similar configurations, that use resources placed in different clock regions. Specifically, this can be observed by comparing the results:

- Separate clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y1) + BUFG (configuration 5.4.2, relative entropy: 1.37145) vs. separate clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) + BUFG (configuration 5.3.6, relative entropy: 2.94546);
- Separate non-clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y1) + BUFG (configuration 5.4.4, relative entropy: 3.48722) vs. separate non-clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) + BUFG (configuration: 5.3.12, relative entropy: 4.65398).

In both cases, the only difference between the compared configurations is the PLL block placement. Regardless of the clock capability of the input pin, the PLL block placement in a less utilized clock region resulted in a lower jitter level.

The measurements comparison of configurations with and without a global buffer between the input buffer and the jitter filtering block (MMCM or PLL) gives non-uniform results. In five out of seven cases, the additional BUFG lowered the jitter level—often significantly. In the remaining two cases, the jitter level increased in the configuration with an additional buffer—in one of these cases the difference was relatively small. Specifically, this can be observed by comparing the results:

- Separate non-clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) (configuration 5.3.10, relative entropy: 1.42141) vs. separate non-clock-capable pin IBUF in X0Y0 region + PLL (X0Y0) + BUFG (configuration 5.3.9, relative entropy: 6.1222);
- Separate clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) (configuration 5.3.4, relative entropy: 1.50762) vs. separate clock-capable pin IBUF in X0Y0 region + PLL (X0Y0) + BUFG (configuration 5.3.3, relative entropy: 3.00739);
- Common IBUF (configuration 5.1.7, relative entropy: 3.89694) vs. common IBUF + BUFG (configuration 5.1.5, relative entropy: 6.20072);
- Separate clock-capable pin IBUF in X0Y1 region + BUFG + MMCM (X0Y1) + BUFG (configuration 5.5.4, relative entropy: 4.36376) vs. separate clock-capable pin IBUF in X0Y1 region + MMCM (X0Y1) + BUFG (configuration 5.5.3, relative entropy: 6.14977);
- Separate non-clock-capable pin IBUF in X0Y1 region + MMCM (X0Y1) + BUFG (configuration 5.5.9, relative entropy: 0.7401) vs. separate non-clock-capable pin IBUF in X0Y1 region + BUFG + MMCM (X0Y1) + BUFG (configuration 5.5.10, relative entropy: 2.11106);
- Separate clock-capable pin IBUF in X0Y1 region + BUFG + PLL (X0Y1) + BUFG (configuration 5.5.6, relative entropy: 1.07626) vs. separate clock-capable pin IBUF in X0Y1 region + PLL (X0Y1) + BUFG (configuration 5.5.5, relative entropy: 1.22945);
- Separate non-clock-capable pin IBUF in X0Y1 region + PLL (X0Y1) + BUFG (configuration 5.5.11, relative entropy: 2.04863) vs. separate non-clock-capable pin IBUF in X0Y1 region + BUFG + PLL (X0Y1) + BUFG (configuration 5.5.12, relative entropy: 2.10493).

The measurements comparison of configurations with and without a global buffer placed after the jitter filtering block (MMCM or PLL) gives non-uniform results as well, though more ambiguous than in the previous part. In four out of seven cases, the additional BUFG lowered the jitter level. In the remaining three cases, the jitter level increased in the configuration with an additional buffer. Specifically, this can be observed by comparing the results:

- Separate clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) (configuration 5.3.4, relative entropy: 1.50762) vs. separate clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) + BUFG (configuration 5.3.6, relative entropy: 2.94546);
- Separate clock-capable pin IBUF in X0Y0 region + PLL (X0Y0) (configuration 5.3.3, relative entropy: 3.00739) vs. separate clock-capable pin IBUF in X0Y0 region + PLL (X0Y0) + BUFG (configuration 5.3.5, relative entropy: 6.12283);
- Separate non-clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) (configuration 5.3.10, relative entropy: 1.42141) vs. separate non-clock-capable pin IBUF in X0Y0 region + BUFG + PLL (X0Y0) + BUFG (configuration 5.3.12, relative entropy: 4.65398);

- Separate non-clock-capable pin IBUF in X0Y0 region + PLL (X0Y0) + BUFG (configuration 5.3.11, relative entropy: 3.20675) vs. separate non-clock-capable pin IBUF in X0Y0 region + PLL (X0Y0) (configuration 5.3.9, relative entropy: 6.1222);
- Common IBUF + BUFG + PLL (X0Y0) (configuration 5.1.7, relative entropy: 3.89694) vs. Common IBUF + BUFG + PLL (X0Y0) + BUFG (configuration 5.1.8, relative entropy: 5.88812);
- Common IBUF + PLL (X0Y0) + BUFG (configuration 5.1.6, relative entropy: 2.40495) vs. Common IBUF + PLL (X0Y0) (configuration 5.1.5, relative entropy: 6.20072);
- Separate MMCM output + BUFG (configuration 5.1.4, relative entropy: 5.79941) vs. Separate MMCM output (configuration 5.1.3, relative entropy: 5.80405).

It can be concluded that with a very careful FPGA resource allocation and routing, any input pin (both clock capable and standard) can be successfully used as a clock signal input, even without a MMCM or PLL block. However, this approach is generally not recommended, as the carelessness in resource placement can lead to a very high jitter level when jitter filtering blocks (MMCM or PLL) are omitted, and the results can vary significantly in different chips. This can potentially be a topic for further research.

The presented relative jitter measurement design and methodology can be applied to different FPGA families, enabling the comparison of different clocking resources and paths.

Supplementary Materials: The following supporting information can be downloaded at https://www.mdpi.com/article/10.3390/electronics12204297/s1, Table S1: Delays of system clock to first flip-flops/latches in TDLs (reported by Xilinx Vivado); Table S2: Delays of system clock to second flip-flops in TDLs (reported by Xilinx Vivado); Table S3: Distribution of the number of detected differences in different configurations with common input pin and a single clock region, at ambient temperature; Table S4: Distribution of the number of detected differences in different configurations with common input pin and a separate clock region, at ambient temperatures; Table S5: Distribution of the number of detected differences in different configurations with separate clock-capable input pin in the same clock region and a single common clock region, at ambient temperatures; Table S6: Distribution of the number of detected differences in different configurations with separate non clock-capable input pin in the same clock region and a single common clock region, at ambient temperatures; Table S7: Distribution of the number of detected differences in different configurations with separate input pin in the same clock region and a separate clock region, at ambient temperatures; Table S8: Distribution of the number of detected differences in different configurations with separate clock-capable input pin in separate clock region and a separate clock region, at ambient temperatures; Table S9: Distribution of the number of detected differences in different configurations with separate non clock-capable input pin in separate clock region and a separate clock region, at ambient temperatures.

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