

Table S1. Delays of system clock to first flip-flops/latches in TDLs (reported by Xilinx Vivado)

TDL A tap index	FAST MAX corner	FAST MIN corner	SLOW MAX corner	SLOW MIN corner	TDL B tap index	FAST MAX corner	FASTMI N corner	SLOW MAX corner	SLOW MIN corner
0	869	593	1682	1539	0	869	593	1682	1539
1	869	593	1682	1539	1	869	593	1682	1539
2	869	593	1682	1539	2	869	593	1682	1539
3	869	593	1682	1539	3	869	593	1682	1539
4	868	592	1681	1538	4	868	592	1681	1538
5	868	592	1681	1538	5	868	592	1681	1538
6	868	592	1681	1538	6	868	592	1681	1538
7	868	592	1681	1538	7	868	592	1681	1538
8	868	592	1681	1538	8	868	592	1681	1538
9	868	592	1681	1538	9	868	592	1681	1538
10	868	592	1681	1538	10	868	592	1681	1538
11	868	592	1681	1538	11	868	592	1681	1538
12	867	591	1680	1537	12	867	591	1680	1537
13	867	591	1680	1537	13	867	591	1680	1537
14	867	591	1680	1537	14	867	591	1680	1537
15	867	591	1680	1537	15	867	591	1680	1537
16	867	591	1679	1536	16	867	591	1679	1536
17	867	591	1679	1536	17	867	591	1679	1536
18	866	590	1679	1536	18	866	590	1679	1536
19	866	590	1679	1536	19	866	590	1679	1536
20	866	590	1678	1535	20	866	590	1678	1535
21	866	590	1678	1535	21	866	590	1678	1535
22	864	589	1677	1534	22	864	589	1677	1534
23	864	589	1677	1534	23	864	589	1677	1534
24	863	588	1676	1533	24	863	588	1676	1533
25	863	588	1676	1533	25	863	588	1676	1533
26	863	588	1676	1533	26	863	588	1676	1533
27	863	588	1676	1533	27	863	588	1676	1533
28	862	588	1674	1532	28	862	588	1674	1532
29	862	588	1674	1532	29	862	588	1674	1532
30	861	587	1673	1531	30	861	587	1673	1531
31	861	587	1673	1531	31	861	587	1673	1531
32	860	586	1672	1530	32	860	586	1672	1530
33	860	586	1672	1530	33	860	586	1672	1530
34	859	585	1670	1528	34	859	585	1670	1528
35	859	585	1670	1528	35	859	585	1670	1528
36	858	584	1669	1527	36	858	584	1669	1527
37	858	584	1669	1527	37	858	584	1669	1527
38	857	583	1668	1527	38	857	583	1668	1527
39	857	583	1668	1527	39	857	583	1668	1527
40	856	582	1667	1526	40	856	582	1667	1526
41	856	582	1667	1526	41	856	582	1667	1526

42	855	582	1664	1524	42	855	582	1664	1524
43	855	582	1664	1524	43	855	582	1664	1524
44	853	580	1663	1523	44	853	580	1663	1523
45	853	580	1663	1523	45	853	580	1663	1523
46	852	579	1661	1521	46	852	579	1661	1521
47	852	579	1661	1521	47	852	579	1661	1521
48	852	579	1661	1521	48	852	579	1661	1521
49	852	579	1661	1521	49	852	579	1661	1521
50	853	580	1663	1523	50	853	580	1663	1523
51	853	580	1663	1523	51	853	580	1663	1523
52	855	582	1664	1524	52	855	582	1664	1524
53	855	582	1664	1524	53	855	582	1664	1524
54	856	582	1667	1526	54	856	582	1667	1526
55	856	582	1667	1526	55	856	582	1667	1526
56	857	583	1668	1527	56	857	583	1668	1527
57	857	583	1668	1527	57	857	583	1668	1527
58	858	584	1669	1527	58	858	584	1669	1527
59	858	584	1669	1527	59	858	584	1669	1527
60	859	585	1670	1528	60	859	585	1670	1528
61	859	585	1670	1528	61	859	585	1670	1528
62	860	586	1672	1530	62	860	586	1672	1530
63	860	586	1672	1530	63	860	586	1672	1530
64	861	587	1673	1531	64	861	587	1673	1531
65	861	587	1673	1531	65	861	587	1673	1531
66	862	588	1674	1532	66	862	588	1674	1532
67	862	588	1674	1532	67	862	588	1674	1532
68	863	588	1676	1533	68	863	588	1676	1533
69	863	588	1676	1533	69	863	588	1676	1533
70	863	588	1676	1533	70	863	588	1676	1533
71	863	588	1676	1533	71	863	588	1676	1533
72	864	589	1677	1534	72	864	589	1677	1534
73	864	589	1677	1534	73	864	589	1677	1534
74	866	590	1678	1535	74	866	590	1678	1535
75	866	590	1678	1535	75	866	590	1678	1535
76	866	590	1679	1536	76	866	590	1679	1536
77	866	590	1679	1536	77	866	590	1679	1536
78	867	591	1679	1536	78	867	591	1679	1536
79	867	591	1679	1536	79	867	591	1679	1536
80	867	591	1680	1537	80	867	591	1680	1537
81	867	591	1680	1537	81	867	591	1680	1537
82	867	591	1680	1537	82	867	591	1680	1537
83	867	591	1680	1537	83	867	591	1680	1537
84	868	592	1681	1538	84	868	592	1681	1538
85	868	592	1681	1538	85	868	592	1681	1538
86	868	592	1681	1538	86	868	592	1681	1538
87	868	592	1681	1538	87	868	592	1681	1538

88	868	592	1681	1538	88	868	592	1681	1538
89	868	592	1681	1538	89	868	592	1681	1538
90	868	592	1681	1538	90	868	592	1681	1538
91	868	592	1681	1538	91	868	592	1681	1538
92	869	593	1682	1539	92	869	593	1682	1539
93	869	593	1682	1539	93	869	593	1682	1539
94	869	593	1682	1539	94	869	593	1682	1539
95	869	593	1682	1539	95	869	593	1682	1539
96	869	593	1682	1539	96	869	593	1682	1539
97	869	593	1682	1539	97	869	593	1682	1539
98	866	591	1670	1529	98	866	591	1670	1529
99	866	591	1670	1529	99	866	591	1670	1529
100	866	591	1670	1529	100	866	591	1670	1529
101	866	591	1670	1529	101	866	591	1670	1529
102	866	591	1670	1529	102	866	591	1670	1529
103	866	591	1670	1529	103	866	591	1670	1529
104	865	590	1669	1528	104	865	590	1669	1528
105	865	590	1669	1528	105	865	590	1669	1528
106	865	590	1669	1528	106	865	590	1669	1528
107	865	590	1669	1528	107	865	590	1669	1528
108	865	590	1669	1528	108	865	590	1669	1528
109	865	590	1669	1528	109	865	590	1669	1528
110	865	590	1669	1528	110	865	590	1669	1528
111	865	590	1669	1528	111	865	590	1669	1528
112	864	589	1668	1527	112	864	589	1668	1527
113	864	589	1668	1527	113	864	589	1668	1527
114	864	589	1668	1527	114	864	589	1668	1527
115	864	589	1668	1527	115	864	589	1668	1527
116	864	589	1667	1526	116	864	589	1667	1526
117	864	589	1667	1526	117	864	589	1667	1526
118	863	588	1667	1526	118	863	588	1667	1526
119	863	588	1667	1526	119	863	588	1667	1526
120	863	588	1666	1525	120	863	588	1666	1525
121	863	588	1666	1525	121	863	588	1666	1525
122	861	587	1665	1524	122	861	587	1665	1524
123	861	587	1665	1524	123	861	587	1665	1524
124	860	586	1664	1523	124	860	586	1664	1523
125	860	586	1664	1523	125	860	586	1664	1523
126	860	586	1664	1523	126	860	586	1664	1523
127	860	586	1664	1523	127	860	586	1664	1523
128	859	586	1662	1522	128	859	586	1662	1522
129	859	586	1662	1522	129	859	586	1662	1522
130	858	585	1661	1521	130	858	585	1661	1521
131	858	585	1661	1521	131	858	585	1661	1521
132	857	584	1660	1520	132	857	584	1660	1520
133	857	584	1660	1520	133	857	584	1660	1520

134	856	583	1658	1518	134	856	583	1658	1518
135	856	583	1658	1518	135	856	583	1658	1518
136	855	582	1657	1517	136	855	582	1657	1517
137	855	582	1657	1517	137	855	582	1657	1517
138	854	581	1656	1517	138	854	581	1656	1517
139	854	581	1656	1517	139	854	581	1656	1517
140	853	580	1655	1516	140	853	580	1655	1516
141	853	580	1655	1516	141	853	580	1655	1516
142	852	580	1652	1514	142	852	580	1652	1514
143	852	580	1652	1514	143	852	580	1652	1514
144	850	578	1651	1513	144	850	578	1651	1513
145	850	578	1651	1513	145	850	578	1651	1513
146	849	577	1649	1511	146	849	577	1649	1511
147	849	577	1649	1511	147	849	577	1649	1511
148	849	577	1649	1511	148	849	577	1649	1511
149	849	577	1649	1511	149	849	577	1649	1511
150	850	578	1651	1513	150	850	578	1651	1513
151	850	578	1651	1513	151	850	578	1651	1513
152	852	580	1652	1514	152	852	580	1652	1514
153	852	580	1652	1514	153	852	580	1652	1514
154	853	580	1655	1516	154	853	580	1655	1516
155	853	580	1655	1516	155	853	580	1655	1516
156	854	581	1656	1517	156	854	581	1656	1517
157	854	581	1656	1517	157	854	581	1656	1517
158	855	582	1657	1517	158	855	582	1657	1517
159	855	582	1657	1517	159	855	582	1657	1517
160	856	583	1658	1518	160	856	583	1658	1518
161	856	583	1658	1518	161	856	583	1658	1518
162	857	584	1660	1520	162	857	584	1660	1520
163	857	584	1660	1520	163	857	584	1660	1520
164	858	585	1661	1521	164	858	585	1661	1521
165	858	585	1661	1521	165	858	585	1661	1521
166	859	586	1662	1522	166	859	586	1662	1522
167	859	586	1662	1522	167	859	586	1662	1522
168	860	586	1664	1523	168	860	586	1664	1523
169	860	586	1664	1523	169	860	586	1664	1523
170	860	586	1664	1523	170	860	586	1664	1523
171	860	586	1664	1523	171	860	586	1664	1523
172	861	587	1665	1524	172	861	587	1665	1524
173	861	587	1665	1524	173	861	587	1665	1524
174	863	588	1666	1525	174	863	588	1666	1525
175	863	588	1666	1525	175	863	588	1666	1525
176	863	588	1667	1526	176	863	588	1667	1526
177	863	588	1667	1526	177	863	588	1667	1526
178	864	589	1667	1526	178	864	589	1667	1526
179	864	589	1667	1526	179	864	589	1667	1526

180	864	589	1668	1527	180	864	589	1668	1527
181	864	589	1668	1527	181	864	589	1668	1527
182	864	589	1668	1527	182	864	589	1668	1527
183	864	589	1668	1527	183	864	589	1668	1527
184	865	590	1669	1528	184	865	590	1669	1528
185	865	590	1669	1528	185	865	590	1669	1528
186	865	590	1669	1528	186	865	590	1669	1528
187	865	590	1669	1528	187	865	590	1669	1528
188	865	590	1669	1528	188	865	590	1669	1528
189	865	590	1669	1528	189	865	590	1669	1528
190	865	590	1669	1528	190	865	590	1669	1528
191	865	590	1669	1528	191	865	590	1669	1528
192	866	591	1670	1529	192	866	591	1670	1529
193	866	591	1670	1529	193	866	591	1670	1529
194	866	591	1670	1529	194	866	591	1670	1529
195	866	591	1670	1529	195	866	591	1670	1529
196	866	591	1670	1529	196	866	591	1670	1529
197	866	591	1670	1529	197	866	591	1670	1529
198	953	673	1853	1703	198	953	673	1853	1703
199	953	673	1853	1703	199	953	673	1853	1703
200	953	673	1853	1703	200	953	673	1853	1703
201	953	673	1853	1703	201	953	673	1853	1703
202	953	673	1853	1703	202	953	673	1853	1703
203	953	673	1853	1703	203	953	673	1853	1703
204	952	672	1852	1702	204	952	672	1852	1702
205	952	672	1852	1702	205	952	672	1852	1702
206	952	672	1852	1702	206	952	672	1852	1702
207	952	672	1852	1702	207	952	672	1852	1702
208	952	672	1852	1702	208	952	672	1852	1702
209	952	672	1852	1702	209	952	672	1852	1702
210	952	672	1852	1702	210	952	672	1852	1702
211	952	672	1852	1702	211	952	672	1852	1702
212	951	671	1851	1701	212	951	671	1851	1701
213	951	671	1851	1701	213	951	671	1851	1701
214	951	671	1851	1701	214	951	671	1851	1701
215	951	671	1851	1701	215	951	671	1851	1701
216	951	671	1850	1700	216	951	671	1850	1700
217	951	671	1850	1700	217	951	671	1850	1700
218	950	670	1850	1700	218	950	670	1850	1700
219	950	670	1850	1700	219	950	670	1850	1700
220	950	670	1849	1699	220	950	670	1849	1699
221	950	670	1849	1699	221	950	670	1849	1699
222	948	669	1848	1698	222	948	669	1848	1698
223	948	669	1848	1698	223	948	669	1848	1698
224	947	668	1847	1697	224	947	668	1847	1697
225	947	668	1847	1697	225	947	668	1847	1697

226	947	668	1847	1697	226	947	668	1847	1697
227	947	668	1847	1697	227	947	668	1847	1697
228	946	668	1845	1696	228	946	668	1845	1696
229	946	668	1845	1696	229	946	668	1845	1696
230	945	667	1844	1695	230	945	667	1844	1695
231	945	667	1844	1695	231	945	667	1844	1695
232	944	666	1843	1694	232	944	666	1843	1694
233	944	666	1843	1694	233	944	666	1843	1694
234	943	665	1841	1692	234	943	665	1841	1692
235	943	665	1841	1692	235	943	665	1841	1692
236	942	664	1840	1691	236	942	664	1840	1691
237	942	664	1840	1691	237	942	664	1840	1691
238	941	663	1839	1691	238	941	663	1839	1691
239	941	663	1839	1691	239	941	663	1839	1691
240	940	662	1838	1690	240	940	662	1838	1690
241	940	662	1838	1690	241	940	662	1838	1690
242	939	662	1835	1688	242	939	662	1835	1688
243	939	662	1835	1688	243	939	662	1835	1688
244	937	660	1834	1687	244	937	660	1834	1687
245	937	660	1834	1687	245	937	660	1834	1687
246	936	659	1832	1685	246	936	659	1832	1685
247	936	659	1832	1685	247	936	659	1832	1685
248	936	659	1832	1685	248	936	659	1832	1685
249	936	659	1832	1685	249	936	659	1832	1685
250	937	660	1834	1687	250	937	660	1834	1687
251	937	660	1834	1687	251	937	660	1834	1687
252	939	662	1835	1688	252	939	662	1835	1688
253	939	662	1835	1688	253	939	662	1835	1688
254	940	662	1838	1690	254	940	662	1838	1690
255	940	662	1838	1690	255	940	662	1838	1690

Table S2. Delays of system clock to second flip-flops in TDLs (reported by Xilinx Vivado)

TDL A tap index	FAST MAX corner	FAST MIN corner	SLOW MAX corner	SLOW MIN corner	TDL B tap index	FAST MAX corner	FAST MIN corner	SLOW MAX corner	SLOW MIN corner
0	869	593	1682	1539	0	890	610	1722	1572
1	869	593	1682	1539	1	890	610	1722	1572
2	869	593	1682	1539	2	890	610	1722	1572
3	869	593	1682	1539	3	890	610	1722	1572
4	868	592	1681	1538	4	889	609	1721	1571
5	868	592	1681	1538	5	889	609	1721	1571
6	868	592	1681	1538	6	889	609	1721	1571
7	868	592	1681	1538	7	889	609	1721	1571
8	868	592	1681	1538	8	889	609	1721	1571
9	868	592	1681	1538	9	889	609	1721	1571
10	868	592	1681	1538	10	889	609	1721	1571
11	868	592	1681	1538	11	889	609	1721	1571
12	867	591	1680	1537	12	888	608	1720	1570
13	867	591	1680	1537	13	888	608	1720	1570
14	867	591	1680	1537	14	888	608	1720	1570
15	867	591	1680	1537	15	888	608	1720	1570
16	867	591	1679	1536	16	888	608	1719	1569
17	867	591	1679	1536	17	888	608	1719	1569
18	866	590	1679	1536	18	887	607	1719	1569
19	866	590	1679	1536	19	887	607	1719	1569
20	866	590	1678	1535	20	887	607	1718	1568
21	866	590	1678	1535	21	887	607	1718	1568
22	864	589	1677	1534	22	885	606	1717	1567
23	864	589	1677	1534	23	885	606	1717	1567
24	863	588	1676	1533	24	884	605	1716	1566
25	863	588	1676	1533	25	884	605	1716	1566
26	863	588	1676	1533	26	884	605	1716	1566
27	863	588	1676	1533	27	884	605	1716	1566
28	862	588	1674	1532	28	883	605	1714	1565
29	862	588	1674	1532	29	883	605	1714	1565
30	861	587	1673	1531	30	882	604	1713	1564
31	861	587	1673	1531	31	882	604	1713	1564
32	860	586	1672	1530	32	881	603	1712	1563
33	860	586	1672	1530	33	881	603	1712	1563
34	859	585	1670	1528	34	880	602	1710	1561
35	859	585	1670	1528	35	880	602	1710	1561
36	858	584	1669	1527	36	879	601	1709	1560
37	858	584	1669	1527	37	879	601	1709	1560
38	857	583	1668	1527	38	878	600	1708	1560
39	857	583	1668	1527	39	878	600	1708	1560
40	856	582	1667	1526	40	877	599	1707	1559
41	856	582	1667	1526	41	877	599	1707	1559

42	855	582	1664	1524	42	876	599	1704	1557
43	855	582	1664	1524	43	876	599	1704	1557
44	853	580	1663	1523	44	874	597	1703	1556
45	853	580	1663	1523	45	874	597	1703	1556
46	852	579	1661	1521	46	873	596	1701	1554
47	852	579	1661	1521	47	873	596	1701	1554
48	852	579	1661	1521	48	873	596	1701	1554
49	852	579	1661	1521	49	873	596	1701	1554
50	853	580	1663	1523	50	874	597	1703	1556
51	853	580	1663	1523	51	874	597	1703	1556
52	855	582	1664	1524	52	876	599	1704	1557
53	855	582	1664	1524	53	876	599	1704	1557
54	856	582	1667	1526	54	877	599	1707	1559
55	856	582	1667	1526	55	877	599	1707	1559
56	857	583	1668	1527	56	878	600	1708	1560
57	857	583	1668	1527	57	878	600	1708	1560
58	858	584	1669	1527	58	879	601	1709	1560
59	858	584	1669	1527	59	879	601	1709	1560
60	859	585	1670	1528	60	880	602	1710	1561
61	859	585	1670	1528	61	880	602	1710	1561
62	860	586	1672	1530	62	881	603	1712	1563
63	860	586	1672	1530	63	881	603	1712	1563
64	861	587	1673	1531	64	882	604	1713	1564
65	861	587	1673	1531	65	882	604	1713	1564
66	862	588	1674	1532	66	883	605	1714	1565
67	862	588	1674	1532	67	883	605	1714	1565
68	863	588	1676	1533	68	884	605	1716	1566
69	863	588	1676	1533	69	884	605	1716	1566
70	863	588	1676	1533	70	884	605	1716	1566
71	863	588	1676	1533	71	884	605	1716	1566
72	864	589	1677	1534	72	885	606	1717	1567
73	864	589	1677	1534	73	885	606	1717	1567
74	866	590	1678	1535	74	887	607	1718	1568
75	866	590	1678	1535	75	887	607	1718	1568
76	866	590	1679	1536	76	887	607	1719	1569
77	866	590	1679	1536	77	887	607	1719	1569
78	867	591	1679	1536	78	888	608	1719	1569
79	867	591	1679	1536	79	888	608	1719	1569
80	867	591	1680	1537	80	888	608	1720	1570
81	867	591	1680	1537	81	888	608	1720	1570
82	867	591	1680	1537	82	888	608	1720	1570
83	867	591	1680	1537	83	888	608	1720	1570
84	868	592	1681	1538	84	889	609	1721	1571
85	868	592	1681	1538	85	889	609	1721	1571
86	868	592	1681	1538	86	889	609	1721	1571
87	868	592	1681	1538	87	889	609	1721	1571

88	868	592	1681	1538	88	889	609	1721	1571
89	868	592	1681	1538	89	889	609	1721	1571
90	868	592	1681	1538	90	889	609	1721	1571
91	868	592	1681	1538	91	889	609	1721	1571
92	869	593	1682	1539	92	890	610	1722	1572
93	869	593	1682	1539	93	890	610	1722	1572
94	869	593	1682	1539	94	890	610	1722	1572
95	869	593	1682	1539	95	890	610	1722	1572
96	869	593	1682	1539	96	890	610	1722	1572
97	869	593	1682	1539	97	890	610	1722	1572
98	866	591	1670	1529	98	887	608	1710	1562
99	866	591	1670	1529	99	887	608	1710	1562
100	866	591	1670	1529	100	887	608	1710	1562
101	866	591	1670	1529	101	887	608	1710	1562
102	866	591	1670	1529	102	887	608	1710	1562
103	866	591	1670	1529	103	887	608	1710	1562
104	865	590	1669	1528	104	886	607	1709	1561
105	865	590	1669	1528	105	886	607	1709	1561
106	865	590	1669	1528	106	886	607	1709	1561
107	865	590	1669	1528	107	886	607	1709	1561
108	865	590	1669	1528	108	886	607	1709	1561
109	865	590	1669	1528	109	886	607	1709	1561
110	865	590	1669	1528	110	886	607	1709	1561
111	865	590	1669	1528	111	886	607	1709	1561
112	864	589	1668	1527	112	885	606	1708	1560
113	864	589	1668	1527	113	885	606	1708	1560
114	864	589	1668	1527	114	885	606	1708	1560
115	864	589	1668	1527	115	885	606	1708	1560
116	864	589	1667	1526	116	885	606	1707	1559
117	864	589	1667	1526	117	885	606	1707	1559
118	863	588	1667	1526	118	884	605	1707	1559
119	863	588	1667	1526	119	884	605	1707	1559
120	863	588	1666	1525	120	884	605	1706	1558
121	863	588	1666	1525	121	884	605	1706	1558
122	861	587	1665	1524	122	882	604	1705	1557
123	861	587	1665	1524	123	882	604	1705	1557
124	860	586	1664	1523	124	881	603	1704	1556
125	860	586	1664	1523	125	881	603	1704	1556
126	860	586	1664	1523	126	881	603	1704	1556
127	860	586	1664	1523	127	881	603	1704	1556
128	859	586	1662	1522	128	880	603	1702	1555
129	859	586	1662	1522	129	880	603	1702	1555
130	858	585	1661	1521	130	879	602	1701	1554
131	858	585	1661	1521	131	879	602	1701	1554
132	857	584	1660	1520	132	878	601	1700	1553
133	857	584	1660	1520	133	878	601	1700	1553

134	856	583	1658	1518	134	877	600	1698	1551
135	856	583	1658	1518	135	877	600	1698	1551
136	855	582	1657	1517	136	876	599	1697	1550
137	855	582	1657	1517	137	876	599	1697	1550
138	854	581	1656	1517	138	875	598	1696	1550
139	854	581	1656	1517	139	875	598	1696	1550
140	853	580	1655	1516	140	874	597	1695	1549
141	853	580	1655	1516	141	874	597	1695	1549
142	852	580	1652	1514	142	873	597	1692	1547
143	852	580	1652	1514	143	873	597	1692	1547
144	850	578	1651	1513	144	871	595	1691	1546
145	850	578	1651	1513	145	871	595	1691	1546
146	849	577	1649	1511	146	870	594	1689	1544
147	849	577	1649	1511	147	870	594	1689	1544
148	849	577	1649	1511	148	870	594	1689	1544
149	849	577	1649	1511	149	870	594	1689	1544
150	850	578	1651	1513	150	871	595	1691	1546
151	850	578	1651	1513	151	871	595	1691	1546
152	852	580	1652	1514	152	873	597	1692	1547
153	852	580	1652	1514	153	873	597	1692	1547
154	853	580	1655	1516	154	874	597	1695	1549
155	853	580	1655	1516	155	874	597	1695	1549
156	854	581	1656	1517	156	875	598	1696	1550
157	854	581	1656	1517	157	875	598	1696	1550
158	855	582	1657	1517	158	876	599	1697	1550
159	855	582	1657	1517	159	876	599	1697	1550
160	856	583	1658	1518	160	877	600	1698	1551
161	856	583	1658	1518	161	877	600	1698	1551
162	857	584	1660	1520	162	878	601	1700	1553
163	857	584	1660	1520	163	878	601	1700	1553
164	858	585	1661	1521	164	879	602	1701	1554
165	858	585	1661	1521	165	879	602	1701	1554
166	859	586	1662	1522	166	880	603	1702	1555
167	859	586	1662	1522	167	880	603	1702	1555
168	860	586	1664	1523	168	881	603	1704	1556
169	860	586	1664	1523	169	881	603	1704	1556
170	860	586	1664	1523	170	881	603	1704	1556
171	860	586	1664	1523	171	881	603	1704	1556
172	861	587	1665	1524	172	882	604	1705	1557
173	861	587	1665	1524	173	882	604	1705	1557
174	863	588	1666	1525	174	884	605	1706	1558
175	863	588	1666	1525	175	884	605	1706	1558
176	863	588	1667	1526	176	884	605	1707	1559
177	863	588	1667	1526	177	884	605	1707	1559
178	864	589	1667	1526	178	885	606	1707	1559
179	864	589	1667	1526	179	885	606	1707	1559

180	864	589	1668	1527	180	885	606	1708	1560
181	864	589	1668	1527	181	885	606	1708	1560
182	864	589	1668	1527	182	885	606	1708	1560
183	864	589	1668	1527	183	885	606	1708	1560
184	865	590	1669	1528	184	886	607	1709	1561
185	865	590	1669	1528	185	886	607	1709	1561
186	865	590	1669	1528	186	886	607	1709	1561
187	865	590	1669	1528	187	886	607	1709	1561
188	865	590	1669	1528	188	886	607	1709	1561
189	865	590	1669	1528	189	886	607	1709	1561
190	865	590	1669	1528	190	886	607	1709	1561
191	865	590	1669	1528	191	886	607	1709	1561
192	866	591	1670	1529	192	887	608	1710	1562
193	866	591	1670	1529	193	887	608	1710	1562
194	866	591	1670	1529	194	887	608	1710	1562
195	866	591	1670	1529	195	887	608	1710	1562
196	866	591	1670	1529	196	887	608	1710	1562
197	866	591	1670	1529	197	887	608	1710	1562
198	953	673	1853	1703	198	974	690	1893	1736
199	953	673	1853	1703	199	974	690	1893	1736
200	953	673	1853	1703	200	974	690	1893	1736
201	953	673	1853	1703	201	974	690	1893	1736
202	953	673	1853	1703	202	974	690	1893	1736
203	953	673	1853	1703	203	974	690	1893	1736
204	952	672	1852	1702	204	973	689	1892	1735
205	952	672	1852	1702	205	973	689	1892	1735
206	952	672	1852	1702	206	973	689	1892	1735
207	952	672	1852	1702	207	973	689	1892	1735
208	952	672	1852	1702	208	973	689	1892	1735
209	952	672	1852	1702	209	973	689	1892	1735
210	952	672	1852	1702	210	973	689	1892	1735
211	952	672	1852	1702	211	973	689	1892	1735
212	951	671	1851	1701	212	972	688	1891	1734
213	951	671	1851	1701	213	972	688	1891	1734
214	951	671	1851	1701	214	972	688	1891	1734
215	951	671	1851	1701	215	972	688	1891	1734
216	951	671	1850	1700	216	972	688	1890	1733
217	951	671	1850	1700	217	972	688	1890	1733
218	950	670	1850	1700	218	971	687	1890	1733
219	950	670	1850	1700	219	971	687	1890	1733
220	950	670	1849	1699	220	971	687	1889	1732
221	950	670	1849	1699	221	971	687	1889	1732
222	948	669	1848	1698	222	969	686	1888	1731
223	948	669	1848	1698	223	969	686	1888	1731
224	947	668	1847	1697	224	968	685	1887	1730
225	947	668	1847	1697	225	968	685	1887	1730

226	947	668	1847	1697	226	968	685	1887	1730
227	947	668	1847	1697	227	968	685	1887	1730
228	946	668	1845	1696	228	967	685	1885	1729
229	946	668	1845	1696	229	967	685	1885	1729
230	945	667	1844	1695	230	966	684	1884	1728
231	945	667	1844	1695	231	966	684	1884	1728
232	944	666	1843	1694	232	965	683	1883	1727
233	944	666	1843	1694	233	965	683	1883	1727
234	943	665	1841	1692	234	964	682	1881	1725
235	943	665	1841	1692	235	964	682	1881	1725
236	942	664	1840	1691	236	963	681	1880	1724
237	942	664	1840	1691	237	963	681	1880	1724
238	941	663	1839	1691	238	962	680	1879	1724
239	941	663	1839	1691	239	962	680	1879	1724
240	940	662	1838	1690	240	961	679	1878	1723
241	940	662	1838	1690	241	961	679	1878	1723
242	939	662	1835	1688	242	960	679	1875	1721
243	939	662	1835	1688	243	960	679	1875	1721
244	937	660	1834	1687	244	958	677	1874	1720
245	937	660	1834	1687	245	958	677	1874	1720
246	936	659	1832	1685	246	957	676	1872	1718
247	936	659	1832	1685	247	957	676	1872	1718
248	936	659	1832	1685	248	957	676	1872	1718
249	936	659	1832	1685	249	957	676	1872	1718
250	937	660	1834	1687	250	958	677	1874	1720
251	937	660	1834	1687	251	958	677	1874	1720
252	939	662	1835	1688	252	960	679	1875	1721
253	939	662	1835	1688	253	960	679	1875	1721
254	940	662	1838	1690	254	961	679	1878	1723
255	940	662	1838	1690	255	961	679	1878	1723

Table S3. Distribution of the number of detected differences in different configurations with common input pin and a single clock region, at ambient temperatures.

Number of '1'	Common IBUF	Common IBUF + BUFG	Separate MMCM output	Separate MMCM output with BUFG	Common IBUF + PLL	Common IBUF + PLL + BUFG	Common IBUF + BUFG + PLL	Common IBUF + BUFG + PLL + BUFG
0	51829 (50.614%)	41462 (40.490%)	39920 (38.984%)	40057 (39.118%)	36521 (35.665%)	45990 (44.912%)	43587 (42.565%)	37767 (36.882%)
1	7818 (7.635%)	2439 (2.382%)	3216 (3.141%)	3136 (3.062%)	2900 (2.832%)	7016 (6.852%)	4648 (4.539%)	2928 (2.859%)
2	9468 (9.246%)	1930 (1.885%)	3358 (3.279%)	3305 (3.228%)	3166 (3.092%)	10828 (10.574%)	6497 (6.345%)	3346 (3.268%)
3	8450 (8.252%)	1351 (1.319%)	2609 (2.548%)	2598 (2.537%)	1589 (1.552%)	9982 (9.748%)	6879 (6.718%)	2771 (2.706%)
4	7326 (7.154%)	1528 (1.492%)	6389 (6.239%)	6418 (6.268%)	2568 (2.508%)	10338 (10.096%)	9429 (9.208%)	3810 (3.721%)
5	5236 (5.113%)	1096 (1.070%)	4417 (4.313%)	4434 (4.330%)	2884 (2.816%)	7812 (7.629%)	8617 (8.415%)	2806 (2.740%)
6	4273 (4.173%)	2216 (2.164%)	5605 (5.474%)	5427 (5.300%)	3284 (3.207%)	5401 (5.274%)	8457 (8.259%)	3996 (3.902%)
7	3007 (2.937%)	1293 (1.263%)	10096 (9.859%)	9745 (9.517%)	2768 (2.703%)	2926 (2.857%)	6087 (5.944%)	3889 (3.798%)
8	2310 (2.256%)	2645 (2.583%)	14218 (13.885%)	14128 (13.797%)	3137 (3.063%)	1462 (1.428%)	4567 (4.460%)	5688 (5.555%)
9	1283 (1.253%)	2258 (2.205%)	9367 (9.147%)	9699 (9.472%)	3729 (3.642%)	453 (0.442%)	2085 (2.036%)	6998 (6.834%)
10	777 (0.759%)	4102 (4.006%)	2938 (2.869%)	3132 (3.059%)	4394 (4.291%)	156 (0.152%)	1045 (1.021%)	7521 (7.345%)
11	368 (0.359%)	3729 (3.642%)	262 (0.256%)	313 (0.306%)	5924 (5.785%)	26 (0.025%)	348 (0.340%)	6977 (6.813%)
12	177 (0.173%)	4840 (4.727%)	5 (0.005%)	8 (0.008%)	6733 (6.575%)	10 (0.010%)	124 (0.121%)	6085 (5.942%)
13	50 (0.049%)	4408 (4.305%)	0 (0.0%)	0 (0.0%)	7240 (7.070%)	0 (0.0%)	26 (0.025%)	3725 (3.638%)
14	24 (0.023%)	5439 (5.312%)	0 (0.0%)	0 (0.0%)	6458 (6.307%)	0 (0.0%)	3 (0.003%)	2458 (2.400%)
15	3 (0.003%)	4354 (4.252%)	0 (0.0%)	0 (0.0%)	4429 (4.325%)	0 (0.0%)	1 (0.001%)	1033 (1.009%)
16	1 (0.001%)	4545 (4.438%)	0 (0.0%)	0 (0.0%)	2828 (2.762%)	0 (0.0%)	0 (0.0%)	448 (0.438%)
17	0 (0.0%)	3524 (3.441%)	0 (0.0%)	0 (0.0%)	1125 (1.099%)	0 (0.0%)	0 (0.0%)	101 (0.099%)
18	0 (0.0%)	3127 (3.054%)	0 (0.0%)	0 (0.0%)	515 (0.503%)	0 (0.0%)	0 (0.0%)	42 (0.041%)
19	0 (0.0%)	2221 (2.169%)	0 (0.0%)	0 (0.0%)	155 (0.151%)	0 (0.0%)	0 (0.0%)	10 (0.010%)
20	0 (0.0%)	1734 (1.693%)	0 (0.0%)	0 (0.0%)	46 (0.045%)	0 (0.0%)	0 (0.0%)	1 (0.001%)
21	0 (0.0%)	1067 (1.042%)	0 (0.0%)	0 (0.0%)	6 (0.006%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
22	0 (0.0%)	657 (0.642%)	0 (0.0%)	0 (0.0%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
23	0 (0.0%)	287 (0.280%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
24	0 (0.0%)	109	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

		(0.106%)						
25	0 (0.0%)	31 (0.030%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
26	0 (0.0%)	7 (0.007%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
27	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
28	0 (0.0%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

Table S4. Distribution of the number of detected differences in different configurations with common input pin and a separate clock region, at ambient temperatures.

Number of '1'	Common IBUF + BUFG + MMCM + BUFG	Common IBUF + BUFG + PLL + BUFG
0	39462 (38.537%)	40166 (39.225%)
1	3320 (3.242%)	3123 (3.05%)
2	4592 (4.484%)	3393 (3.313%)
3	3639 (3.554%)	2595 (2.534%)
4	5007 (4.890%)	4468 (4.363%)
5	4687 (4.577%)	4778 (4.666%)
6	7346 (7.174%)	5639 (5.507%)
7	7125 (6.958%)	6505 (6.353%)
8	7979 (7.792%)	7354 (7.182%)
9	6664 (6.508%)	7245 (7.075%)
10	5517 (5.388%)	6306 (6.158%)
11	3496 (3.414%)	4780 (4.668%)
12	2031 (1.983%)	3087 (3.015%)
13	935 (0.913%)	1727 (1.687%)
14	402 (0.393%)	796 (0.777%)
15	134 (0.131%)	305 (0.298%)
16	47 (0.046%)	96 (0.094%)
17	10 (0.010%)	27 (0.026%)
18	5 (0.005%)	10 (0.010%)
19	2 (0.002%)	0 (0.0%)

Table S5. Distribution of the number of detected differences in different configurations with separate clock-capable input pin in the same clock region and a single common clock region, at ambient temperatures.

Number of '1'	Separate IBUF	Separate IBUF + BUFG	Separate IBUF + PLL	Separate IBUF + BUFG + PLL	Separate IBUF + PLL + BUFG	Separate IBUF + BUFG + PLL + BUFG
0	49493 (48.333%)	47476 (46.363%)	44506 (43.463%)	48779 (47.636%)	35954 (35.111%)	45113 (44.056%)
1	3931 (3.839%)	2858 (2.791%)	6320 (6.172%)	9952 (9.719%)	2875 (2.808%)	6299 (6.151%)
2	8094 (7.904%)	6557 (6.403%)	9211 (8.995%)	13266 (12.955%)	3029 (2.958%)	8904 (8.695%)
3	5550 (5.420%)	4558 (4.451%)	8513 (8.313%)	10219 (9.979%)	2407 (2.351%)	8676 (8.473%)
4	7493 (7.317%)	7074 (6.908%)	10001 (9.767%)	8666 (8.463%)	2959 (2.89%)	10179 (9.940%)
5	4558 (4.451%)	4618 (4.510%)	7781 (7.599%)	5466 (5.338%)	2479 (2.421%)	7779 (7.597%)
6	5534 (5.404%)	6245 (6.099%)	6899 (6.737%)	3271 (3.194%)	3411 (3.331%)	6748 (6.590%)
7	3261 (3.185%)	4160 (4.062%)	4349 (4.247%)	1602 (1.564%)	2700 (2.637%)	4205 (4.106%)
8	3640 (3.555%)	5090 (4.971%)	2895 (2.827%)	787 (0.769%)	3295 (3.218%)	2658 (2.596%)
9	2023 (1.976%)	3074 (3.002%)	1205 (1.177%)	271 (0.265%)	4224 (4.125%)	1096 (1.070%)
10	1981 (1.935%)	3461 (3.380%)	485 (0.474%)	91 (0.089%)	5213 (5.091%)	500 (0.488%)
11	1014 (0.990%)	1911 (1.866%)	178 (0.174%)	25 (0.024%)	6136 (5.992%)	167 (0.163%)
12	983 (0.960%)	1796 (1.754%)	43 (0.042%)	4 (0.004%)	6938 (6.775%)	63 (0.062%)
13	462 (0.451%)	910 (0.889%)	9 (0.009%)	1 (0.001%)	6168 (6.023%)	7 (0.007%)
14	522 (0.510%)	761 (0.743%)	2 (0.002%)	0 (0.0%)	5572 (5.441%)	6 (0.006%)
15	330 (0.322%)	380 (0.371%)	2 (0.002%)	0 (0.0%)	3755 (3.667%)	0 (0.0%)
16	325 (0.317%)	322 (0.314%)	1 (0.001%)	0 (0.0%)	2669 (2.606%)	0 (0.0%)
17	266 (0.260%)	204 (0.199%)	0 (0.0%)	0 (0.0%)	1362 (1.330%)	0 (0.0%)
18	223 (0.218%)	197 (0.192%)	0 (0.0%)	0 (0.0%)	744 (0.727%)	0 (0.0%)
19	222 (0.217%)	127 (0.124%)	0 (0.0%)	0 (0.0%)	313 (0.306%)	0 (0.0%)
20	228 (0.223%)	113 (0.110%)	0 (0.0%)	0 (0.0%)	132 (0.129%)	0 (0.0%)
21	186 (0.182%)	74 (0.072%)	0 (0.0%)	0 (0.0%)	42 (0.041%)	0 (0.0%)
22	189 (0.185%)	72 (0.070%)	0 (0.0%)	0 (0.0%)	17 (0.017%)	0 (0.0%)
23	157 (0.153%)	58 (0.057%)	0 (0.0%)	0 (0.0%)	4 (0.004%)	0 (0.0%)
24	191 (0.187%)	43 (0.042%)	0 (0.0%)	0 (0.0%)	2 (0.002%)	0 (0.0%)

25	139 (0.136%)	41 (0.040%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
26	127 (0.124%)	37 (0.036%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
27	105 (0.103%)	36 (0.035%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
28	113 (0.110%)	27 (0.026%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
29	115 (0.112%)	19 (0.019%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
30	83 (0.081%)	17 (0.017%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
31	87 (0.085%)	14 (0.014%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
32	96 (0.094%)	11 (0.011%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
33	63 (0.062%)	3 (0.003%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
34	69 (0.067%)	6 (0.006%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
35	57 (0.056%)	5 (0.005%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
36	64 (0.062%)	4 (0.004%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
37	43 (0.042%)	4 (0.004%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
38	53 (0.052%)	7 (0.007%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
39	42 (0.041%)	4 (0.004%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
40	43 (0.042%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
41	24 (0.023%)	4 (0.004%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
42	33 (0.032%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
43	33 (0.032%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
44	31 (0.030%)	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
45	15 (0.015%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
46	14 (0.014%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
47	14 (0.014%)	6 (0.006%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
48	8 (0.008%)	5 (0.005%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
49	9 (0.009%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
50	7 (0.007%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
51	10 (0.010%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
52	6 (0.006%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
53	8 (0.008%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
54	6 (0.006%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

55	6 (0.006%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
56	3 (0.003%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
57	3 (0.003%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
58	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
59	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
60	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
61	4 (0.004%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
62	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
63	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
64	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
65	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
66	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
67–77	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
78	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
79–101	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
102	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
103–113	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
114	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
115–147	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
148	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

Table S6. Distribution of the number of detected differences in different configurations with separate non clock-capable input pin in the same clock region and a single common clock region, at ambient temperatures.

Number of '1'	Separate IBUF	Separate IBUF + BUFG	Separate IBUF + PLL	Separate IBUF + BUFG + PLL	Separate IBUF + PLL + BUFG	Separate IBUF + BUFG + PLL + BUFG
0	51585 (50.376%)	48524 (47.387%)	36886 (36.021%)	48910 (47.764%)	43404 (42.387%)	41831 (40.851%)
1	6002 (5.861%)	3768 (3.680%)	2925 (2.856%)	10267 (10.026%)	5802 (5.666%)	3799 (3.710%)
2	11252 (10.988%)	7808 (7.625%)	3127 (3.054%)	13740 (13.418%)	9356 (9.137%)	5152 (5.031%)
3	7894 (7.709%)	5530 (5.400%)	1760 (1.719%)	9959 (9.726%)	8568 (8.367%)	4984 (4.867%)
4	9031 (8.819%)	7786 (7.604%)	2747 (2.683%)	8689 (8.485%)	9865 (9.634%)	7707 (7.526%)
5	4678 (4.568%)	4917 (4.802%)	3146 (3.072%)	5011 (4.894%)	8476 (8.277%)	7119 (6.952%)
6	4642 (4.533%)	6517 (6.364%)	3528 (3.445%)	3168 (3.094%)	7226 (7.057%)	8193 (8.001%)
7	2086 (2.037%)	3793 (3.704%)	3168 (3.094%)	1493 (1.458%)	4752 (4.641%)	7269 (7.099%)
8	1941 (1.896%)	4620 (4.512%)	3754 (3.666%)	778 (0.760%)	2962 (2.893%)	6602 (6.447%)
9	839 (0.819%)	2491 (2.433%)	4564 (4.457%)	255 (0.249%)	1296 (1.266%)	4374 (4.271%)
10	796 (0.777%)	2515 (2.456%)	5433 (5.306%)	98 (0.096%)	496 (0.484%)	2844 (2.777%)
11	362 (0.354%)	1170 (1.143%)	6359 (6.210%)	20 (0.020%)	148 (0.145%)	1434 (1.400%)
12	378 (0.369%)	998 (0.975%)	6772 (6.613%)	11 (0.011%)	32 (0.031%)	690 (0.674%)
13	177 (0.173%)	493 (0.481%)	6292 (6.145%)	1 (0.001%)	12 (0.012%)	276 (0.270%)
14	187 (0.183%)	389 (0.380%)	5101 (4.981%)	0 (0.0%)	5 (0.005%)	102 (0.100%)
15	105 (0.103%)	253 (0.247%)	3304 (3.227%)	0 (0.0%)	0 (0.0%)	21 (0.021%)
16	105 (0.103%)	233 (0.228%)	2116 (2.066%)	0 (0.0%)	0 (0.0%)	2 (0.002%)
17	60 (0.059%)	123 (0.120%)	825 (0.806%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
18	84 (0.082%)	114 (0.111%)	400 (0.391%)	0 (0.0%)	0 (0.0%)	1 (0.001%)
19	45 (0.044%)	75 (0.073%)	131 (0.128%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
20	41 (0.040%)	77 (0.075%)	53 (0.052%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
21	19 (0.019%)	49 (0.048%)	8 (0.008%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
22	27 (0.026%)	46 (0.045%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
23	16 (0.016%)	22 (0.021%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
24	21 (0.021%)	36 (0.035%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

25	7 (0.007%)	12 (0.012%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
26	6 (0.006%)	16 (0.016%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
27	3 (0.003%)	3 (0.003%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
28	4 (0.004%)	6 (0.006%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
29	0 (0.0%)	3 (0.003%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
30	4 (0.004%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
31	1 (0.001%)	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
32	0 (0.0%)	4 (0.004%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
33	1 (0.001%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
34	1 (0.001%)	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
35	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
36	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
37	0 (0.0%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
38	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
39	0 (0.0%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
40	0 (0.0%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

Table S7. Distribution of the number of detected differences in different configurations with separate input pin in the same clock region and a separate clock region, at ambient temperatures.

Number of '1'	clock-capable input pin		non clock-capable input pin	
	Separate IBUF + BUFG + MMCM + BUFG	Separate IBUF + BUFG + PLL + BUFG	Separate IBUF + BUFG + MMCM + BUFG	Separate IBUF + BUFG + PLL + BUFG
0	43415 (42.397%)	49006 (47.857%)	45399 (44.335%)	44153 (43.118%)
1	5348 (5.223%)	10444 (10.199%)	8321 (8.126%)	5625 (5.493%)
2	8030 (7.842%)	13293 (12.981%)	11603 (11.331%)	7359 (7.187%)
3	7404 (7.23%)	10694 (10.443%)	9477 (9.255%)	7400 (7.227%)
4	9644 (9.418%)	8885 (8.677%)	9754 (9.525%)	9642 (9.416%)
5	7929 (7.743%)	5256 (5.133%)	7086 (6.920%)	8144 (7.953%)
6	7449 (7.274%)	2941 (2.872%)	5370 (5.244%)	7575 (7.397%)
7	5346 (5.221%)	1142 (1.115%)	2872 (2.805%)	5161 (5.040%)
8	3984 (3.891%)	513 (0.501%)	1532 (1.496%)	3635 (3.550%)
9	1999 (1.952%)	156 (0.152%)	622 (0.607%)	1971 (1.925%)
10	1147 (1.120%)	54 (0.053%)	268 (0.262%)	1071 (1.046%)
11	451 (0.440%)	11 (0.011%)	71 (0.069%)	440 (0.430%)
12	181 (0.177%)	4 (0.004%)	23 (0.022%)	158 (0.154%)
13	58 (0.057%)	1 (0.001%)	1 (0.001%)	48 (0.047%)
14	11 (0.011%)	0 (0.0%)	0 (0.0%)	16 (0.016%)
15	2 (0.002%)	0 (0.0%)	1 (0.001%)	2 (0.002%)
16	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

Table S8. Distribution of the number of detected differences in different configurations with separate clock-capable input pin in separate clock region and a separate clock region, at ambient temperatures.

Number of '1'	Separate IBUF	Separate IBUF + BUFG	Separate IBUF + MMCM + BUFG	Separate IBUF + BUFG + MMCM + BUFG	Separate IBUF + PLL + BUFG	Separate IBUF + BUFG + PLL + BUFG
0	56500 (55.176%)	55576 (54.273%)	36316 (35.465%)	42309 (41.317%)	49516 (48.355%)	50480 (49.297%)
1	13107 (12.8%)	11813 (11.536%)	2948 (2.879%)	4191 (4.093%)	10468 (10.223%)	11543 (11.272%)
2	13109 (12.802%)	12849 (12.548%)	3437 (3.356%)	6073 (5.931%)	13982 (13.654%)	14118 (13.787%)
3	9508 (9.285%)	9509 (9.286%)	1590 (1.553%)	5223 (5.101%)	10809 (10.556%)	10487 (10.241%)
4	5669 (5.536%)	6284 (6.137%)	2376 (2.320%)	8538 (8.338%)	8979 (8.769%)	7920 (7.734%)
5	2711 (2.647%)	3231 (3.155%)	2941 (2.872%)	7856 (7.672%)	4916 (4.801%)	4424 (4.320%)
6	1228 (1.199%)	1950 (1.904%)	3187 (3.112%)	8266 (8.072%)	2506 (2.447%)	2213 (2.161%)
7	404 (0.395%)	746 (0.729%)	2743 (2.679%)	6787 (6.628%)	848 (0.828%)	818 (0.799%)
8	137 (0.134%)	316 (0.309%)	3104 (3.031%)	5890 (5.752%)	277 (0.271%)	307 (0.300%)
9	21 (0.021%)	93 (0.091%)	3412 (3.332%)	3553 (3.470%)	79 (0.077%)	65 (0.063%)
10	5 (0.005%)	26 (0.025%)	4109 (4.013%)	2214 (2.162%)	18 (0.018%)	23 (0.022%)
11	1 (0.001%)	5 (0.005%)	5360 (5.234%)	951 (0.929%)	2 (0.002%)	2 (0.002%)
12	0 (0.0%)	2 (0.002%)	6175 (6.030%)	415 (0.405%)	0 (0.0%)	0 (0.0%)
13	0 (0.0%)	0 (0.0%)	6686 (6.529%)	97 (0.095%)	0 (0.0%)	0 (0.0%)
14	0 (0.0%)	0 (0.0%)	6461 (6.310%)	25 (0.024%)	0 (0.0%)	0 (0.0%)
15	0 (0.0%)	0 (0.0%)	4840 (4.727%)	11 (0.011%)	0 (0.0%)	0 (0.0%)
16	0 (0.0%)	0 (0.0%)	3447 (3.366%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
17	0 (0.0%)	0 (0.0%)	1726 (1.686%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
18	0 (0.0%)	0 (0.0%)	949 (0.927%)	1 (0.001%)	0 (0.0%)	0 (0.0%)
19	0 (0.0%)	0 (0.0%)	377 (0.368%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
20	0 (0.0%)	0 (0.0%)	156 (0.152%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
21	0 (0.0%)	0 (0.0%)	40 (0.039%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
22	0 (0.0%)	0 (0.0%)	17 (0.017%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
23	0 (0.0%)	0 (0.0%)	2 (0.002%)	0 (0.0%)	0 (0.0%)	0 (0.0%)
24	0 (0.0%)	0 (0.0%)	1 (0.001%)	0 (0.0%)	0 (0.0%)	0 (0.0%)

Table S9. Distribution of the number of detected differences in different configurations with separate non clock-capable input pin in separate clock region and a separate clock region, at ambient temperatures.

Number of '1'	Separate IBUF	Separate IBUF + BUFG	Separate IBUF + MMCM + BUFG	Separate IBUF + BUFG + MMCM + BUFG	Separate IBUF + PLL + BUFG	Separate IBUF + BUFG + PLL + BUFG
0	55978 (54.666%)	53481 (52.228%)	51153 (49.954%)	46439 (45.351%)	47447 (46.335%)	47123 (46.019%)
1	9181 (8.966%)	9512 (9.289%)	12994 (12.689%)	8255 (8.062%)	8221 (8.028%)	7998 (7.811%)
2	13471 (13.155%)	10877 (10.622%)	15634 (15.268%)	11589 (11.317%)	11062 (10.803%)	11521 (11.251%)
3	8604 (8.402%)	9254 (9.037%)	10512 (10.266%)	9836 (9.605%)	10117 (9.880%)	9670 (9.443%)
4	7884 (7.699%)	7672 (7.492%)	7006 (6.842%)	10332 (10.090%)	10248 (10.008%)	9996 (9.762%)
5	3296 (3.219%)	5335 (5.210%)	3216 (3.141%)	6998 (6.834%)	7181 (7.013%)	6881 (6.720%)
6	2523 (2.464%)	3570 (3.486%)	1354 (1.322%)	4755 (4.644%)	4629 (4.521%)	4832 (4.719%)
7	807 (0.788%)	1700 (1.66%)	395 (0.386%)	2396 (2.340%)	2060 (2.012%)	2454 (2.396%)
8	504 (0.492%)	786 (0.768%)	110 (0.107%)	1194 (1.166%)	981 (0.958%)	1197 (1.169%)
9	104 (0.102%)	177 (0.173%)	24 (0.023%)	409 (0.399%)	322 (0.314%)	472 (0.461%)
10	45 (0.044%)	35 (0.034%)	2 (0.002%)	160 (0.156%)	91 (0.089%)	170 (0.166%)
11	2 (0.002%)	1 (0.001%)	0 (0.0%)	27 (0.026%)	33 (0.032%)	64 (0.062%)
12	1 (0.001%)	0 (0.0%)	0 (0.0%)	6 (0.006%)	8 (0.008%)	17 (0.017%)
13	0 (0.0%)	0 (0.0%)	0 (0.0%)	4 (0.004%)	0 (0.0%)	3 (0.003%)
14	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	1 (0.001%)
15	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	0 (0.0%)	1 (0.001%)