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Temperature and Power Supply Compensated CMOS Clock Circuit Based on Ring Oscillator

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Abstract: Improved performance operational amplifier demand has continuously increased. IC designers use the charge pump technique as an advanced solution to implement the amplifier's rail−to−rail input stage, but the need for a large load capacitor is a serious downside. To reduce this passive component value, high−frequency clock circuits with a 50% duty cycle should be implemented. This paper focuses on designing such a circuit that is further compensated with temperature and power supply, maintaining these performances even when process variations occur, starting from a ring oscillator as the architecture core. A pre−layout 50 MHz center frequency at 25 °C with a 1.6 temperature percentage error was achieved. Post−layout simulations to account for parasitic effects were also performed, with a 48.9 MHz center frequency reached. Distinct methods that control the frequency variation were discussed and established. Performance comparison of the designed PLL with previously reported clock circuits in the CMOS process was concluded, with superior results such as power consumption, die area, and temperature range accomplished.

Keywords: ring oscillator; LDO; frequency oscillation; CMOS technology; level−shifter; charge−pump

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1. Introduction

Operational amplifiers (Op−amps) in CMOS technology have evolved from classical differential stages with active load and single−ended output [1] into complex architectures that minimize the offset voltage V_{OS} and the noise spectral density, with simultaneous cost reduction and improved performance. New state−of−the−art topologies are frequently developed alongside CMOS technology with continuous improvement (decreasing the leakage currents or the transistor die size, for example). A main topic currently is finding the most efficient approach to implement the amplifier rail−to−rail input stage.

One common design solution uses complementary $pMOS - nMOS$ differential input pairs with architectures that control the transistor currents, to maintain constant transconductance g_m for the whole input range. Some topologies are presented in [2], but one of this method's disadvantages is the offset voltage, which is slightly different from stage to stage. A further drawback that must be considered is the variable transconductance in the regions where the transition between the complementary input stages occurs due to the current that passes from one branch to another.

Another more valuable approach implies using charge pump circuits that level up the potential around the input stage with a known value above supply voltage (V_{DD}). In this case, one single differential pair is active for the entire common input range; thus, no complementary pair is longer required. The transconductance and the offset voltage in this situation will be constant regardless of what signal is applied at the transistor's input.

Charge pump architectures are based on clock signals and fast switching to charge/discharge capacitors to obtain higher voltages than the supply. A popular topology is the Dickson charge pump [3,4], but more optimized and efficient circuits have now been established. One downside of this approach is the higher currents that must be drawn

from the charge pump output, mainly the differential pair tail current, but additional currents may be needed depending on the designer's approach. This will require large load capacitances to maintain a low ripple voltage at the circuit output; accordingly, the circuit die size will increase.

A key idea in solving this inconvenience and therefore having a lower capacitance value is reaching a clock frequency where the power supply rejection ratio (PSRR) in alternative current (AC) is high enough that the ripple at the amplifier's output will be considerably reduced. This usually happens at frequencies on the order of tens of MHz; thus, oscillators that can reach such high oscillation period values with lower current consumption and die area must be implemented.

Another aspect to remember in the oscillator design stages used in a charge−pump architecture is the frequency process variation. The differential input tail current in an op−amp has a PTAT characteristic, so that the transconductance is compensated with temperature; thus, a constant unity gain bandwidth (UGBW) and an improved offset voltage thermal coefficient (TC_{VOS}) are obtained. In corners, this current is lower, slow−slow process (SS), respective to the higher, fast−fast process (FF). Frequency process compensation would lead, for example, in FF to higher charge−pump ripple at its output, which is undesirable in a precision op−amp architecture.

Designing relaxation oscillators [5,6], for example, is not suitable because, first and foremost, to obtain 50% duty cycles with this approach, frequency divider circuits (DFF) are required, finally leading to two times higher clock period values. Furthermore, higher frequencies will conduce to an increase in their dependence on the delay given by the signal's propagation through the circuits, which is unacceptable for applications where the frequency oscillation must be accurately determined.

This paper presents an innovative clock circuit concept that eliminates the above-mentioned impediments and achieves compensation with temperature and power supply, maintaining these performances even when process variations occur. The block diagram is presented in Figure 1. Clock architecture is accomplished based on a ring oscillator circuit [7–9]. The frequency dependence given by the supply voltage is reduced using a low−dropout regulator (LDO). One non−overlapping circuit is also implemented alongside a level shifter block [10] that restores the clock signal's maximum value. V_{REF} is a reference potential established by using a bandgap voltage. Cascaded current−starved mirrors are used to fulfill temperature compensation. The circuit works at high temperatures (maximum 150 °C), so that its applicability is extended to the automotive industry.

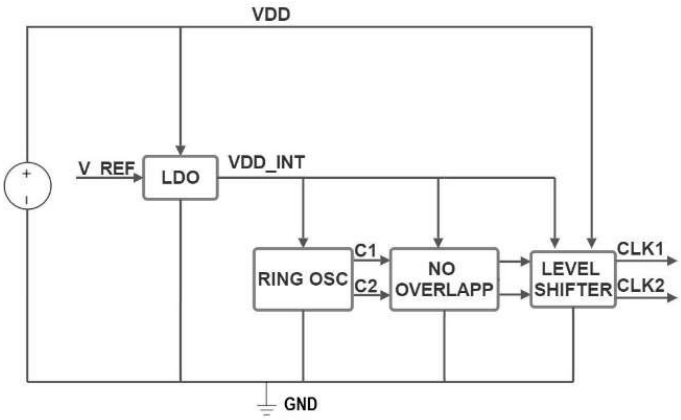


Figure 1. Proposed clock circuit block diagram with ring oscillator.

2. Design and Implementation

2.1. Classical Current Starved Ring VCO

This subchapter presents the well−known current starved ring VCO that is the starting point [11] for the improved and more efficient architecture presented in this paper. The schematic is presented in Figure 2. One NAND gate provides an on−and−off switching

option for the circuit. When the enable pin is "0" logic, the NAND gate output will remain "1", regardless of what signal is on the other input; thus, no oscillation will occur. When the enable pin is "1", the NAND gate will behave identically as an inverter, creating favorable conditions for oscillation appearance. Odd numbers of logical gates are required in the reaction loop. Capacitors $C_1 - C_4$ are added to further control the output frequency [7]:

$$t_{cap} = \frac{C \cdot V_{th}}{I_{cont}} \tag{1}$$

where V_{th} is the inverter threshold point, C the capacitor value, and I_{cont} the current that passes through the inverter.

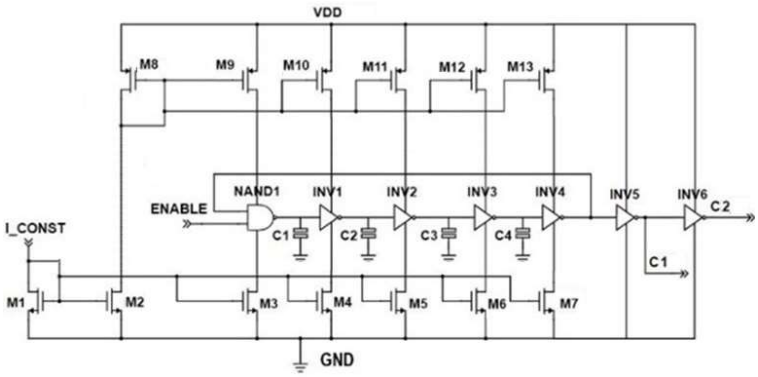


Figure 2. Classical current−starved ring VCO.

The generated signal period is [7]:

$$T_{clk} = 2(t_{nand} + 4 \cdot t_{inv} + 4 \cdot t_{cap}) \tag{2}$$

where t_{nand} is the NAND logic gate delay time and t_{inv} is the inverter logic gate delay time.

This architectures downside is that M1 and M8 transistors are in diode configuration. Thus their drain−source voltage is well fixed and equal to their gate−source voltage, while nMOS transistors M2–M7 and pMOS transistors M9–M13 VDS are supply voltage dependent. This will cause a shift in the logic gates propagation delay and the C1−C4 capacitor's charge/discharge time with the supply voltage, given by the drain current short−channel effect; hence the ring VCO frequency is affected. Moreover, the gate−source voltage of the M1 and M8 transistors is complementary to absolute temperature (CTAT), leading to a change in frequency with temperature.

2.2. Proposed Ring Oscillator Technique

The proposed ring oscillator technique keeps the current mirror drain−source voltage equal, regardless of the supply voltage and temperature. Figure 3 shows the proposed architecture. $pMOS - nMOS$ cascade current mirror pairs have been implemented. Using this topology complementary with designing a zero to absolute temperature (ZTAT) current, the switching current is well controlled, and compensation with temperature is achieved.

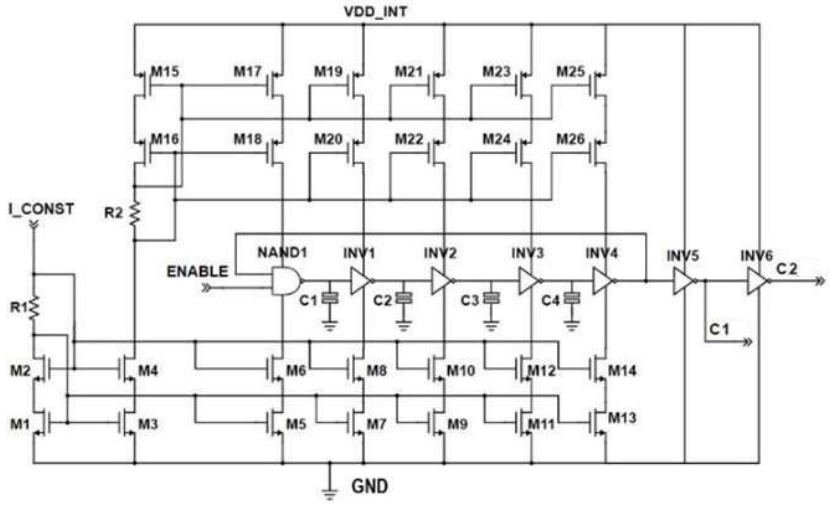


Figure 3. Proposed design architecture for the ring oscillator circuit.

The logic gate delay time is strongly influenced by the circuit supply voltage due to the gate potential that is detected by each transistor. As a result of using the cascade current mirrors, the established potential in the sources of *pMOS* and *nMOS* devices, which forms the logic gates in the ring oscillator, are not connected directly to V_{DD} and GND:

$$V_{Snmos} = V_{DS\_Ncascade} + V_{DS\_Nmirror} \tag{3}$$

$$V_{Spmos} = V_{DD} - V_{SD\_Pmirror} - V_{SD\_Pcascade} \tag{4}$$

The current mirror V_{DS} voltage is well determined by the potentials across R_1 and R_2 resistors. On the other hand, the cascades V_{DS} is not biased at a fixed point; thus, variations with switching the supply voltage may occur. This can cause a change in the logic gate's delay time, and fluctuations in the oscillation frequency are expected. To avoid such inconvenience, an internal 2 V voltage compensated with temperature and V_{DD} is used.

A 50% duty cycle is ensured by fixing the logic gates' threshold points at half of V_{DD} when they were simulated independently. The desired clock frequency in this paper is 50 MHz at room temperature. Transistor dimensions and other component values that form the ring oscillator are charted in Table 1.

Table 1. Design parameters for ring oscillator.

Parameter	Value
R1, R2	350 kΩ, 300 kΩ
C1−C4	32.8 fF
(W/L) M1–M3, M5–M7–M9–M11–M13	6/3, 18/3 µm/µm
(W/L) M2–M4, M6–M8–M10–M12–M14	4/2, 12/2 µm/µm
(W/L) M15, M17–M19–M21–M23–M25	22/4, 66/4 µm/µm
(W/L) M16, M18–M20–M22–M24–M26	18/3, 54/3 µm/µm

2.3. Low—Dropout Voltage Concept

The *LDO* circuit is established by using a two−stage operational amplifier [12,13], as seen in Figure 4. transistors M_1–M_2 form the differential pair, M_3–M_4 adjacent *pMOS* transistors serve as active loads and M_5 is the class A output stage. A Miller compensation [14] is used to ensure that stability is achieved.

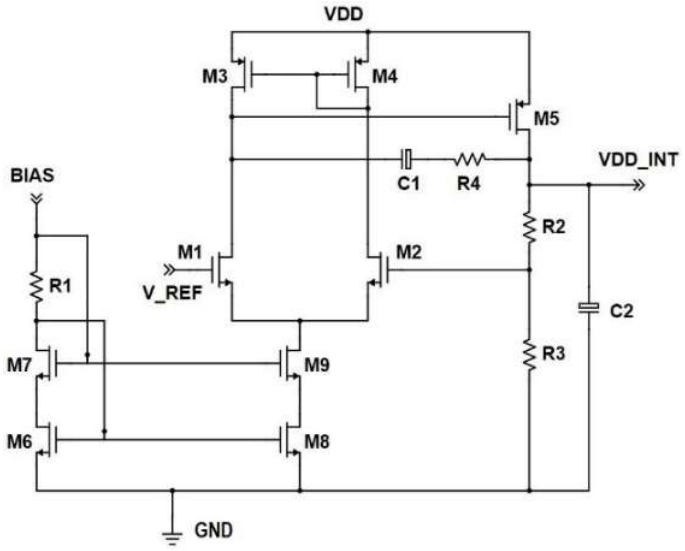


Figure 4. Low−dropout regulator schematic.

V_{DD_INT} voltage is obtained using a resistive divider between the amplifier's output and the negative input, thus creating negative feedback. Considering $V_{IN-} = V_{IN+} + V_{OS}$, the following equation is reached:

$$V_{DD\_INT} = \left(1 + \frac{R_2}{R_3}\right)(V_{REF} + V_{OS}) \quad (5)$$

Scaling down the V_{DD_INT} dependency on the offset voltage is important, and methods to minimize this key parameter have to be applied [15], but the circuit's total die size must be considered at the same time. Capacitor C_2 helps to reduce the output ripple given by the ring oscillator.

If V_{REF} voltage is 1.25 V and V_{OS} is neglected, the ratio of the resistors R_2 and R_3 should be approximately 0.6 to obtain the desired 2 V internal voltage.

Transistor dimensions and other component values that form LDO are presented in Table 2.

Table 2. Design parameters for LDO.

Parameter	Value
R1, R2, R3, R4	200 kΩ, 200 kΩ, 600 kΩ, 28.9 kΩ
C1, C2	1.15 pF, 11.5 pF
(W/L) M1–M2	20/2 µm/µm
(W/L) M3–M4, M5	80/0.5, 160/0.5 µm/µm
(W/L) M6–M7, M8–M9	12/2, 60/2 µm/µm

3. Simulations and Results

3.1. Schematic Level Simulations

In this subchapter, schematic level simulations were performed in the Cadence Virtuoso environment work system using a 250 nm CMOS technology. Figure 5 shows the internal constant voltage V_{DD_INT} change with temperature. The curvature determined by the bandgap voltage characteristic can be observed. For the 2 V supply voltage, a waveform flattening occurs due to the very small difference between V_{DD} and V_{DD_INT}. This will determine the low−dropout circuit output stage (M_5 transistor) to work in the linear region. This will lead to a smaller fluctuation in the internal constant voltage even with the process and mismatch.

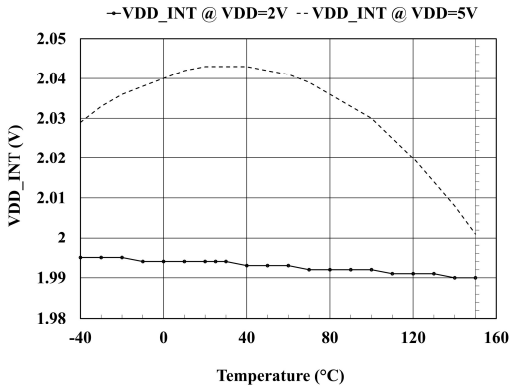


Figure 5. Constant internal supply voltage adjustment with temperature.

The typical minimum and maximum V_{DD_INT} potentials reached for each simulated supply voltage were 1.99 V with 1.995 V for $V_{DD} = 2\ V$ and 2.001 V with 2.043 V for $V_{DD} = 5\ V$. These numbers show that a 2 V voltage source compensated with V_{DD} and temperature was achieved.

The frequency dependency given by supply voltage is illustrated in Figure 6. In the first one (a), the basic ring oscillator is implemented, with the internal supply voltage and the current−starved disconnected from the circuit. As expected, the PLL dependency on supply voltage is almost linear, the minimum and maximum values being 119.4 MHz ($V_{DD} = 2\ V$) and 387.6 MHz ($V_{DD} = 5\ V$). This high−frequency range is unacceptable for applications where precision is critical.

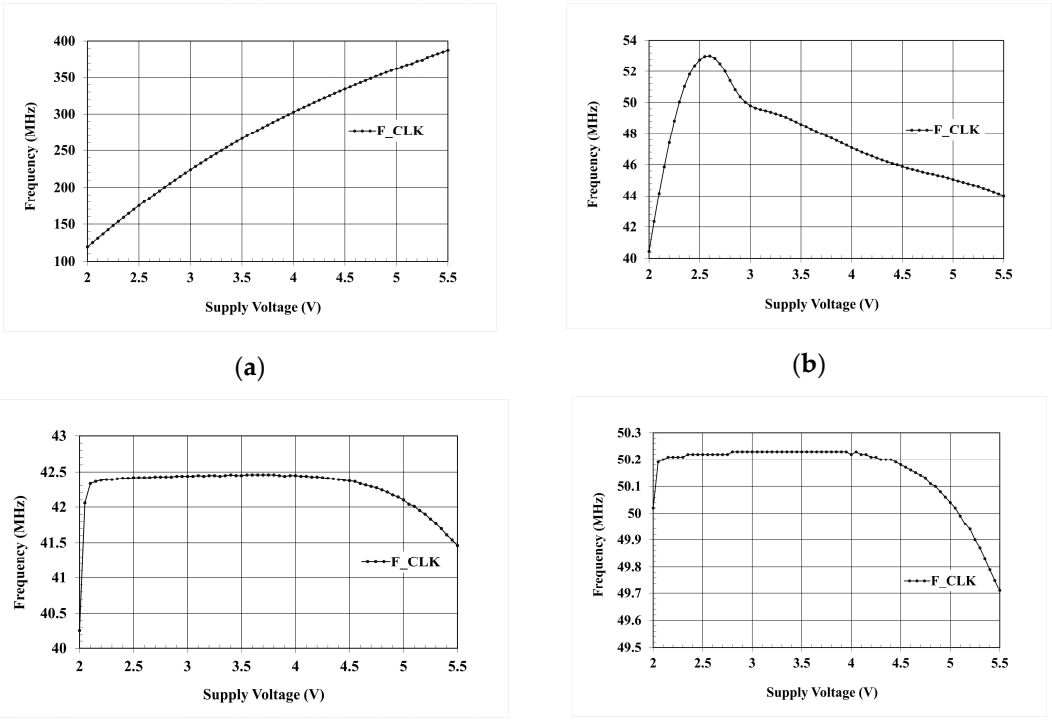


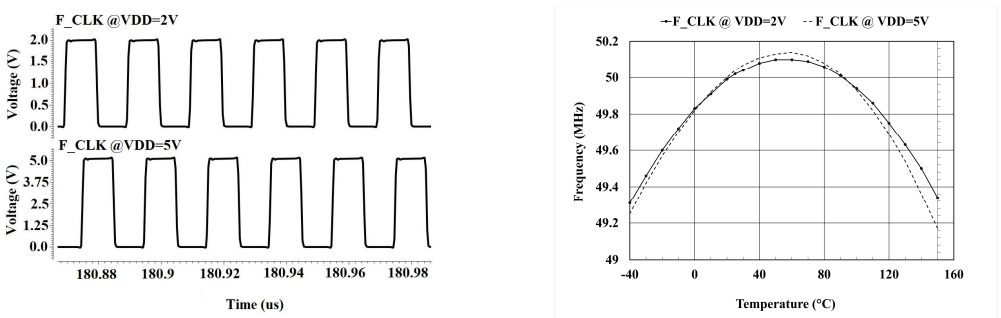
Figure 6. Frequency dependency given by supply voltage for the ring oscillator. (**a**) Basic implementation; (**b**) Current−starved added; (**c**) Internal supply voltage and current−starved connected; (**d**) Proposed design with cascaded current−starved.

In the second picture (b), the current−starved ring oscillator is designed and simulated. The frequency range is considerably decreased compared to (a), with a minimum frequency

reached at 2 V (40.43 MHz) and a peak value around 2.6 V (53 MHz). The third one (c) uses both the current−starved architecture and the internal supply voltage generated by the LDO. The frequency range is tighter (40.25 MHz; 42.45 MHz); thus, the frequency stability when V_{DD} changes is improved. A decrease in frequency can be observed when the supply voltage exceeds 4 V, with a local minimum value of 41.45 MHz being reached.

The fourth picture (d) highlights the results obtained using the proposed PLL circuit described in this paper. The cascaded current−starved improves the frequency variation at the start and the end of the graph, reducing the current variation given by the fluctuation of the internal supply voltage; thus, the difference between the maximum and minimum value is only 0.53 MHz, a 1.67 MHz improvement compared to (c). Furthermore, using cascaded current−starved mirrors, the temperature effects over time are minimized due to the mirror drain−source voltage being equal and the dependency given by the short channel effect being discarded. Hence, the same current flows through all inverters and capacitors in the ring oscillator.

Figure 7a reports the time response at room temperature after the level shifter for the clock signal, considering two supply voltages: 2 V and 5 V. To better understand the results obtained, zoom is made on the $x-$axis.



(**a**) (**b**)

Figure 7. Typical simulation results for the clock circuit. (**a**) Time response; (**b**) Frequency variation with temperature and VDD.

The two waveforms' duty cycle is approximately 50%. This means that, in a charge pump architecture, by using the designed oscillator in this paper, the capacitor's charge and discharge time will be equal and the output ripple reduced.

The oscillator frequencies obtained at room temperature for the two supply voltages mentioned above are 50.01 MHz ($V_{DD} = 2\ V$) and 50.04 MHz ($V_{DD} = 5\ V$), close to the 50 MHz desired value.

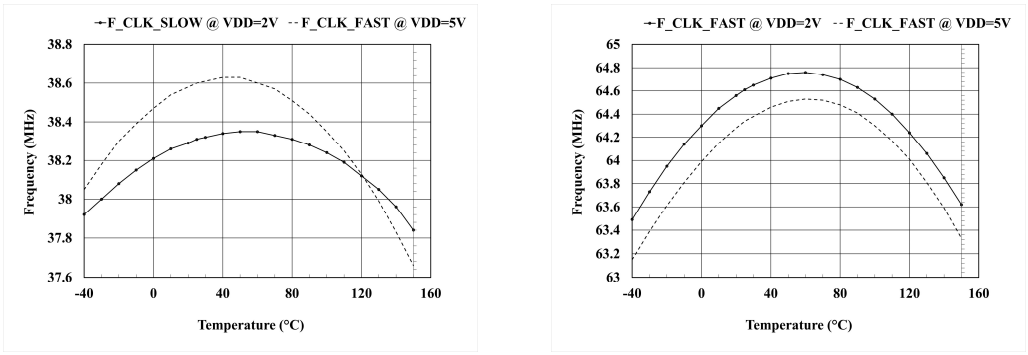
Figure 7b illustrates the frequency variation in a typical corner with temperature for the same supply voltages. The constant current and the potentials are derived from a circuit that uses bandgap voltage theory [16]. The same curvature with temperature for the clock frequency is obtained. Typical peak values of 50.1 MHz (for $V_{DD} = 2\ V$) and 50.15 MHz (for $V_{DD} = 5\ V$) are recorded around 60 °C, while the minimum value (49.2 MHz) was reached for 5 V supply voltage at 150 °C. The temperature percentage error ε_{osc} obtained using the formula below is 1.6.

$$\varepsilon_{osc} = \left| \frac{S_{val} - T_{val}}{T_{val}} \right| \cdot 100 \tag{6}$$

where S_{val} represents the experimental value and T_{val} the theoretical one.

Process variations can affect the oscillator frequency compensation with temperature and power supply. To evaluate the circuit performance considering this aspect, slow and fast corner simulations are performed. In the slow corner (Figure 8a), the transistors

threshold point is shifted to a higher value; thus, a greater VGS voltage is required to turn the devices on.



(**a**) (**b**)

Figure 8. Frequency variation with temperature and VDD in corners. (**a**) Slow; (**b**) Fast.

A decreased center frequency value of around 38.3 MHz (for $V_{DD} = 2\ V$) and 38.5 MHz (for $V_{DD} = 5\ V$) was obtained due to the lower constant current generated in this corner. In the fast corner (Figure 8b), the transistor's threshold point is shifted to a lower value, leading to the decreased VGS voltage needed to turn the devices on. An increased average frequency value of around 64.1 MHz (for $V_{DD} = 2\ V$) and 63.9 MHz (for $V_{DD} = 5\ V$) is obtained. Compensation with temperature and power supply is achieved even in these corners, representing the worst process variation scenarios. To further reduce the curvature, second−order compensation for the bandgap circuit has to be implemented.

The average current consumed by the designed ring oscillator doesn't exceed 20 µA regardless of supply voltage, as seen in Figure 9. The entire circuit that includes all the functional architecture blocks requires less than 125 µA.

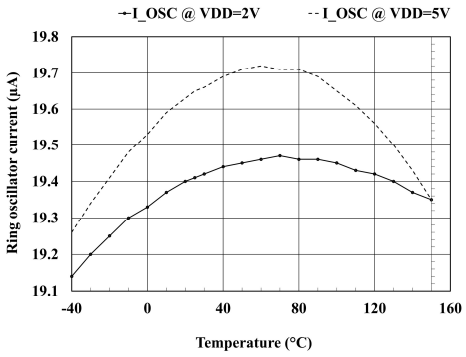
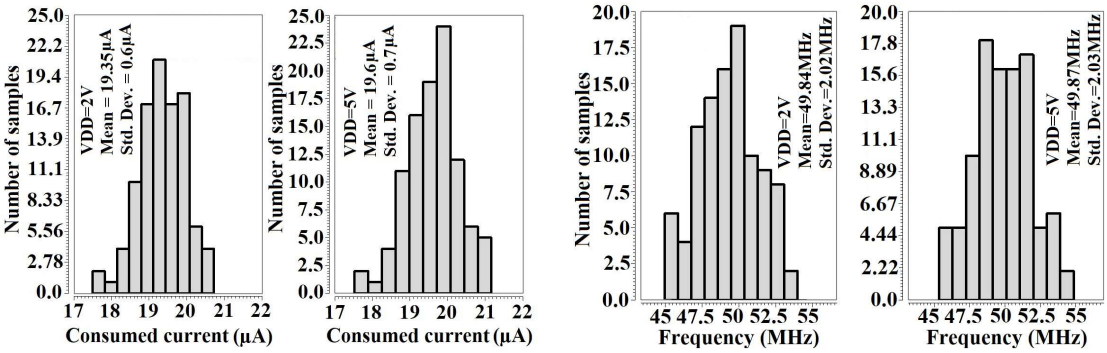


Figure 9. Ring oscillator quiescent current variation with temperature and VDD.

Figure 10a shows the results obtained using the Monte Carlo sampling technique for the clock signal at two supply voltages. The means and standard deviations are 49.84 MHz and 2.019 MHz for $V_{DD} = 2\ V$, respectively 49.87 MHz and 2.023 MHz for $V_{DD} = 5\ V$. The numbers show that even if the mismatch influences the oscillator frequency, the variation given by the change in supply voltages is negligible.



(**a**) (**b**)

Figure 10. Monte Carlo simulations histograms. (**a**) Oscillation frequency; (**b**) ring oscillator consumed current.

Figure 10b presents, at room temperature, the Monte Carlo simulation results over the total current consumed by the proposed ring oscillator for the same supply voltages as mentioned above. The means and standard deviations are 19.35 µA and 0.6 µA for $V_{DD} = 2\ V$, respectively 19.6 µA and 0.7 µA for $V_{DD} = 5\ V$. The maximum current is listed in Table 3.

Table 3. Results summary for 2 V supply voltage.

Parameter	Typical Value @ 25 °C	Monte Carlo (Mean ± 6 σ) @ 25 °C	Min. and Max. Typ. Values over Temperature
Clock frequency (MHz)	50.01	(37.72; 61.98)	(49.3; 50.1)
IQ ring oscillator (µA)	19.34	<22.95	(19.1; 19.38)
IQ total (µA)	62.24	<75	(60.14; 64.69)
VDD_INT (V)	1.994	(1.966; 2.019)	(1.99; 1.995)

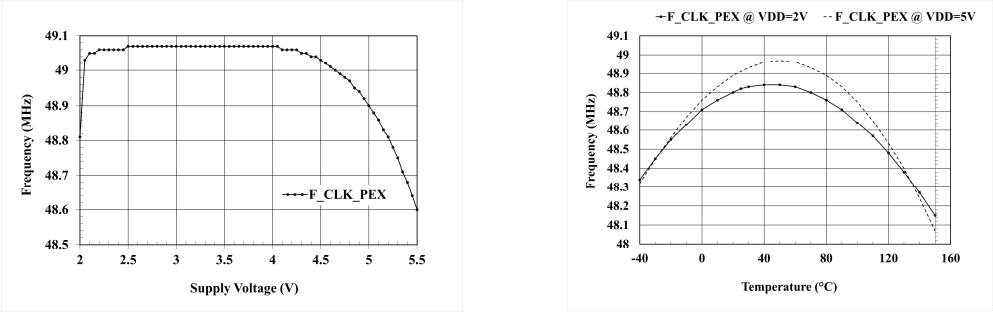
The outcome of the schematic level simulations proves that the suggested design is suitable for applications that require low power consumption [17]. A summary of the results obtained from the architecture is presented in Tables 3 and 4.

Table 4. Results summary for 5 V supply voltage.

Parameter	Typical Value @ 25 °C	Monte Carlo (Mean ± 6 σ) @ 25 °C	Min. and Max. Typ. Values over Temperature
Clock frequency (MHz)	50.04	(37.73; 62)	(49.2; 50.15)
IQ ring oscillator (µA)	19.65	<24	(19.34; 19.72)
IQ total (µA)	103.2	<125	(98.52; 107.9)
VDD_INT (V)	2.043	(1.84; 2.23)	(2.001; 2.043)

3.2. Post Layout Simulations

Parasitic effects can influence the oscillator frequency compensation with temperature and power supply. To evaluate the circuit performance, post−layout simulations were performed using the parasitic extraction method. The results are presented in Figure 11.



(**a**) (**b**)

Figure 11. Frequency characteristics with PEX simulations. (**a**) vs. supply voltage; (**b**) vs. temperature.

The frequency dependency given by supply voltage is illustrated in Figure 11a. A center frequency value of around 48.9 MHz is obtained. Peak and minimum values with parasitic extraction are 49.07 MHz and 48.6 MHz. Figure 11b shows the typical temperature influence over the proposed ring oscillator technique at two supply voltages. Peak and minimum values are 48.83 MHz, 48.14 MHz (for $V_{DD} = 2\ V$) and 48.95 MHz, 48.06 MHz (for $V_{DD} = 5\ V$). The temperature percentage error with PEX is 1.71, comparable to that accomplished from schematic level simulations. These values confirm that temperature and supply voltage compensation are achieved despite parasitic effects.

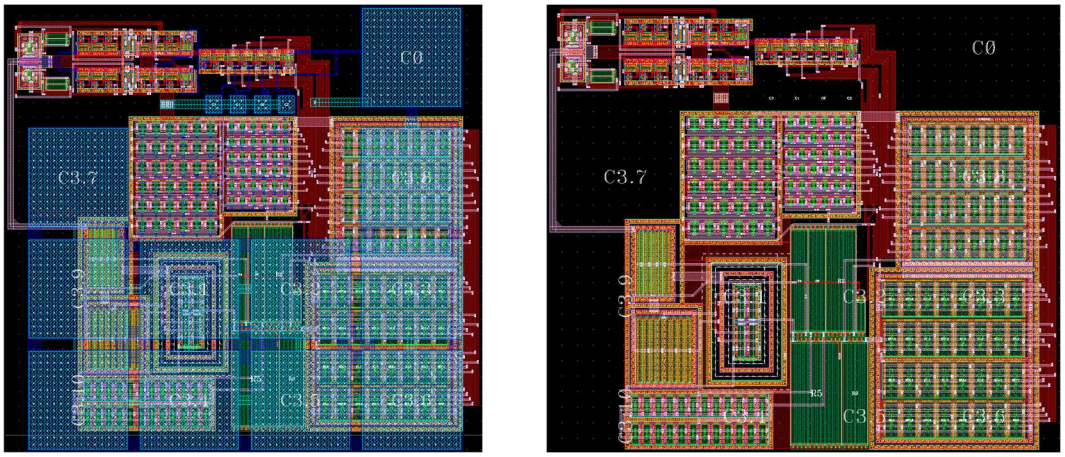
Table 5 lists ring VCO architectures performance obtained with parasitic effects compared to previously reported works in the literature. The proposed technique performed better than [7,18–20] in terms of power consumption, die area, and temperature range and was close to [7] regarding frequency variation with temperature.

Table 5. Comparison results with previously reported work.

Parameter	[7]	[18]	[19]	[20]	This Work
Technology (nm)	250	180	130	250	250
Supply voltage (V)	2.2	1.8	3.3	3	2
Power consumption (mW) @ Center frequency	1.5	0.437	19.8	N/A	0.124
Center frequency (MHz)	7	100	1250	1	48.9
Frequency variation (with temperature) (%)	0.84	4.49	4.8	3.33	1.71
Die Area (mm^2)	1.6	N/A	20	162	0.023
Temperature range	−40 °C–125 °C	−40 °C–125 °C	−40 °C–120 °C	−40 °C–125 °C	−40 °C–150 °C

4. Layout Implementation

The circuit layout is presented in Figure 12. For the floorplan, the main goal was to isolate the ring oscillator digital gates as far as possible from the rest of the circuit to reduce the wire's parasitic capacitance. The ring oscillator digital block and the no−overlap schematic were placed on the layout's upper side, close to each other, to achieve short clock wires. Because no standardized digital cells were used in the schematic, all the digital blocks were designed to obtain minimum interconnect capacitances and resistances [21].



(**a**) (**b**)

Figure 12. Circuit layout. (**a**) including M3 and M4 masks; (**b**) without MIM capacitors.

The capacitors were placed over the circuit analogic part to improve the die area. Capacitors used were MIM type and made of upper metal layers, M3 and M4, to reduce parasitic elements. The clock wires were drawn on a higher metal to reduce vertical capacitances even more. The no−overlap block was designed with full symmetry to match the possible delays on the signal path.

For the LDO and the current mirrors in the ring oscillator, a common−centroid matching with two axes of symmetry was used [22]. For the current mirrors in the ring oscillator, dummies were used to achieve the rows and columns number with minimum distance between transistors for better matching and minimum wires above each row. The interconnects mostly used M1 (red) and M2 (pink), M1 for vertical interconnects, and M2 for horizontal ones. M2 was used for routing over transistors instead of a superior metal due to capacitors and to reduce cost. For the differential pair, cross−coupled matching was used. The last layout part was implemented to achieve the wire's full symmetry (according to the current flow) and was placed in the middle for better isolation. Multiple contact guard rings were used around all blocks to reduce susceptibility to latch−up. All resistors were placed together (green color), with minimum distance between them to reduce possible etching errors. LVS and DRC verifications were done to check for design errors. The circuit layout die area was 0.023 mm^2.

5. Conclusions

This paper focused on designing a clock circuit, compensated with temperature and power supply, maintaining these performances even when process variations occur, starting from a ring oscillator as the architecture core. Simulations were performed using 250 nm CMOS technology. A pre−layout 50 MHz center frequency at 25 °C with a 1.6 temperature percentage error was achieved. Cascade current mirrors, together with a constant current as a reference, were used to reduce the circuit's total power consumption along with temperature variation. At room temperature, the maximum current required for the ring oscillator was 24 µA, and the architecture's overall maximum current was 125 µA. A low−dropout block ensured a regular period with a change in the supply voltage. The generated signal rebounded to V_{DD} using a level shifter. The logic gate's threshold point was established at half of the supply voltage to provide a 50% duty cycle. Post−layout simulations to account for parasitic effects were performed to confirm temperature and supply voltage compensation was achieved even with parasitic effects. A 48.9 MHz center frequency was reached in this case. Performance comparison of the designed PLL with previously reported clock circuits in the CMOS process was also concluded.

These results highlight the fact that the proposed circuit can be used in charge pump architectures to implement the operational amplifier's rail−to−rail input stage.

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