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A Novel Bidirectional-Switched-Capacitor-Based Interlaced DC-DC Converter

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Abstract: This study proposes a novel bidirectional-switched-capacitor-based interleaved converter. In view of the shortcomings of the two well-known unidirectional-switched-capacitor-based interleaved converters, this study improves such converters through combining the novel structure of a switched capacitor circuit. The first effort was to overcome the drawback of the Cockcroft–Walton-based interleaved converter, whose circuit impedance and ripple cause a serious output voltage drop. The second was to solve the Dickson-based interleaved converter with its capacitors subjected to high-voltage stress. The third was to relax the unidirectional boost function of the Cockcroft–Walton- or Dickson-based interleaved converter. This study avoided not only high-circuit impedance and ripple, as in the case of the Cockcroft–Walton converter, but also it had lower component stress than the Dickson converter. In addition, this study redesigned the unidirectional boost function of the Cockcroft–Walton- or Dickson-based interleaved converter, such that the switch-capacitor-based interleaved converters became bidirectional DC-DC converters. Finally, the experimental results are provided to verify the feasibility of the proposed method.

Keywords: high-voltage conversion ratio; switched capacitor voltage multiplier; interleaved converter; bidirectional DC-DC converter

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1. Introduction

High-voltage power supplies have been widely used in various home appliances, as well as in industrial and medical applications. Equipment such as microwave ovens, X-ray generators, electrostatic generators, and scanning electron microscopes all require high voltages. Recently, there has been a lot of research on the DC-DC converter with a high voltage conversion ratio. The use of very high turn ratio transformers to achieve high-voltage gain is limited by its large leakage inductance and parasitic capacitance, making the circuit design complex. Thus, a voltage multiplier (VM) with simple architecture is a good choice for obtaining high voltage [1].

It is known that a multi-phase interleaved boost circuit, a two-switch boost converter topology for which voltage gain is determined by the duty cycle [2], can reduce current ripple, increase the rated current, increase the voltage conversion ratio, and reduce the size of the inductor.

However, the voltage conversion ratio of the interleaved converter is limited by the duty cycle of the boost converter [3]. To obtain a higher conversion ratio, one of the solutions is to combine an interleaved converter with a coupled inductor or a high-frequency transformer [4,5]. However, this makes the design of magnetic components complicated.

Another solution is a non-isolated architecture that combines an interleaved converter with a voltage multiplier [6–8]. This type of circuit architecture is simple to implement. In unidirectional boost applications, the interleaved converter boosts the low DC voltage and outputs a square wave voltage to the voltage multiplier. The square wave voltage is rectified by the voltage multiplier and further boosted. Finally, the converter achieves a high-voltage conversion ratio.

The converter that combines an interleaved circuit and a VM has advantages such as (1) reducing the current ripple on the low voltage side and increasing the rated current; (2) achieving a higher voltage conversion ratio using VM; (3) using a low voltage stress switch and diode [9].

The switched capacitor circuit (SCC), due to its simple structure, is one of the easiest voltage multipliers to implement. Two well-known SCCs are the Cockcroft–Walton and Dickson. In the Cockcroft–Walton VMC, each negative side of the odd capacitor is connected to the positive side of the previous odd capacitor, and each negative side of the even capacitor is connected to the positive side of the previous even capacitor [10,11]. However, in a real case, with the increase in the stages, the actual output voltage is lower than the ideal value. This is mainly because the capacitor impedance in the Cockcroft–Walton voltage multiplier increases with the increase in the stage number. Moreover, the ripple of the capacitor also increases rapidly with the increase in the stages. Thus, the Cockcroft–Walton VMC is not suitable in terms of adding too many stages.

Later, the Dickson SCC structure was found to greatly reduce the capacitance impedance and ripple of the VM [11], thereby improving the voltage drop of the Cockcroft–Walton voltage multiplier. However, the connection method causes the voltage stress on the capacitor to increase with the increase in the stage number. Thus, the Dickson SCC requires the use of high-voltage capacitors.

In [12], the two-phase interleaved boost converter combined with the Cockcroft–Walton improved the voltage conversion ratio. The circuit component had lower voltage stress, but the circuit impedance and ripple were very large. Reference [13] used a two-phase interleaved boost converter combined with a Dickson voltage multiplier. It was also able to achieve a higher voltage conversion ratio, but capacitors on the SCC needed to withstand high-voltage stress.

Observing the interleaved converters based on Cockcroft–Walton or Dickson SCCs [12,13], one can see that the Cockcroft–Walton structure has lower capacitor voltage stress, but its output voltage drops rapidly as the stage of the voltage multiplier increases. Although the Dickson structure improves the output impedance problem, it does so at the expense of higher capacitor voltage stress.

Observing the above-mentioned shortcomings of the interleaved converter on the basis of Cockcroft–Walton or Dickson SCCs [12,13], this study proposes an interleaved converter based on the hybrid SCC [14]. The achievable output voltage of this type of SCC, for a given capacitor voltage limit, is higher than the Dickson SCC. On the other hand, its output impedance is lower than the Cockcroft–Walton SCC.

Moreover, different from the unidirectional interleaved converter based on Cockcroft–Walton or Dickson SCCs, the proposed interleaved converter based on the hybrid SCC is a bidirectional converter.

Finally, the paper is organized as follows:

Section 2 illustrates the proposed SCC, including the operation modes and the working principle.

Section 3 describes the demonstrates the matching of the mathematical model with simulation results and a comparison of the key parameters with the popular SCCs.

Section 4 describes the physical implementation and shows the measurement results.

Section 5 summarizes the author's conclusions.

2. Circuit Topology

2.1. Main Circuit

The proposed bidirectional DC-DC converter consists of a two-phase interleaved converter circuit and a SCC, which is a hybrid of the Cockcroft–Walton and Dickson SCCs [15]. The ideal voltage conversion ratio of the converter depends on the switching duty cycle of the interleaved converter and the stage number of the SCC.

In this study, a stage is defined as a capacitor plus a switch. Taking the two-phase interleaved converter with an eight-stage hybrid as an example, the circuit diagram is shown in Figure 1. In it, the i-th stage ($i = 1, 2 \ldots 8$) is the pair of Q_i and C_i.

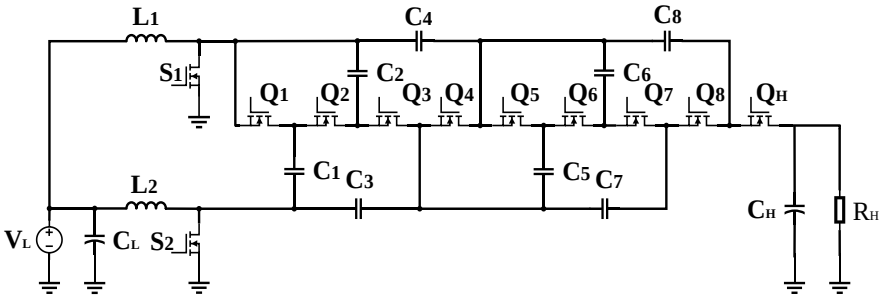

Figure 1. Proposed converter with an eighth-stage hybrid switched capacitor circuit.

2.2. Circuit Operation

A complete operation of the converter has four switching intervals, being composed of three working modes, namely, mode I, mode II, and mode III. The control signals of the switches S_1 and S_2 are 180° out of phase with each other, and with duties greater than 50%. The duties of S_1 and S_2 can be different. The odd-numbered switches, Q_i, $i = odd$, and switch S_1 exhibit complementary conduction states, while the even-numbered switches, Q_i, $i = even$, exhibit complementary conduction with switch S_2. When the stage number of SCC is odd, the control signal of the high-side switch Q_H is the same as even-numbered switches. On the contrary, when the stage number of the switched capacitor circuit is even, the control signal of the high-side switch Q_H is the same as odd-numbered switches.

Now, the boost mode is firstly discussed. Figure 2 shows the key signals of the switching signals and the inductor currents.

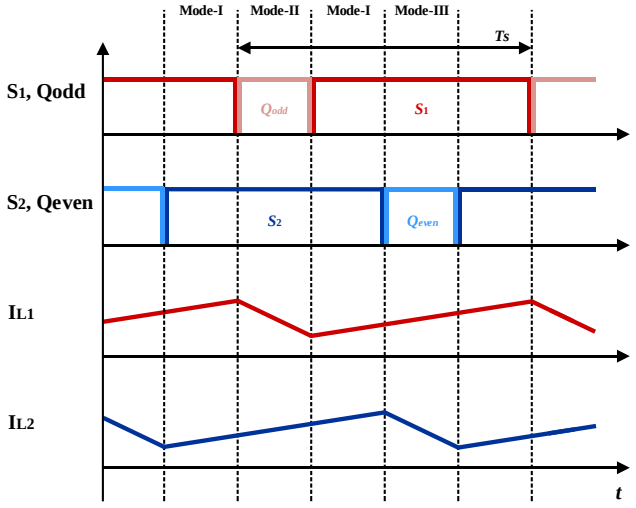

Figure 2. Circuit operation sequence of boost mode.

2.2.1. The First Switching Interval

The circuit operation in this switching interval is in mode I. As shown in Figure 3, S_1 and S_2 are both in the on state, the low-side V_L charges the two inductors, and the inductor currents increase. All the switches on the SCC and the high-side Q_H are non-conducting, and the capacitor voltages on them remain unchanged. The load energy is provided by the high-side C_H.

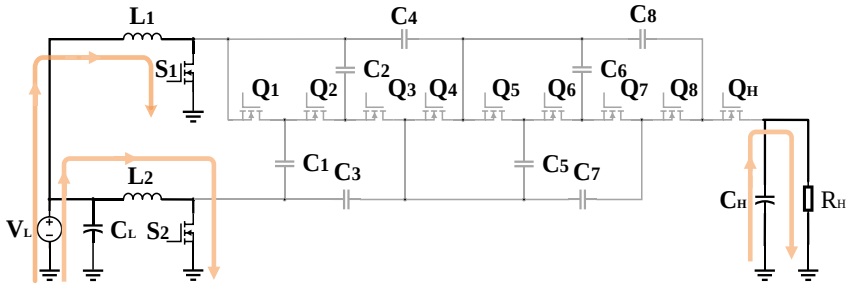

Figure 3. Mode I of boost mode.

2.2.2. The Second Switching Interval

This interval is mode II, as shown in Figure 4. At this time, S_1 is off, and S_2 is on. The odd-numbered switches on SCC are all turned on, while the even-numbered switches are not. The current I_{L1} of L_1 flows through the SCC, thereby charging the odd-stage capacitors and discharges the even-stage capacitors. Then, current I_{L1} decreases. Moreover, the high-side switch Q_H is turned on. In this condition, the current flows through Q_H to charge the output capacitor and provides energy to the load.

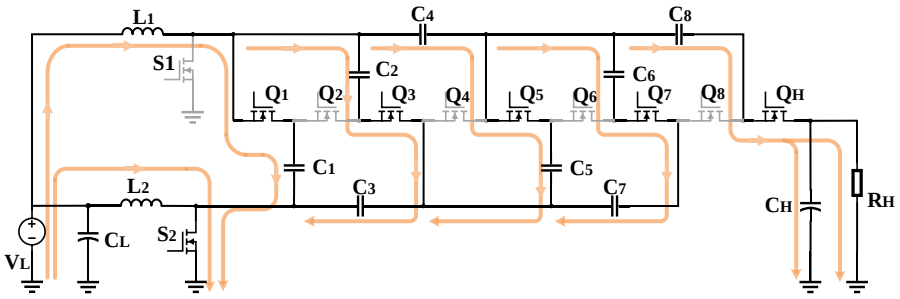

Figure 4. Mode II of boost mode.

2.2.3. The Third Switching Interval

The circuit in this interval is mode I, the same as the first switching interval.

2.2.4. The Fourth Switching Interval

The circuit in the fourth switching interval is mode III, as shown in Figure 5. At this time, S_1 is on, and S_2 is off. All the odd stage switches are non-conducting, and the even stage switches are turned on. The current I_{L2} of L_2 flows through SCC, thereby charging the even-stage capacitors and discharging the odd-stage capacitors. Moreover, the high-side Q_H is not turned on. Thus, the output capacitor provides energy to the load.

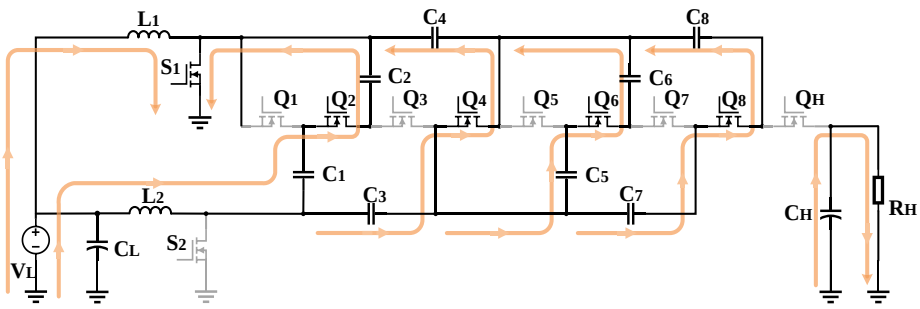

Figure 5. Mode III of boost mode.

In an ideal situation, except for the current direction, the converter has the same operations in boost and buck modes, as well as having the same voltage conversion ratios.

The important characteristics of the proposed converter were compared with several SCCs such as Cockcroft–Walton, Dickson, and hybrid. Section 2.3 describes and analyzes the proposed interleaved boost and buck converter.

2.3. Switched Capacitor Circuit

Figure 6 shows the eight-stage Cockcroft–Walton, Dickson, and hybrid SCCs.

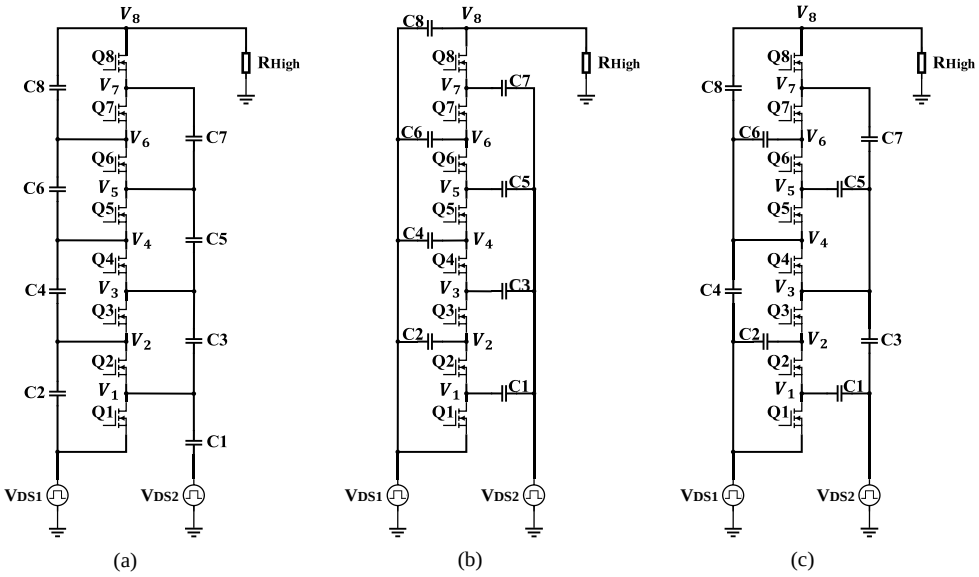

Figure 6. Eight-stage SCCs: (**a**) Cockcroft–Walton; (**b**) Dickson; (**c**) hybrid.

We assumed that the high-side current I_H and the switching frequency F_{sw} of the three SCCs were the same. Moreover, the charge flowing through each wire in each switching cycle was assumed to be the same. The charge q is defined as the amount charge transferred to the high-voltage side load in a switching period in the boost mode, which is also the charge output from the high-voltage side power supply in a switching period in the buck mode, as in (1), where $\langle I_H \rangle$ is the average of the high-side current I_H.

$$q = \frac{\langle I_H \rangle}{F_{sw}} \tag{1}$$

We assumed that the voltages of each stage capacitor were equal. In the second and fourth intervals in the boost mode, the inductors L_1 and L_2 transferred charge 4q to SCC, as shown in Figure 7; conversely, in the buck mode, the inductors L_1 and L_2 received charge 4q from the SCC, as shown in Figure 8.

Figures 9 and 10 show the voltages of SCC in boost and buck modes, respectively. The left part shows ideal voltages, and the right part shows non-ideal ones.

Ideally, when capacitors are large enough, the voltages of SCC in boost and buck modes are as shown in the left part of Figures 10 and 11, respectively. The blue line segments are the drain terminal voltages (V_1, V_3, V_5, V_7) of the odd-numbered switches; the light blue line segment shows the voltage V_{DS2}; the red line segments are the drain terminal voltages of the even-numbered switches (V_2, V_4, V_6, V_8); the light red line segment is the voltage V_{DS1}; the orange line segment represents the high-side voltage; the green line segment represents the low-side voltage.

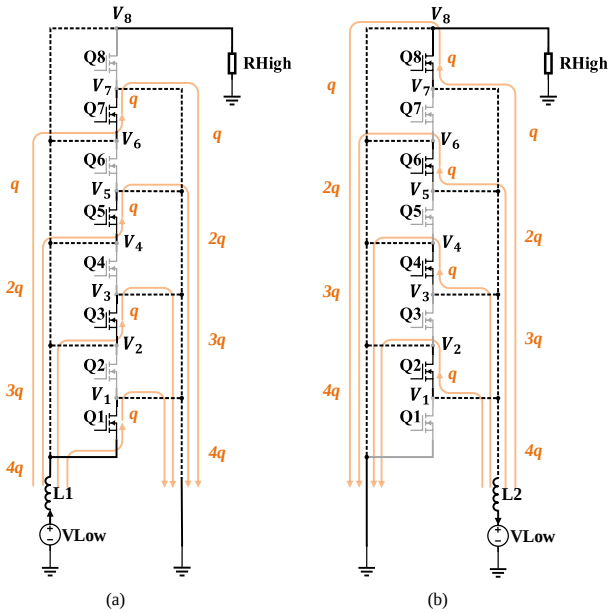

Figure 7. Charge flow in boost mode: (**a**) second interval; (**b**) fourth interval.

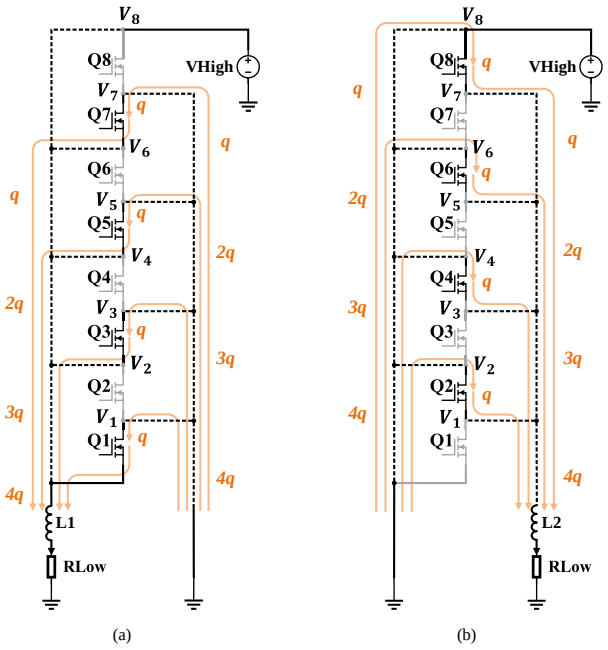

Figure 8. Charge flow in buck mode: (**a**) second interval; (**b**) fourth interval.

Observing the left parts of Figures 10 and 11, one can see that the voltages of SCC in boost and buck modes are ideally the same, and the voltage conversion ratios are also the same. The peak-to-peak amplitudes of V_1, V_3, V_5, and V_7 are equal to the peak-to-peak amplitude of V_{DS2}. Except the fourth interval, one sees that S_2 is short to ground; V_1, V_3, V_5, and V_7 remain stable without ripples; and the peak-to-peak voltages V_2, V_4, V_6, and V_8 are equal the peak-to-peak of V_{DS1}. On the contrary, except for the second interval, one sees S_1 is short to ground, and voltages V_2, V_4, V_6, and V_8 remain stable without ripples.

In the ideal case of infinite capacitors, the voltages of Cockcroft–Walton or Dickson SCCs will be the same as those of the hybrid.

In fact, the capacitor is finite. In this case, the flow of charge will cause ripples at both ends of the capacitor, making V_1 to V_8 have ripples. In addition, V_{DS1} in the second interval

and V_{DS2} in the fourth interval will not be ideal. These will make the output voltage of the SCC-based converter deviate from the ideal.

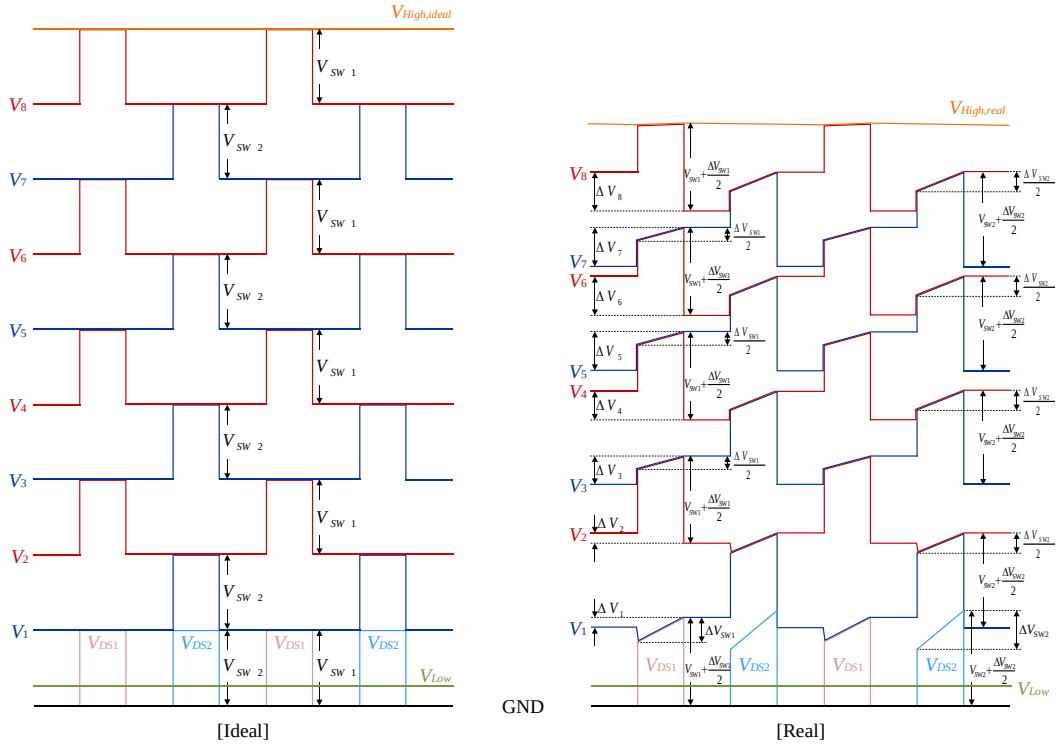

Figure 9. The ideal and actual waveforms of the circuit in boost mode.

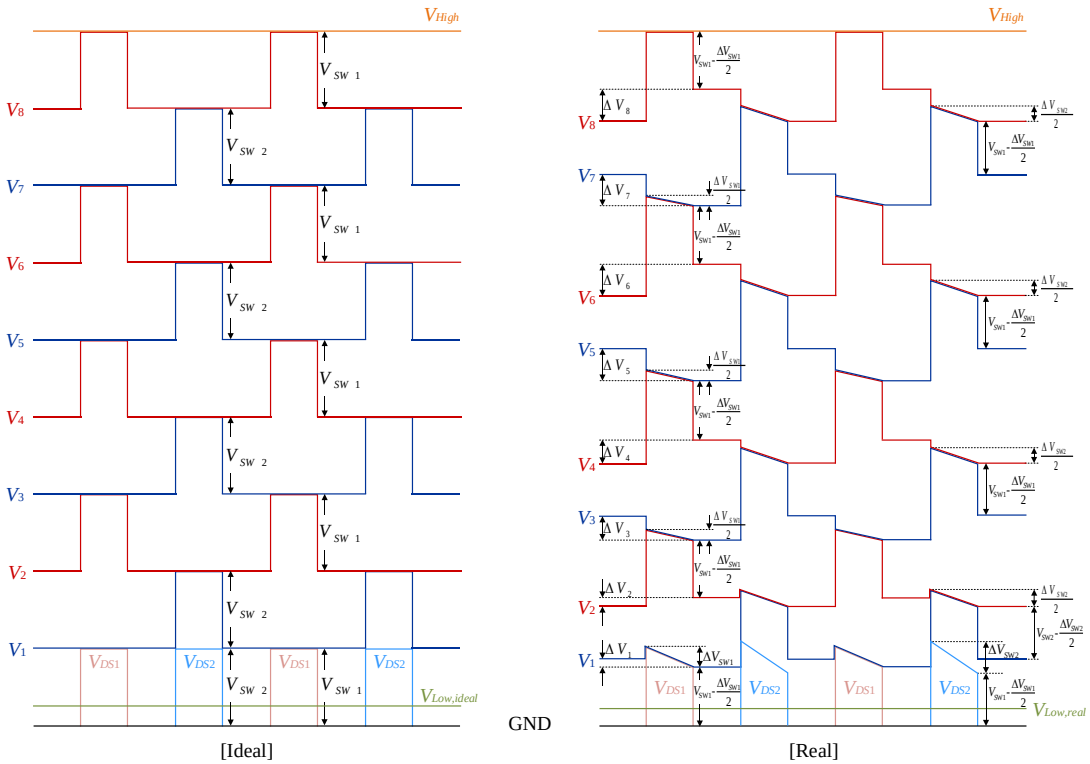

Figure 10. The ideal and actual waveforms of the circuit in buck mode.

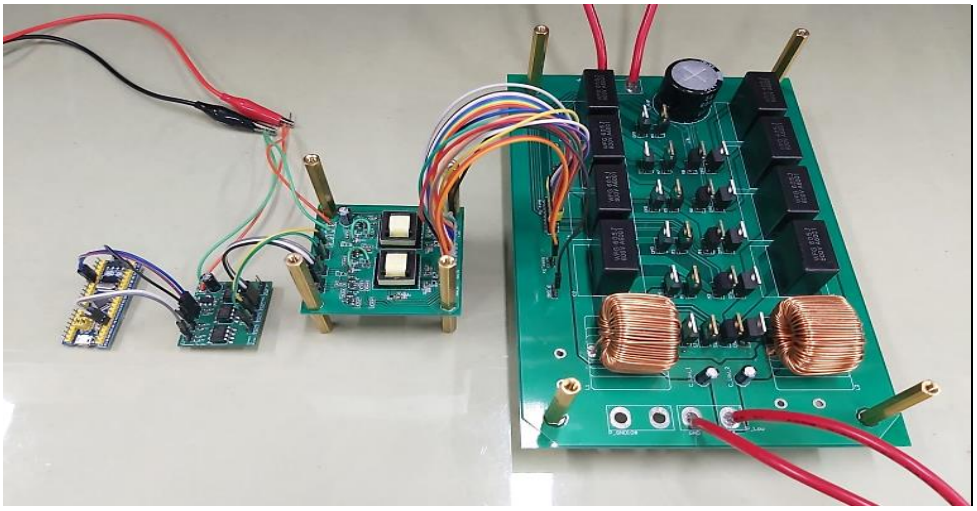

Figure 11. The experimental system.

We defined the ripple voltages on V_i, i = 1, 2. . . 8 as ΔV_i; the average voltage of V_{DS1} in the second switching interval as V_{SW1}; and ΔV_{SW1} as the difference between the minimum and maximum voltages of V_{DS1} in the second interval. Furthermore, the average of V_{DS2} in the fourth switching interval was V_{SW2}, and ΔV_{SW2} was the difference between the maximum and minimum voltages of V_{DS2} in the fourth interval. These definitions are applicable to both boost and buck modes.

If the capacitors are finite in reality, the voltages of the converter in the boost mode are as shown in the right part of Figure 10. It can be observed that V_1 is expressed as $V_{SW1} + \frac{\Delta V_{SW1}}{2}$ and is built on the lowest potential ΔV_1 of V_1; moreover, V_2 is expressed as $V_{SW2} + \frac{\Delta V_{SW2}}{2}$ and is built on the lowest potential ΔV_2 of V_2, and so on. In the boost mode, although ΔV_{SW1} and ΔV_{SW2} increase the output voltage slightly, the sum of the ripple voltages from ΔV_1 to ΔV_8 is much larger than $\left(\frac{\Delta V_{SW1}}{2} + \frac{\Delta V_{SW2}}{2}\right) \times 4$; therefore, the final output voltage will be lower than the ideal one.

On the contrary, when the converter operates in the buck mode with limited capacitance, the voltages are as shown in the right part of Figure 10. Similar to the boost mode, the difference is V_i, i = 1,2,. . . 8, is expressed as $V_{SWi} - \frac{\Delta V_{SWi}}{2}$, and is built on the highest potential ΔV_i of V_i. One can see the sum of ΔV_1 to ΔV_8 in the boost mode is much larger than $\left(\frac{\Delta V_{SW1}}{2} + \frac{\Delta V_{SW2}}{2}\right) \times 4$; however, in the buck mode, the sum of ΔV_1 to ΔV_8 will only be slightly larger than $\left(\frac{\Delta V_{SW1}}{2} + \frac{\Delta V_{SW2}}{2}\right) \times 4$. Therefore, the final output voltage will be slightly lower than the ideal output voltage.

When considering the case of finite capacitance, the voltages of the converter with Cockcroft–Walton or Dickson SCCs are similar to those of hybrid. The main difference lies in the ripple caused by their different structures of SCCs. The performance differences caused by the three different structures are discussed later.

3. Voltage Conversion Ratio

3.1. Ideal Case

When the circuit operates in modes I and III, S_1 is turned on, and the voltage of L_1 is equal to the low-side V_L. When the circuit operates in mode II, S_1 is turned off; the odd-numbered switches are turned on. In this case, the even-numbered switches are turned off, and the voltage of L_1 is equal to the difference between the low-side V_L and the voltage of C_1. From the volt-second balance of the inductance L_1, one has

$$V_L D_1 T_S + (V_L - V_{C1})(1 - D_1) T_S = 0 \tag{2a}$$

or

$$V_{C1} = \frac{V_L}{(1 - D_1)} \tag{2b}$$

Similarly, when the circuit operates in mode I and II, the switch S_2 is turned on, and the voltage of the inductor L_2 is equal to the low-side V_L; when the circuit operates in mode III, S_2 is turned off, and the odd-numbered switches are turned off, and the even-numbered switches are turned on. Thus, (3) can be derived from the volt-second balance of L_2.

$$V_L D_2 T_S + (V_L + V_{C1} - V_{C2})(1 - D_2) T_S = 0 \tag{3a}$$

or

$$V_{C2} - V_{C1} = \frac{V_L}{(1 - D_2)} \tag{3b}$$

According to Kirchhoff's voltage law, in mode II, the capacitor voltage is expressed as (4), which is also the voltage stress on S_1 in the second switching interval.

$$\begin{array}{c} V_{C1} = V_{C3} - V_{C2} = V_{C3} + V_{C5} - V_{C4} \\ = V_{C3} + V_{C7} - V_{C4} - V_{C6} \\ = V_H - V_{C4} - V_{C8} = \frac{V_L}{(1 - D_1)} \end{array} \tag{4}$$

In mode III, the capacitor voltage is expressed as (5).

$$\begin{array}{c} V_{C2} - V_{C1} = V_{C4} - V_{C3} = V_{C4} + V_{C6} - V_{C5} - V_{C3} \\ = V_{C4} + V_{C8} - V_{C7} - V_{C3} = \frac{V_L}{(1 - D_2)} \end{array} \tag{5}$$

Similarly, this voltage is also the voltage stress on S_2 in the fourth switching interval. From (4) and (5), the following capacitor voltages can be obtained:

$$V_{C1} = \frac{V_L}{(1 - D_1)} \tag{6a}$$

$$V_{C2} = V_{C5} = V_{C6} = \frac{V_L}{(1 - D_1)} + \frac{V_L}{(1 - D_2)} \tag{6b}$$

$$V_{C3} = \frac{2V_L}{(1 - D_1)} + \frac{V_L}{(1 - D_2)} \tag{6c}$$

$$V_{C4} = V_{C7} = V_{C8} = \frac{2V_L}{(1 - D_1)} + \frac{2V_L}{(1 - D_2)} \tag{6d}$$

Now, substituting (6) into (4) gives the voltage conversion ratio between the high-side V_H and the low-side V_L as

$$V_H = \frac{5V_L}{(1 - D_1)} + \frac{4V_L}{(1 - D_2)} \tag{7}$$

Similarly, it can be extended to converters with N-stage SCC. For odd or even N, the voltage conversion ratio is shown in (8) or (9).

$N = odd\ number$:

$$V_H = \frac{(N+1)}{2} \cdot \frac{V_L}{(1 - D_1)} + \frac{(N+1)}{2} \cdot \frac{V_L}{(1 - D_2)} \tag{8}$$

$N = even\ number$:

$$V_H = \frac{(N+2)}{2} \cdot \frac{V_L}{(1 - D_1)} + \frac{(N)}{2} \cdot \frac{V_L}{(1 - D_2)} \tag{9}$$

If $D_1 = D_2 = D$, one has

$$V_H = (N+1) \cdot \frac{V_L}{(1-D)} \tag{10}$$

The ideal voltage conversion ratios (8)–(10) are also applicable to converters with Cockcroft–Walton or Dickson SCCs. However, in a real case, SCCs with different structures result in different impedance and ripple; therefore, these differences cause different voltage drops on the output voltage, and capacitor voltage stresses are expected.

3.2. Actual Case

The IC designs are where the bottom stray capacitors are used as charge pumping elements [15]. The stray capacitors lead to a significant reduction of the power conversion efficiency [16]. Furthermore, as the word line (WL) capacitance increases, the CP area would have to increase to keep the WL rise time unchanged, which would result in larger silicon arca and higher power [17]. However, in the application of the power system case, the parasitic capacitors are much smaller than the pumping ones. To simplify the analysis, the parasitic capacitors on the power system are ignored.

3.2.1. Ripple Voltage ΔV

The charge q stored in the capacitor is proportional to its potential V_C as

$$V_C = \frac{q}{C} \tag{11}$$

Substituting (1) into (11), one obtains

$$V_C = \frac{\langle I_H \rangle}{CF_{sw}} \tag{12}$$

It should be noted that when (1) and (12) are used to calculate the capacitor ripple voltage in boost mode, $\langle I_H \rangle$ is the average current of the high-side load. However, when (1) and (12) are used to calculate the capacitor ripple voltage in the buck mode, because the loss in the buck mode is relatively large, $\langle I_H \rangle$ needs to take the average current of the low-side load, and the output current of the high-side is calculated backward through the voltage conversion ratio.

Defining ΔV of N-stage converter as the sum from ΔV_1 to ΔV_N, one has (13).

$$\Delta V = \sum_{m=1}^{N} \Delta V_m \tag{13}$$

Therefore, the ΔV of an eight-stage SCC is shown as

$$\begin{aligned} \Delta V &= \Delta V_1 + \Delta V_2 + \Delta V_3 + \Delta V_4 + \Delta V_5 + \Delta V_6 + \Delta V_7 + \Delta V_8 \\ &= \sum_{m=1}^{8} \Delta V_m \end{aligned} \tag{14}$$

According to Figure 6, and the charge flow diagrams shown in Figures 7 and 8, the ripple voltages on V_1 to V_8 can, respectively, be ΔV_1 to ΔV_8. Table 1 shows the ripple voltages of the eighth-stage Cockcroft–Walton, Dickson, and hybrid switched capacitor circuits [18].

Table 1. Ripple voltages of Cockcroft–Walton, Dickson, and the hybrid.

ΔV_N	Cockcroft–Walton	Dickson	Hybrid
ΔV_1	$\frac{4q}{C}$	$\frac{q}{C}$	$\frac{q}{C}$
ΔV_2	$\frac{4q}{C}$	$\frac{q}{C}$	$\frac{q}{C}$
ΔV_3	$\frac{4q}{C} + \frac{3q}{C}$	$\frac{q}{C}$	$\frac{3q}{C}$
ΔV_4	$\frac{4q}{C} + \frac{3q}{C}$	$\frac{q}{C}$	$\frac{3q}{C}$
ΔV_5	$\frac{4q}{C} + \frac{3q}{C} + \frac{2q}{C}$	$\frac{q}{C}$	$\frac{3q}{C} + \frac{q}{C}$
ΔV_6	$\frac{4q}{C} + \frac{3q}{C} + \frac{2q}{C}$	$\frac{q}{C}$	$\frac{3q}{C} + \frac{q}{C}$
ΔV_7	$\frac{4q}{C} + \frac{3q}{C} + \frac{2q}{C} + \frac{q}{C}$	$\frac{q}{C}$	$\frac{3q}{C} + \frac{q}{C}$
ΔV_8	$\frac{4q}{C} + \frac{3q}{C} + \frac{2q}{C} + \frac{q}{C}$	$\frac{q}{C}$	$\frac{3q}{C} + \frac{q}{C}$
ΔV	$\frac{60q}{C}$	$\frac{8q}{C}$	$\frac{24q}{C}$

For a converter with a Cockcroft–Walton, when N is odd, the sum of its ripple voltage is as (15), and when N is even, the sum of its ripple voltage is as (16).

$N = odd\ number$:

$$\Delta V_{Cockcroft} = \frac{q}{C}\left[\left(\sum_{m=0}^{\frac{N+1}{2}-1}\left(\frac{N+1}{2} - m\right)^2\right) + \left(\sum_{m=0}^{\frac{N-1}{2}-1}\left(\frac{N-1}{2} - m\right)^2\right)\right] \tag{15}$$

$N = even\ number$:

$$\Delta V_{Cockcroft} = \frac{2q}{C} \cdot \sum_{m=0}^{\frac{N}{2}-1}\left(\frac{N}{2} - m\right)^2 \tag{16}$$

Note that (15) and (16) of the Cockcroft–Walton SCC are only applicable to N $\geq$ 2. If N = 1, $\Delta V_{Cockcroft} = \frac{q}{C}$.

For converters with Dickson SCC, whether N is odd or even, the sum of the ripple voltage $\Delta V_{Dickson}$ is invariant as (17).

$$\Delta V_{Dickson} = \frac{Nq}{C} \tag{17}$$

For converters with the hybrid SCC, the sum of its ripple voltage is different for odd or even N,

$N = odd\ number$:

$$\Delta V_{Hybrid} = \frac{q}{C}\left[\left(\sum_{m=2}^{\frac{N-1}{2}} m^2\right) + \left(\frac{N+1}{2} + 1\right)\right] \tag{18}$$

$N = even\ number$:

$$\Delta V_{Hybrid} = \frac{2q}{C}\left[\left(\sum_{m=0}^{\lfloor \frac{N}{4} \rfloor - 1}\left(\frac{N-2-4m}{2}\right)^2\right) + \left(\left\lfloor \frac{N}{4} \right\rfloor + 1\right)\right] \tag{19}$$

In (19), $\lfloor\ \rfloor$ represents the largest integer not greater than x. Moreover, (18) and (19) of the hybrid SCC are only applicable to $N \geq 5$. If $N \leq 4$, $\Delta V_{Hybrid} = \frac{Nq}{C}$.

3.2.2. Ripple Voltages ΔV_{SW1} and ΔV_{SW2}

The ΔV_{SW1} and ΔV_{SW2} in the boost and buck modes are the same as

$$\Delta V_{SW1} = \frac{\langle I_{L1} \rangle \cdot (1 - D_1)}{2CF_{sw}} \tag{20}$$

$$\Delta V_{SW2} = \frac{\langle I_{L2} \rangle \cdot (1 - D_2)}{CF_{sw}} \tag{21}$$

where $\langle I_{L1} \rangle$ and $\langle I_{L2} \rangle$ are the average values of I_{L1} and I_{L2}, respectively.

3.2.3. Actual Voltage Conversion Ratio in Boost Mode

From the actual voltages of the converter with an eight-stage SCC in the right part of Figure 9, one obtains

$$V_H = 5\left(V_{SW1} + \frac{\Delta V_{SW1}}{2}\right) + 4\left(V_{SW2} + \frac{\Delta V_{SW2}}{2}\right) - \Delta V \tag{22}$$

where V_{SW1} and V_{SW1} can be obtained from the volt-second balance of L_1 and L_2, respectively; ΔV_{SW1} and ΔV_{SW2} are given in (20) and (21); and ΔV can be calculated through (15) to (19). Consequently, the actual voltage conversion ratio in boost mode can be

$$V_H = 5\left(\frac{V_L}{(1 - D_1)} + \frac{\langle I_{L1} \rangle \cdot (1 - D_1)}{4CF_{sw}}\right) + 4\left(\frac{V_L}{(1 - D_2)} + \frac{\langle I_{L2} \rangle \cdot (1 - D_2)}{2CF_{sw}}\right) - \Delta V \tag{23}$$

Similarly, the voltage conversion ratios, for the odd and even stage N, are shown in (24) and (25), respectively.

$N = odd\ number$:

$$V_H = \frac{(N+1)}{2} \cdot \left(\frac{V_L}{(1 - D_1)} + \frac{\langle I_{L1} \rangle \cdot (1 - D_1)}{4CF_{sw}}\right) + \frac{(N+1)}{2} \cdot \left(\frac{V_L}{(1 - D_2)} + \frac{\langle I_{L2} \rangle \cdot (1 - D_2)}{2CF_{sw}}\right) - \Delta V \tag{24}$$

$N = even\ number$:

$$V_H = \frac{(N+2)}{2} \cdot \left(\frac{V_L}{(1 - D_1)} + \frac{\langle I_{L1} \rangle \cdot (1 - D_1)}{4CF_{sw}}\right) + \frac{(N)}{2} \cdot \left(\frac{V_L}{(1 - D_2)} + \frac{\langle I_{L2} \rangle \cdot (1 - D_2)}{2CF_{sw}}\right) - \Delta V \tag{25}$$

The derivation of the actual voltage conversion ratio in boost mode is also applicable to converters with Cockcroft–Walton, Dickson, or hybrid switching capacitor circuits. However, because the ΔV of the three are quite different, as shown in Table 1, one can see that V_{SW1}, V_{SW2}, ΔV_{SW1}, and ΔV_{SW2} are also different. Therefore, the actual output voltages of the three are different.

3.2.4. Actual Voltage Conversion Ratio in Buck Mode

Observing the actual voltages in the right part of Figure 10, one obtains

$$V_H + 5\left(\frac{\Delta V_{SW1}}{2}\right) + 4\left(\frac{\Delta V_{SW2}}{2}\right) - \Delta V = 5V_{SW1} + 4V_{SW2} \tag{26}$$

Note that

$$\frac{V_{SW1}}{V_{SW2}} = \frac{(1 - D_2)}{(1 - D_1)} \tag{27}$$

Therefore, substituting (27) into (26) gives

$$V_H + 5\left(\frac{\Delta V_{SW1}}{2}\right) + 4\left(\frac{\Delta V_{SW2}}{2}\right) - \Delta V = 5V_{SW1} + 4 \cdot \frac{(1 - D_1)}{(1 - D_2)} \cdot V_{SW1} = 5 \cdot \frac{(1 - D_2)}{(1 - D_1)} \cdot V_{SW2} + 4V_{SW2} \tag{28}$$

It is noticed that the non-ideal V_{SW1} and V_{SW2} are used in the buck mode to obtain

$$V_H + 5\left(\frac{\langle I_{L1}\rangle \cdot (1-D_1)}{4CF_{sw}}\right) + 4\left(\frac{\langle I_{L2}\rangle \cdot (1-D_2)}{2CF_{sw}}\right) - \Delta V = 5V_{SW1} + 4 \cdot \frac{(1-D_1)}{(1-D_2)} \cdot V_{SW1} = 5 \cdot \frac{(1-D_2)}{(1-D_1)} \cdot V_{SW2} + 4V_{SW2} \quad (29)$$

Next, one uses V_{SW1} and V_{SW2} to calculate the actual voltage conversion ratio of the converter with an eight-stage switched capacitor circuit in the buck mode as

$$V_L = V_{SW1} \cdot (1-D_1) = V_{SW2} \cdot (1-D_2) \quad (30)$$

Similarly, when the stage number N is odd or even, the voltage conversion ratio can be

$N = odd\ number$:

$$V_H + \frac{(N+1)}{2} \cdot \left(\frac{\Delta V_{SW1}}{2}\right) + \frac{(N+1)}{2} \cdot \left(\frac{\Delta V_{SW2}}{2}\right) - \Delta V = \frac{(N+1)}{2} \cdot V_{SW1} + \frac{(N+1)}{2} \cdot V_{SW2} \quad (31)$$

$N = even\ number$:

$$V_H + \frac{(N+2)}{2} \cdot \left(\frac{\Delta V_{SW1}}{2}\right) + \frac{(N)}{2} \cdot \left(\frac{\Delta V_{SW2}}{2}\right) - \Delta V = \frac{(N+2)}{2} \cdot V_{SW1} + \frac{(N)}{2} \cdot V_{SW2} \quad (32)$$

The actual voltage conversion ratio in buck mode is also applicable to converters with Cockcroft–Walton, Dickson, and hybrid switching capacitor circuits. Since the ΔV, ΔV_{SW1}, and ΔV_{SW2} of the three are different, the actual output voltages of three are also different.

3.3. Capacitor Voltage Stress and Stored Energy

The choice of capacitor depends on the energy it needs to store. This affects the circuit size and cost of the converter.

Here, the voltage stress of the capacitor and the energy stored in it will be discussed. It is assumed here that the switched capacitor circuit is ideal, ignoring the ripple of the capacitor, and every odd stage of the switched capacitor circuit equally generates the voltage V_{SW2}, and each even stage also equally generates the voltage V_{SW1}.

Let N be the total stage of the switched capacitor circuit and n be the n-th stage on the N-stage circuit. Note that the voltage stress of the capacitor varies in accordance with the SCC structure and the stage n where it is located.

In the Cockcroft–Walton converter, the high-voltage side voltage will be equally shared by the capacitors of each stage. Therefore, the capacitor voltage stress of the Cockcroft–Walton circuit will not increase with the superposition of the stages. The capacitor voltage stress $V_{Cn,C-W}$ and the maximum capacitor voltage stress $V_{C,max,C-W}$ of the n-th stage of the Cockcroft–Walton are given as

$$V_{Cn,C-W} = V_{SW1} + V_{SW2} \quad (33)$$

$$V_{C,max,C-W} = V_{SW1} + V_{SW2} \quad (34)$$

The capacitors on the Dickson circuit are connected in parallel. Therefore, when the stage is increased, the voltage stress of each capacitor increases. The capacitor voltage stress $V_{Cn,D}$ of the n-th stage of the Dickson switched capacitor circuit for odd n and even n are shown in (35) and (36), respectively.

$n = odd\ number$:

$$V_{Cn,D} = \left(\frac{n+1}{2}\right) \cdot V_{SW1} + \left(\frac{n-1}{2}\right) \cdot V_{SW2} \quad (35)$$

$n = even\ number$:

$$V_{Cn,D} = \left(\frac{n}{2}\right) \cdot (V_{SW1} + V_{SW2}) \quad (36)$$

Because the maximum capacitor voltage stress $V_{C,max,D}$ on the Dickson on the last-stage capacitor, we replaced n in the $V_{Cn,D}$ with N. One has the maximum capacitor voltage stress of the Dickson circuit as

$N = odd\ number$:

$$V_{C,max,D} = \left(\frac{N+1}{2}\right) \cdot V_{SW1} + \left(\frac{N-1}{2}\right) \cdot V_{SW2} \tag{37}$$

$N = even\ number$:

$$V_{C,max,D} = \left(\frac{N}{2}\right) \cdot (V_{SW1} + V_{SW2}) \tag{38}$$

However, the hybrid switched capacitor circuit mixes the structures of Cockcroft–Walton and Dickson switched capacitor circuits. Although the capacitor voltage stress of the hybrid circuit is not as low as that of the Cockcroft–Walton circuit, the hybrid circuit can limit the voltage stress of the capacitor in a certain value without increasing infinitely like the Dickson circuit. This is the main advantage of the hybrid circuit.

To obtain the capacitor voltage stress $V_{Cn,H}$ of the n-th stage of the hybrid switched capacitor circuit, one first uses (39) to obtain the constant m, where Mod is the remainder operation, that is, dividing the two numbers; if $m = 1, 2$, one has $V_{Cn,H}$ as (40), and if $m = 0, 3$, one gets $V_{Cn,H}$ as (41).

$$m = nMod4 \tag{39}$$

$$m = 1, 2:\ V_{Cn,H} = V_{SW1} + V_{SW2} \tag{40}$$

$$m = 0, 3:\ V_{Cn,H} = 2V_{SW1} + 2V_{SW2} \tag{41}$$

The maximum capacitor voltage stress $V_{C,max,H}$ of the hybrid switched capacitor circuit is limited in a certain value, as shown in (42).

$$V_{C,max,H} = 2V_{SW1} + 2V_{SW2} \tag{42}$$

The capacitor voltage stress equations (41) to (43) of the hybrid circuit are only applicable to $n \geq 4$. If $n < 4$, the n-th stage capacitor voltage stress and the maximum capacitor voltage stress are the same as the Dickson switched capacitor circuit.

This study has obtained the voltage stress of each capacitor on the converter with eight-stage Cockcroft–Walton, Dickson, and hybrid switched capacitor circuits, as listed in Table 2. In it, the voltage $V_{C,sum}$ is the sum of voltages from V_{C1} to V_{C8}.

Table 2. Capacitor voltage stress of Cockcroft–Walton, Dickson, and hybrid SCCs.

V_{Cn}	Cockcroft–Walton	Dickson	Hybrid
V_{C1}	V_{SW1}	V_{SW1}	V_{SW1}
V_{C2}	$V_{SW1} + V_{SW2}$	$V_{SW1} + V_{SW2}$	$V_{SW1} + V_{SW2}$
V_{C3}	$V_{SW1} + V_{SW2}$	$2V_{SW1} + V_{SW2}$	$2V_{SW1} + V_{SW2}$
V_{C4}	$V_{SW1} + V_{SW2}$	$2V_{SW1} + 2V_{SW2}$	$2V_{SW1} + 2V_{SW2}$
V_{C5}	$V_{SW1} + V_{SW2}$	$3V_{SW1} + 2V_{SW2}$	$V_{SW1} + V_{SW2}$
V_{C6}	$V_{SW1} + V_{SW2}$	$3V_{SW1} + 3V_{SW2}$	$V_{SW1} + V_{SW2}$
V_{C7}	$V_{SW1} + V_{SW2}$	$4V_{SW1} + 3V_{SW2}$	$2V_{SW1} + 2V_{SW2}$
V_{C8}	$V_{SW1} + V_{SW2}$	$4V_{SW1} + 4V_{SW2}$	$2V_{SW1} + 2V_{SW2}$
$V_{C,max}$	$V_{SW1} + V_{SW2}$	$4V_{SW1} + 4V_{SW2}$	$2V_{SW1} + 2V_{SW2}$
$V_{C,sum}$	$8V_{SW1} + 7V_{SW2}$	$20V_{SW1} + 16V_{SW2}$	$12V_{SW1} + 10V_{SW2}$

The energy stored in a capacitor, denoted as E_C, depends on its capacitance and voltage stress.

$$E_C = \frac{1}{2} C V_C^2 \tag{43}$$

The total amount of capacitor energy for Cockcroft–Walton, Dickson, and hybrid switching capacitor circuits are denoted as $E_{C,C-W}$, $E_{C,D}$, and $E_{C,H}$, respectively, given as

$$E_{C,C-W} = \frac{1}{2}C\left[8V_{SW1}^2 + 7V_{SW2}^2 + 14V_{SW1}V_{SW2}\right] \quad (44)$$

$$E_{C,D} = \frac{1}{2}C\left[60V_{SW1}^2 + 44V_{SW2}^2 + 100V_{SW1}V_{SW2}\right] \quad (45)$$

and

$$E_{C,H} = \frac{1}{2}C\left[20V_{SW1}^2 + 16V_{SW2}^2 + 34V_{SW1}V_{SW2}\right] \quad (46)$$

Observing (45)~(47), one sees the total capacitance energy of the Dickson SCC as the greatest. This becomes a disadvantage of the Dickson SCC in converter applications.

4. Experimental Results

The converter circuit proposed in this paper is suitable for battery-powered equipment, such as portable high-voltage antibacterial modules. The antibacterial modules require miniaturization and a high voltage conversion ratio, and these must be able to charge and discharge the battery. Using a bidirectional power supply system can effectively reduce the size of the portable module.

To verify the feasibility of the proposed method, a bidirectional two interlaced converter with an eight-stage hybrid switched capacitor circuit was implemented, as shown in Figure 11. The hardware circuit was divided into two parts, namely, the drive circuit and the switched capacitor bidirectional converter circuit. Moreover, the micro-controller STM32F103 was used to generate the PWM switching control signal Qi that turns on and turns on the MOSFET.

The components used for the prototype of the proposed converter shown in Figure 1 are listed in Table 3.

Table 3. Component list for the experimental prototype.

Item	Reference	Rating	Part No.
Inductor	L1, L2	1 mH	—
MOSFET	S1, S2, QH, Q1~Q8	200 V, 56 A, Rdson = 40 mΩ	IRFB260NPBF Infineon
Capacitor	C1~C8	6 uF, 800 V	ECW-FG80605J Panasonic
Capacitor	CL	68 uF, 35 V	EEU-FR1V680 Panasonic
Capacitor	CH	56 uF, 600 V	LGN2X560MELB25 Nichicon

A. Boost mode

In the experiment, the low-side input voltage was set to 5 V; the duty cycle of switches S_1 and S_2 were both 75%; and the switching frequency was 10 KHz. In this case, the ideal output voltage was 180 V.

Figure 12 shows the currents of L_1 and L_2 and the gate control signals of S_1 and S_2. Figure 13 provides the drain-source voltages of S_1 and S_2 and their gate drive voltages.

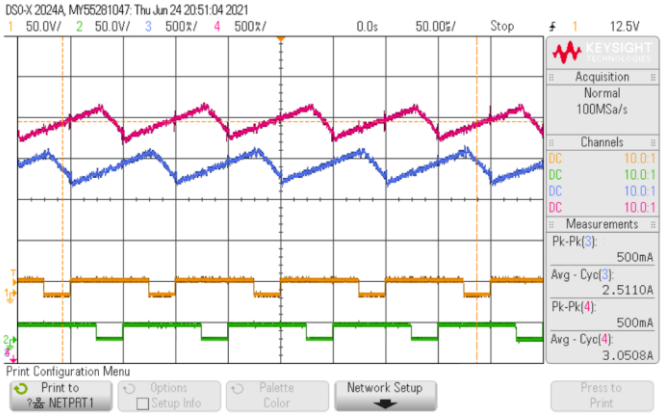

Figure 12. Currents of L_1 and L_2 in boost mode.

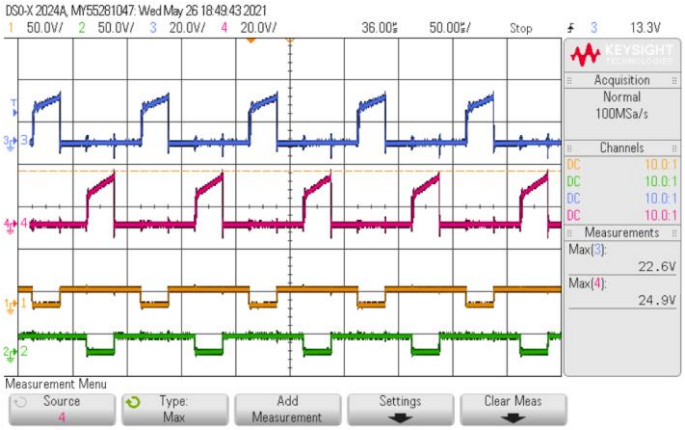

Figure 13. Drain-source voltage of S_1 and S_2 in boost mode.

Figures 14 and 15 show the node voltages V_1 to V_4 and V_5 to V_8, respectively. Observing the voltage waveforms of each stage, one can see the capacitor ripple on the output voltage.

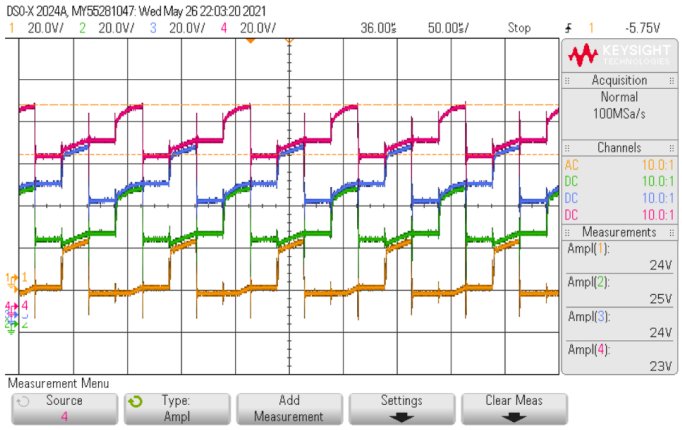

Figure 14. Node voltages V_1 to V_4 of the SCC in boost mode.

Figure 15. Node voltage V_5 to V_8 of the SCC in boost mode.

Figure 16 shows the efficiency of the converter in boost mode. When the output power was 3 W, the converter had the highest efficiency, which can reach 96.8%.

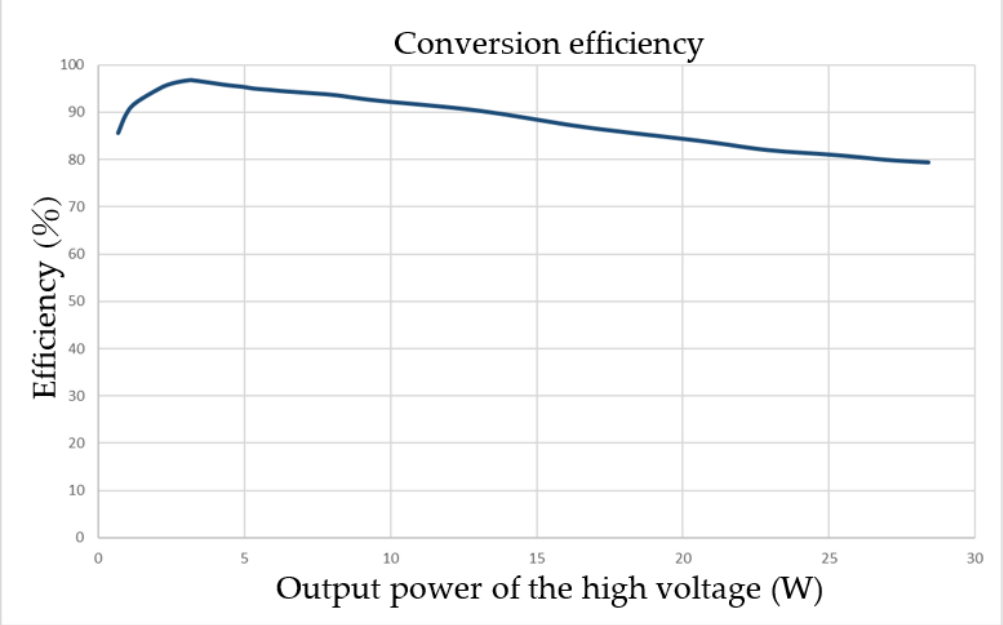

Figure 16. Converter efficiency in boost mode.

B. Buck mode

The following is the experimental results in buck mode. The input high-side voltage was 180 V; the duty cycle of switches S_1 and S_2 were both 75%; and the switching frequency was 10 KHz. The ideal output voltage here was 5 V.

Figure 17 shows the currents of L_1 and L_2 and the gate control signals of S_1 and S_2, respectively. Figure 18 provides the drain-source voltages of S_1 and S_2 and their respective gate drive voltages.

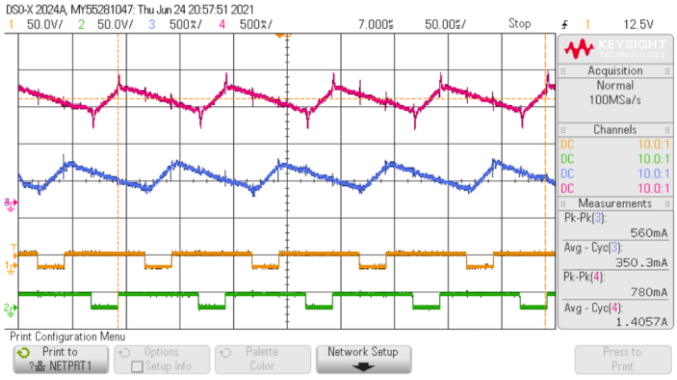

Figure 17. Currents of L_1 and L_2 in buck mode.

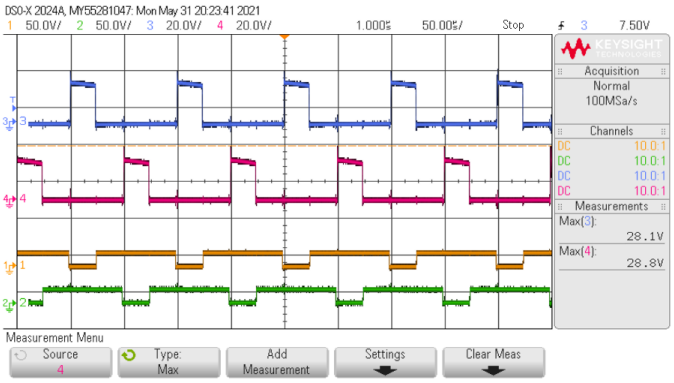

Figure 18. Drain-source voltages of S_1 and S_2 in buck mode.

Figures 19 and 20 show the node voltages V_1 to V_4, and V_5 to V_8, respectively.

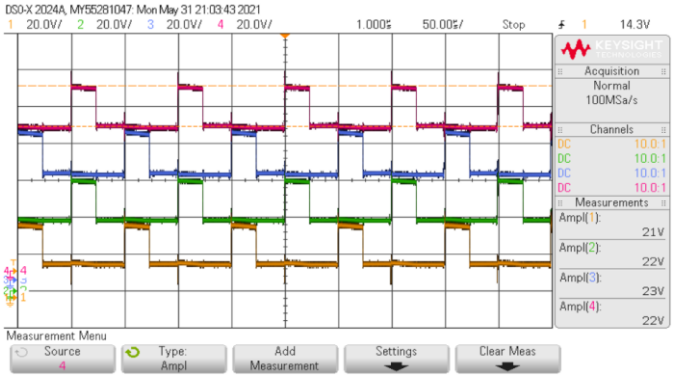

Figure 19. Node voltages V_1 to V_4 of SCC in buck mode.

Figure 21 shows the efficiency of the converter in buck mode. The converter had the highest efficiency of 88.4% when the input power was 6.76 W.

It can be seen from Figures 17–21 that the experimental results coincided with the theoretical results, as expected.

A summary of the three VM circuits is shown in Table 4. In it, three VM circuits were with an eight-stage voltage multiplier for feature comparison. Whether it was a Cockcroft–Walton, Dickson, or hybrid circuit, the MOSFET voltage stresses V_{S1} and V_{s2} of switches S_1 and S_2 were the same. Under the ideal condition, the MOSFET voltage stresses V_{Qx} of all the switches, Q_1 to Q_8 and Q_H, will be the same too.

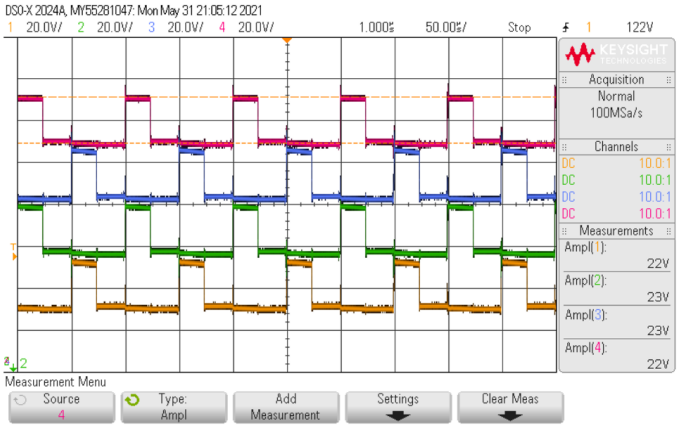

Figure 20. Node voltages V_5 to V_8 of SCC in buck mode.

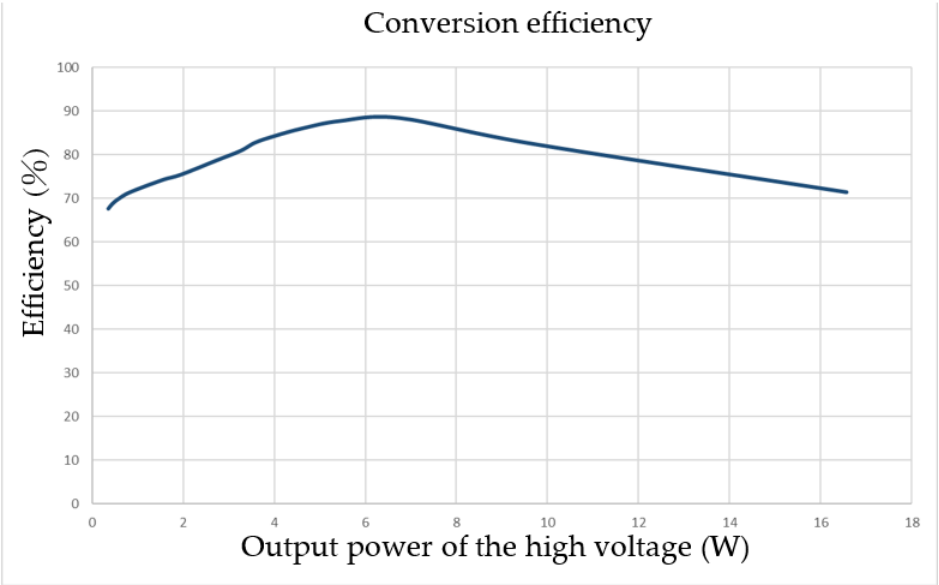

Figure 21. Converter efficiency in buck mode.

Table 4. Feature comparison.

Voltage Multiplier	Cockcroft–Walton	Dickson	Hybrid
Voltage gain	$V_H = (N+1) \cdot \frac{V_L}{(1-D)}$	$V_H = (N+1) \cdot \frac{V_L}{(1-D)}$	$V_H = (N+1) \cdot \frac{V_L}{(1-D)}$
V_{S1}	$V_{S1} = \frac{V_L}{(1-D_1)}$	$V_{S1} = \frac{V_L}{(1-D_1)}$	$V_{S1} = \frac{V_L}{(1-D_1)}$
V_{S2}	$V_{S2} = \frac{V_L}{(1-D_2)}$	$V_{S2} = \frac{V_L}{(1-D_2)}$	$V_{S2} = \frac{V_L}{(1-D_2)}$
V_{Qx}	$\frac{V_L}{(1-D_1)} + \frac{V_L}{(1-D_2)}$	$\frac{V_L}{(1-D_1)} + \frac{V_L}{(1-D_2)}$	$\frac{V_L}{(1-D_1)} + \frac{V_L}{(1-D_2)}$
$V_{C,max}$	$V_{SW1} + V_{SW2}$	$4V_{SW1} + 4V_{SW2}$	$2V_{SW1} + 2V_{SW2}$
$V_{C,sum}$	$8V_{SW1} + 7V_{SW2}$	$20V_{SW1} + 16V_{SW2}$	$12V_{SW1} + 10V_{SW2}$
ΔV	$\frac{60q}{C}$	$\frac{8q}{C}$	$\frac{24q}{C}$

The maximum capacitor voltage stress $V_{C,max}$ and the sum of capacitor voltages $V_{C,sum}$ of the Cockcroft–Walton, Dickson, and hybrid switched capacitor circuits were Dickson > Hybrid > Cockcroft–Walton. In addition, the sum of the ripple voltage ΔV of the proposed converter were compared with several SCCs, and then the result was $\Delta V_{Cockcroft} > \Delta V_{Hybrid} > \Delta V_{Dickson}$. However, the hybrid switched capacitor circuit mixed

the structures of the Cockcroft–Walton and Dickson switched capacitor circuits, and the characteristics of the proposed converter showed a similar intermediate performance.

5. Conclusions

The drawback of the interleaved converter with the Cockcroft–Walton switched capacitor circuit is that its circuit impedance and ripple will cause a serious output voltage drop. Although one uses the Dickson SCC instead to improve the output voltage performance, its capacitor will be subjected to high voltage stress, which requires extremely high voltage capacitors.

This study combined the interleaved converter with the hybrid switched capacitor circuit. Its capacitor voltage can be limited to a certain value. No matter how the stage of the hybrid switched capacitor circuit increases, there is no need to increase the voltage stress of the capacitor, as is the case in the Dickson SCC. Thus, the capacitors of the proposed method can use lower voltage stress than those of the Dickson SCC. In addition, the circuit ripple and impedance of the proposed method were much lower than the Cockcroft–Walton switched capacitor circuit, resulting in better output voltage performance. Therefore, compared with interleaved converters combined with Cockcroft–Walton and Dickson SCCs, the proposed converter is more competitive in high-stage and high-voltage applications.

Moreover, those interleaved converters with Cockcroft–Walton or Dickson SCC had only the voltage boost function. Thus, the proposed converter has the boost and buck advantage of bidirectional power transmission function, compared with those converters with Cockcroft–Walton or Dickson switched capacitor circuits.

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