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Research on Five-Level PFC Circuit Topology Based on Switch-Diode-Capacitor Network

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Abstract: In this paper, a family of a novel single-phase three-level PFC based on a switch-capacitor cell is proposed. The proposed PFC topologies have the characteristics of high power factor, low voltage stresses, and low power losses. Firstly, the derivation process of the novel PFC topologies is introduced in detail. Based on a representative circuit of the proposed novel PFC topologies, its operation principle is analyzed from the aspects of working current paths, key waveforms, and pulse distribution. Meanwhile, its equivalent circuit model is deduced. Secondly, the performance of the proposed PFC topologies is analyzed. Then the modulation technology based on capacitor voltage balancing is designed for the proposed topologies. Finally, an experimental prototype with a rated power of 800 W and a DC output voltage of 400 V is built. The experimental analysis is carried out from both the steady state and dynamic state. The experimental results verify the feasibility of the proposed novel three-level PFC topologies and the effectiveness of the modulation technology.

Keywords: three-level topology; power factor correction; single-phase rectifier; switch-capacitor cell

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1. Introduction

International standards such as IEEE 519, IEC 100-3-2, and IEC61000-3-2 put forward restrictions on harmonic currents injected into the power grid by rectifiers, especially for motor drives, lighting equipment, and special industrial products [1–3]. The common way to meet the requirements is to use active power factor correction (APFC) rectifiers for the advantages of high power factor, continuous input current, and high efficiency [4]. However, the semiconductor devices in conventional two-level APFC rectifiers withstand excessive voltage stresses, resulting in high switching losses. To improve the efficiency, a better method is to use multilevel technology [5]. It is well known that applying multilevel technology can reduce the voltage stresses of switching devices in PFC rectifiers and effectively reduce the filter size and weight [6–10].

In the relevant studies on the structures of the multilevel PFC topologies, many multilevel PFC topologies with remarkable features have been developed. A novel bridgeless three-level PFC topology is proposed in [11]. This topology replaces half of the controllable switches in the traditional three-level PFC with diodes, reducing the number of active switches and improving the performance of the converter. In [12], a five-level boost PFC rectifier using a reduced number of switches is developed, which remarkably reduces the size of the manufactured box and the current harmonics. In [13], a novel single-phase five-level PFC rectifier is proposed, which has fewer active switches, a simpler drive, and lower power losses compared to similar PFC rectifiers. In order to improve the efficiency and optimize the output performance, many scholars improve the performance of multilevel PFC topology mainly from the overall multi-objective optimization of the converter [14–16]. The above literature optimizes the existing PFC topologies to a certain extent and improves the performance and efficiency, but the original PFC topology structures are not changed substantially.

Based on the careful analysis and summary of the above multilevel PFC topologies, a family of novel single-phase three-level PFC topologies based on switch-capacitor cells are developed in this paper. The proposed topologies enrich the existing three-level PFC topology types and have the characteristics of a low number of active switches, low power losses, and high reliability. The organization of this paper is as follows. In Section 2, the derivation process and the operation principle of the proposed novel three-level PFC topologies are presented in detail. In Section 3, the voltage stresses of power devices are analyzed. Meanwhile, the calculation and comparison of the switching device losses are given. In Section 4, the modulation technology of the proposed PFC is presented. The detailed experimental validation is given in Section 5, and the conclusions are summarized in Section 6.

2. Topology Deduction and Operation Principle

2.1. Deduction Process of Novel PFC Topologies

The traditional three-level power factor correction circuit (TTL-PFC) shown in Figure 1a uses diodes to clamp the voltage of the corresponding active switches and ensures the bidirectional flow of current [17]. However, in the application of unidirectional power flow, the number of active switches is a significant disadvantage of this approach. As shown in Figure 1b, it is a unidirectional three-level power factor correction circuit (UTL-PFC), which reduces four active switches and improves the efficiency compared to the TTL-PFC topology [11]. Unfortunately, there are four modes that have two active switches conducting at the same time among all six operating modes of the UTL-PFC, which results in the disadvantages of excessive switching losses and complexity of control.

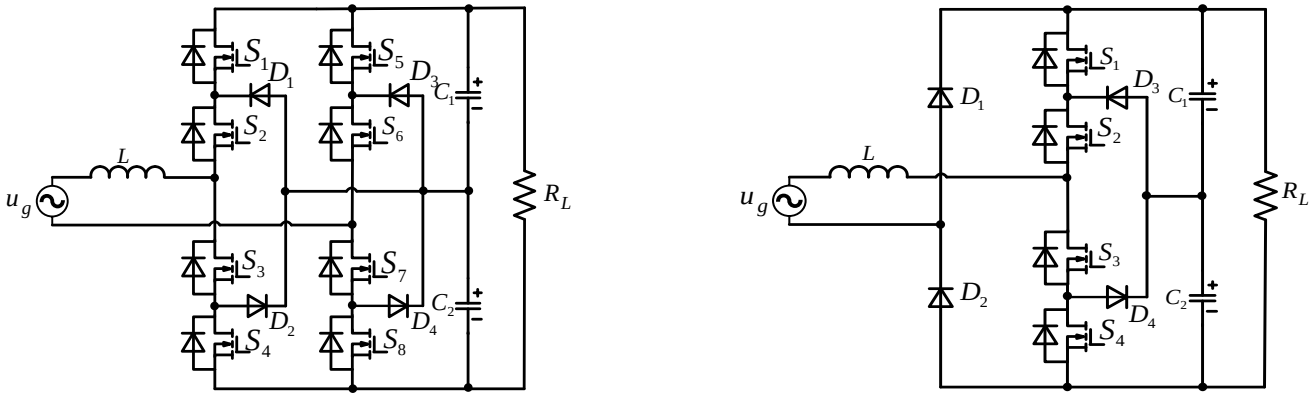


Figure 1. Two typical single-phase three-level PFC topologies. (**a**) TTL-PFC. (**b**) UTL-PFC.

Generally, three-level PFC topologies usually adopt capacitors in parallel on the DC side for voltage regulation [18–20]. According to the topology characteristics, the link structure of the switch, diode, and capacitor can be defined as a switch-capacitor cell (SCC), which is divided into two forms: common anode SCC and common cathode SCC, as shown in Figure 2.

Figure 2. Two forms of the switch-capacitor cell. (**a**) common anode SCC. (**b**) common cathode SCC.

In order to facilitate the pulse distribution and reduce the switching losses of the UTL-PFC, this paper uses the cells shown in Figure 2 to reconstruct the upper and lower controllable switch bridge arms of the UTL-PFC topology and obtains a family of a novel single-phase three-level PFC topologies, as shown in Figure 3. In Figure 3a, switch S_1, the capacitor C_1, and the diode D_5 form a common cathode SCC. Meanwhile, the switch S_2, the capacitor C_2, and the diode D_6 form a common anode SCC. In order to prevent the bidirectional flow of current, the diodes D_3 and D_4 are connected in series on the branches of switches S_1 and S_2, respectively. By connecting the source of the switch S_2 in Figure 3a to point *a* or the drain of switch S_1 to point *a*, the PFC topologies shown in Figure 3b,c can be obtained. The topology shown in Figure 3b uses only one common cathode SCC, which is composed of switch S_1, diode D_5, and capacitor C_1. Correspondingly, only one common anode SCC is used in the topology shown in Figure 3c, which is formed by the switch S_2, the diode D_6, and the capacitor C_2. In all three proposed PFC topologies, diodes D_5 and D_6 can ensure the unidirectional flow of power and prevent the energy of capacitors from returning to the input side.

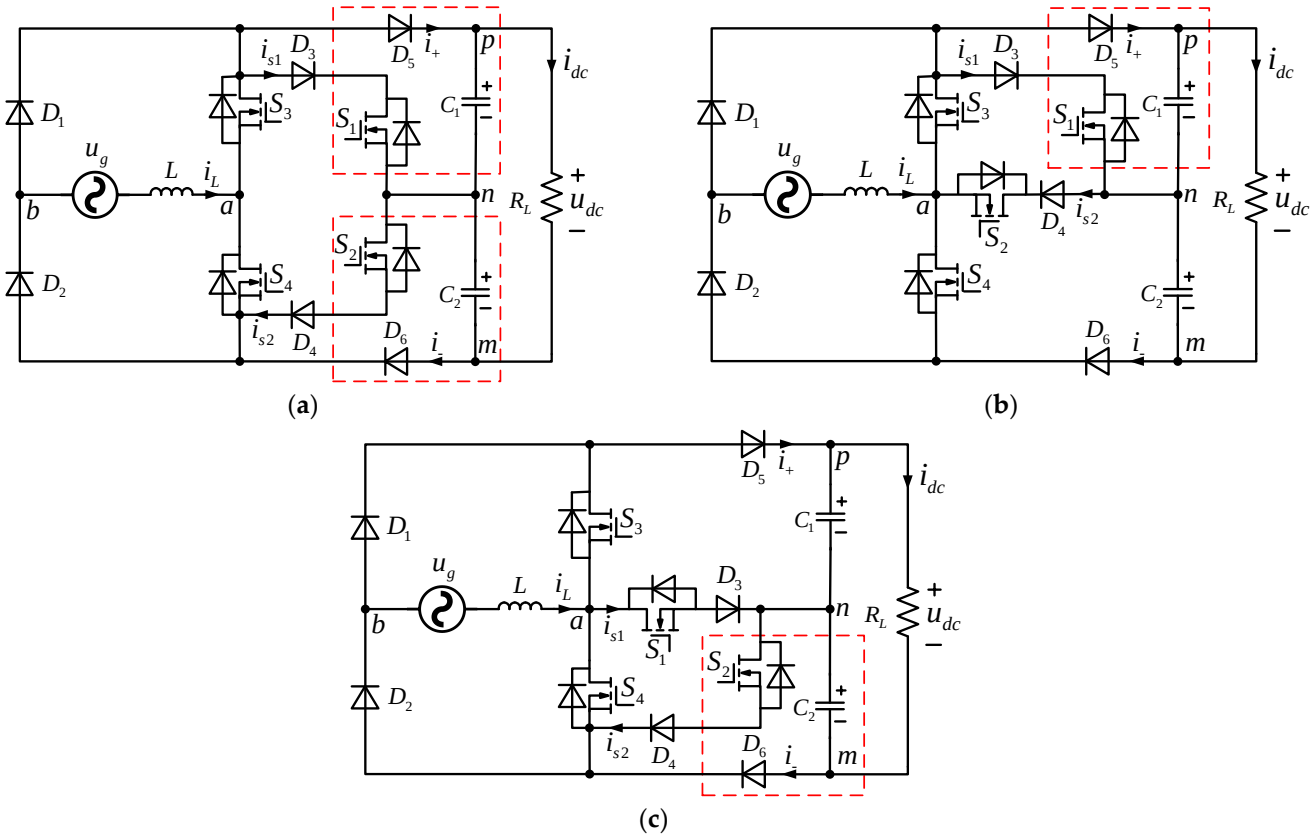


Figure 3. Three novel single-phase three-level PFC. (**a**) STL-PFC. (**b**) UATL-PFC. (**c**) LATL-PFC.

The proposed three-level PFC topologies are named respectively according to the topological structure characteristics. Figure 3a–c are defined as symmetrical three-level PFC (STL-PFC), upper asymmetrical three-level PFC (UATL-PFC), and lower asymmetrical three-level PFC (LATL-PFC), respectively. Compared with the UTL-PFC topology, the proposed PFC topologies work with only one active switch at most in each operating mode, which reduces the switching losses and the difficulty of the control system design. Meanwhile, the proposed novel PFC topologies have the same switching pulse signal distribution, which means they can use the same modulation method.

2.2. Operation Principle of Novel PFC Topologies

As the pulse signal distribution of the STL-PFC, UATL-PFC, and LATL-PFC is the same, this section takes the STL-PFC topology as an example to analyze the operation principle, and other proposed topologies can be analyzed in the same way. The STL-PFC topology is formed by an AC voltage source u_g, one inductor L, four switches S_1–S_4, six diodes D_1–D_6, and two identical capacitors C_1–C_2. The STL-PFC has six operating modes in one power frequency period at a steady state, and the current path corresponding to each operating mode is shown in Figure 4. The key waveforms of the STL-PFC topology during one power frequency period are shown in Figure 5. The analysis of each operating mode is given as follows.

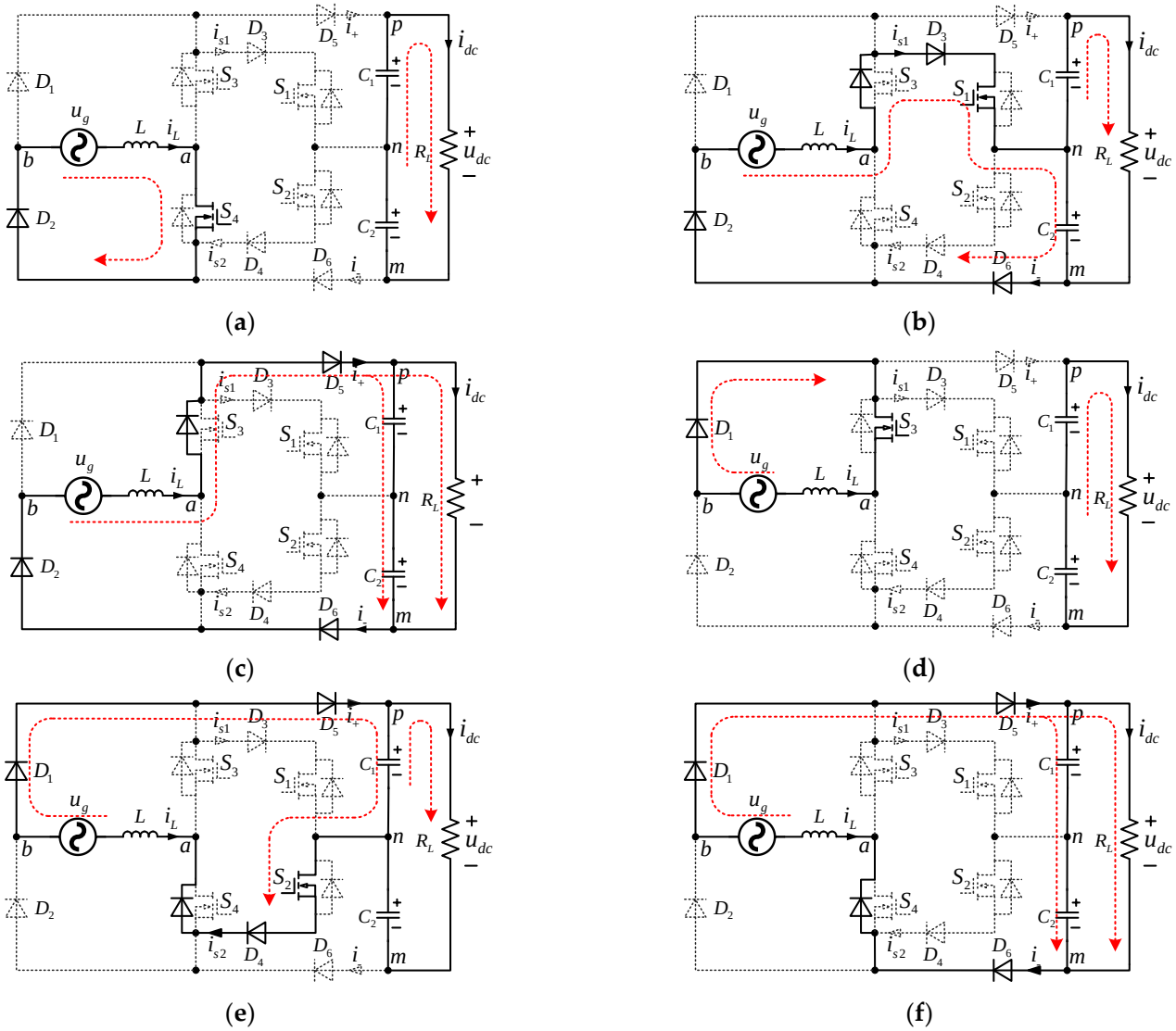


Figure 4. Current paths corresponding to six operating modes of the STL-PFC: (**a**) Mode 1 ($i_L > 0$, $u_{ab} = +0$); (**b**) Mode 2 ($i_L > 0$, $u_{ab} = +0.5u_{dc}$); (**c**) Mode 3 ($i_L > 0$, $u_{ab} = +u_{dc}$); (**d**) Mode 4 ($i_L < 0$, $u_{ab} = -0$); (**e**) Mode 5 ($i_L < 0$, $u_{ab} = -0.5u_{dc}$); (**f**) Mode 6 ($i_L < 0$, $u_{ab} = -u_{dc}$).

Mode 1 [$t \in (t_0,t_1) \cup (t_2,t_3)$]: Only the switch S_4 is turned ON as shown in Figure 4a. The inductor L is in the energy storage state. Meanwhile, the capacitors C_1 and C_2 supply power to the load R_L. During this state, the voltage $u_{ab} = +0$. The equation of this mode can be expressed as:

$$Ldi_L/dt = u_g \quad (1)$$

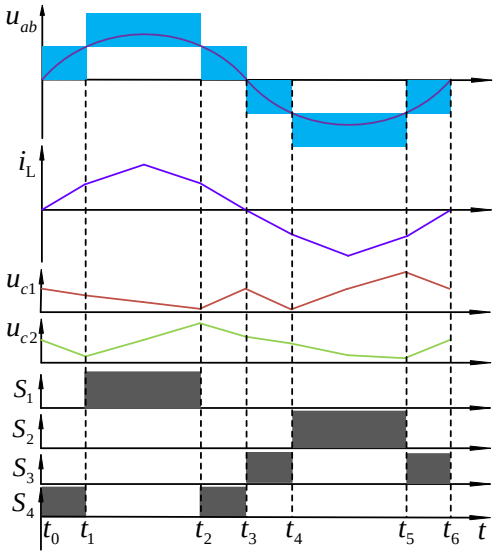


Figure 5. Key operating waveforms of the STL-PFC in theory.

Mode 2 [$t\in(t_0,t_3)$]: Only the switch S_1 is turned ON, as shown in Figure 4b. In this mode, the capacitor C_2 is charged, the capacitor C_1 provides energy to the load R_L, and the voltage $u_{ab} = +u_{c2} = +0.5u_{dc}$. During this state, if the power supply voltage is higher than $0.5u_{dc}$, the inductor current i_L increases linearly. Correspondingly, if the power supply voltage is lower than $0.5u_{dc}$, the inductor current i_L decreases linearly. The equation of this mode can be obtained as follows:

$$Ldi_L/dt = u_g - u_{dc}/2 \tag{2}$$

Mode 3 [$t\in(t_1,t_2)$]: All switches are turned OFF, as shown in Figure 4c. During this state, the inductor L provides energy to the load R_L. At the same time, the capacitors C_1 and C_2 are charged, and the voltage $u_{ab} = u_{c1} + u_{c2} = u_{dc}$. The equation of this mode can be obtained as follows:

$$Ldi_L/dt = u_g - u_{dc} \tag{3}$$

Mode 4 [$t\in(t_3,t_4)\cup(t_5,t_6)$]: Only the switch S_3 is turned ON, as shown in Figure 4d. The inductor current i_L increases linearly. Meanwhile, the capacitors C_1 and C_2 supply power to the load R_L, the voltage $u_{ab} = -0$. The equation of this mode can be obtained as follows:

$$Ldi_L/dt = -u_g \tag{4}$$

Mode 5 [$t\in(t_3,t_6)$]: Only the switch S_2 is turned ON as shown in Figure 4e. In this mode, the capacitor C_1 is charged, the capacitor C_2 discharges energy to the load R_L, and the voltage $u_{ab} = -u_{c1} = -0.5u_{dc}$. During this state, if the absolute value of the power supply voltage is higher than $0.5u_{dc}$, the inductor current i_L increases linearly. Correspondingly, if the absolute value of the power supply voltage is lower than $0.5u_{dc}$, the inductor current i_L decreases linearly; the equation of this mode can be obtained as:

$$Ldi_L/dt = -u_g - u_{dc}/2 \tag{5}$$

Mode 6 [$t\in(t_4,t_5)$]: All switches are turned OFF, as shown in Figure 4f. In this mode, the capacitors C_1 and C_2 are charged, the inductor current i_L decreases linearly, and the voltage u_{ab} = -u_{c1} − u_{c2} = $-u_{dc}$. The equation of this mode can be obtained as follows:

$$Ldi_L/dt = -u_g - u_{dc} \tag{6}$$

2.3. Equivalent Circuit Model

According to the detailed analysis of the operation principle of the STL-PFC topology in Section 2.2, the switching pulse distribution and system parameters of the STL-PFC can be summarized in Table 1, where the "ON" and "OFF" states of the switches are represented by "1" and "0", respectively. The currents i_+ and i_- represent the upper and lower DC bus currents, respectively. The branch currents i_{s1} and i_{s2} represent the currents flowing through the switches S_1 and S_2, respectively. From Table 1, the upper DC bus current i_+ is not equal to zero in modes 3, 5, and 6. Correspondingly, the lower DC bus current i_- is not equal to zero in modes 2, 3, and 6. The branch current i_{s1} is not equal to zero only in mode 2.

Table 1. Switching states and system parameters.

Modes		Switching States				System Parameters								
		S_1	S_2	S_3	S_4	i_+	i_-	i_{s1}	i_{s2}	i_{s3}	i_{s4}	u_{ab}	u_{c1}	u_{c2}
$i_L > 0$	1	0	0	0	1	0	0	0	0	0	i_L	0	↓	↓
	2	1	0	0	0	0	i_L	i_L	0	i_L	0	u_{c2}	↓	↑
	3	0	0	0	0	i_L	i_L	0	0	i_L	0	$u_{c1}+u_{c2}$	↑	↑
$i_L < 0$	4	0	0	1	0	0	0	0	0	$-i_L$	0	0	↓	↓
	5	0	1	0	0	$-i_L$	0	0	$-i_L$	0	$-i_L$	$-u_{c1}$	↑	↓
	6	0	0	0	0	$-i_L$	$-i_L$	0	0	0	$-i_L$	$-u_{c1}-u_{c2}$	↑	↑

Meanwhile, the branch current i_{s2} is not equal to zero only in mode 5. Based on the above analysis, the currents i_+, i_-, i_{s1}, and i_{s2} can be calculated as:

$$\begin{aligned} i_+ &= \overline{S}_1\overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1+\mathrm{sgn}(i_L)}{2}i_L - \overline{S}_3\overline{S}_4\tfrac{1-\mathrm{sgn}(i_L)}{2}i_L \\ &= (A-B)i_L \end{aligned} \tag{7}$$

$$\begin{aligned} i_- &= \overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1+\mathrm{sgn}(i_L)}{2}i_L - \overline{S}_1\overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1-\mathrm{sgn}(i_L)}{2}i_L \\ &= (C-D)i_L \end{aligned} \tag{8}$$

$$\begin{aligned} i_{s1} = {} & S_1\overline{S}_2\overline{S}_3\tfrac{1+\mathrm{sgn}(i_L)}{2}i_L - \overline{S}_1\overline{S}_2\overline{S}_3\tfrac{1-\mathrm{sgn}(i_L)}{2}i_L \\ & -\overline{S}_1\overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1-\mathrm{sgn}(i_L)}{2}i_L = (E-F-D)i_L \end{aligned} \tag{9}$$

$$\begin{aligned} i_{s2} &= \overline{S}_1\overline{S}_2\overline{S}_3\tfrac{1-\mathrm{sgn}(i_L)}{2}i_L - \overline{S}_3\overline{S}_4\tfrac{1-\mathrm{sgn}(i_L)}{2}i_L \\ &= (F-B)i_L \end{aligned} \tag{10}$$

where:

$$\begin{aligned} &A = \overline{S}_1\overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1+\mathrm{sgn}(i_L)}{2},\ B = \overline{S}_3\overline{S}_4\tfrac{1-\mathrm{sgn}(i_L)}{2}, \\ &C = \overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1+\mathrm{sgn}(i_L)}{2},\ D = \overline{S}_1\overline{S}_2\overline{S}_3\overline{S}_4\tfrac{1-\mathrm{sgn}(i_L)}{2}, \\ &E = S_1\overline{S}_2\overline{S}_3\tfrac{1+\mathrm{sgn}(i_L)}{2},\ F = \overline{S}_1\overline{S}_2\overline{S}_3\tfrac{1-\mathrm{sgn}(i_L)}{2}, \\ &\mathrm{sgn}(i_L) = \begin{cases} 1, \text{ if } i_L > 0 \\ -1, \text{ if } i_L < 0 \end{cases}. \end{aligned}$$

It can be seen from Table 1 that the bridge-arm voltage u_{ab} has five different levels during one power frequency period so that the voltage u_{ab} can be expressed as:

$$u_{ab} = (A-B)u_{c1} + (E+A-D)u_{c2} \tag{11}$$

Through different combinations of A, B, D, and E, the bridge-arm voltage u_{ab} can be converted between the five levels of u_{dc}, $u_{dc}/2$, 0, $-u_{dc}/2$, and $-u_{dc}$. According to (7)–(11), the equivalent circuit model of the STL-PFC topology can be obtained, as shown in Figure 6, where r_L is the parasitic resistance of the inductor. The equivalent model shown in Figure 6 is also applicable to the UATL-PFC and the LATL-PFC.

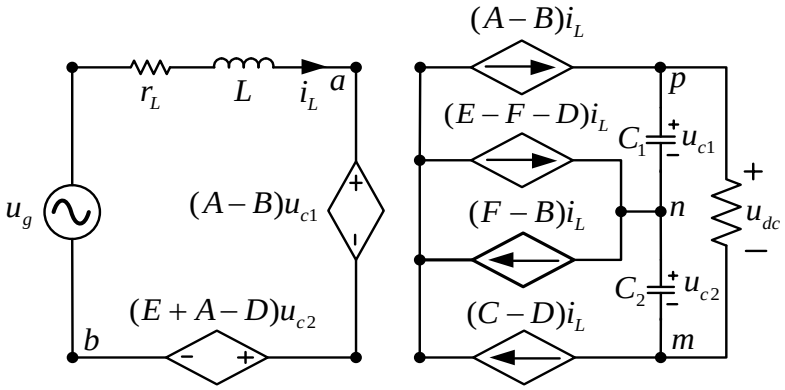


Figure 6. The equivalent circuit model of the STL-PFC topology.

3. Performance Analysis of the Proposed Topologies

3.1. Analysis of Voltage Stresses of Switching Devices

The maximum voltage stresses of the switching devices in the proposed three-level PFC topologies are analyzed under the condition of the same output power level, and the results are summarized in Table 2. It can be seen from Table 2 that the maximum voltage stresses of switches S_1 and S_2 in the switch-capacitor cells of all three proposed PFC topologies are halved, which is beneficial for reducing the switching losses.

Table 2. Maximum voltage stresses of the switching devices in the proposed topologies.

Switching Devices	STL-PFC	UATL-PFC	LATL-PFC
S_1	$0.5u_{dc}$	$0.5u_{dc}$	$0.5u_{dc}$
S_2	$0.5u_{dc}$	$0.5u_{dc}$	$0.5u_{dc}$
S_3	u_{dc}	u_{dc}	u_{dc}
S_4	u_{dc}	u_{dc}	u_{dc}
D_1, D_2	u_{dc}	u_{dc}	u_{dc}
D_3, D_4	$0.5u_{dc}$	$0.5u_{dc}$	$0.5u_{dc}$
D_5, D_6	u_{dc}	u_{dc}	u_{dc}

3.2. Calculation and Comparison of the Switching Device Losses

The losses of switching devices have a significant impact on the efficiency of PFC converters, which is mainly composed of the losses of MOSFETs and diodes [21]. Table 3 shows the switching devices in a conduction state in the proposed PFC topologies under different operating modes, where D_4 and D_6 represent diodes with rated voltages of 400 V and 600 V, respectively. M_4 and M_6 represent MOSFETs with rated voltage of 400 V and 600 V, respectively. It can be seen from Table 3 that in modes 2 and 5, the STL-PFC has one more diode with a rated voltage of 600 V for conduction than the LATL-PFC and the UATL-PFC, respectively. Hence, the power loss of the STL-PFC is slightly larger than that of the LATL-PFC and the UATL-PFC in the two operating modes. Correspondingly, the number of the conductive switching devices of the STL-PFC, LATL-PFC, and UATL-PFC is the same under other operating modes, so the power losses of the three proposed PFC topologies are similar. In summary, the STL-PFC has the largest power losses among the three proposed PFC topologies.

To verify the validity of the proposed PFC topologies, the representative STL-PFC is selected for loss comparisons with the two typical three-level PFC topologies shown in Figure 1. The specific calculation method of the switching device losses can refer to [22], and the results are shown in Figure 7. It can be seen from Figure 7 that the loss of the STL-PFC is the lowest under different load conditions because, at most, one active switch in each operating mode of the STL-PFC is in a conduction state, further proving that the efficiency of the proposed novel PFC topologies is higher.

Table 3. Switching devices in conduction state under different operation modes.

Operating Modes	Devices(Number × Rated Voltage)			Voltage u_{ab}
	STL-PFC	UATL-PFC	LATC-PFC	
Mode 1	$1 \times D_{6,1} \times M_6$	$1 \times D_{6,1} \times M_6$	$1 \times D_{6,1} \times M_6$	+0
Mode 2	$1 \times D_{4,3} \times D_{6,1} \times M_4$	$1 \times D_{4,3} \times D_{6,1} \times M_4$	$1 \times D_{4,2} \times D_{6,1} \times M_4$	$+0.5u_{dc}$
Mode 3	$4 \times D_6$	$4 \times D_6$	$4 \times D_6$	$+u_{dc}$
Mode 4	$1 \times D_{6,1} \times M_6$	$1 \times D_{6,1} \times M_6$	$1 \times D_{6,1} \times M_6$	0
Mode 5	$1 \times D_{4,3} \times D_{6,1} \times M_4$	$1 \times D_{4,2} \times D_{6,1} \times M_4$	$1 \times D_{4,3} \times D_{6,1} \times M_4$	$-0.5u_{dc}$
Mode 6	$4 \times D_6$	$4 \times D_6$	$4 \times D_6$	$-u_{dc}$

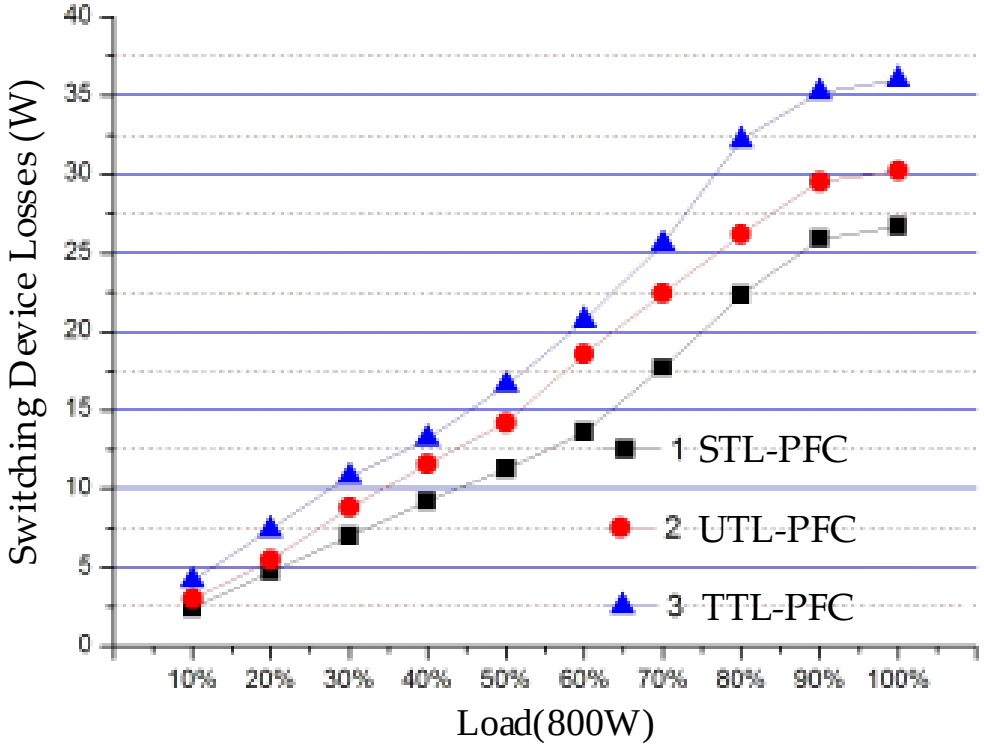


Figure 7. Switching device losses of three PFC topologies under different load conditions.

4. Multicarrier Modulation Technology Based on Capacitor Voltage Balancing

The novel three-level PFC topologies proposed in this paper adopt four-carrier modulation technology to realize pulse signal distribution. As shown in Figure 8, the four equal amplitude and in-phase triangular carriers (Cr_1, Cr_2, Cr_3, and Cr_4) are compared with the sinusoidal modulation wave u_{ref}. When the value of the modulation wave is larger than that of the carrier, the output PWM signal is high level; otherwise, the output PWM signal is at a low level [23]. According to the comparison, the four PWM waves (u_{pwm1}, u_{pwm2}, u_{pwm3}, and u_{pwm4}) can be generated. The pulse signals of the switches (S_1~S_4) in the proposed PFC topologies can be generated by a logical combination of the four PWM waves (u_{pwm1}~u_{pwm4}) and the modulation wave u_{ref}. The logical relation can be expressed as:

$$S_1 = \overline{u}_{pwm1} u_{pwm2} \tag{12}$$

$$S_2 = \overline{u}_{pwm3} u_{pwm4} \tag{13}$$

$$S_3 = u_{pwm3} u_{pwm4} \frac{1 + \mathrm{sgn}(u_{ref})}{2} \tag{14}$$

$$S_4 = \overline{u}_{pwm1}\overline{u}_{pwm2}\frac{1-\mathrm{sgn}(u_{ref})}{2} \tag{15}$$

where: $\mathrm{sgn}(u_{ref}) = \begin{cases} 1, \text{ if } u_{ref} > 0 \\ -1, \text{ if } u_{ref} < 0 \end{cases}$.

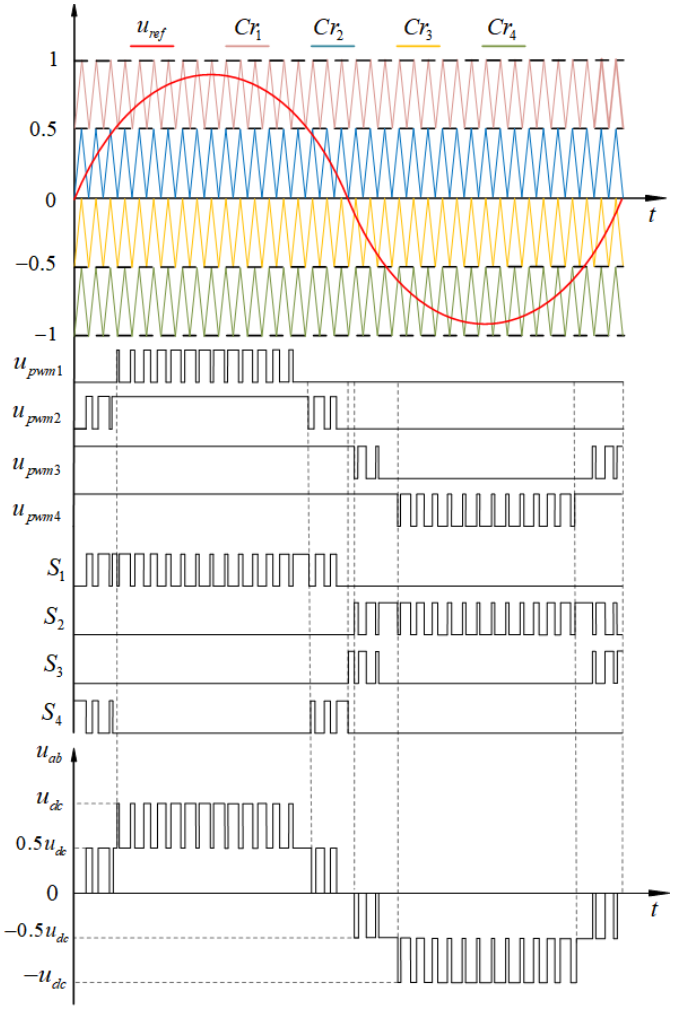


Figure 8. The pulse width modulation principle of the proposed PFC.

In the pulse signal waveforms of the switches S_1, S_2, S_3, and S_4, the high-level and the low-level represent the "ON" and "OFF" signals of the switches, respectively. The proposed PFC topologies can operate according to the modes in Table 1 through the mutual cooperation between the pulse signals of each switch, so that the bridge-arm voltage u_{ab} can be three-level.

As generally recognized, the phenomenon of unbalanced dc-link capacitor voltage in three-level PFC topologies will increase the voltage stresses of power devices and even lead to device damage in serious cases [24–27]. Therefore, this problem should be taken into consideration in the control design. Modes 2 and 5 of the proposed novel three-level PFC topologies directly affect the balance of dc-link capacitor voltage. In mode 2, the upper capacitor C_1 is charged, and its voltage increases. Meanwhile, the lower capacitor C_2 is discharged, and its voltage decreases. However, in mode 5, the voltage fluctuation of the two capacitors is opposite to mode 2. To solve this problem, this paper uses the capacitor voltage balancing method based on multicarrier modulation to achieve the

balance of dc-link capacitor voltage. The voltage-current relationship of the capacitor can be expressed as

$$u_c(t) = \int_{t_0}^{t_0+D_iT_s} i(t)dt/C_i \tag{16}$$

where $i(t)$ is the charging current of the capacitor, D_iT_s is the charging time of the capacitor, and C_i (I = 1,2) is the value of the capacitor.

According to (16), the balance of dc-link capacitor voltage can be realized by changing the charging and discharging time of the capacitors, that is, changing the duty cycle D_i. Therefore, the modulation wave needs to be modified. This paper uses the PI controller to output the balancing factor α and add it to the original modulation wave to adjust the duty cycle D_i. The modified modulation wave can be obtained as

$$u_{ref} = \alpha m \sin\theta \tag{17}$$

where θ is the reference phase angle of the modulation wave, m is the modulation ratio, and the value range of the balancing factor α is $0.5 < |\alpha| < 1$.

The modified modulation wave can change the operating time of modes 2 and 5 to adjust the charging and discharging time of the upper and lower capacitors, thus realizing the balance of the capacitor voltage.

5. Experimental Validation

In order to verify the feasibility of the proposed novel three-level PFC topologies, the representative STL-PFC is selected to build the experimental platform, as shown in Figure 9. The main parameters of the experimental circuit are listed in Table 4. The single-phase input AC power is provided by the AC voltage regulator TDGC2-3 kVA, and the controller adopts DSP TMS320F28335. The experimental waveforms are obtained by a Tek-2024B oscilloscope, and the power quality tester adopts E6000.

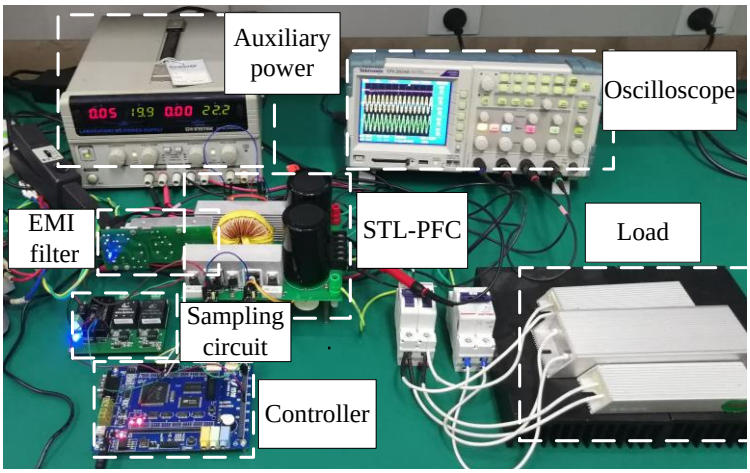


Figure 9. Experimental prototype platform.

Table 4. Main Parameters of The Experimental Circuit.

Description	Label	Value
Input voltage	u_{AC}	220 V_{rms}
Output rated voltage	u_{dc}	400 V
Rated output power	P_o	800 W
Switching frequency	f	50 kHz
Inductor	L	2 mH
Capacitor	C_1/C_2	1000 μF
MOSFETs	S_1~S_4	STW26NM60N
Diodes	D_1~D_6	RHPR3060

Figure 10 displays the pulse distribution of the switches S_1~S_4, which is consistent with the theoretical analysis results, indicating that the proposed topology has the advantage of reducing switching losses.

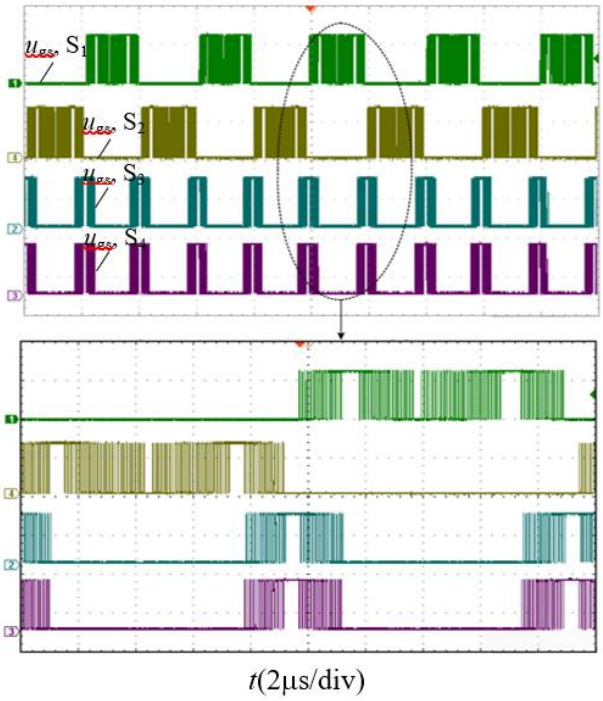


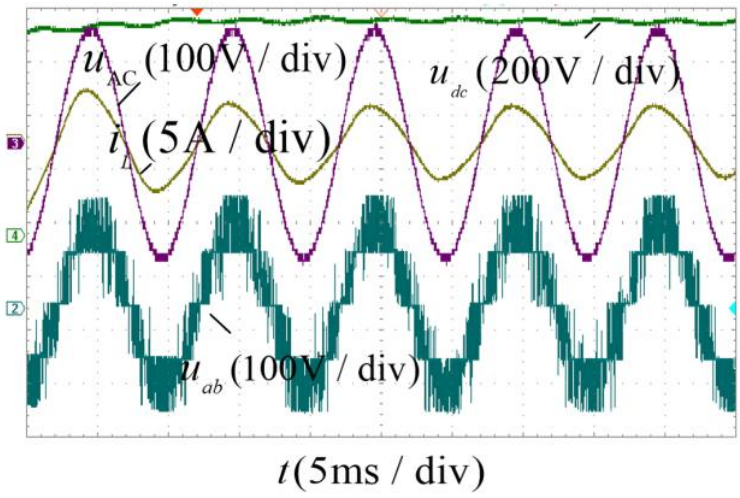
Figure 10. The pulse distribution waveforms of four switches in the STL-PFC.

The experimental results of the STL-PFC operating in a steady state are shown in Figure 11. Here u_{AC} and i_L denote the voltage and current of the grid side, respectively, while u_{dc} and u_{ab} represent the output voltage of the DC side and the bridge-arm voltage, respectively. Additionally, u_{c1} and u_{c2} indicate the voltage of the capacitors C_1 and C_2, respectively. From Figure 11a, the waveform of input voltage u_{AC} is in phase with the waveform of input current i_L, meeting the unity power factor. The output DC voltage u_{dc} is stable at 400 V, and the peak value of the ripple voltage is 5.3 V. The bridge-arm voltage u_{ab} has five voltage levels, which is consistent with the theoretical analysis. From Figure 11b, it can be seen that the voltage waveforms of the two dc-link capacitors maintain dynamic balance, which proves the correctness of the modulation strategy based on capacitor voltage balancing. From Figure 11c, it can be seen that the current harmonic content is 3.99%, which meets the requirement that the harmonic content is less than 5%.

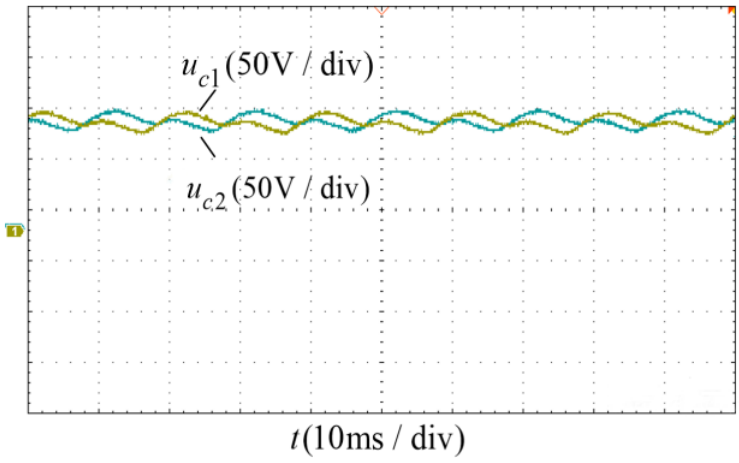
The experimental results of the STL-PFC operating in a dynamic state are shown in Figure 12, where u_{dc}^{*} and u_{gsp} represent the reference of the DC side voltage and the driving voltage signal, respectively.

Figure 12a shows that when the reference voltage u_{dc}^{*} breaks, the DC side voltage u_{dc} follows the change and remains at about 500 V, and the input current i_L remains sinusoidal after a spike occurs. Still, a large noise interference occurs in the voltage u_{ab} due to parameters exceeding design criteria. Figure 12b shows that when the driving signal is lost, the proposed PFC can still work in the uncontrolled rectification state to ensure a reliable power supply for the load. However, a large distortion appears in the voltage u_{ab} and the input current i_L in this state, and at the same time, the power factor of the proposed PFC is low. Figure 12c shows that when the load changes, the proposed PFC can still achieve power factor correction, and there is only a certain range of small fluctuations in the voltage of the DC side. Figure 12d shows that the voltage waveforms of the upper and lower dc-link capacitors can still maintain good stability when the load increases or decreases by 50%. As the output voltage level increases, the output current will decrease for the same output power, leading to shorter conduction and turn-off times of the switching

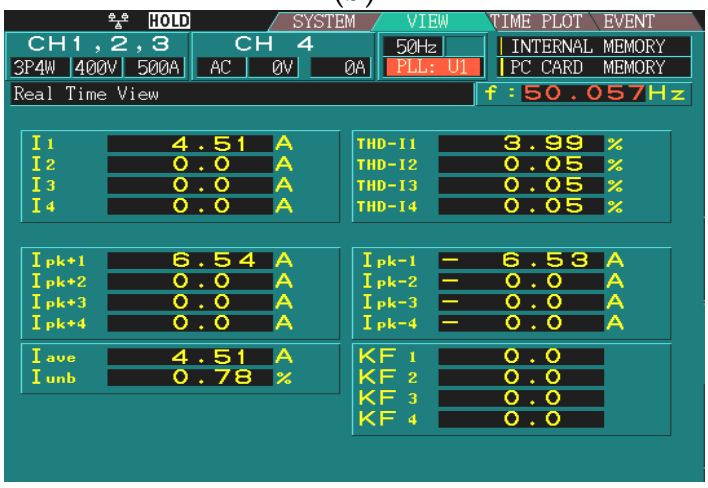
devices, reducing their switching losses. According to Figure 12e, the efficiency of the STL-PFC also improves. Additionally, the efficiency of the STL-PFC exceeds 97.3%.



(**a**)



(**b**)



(**c**)

Figure 11. The experimental results in a steady state. (**a**) The DC output voltage u_{dc}, the input voltage v_{AC}, the inductor current i_L, and the bridge-arm voltage u_{ab}. (**b**) The capacitor voltage u_{c1}, u_{c2}. (**c**) Analysis of harmonic content.

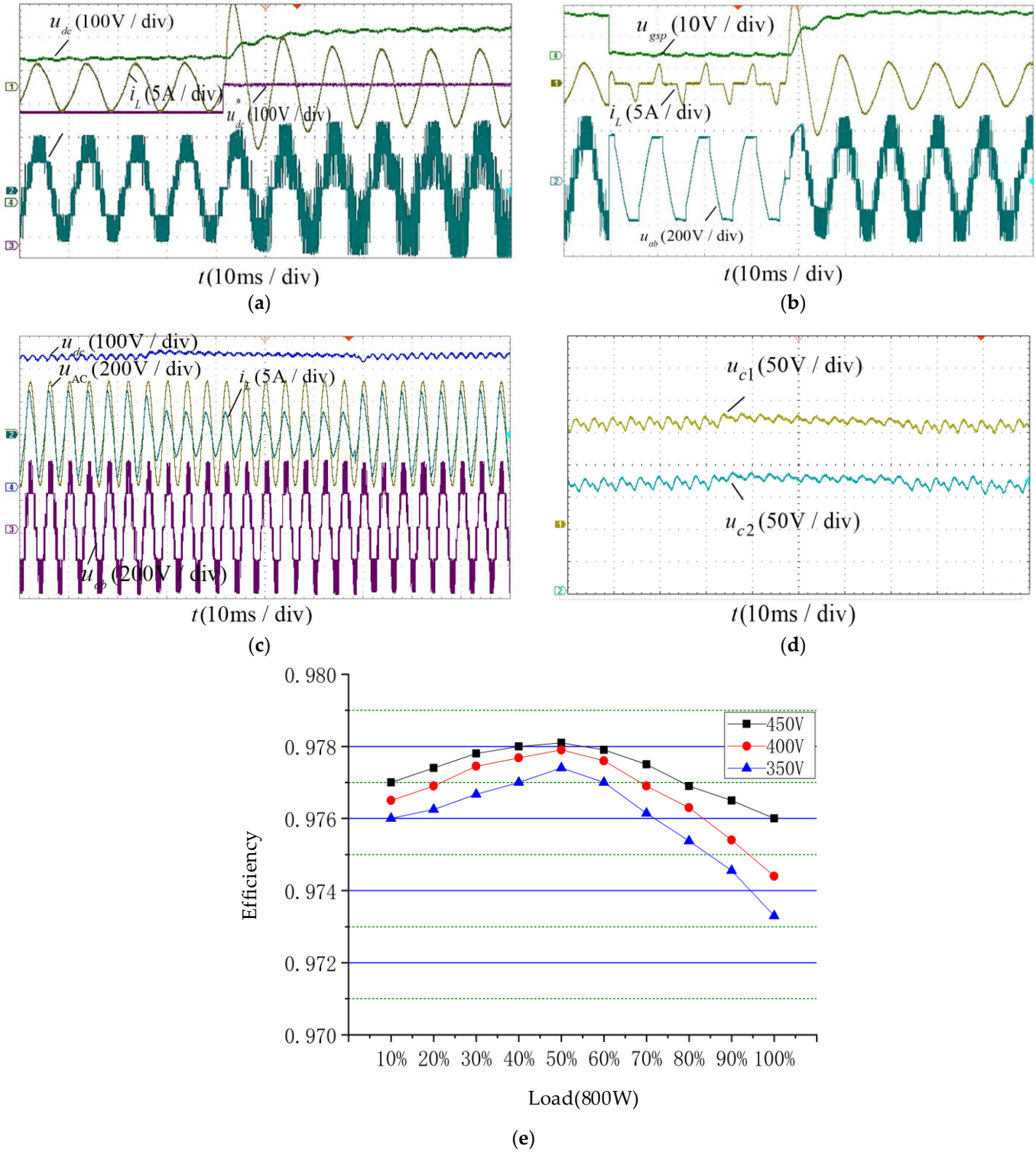


Figure 12. The experimental results in a dynamic state. (**a**) Experimental waveforms during the reference voltage increase from 400 V to 500 V. (**b**) Experimental waveforms from uncontrolled process jump to controllable process. (**c**) Experimental waveforms when the load increases or decreases by 50%. (**d**) The capacitor voltage waveforms when the load increases or decreases by 50%. (**e**) Efficiency comparison at different output voltage levels.

6. Conclusions

In this paper, a new family of single-phase, three-level power factor correction (PFC) topologies based on switch-capacitor cells has been presented. The three proposed PFC

topologies share the same switching pulse distribution, making utilizing the same modulation method possible. Moreover, these PFC topologies can achieve diode rectification in the event of a switch failure, ensuring a reliable power supply to the load. By limiting the operation to a maximum of one active switch in each mode, the proposed PFC topologies significantly reduce switching losses. The deduction process, operating principle, and circuit characteristics of the PFC topologies have been analyzed in detail, and a suitable modulation technology based on capacitor voltage balancing has been designed. Finally, a laboratory prototype with a rated power of 800 W has been built and tested, with experimental results demonstrating the feasibility and superiority of the proposed PFC topologies.

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