

Article **Study of the Within-Batch TID Response Variability on Silicon-Based VDMOS Devices**

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Abstract: Silicon-based vertical double-diffused MOSFET (VDMOS) devices are important components of the power system of spacecraft. However, VDMOS is sensitive to the total ionizing dose (TID) effect and may have TID response variability. The within-batch TID response variability on silicon-based VDMOS devices is studied by the 60 Co gamma-ray irradiation experiment in this paper. The variations in device parameters after irradiation is obtained, and the damage mechanism is revealed. Experimental results show that the standard deviations of threshold voltage, subthreshold swing, output capacitance, and diode forward voltage increase, while the standard deviation of maximum transconductance decreases after irradiation. The standard deviation of on-state resistance is basically unchanged before and after irradiation. By separating the trapped charges generated by TID irradiation, it is found that the deviation of the oxide trapped charges and the interface traps increase with the increase in the total dose. The reasons for the variation in device parameters after irradiation are revealed by establishing the relationship between the trapped charges and the electrical parameters before and after irradiation.

Keywords: VDMOS; total ionizing dose (TID); variability; oxide trapped charges; interface traps

1. Introduction

Silicon-based vertical double-diffused MOSFET (VDMOS) devices are widely used in the power system of spacecraft due to the high input impedance, large current gain, excellent noise margin, and small conduction loss, as well as a negative temperature coefficient and no secondary breakdown effect [\[1](#page-11-0)[,2\]](#page-11-1). However, VDMOS is sensitive to the total ionizing dose (TID) effect since there is a parasitic NPN transistor in the VDMOS structure [\[3\]](#page-11-2). Moreover, process variation in VDMOS manufacturing occurs with different temperature distributions, impurity diffusion, and injection. The TID response is sensitive to process variations, as evidenced by the different TID responses of devices produced from the same wafer (within-wafer) or devices produced from the same batch (within-batch).

The TID response variability has been studied in previous works. Within-wafer TID response variability of NMOSFET and PMOSFET was measured by Hu et al. and Gerardin et al. [\[4,](#page-11-3)[5\]](#page-11-4). They attributed the within-wafer TID response variability to the process variation in shallow trench isolation (STI) and random doping. The TID response variability of 25 nm single-level cell non-volatile memory device (NAND) flash memories from two different lots was studied by Bagatin et al. [\[6\]](#page-11-5). The statistical parameters such as mean value, standard deviation, and shapes of the error distributions were studied. Part-to-part and lot-to-lot variability of TID response in bipolar linear devices was studied by Guillermin et al. [\[7\]](#page-11-6). The three-sigma method and one-sided tolerance limit method were commonly used to take the variability into account. Within-wafer TID response variability

Citation: Li, X.; Cui, J.; Zheng, Q.; Li, P.; Cui, X.; Li, Y.; Guo, Q. Study of the Within-Batch TID Response Variability on Silicon-Based VDMOS Devices. *Electronics* **2023**, *12*, 1403. [https://doi.org/10.3390/](https://doi.org/10.3390/electronics12061403) [electronics12061403](https://doi.org/10.3390/electronics12061403)

Academic Editor: Adel M. Sharaf

Received: 13 January 2023 Revised: 8 March 2023 Accepted: 10 March 2023 Published: 15 March 2023

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on the buried oxide (BOX) layer of silicon-on-insulator (SOI) technology was investigated by Zheng et al. [\[8,](#page-11-7)[9\]](#page-11-8). The larger standard deviation of threshold voltage and off-state leakage distribution for irradiated devices than un-irradiated devices were observed. They attributed it to the evolution of net trapped charges induced by TID in BOX affecting by positively charged silicon nanoclusters introduced by silicon ion implantation. The device variability induced by the TID effects was investigated by Ma et al. in commercial 16 nm bulk nFinFETs with a small number of samples [\[10\]](#page-11-9). It was found that transistors characterized by higher drain currents exhibit the worst TID degradation. They attributed this phenomenon to the impact of random dopant fluctuations on the TID effects and/or to variations in the hydrogen concentration responsible for the TID-induced interface traps. The above studies confirmed the fluctuation of the TID response of the devices in the wafer, as well as the variability of the radiation damage of device modules from different batches and within-batch. There have been studies on the TID effect of VDMOS [\[11](#page-11-10)[–15\]](#page-11-11). However, to our best knowledge, there is no report on the within-batch TID response variability on silicon-based VDMOS devices.

Within-batch TID response variability on silicon-based VDMOS devices is investigated by irradiation experiment in this paper. The variability of threshold voltage, subthreshold swing, maximum transconductance, output capacitance, diode forward voltage, and onstate resistance before and after irradiation is analyzed. The reasons for the variation in device parameters under irradiation are revealed by analyzing the trapped charge induced by irradiation.

2. Experiment Details

The devices under test (DUT) are N-channel enhanced VDMOS within the same batch. When the device is turned on, the maximum drain current is 120A. The maximum gatesource voltage is 20 V. The device has three terminals, gate, drain, and source. The device is packaged with TO247. The numbers of DUT are from 1 to 68. The experiments were conducted by ⁶⁰Co gamma-ray at room temperature in the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences. The dose rate was 50.24 rad(Si)/s and the dose levels were 5 krad(Si), 10 krad(Si), 15 krad(Si), 20 krad(Si), and 25 krad(Si). It was found that the ON bias condition ($V_{DS} = 0 \text{ V}$, $V_{GS} = 20 \text{ V}$) can induce greater radiation damage than other bias conditions. All devices were kept ON bias condition during the irradiation process.

The transfer characteristic curves ($I_{DS} - V_{GS}$) of the devices were measured by Keysight B1500A semiconductor parameter analyzer at room temperature, while the drain voltage was set to 0.1 V, the gate voltage swept between -0.5 V and 5 V, and the source was grounded. The threshold voltage (V_{TH}) of the device was extracted by the constant current method. *VTH* is equal to the gate-source voltage (*VGS*) when the drain current is equal to 250 µA. The subthreshold swing (*SS*) of the device was calculated by $SS = \frac{dV_{GS}}{d(\log L)}$ $\frac{dV_{GS}}{d(log I_{DS})}$. The transconductance was calculated by $G_M = \frac{dI_{DS}}{dV_{CS}}$ $\frac{u_{DSS}}{dV_{GS}}$. G_{MMAX} is the max transconductance. The output capacitance (*COSS*) was measured, while the frequency was 1.0 MHz, the gate-source voltage was 0 V, and the drain-source voltage was 25 V. The on-state resistance $\left(R_{DS(ON)}\right)$ and diode forward voltage (V_{SD}) were measured by BC3193 Semiconductor Discrete Device Test System at room temperature. The specific parameters and test conditions are shown in Table [1.](#page-2-0)

Table 1. Test parameters of silicon-based VDMOS.

3. Experimental Results

The $I_{DS} - V_{GS}$ curves of 68 devices before and after TID irradiation are shown in Figure 1. It can be seen that the $I_{DS} - V_{GS}$ curves of the devices shift negatively as the dose increases. The variability between devices increases after irradiation.

Figure 1. The shift of transfer characteristic curves of VDMOS devices before and after irradiation.

The variation in threshold voltage, subthreshold swing, and maximum transconductance extracted by the $I_{DS} - V_{GS}$ curves after irradiation is shown in Figure 2a, Figure 2b, and Figure 2c respectively. The mean value and standard deviation (σ) of the electrical parameters are calculated. With the increase in the total dose, the standard deviation of threshold voltage and subthreshold swing increase, while the standard deviation of maximum transconductance decreases. The experiment results verify the within-batch TID response variability on the VDMOS device since standard deviation measures the dispersion of a dataset relative to its mean value [8].

Figure 2. *Cont.*

 -2

 $\overline{0}$

 V_{TH} (V)

2

4

Figure 2. The variation in (a) V_{TH} , (b) SS, and (c) G_{MMAX} of the devices before and after irradiation.

value and standard deviation of the electrical parameters increase after irradiation, which indicates that output capacitance variability also increases after irradiation. The variation in output capacitance after irradiation is shown in Figure [3.](#page-4-1) The mean

Figure 3. The variation in C_{OSS} of the devices before and after irradiation.

The variation in diode forward voltage and the on-state resistance after irradiation is shown in Figures 4 and 5, respectively. It can be seen that the variability of diode forward voltage increases as the total dose increases. The variability of on-state resistance is basically unchanged before and after irradiation.

Figure 4. The variation in V_{SD} of the devices before and after irradiation.

Figure 5. The variation in $R_{DS(ON)}$ of the devices before and after irradiation.

It can be seen from the above results that there is within-batch TID response variability of VDMOS devices in this paper. The changes in parameter variability after irradiation are listed in Table [2.](#page-6-0)

Table 2. The variation in test parameters of the devices after irradiation.

4. Discussion

For MOS devices, the initial electron–hole pairs generated by TID irradiation will eventually affect the electrical parameters of devices through a series of evolution. Four physical processes illustrate the evolution of electron-hole pairs generated by ionizing radiation at the interface of the $SiO₂$ gate and Si substrate, as shown in Figure [6](#page-6-1) [\[16\]](#page-11-12).

Figure 6. Band diagram of a MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation [\[16\]](#page-11-12).

 $\frac{1}{\sqrt{1-\frac{1}{1-\$ The specific process is as follows [\[16–](#page-11-12)[19\]](#page-11-13):

- 1. The ionization of radiation particles in $SiO₂$ produces electron–hole pairs, the number of radiation is related to the ionization does of which is related to the ionization dose.
- of which is related to the ionization dose. 2. When the positive bias is applied to the gate, the drift motion of the electron–hole 2. When the positive bias is applied to the gate, the drift motion of the electron–hole pairs in the oxide layer is the most significant. The electrons are removed by a fast pairs in the oxide layer is the most significant. The electrons are removed by a fast drift (ps magnitude) towards the anodic ohmic contact, and the holes are relatively drift (ps magnitude) towards the anodic ohmic contact, and the holes are relatively slow (s magnitude) to the cathodic ohmic contact.
- 3. In the drift process, some holes are captured to form the trap center. In the shallowlevel trap center located in the gap of SiO_2 , about 1 eV is distributed in the whole SiO_2 body. The holes can be transported in a jump mode. The center of the deep-level trap $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

with more than 3 eV in the gap of $SiO₂$ is mainly distributed near the $SiO₂$ -Si interface, which is the relatively stable positive charge (*Not*) trapped by the oxide layer.

- 4. In the transition layer of the SiO2-Si interface, the holes captured by the oxide layer are exchanged with the electrons in the substrate Si through the tunneling effect and finally captured by the defects at the interface to form the interface traps (N_{it}) .
- 5. Therefore, the main reason for the variation in device parameters after irradiation is that the ionizing radiation destroys the energy band equilibrium, generates electron– hole pairs, and forms oxide-trapped charges and interface traps. The oxide layer is the most sensitive part to TID radiation in the MOS system [\[19\]](#page-11-13).

A technique for separating the density of oxide-trapped charges (*Not*) and the density of interface traps (N_{it}) in MOS transistors through $I - V$ curves is proposed by McWhorter and Winokur [\[20](#page-11-14)[,21\]](#page-11-15). In order to reveal the mechanism of the TID variability response of devices within-batch, the *Not* and *Nit* of devices used in this paper were extracted, as shown in Figure [7.](#page-7-0) The variability of *Not* and *Nit* of the devices increases as the total dose increases. It shows that the trapped charges induced by total dose irradiation have fluctuation, which causes the variability of relevant sensitive electrical parameters. The density of *Not* is much higher than the density of N_{it} , while N_{ot} is about $10^{12}/\text{cm}^2$, and N_{it} is about $10^{11}/\text{cm}^2$ at 25 krad(Si).

Figure 7. The variation in (a) oxide trapped charge (N_{ot}) density, (b) interface trap charge (N_{it}) density of the devices after irradiation. density of the devices after irradiation.

Figure [8](#page-8-0) shows the relation between the shift of threshold voltage (ΔV_{TH}) and the trapped charges (|*N*_{*ot*}| − |*N*_{*it*}|) of the within-batch devices after irradiation. As seen from the fit curve in Figu[re](#page-8-0) 8, the ΔV_{TH} and the $|N_{ot}| - |N_{it}|$ present the linear growth trend. For NMOSFET, the oxide-trapped charges cause a negative shift of the threshold voltage, while the interface traps cause a positive shift of the threshold volt[ag](#page-11-2)[e \[](#page-11-13)3,19]. The calculation formula between ∆*V*_{*TH*} and trapped charg[es i](#page-11-16)[s \[1](#page-11-17)[3,2](#page-11-18)2–24]:

$$
\Delta V_{TH} = -\frac{q|N_{ot}|-|N_{it}|}{C_{ox}}\tag{1}
$$

where q (amount of charge) and C_{ox} (the gate oxide capacitance per unit area) are constant values. Since the density of *Not* is much higher than the density of *Nit*, the variability of the threshold voltage is mainly affected by the variability of *Not*.

Figure 8. Relation between the shift of threshold voltage (∆*VTH*) and the trapped charges $(|N_{ot}|-|N_{it}|)$ of the devices after irradiation.

 V_{SD} is the forward voltage of the diode between the source and the drain. The threshold voltage reduces significantly or even becomes negative after irradiation, resulting in a conductive channel. Additionally, V_{SD} is across the source, channel, and drain [\[18](#page-11-19)[,25\]](#page-11-20). *VSD* is mainly affected by the threshold voltage, so the trend of within-batch variability is the same as the threshold voltage after irradiation.

Subthreshold swing and maximum transconductance are mainly affected by radiationinduced interface traps [\[26](#page-11-21)[–29\]](#page-12-0). Interface traps are formed by TID irradiation at the interface between the device gate dielectric and the silicon substrate. The increase in the interface traps degrades the subthreshold swing of the devices [\[26\]](#page-11-21). The formula for *SS* is [\[21,](#page-11-15)[30\]](#page-12-1):

$$
SS = (In10) \left(\frac{KT}{q}\right) \left(\frac{C_{ox} + C_D + C_{it}}{C_{ox}}\right)
$$
 (2)

$$
C_{it} = q^2 D_{it} = \beta N_{it} \tag{3}
$$

where *K* is the Boltzmann constant, *T* is the absolute temperature, C_D is the depletion layer capacitance, C_{it} is the interface traps capacitance, D_{it} is the interface traps density, and β is the correlation coefficient. Therefore, the within-batch variability of subthreshold swing increases after irradiation.

The variability of maximum transconductance is negatively correlated with the interface traps variability, while the variability trends of maximum transconductance and subthreshold swing are opposite. The formula for *GMMAX* and *Nit* is [\[2](#page-11-1)[,31](#page-12-2)[,32\]](#page-12-3):

$$
G_{MMAX} = G_{M0} \frac{1}{1 + \alpha N_{it}} \tag{4}
$$

where *GM*⁰ and *GMMAX* are the maximum transconductance values before and after irradiation, and α is the process fluctuation constants of the devices.

Figure [9](#page-9-0) shows the relation between the shift of output capacitance (∆*Coss*) and *N_{ot}* of the within-batch devices after irradiation. As seen from the fit curve in Figure [9,](#page-9-0) the variation in ∆*COSS* and the *Not* presents the exponential growth trend. Therefore, the variability of output capacitance increases sharply at 25 krad(Si) in Figure [3.](#page-4-1) The output capacitance is equal to the sum of the drain-source capacitance and the gate-drain capacitance. The drain-source capacitance is the junction capacitance, which is not changed by the increase in radiation dose [\[19](#page-11-13)[,33\]](#page-12-4). Therefore, the variation in output capacitance induced by TID is mainly affected by the gate-drain capacitance, which is a function of oxide capacitance, reverse capacitance, and depleted capacitance [\[33,](#page-12-4)[34\]](#page-12-5). The output capacitance is sensitive to *Not*, so as to characterize the correlation between *COSS* and *Not*.

Figure 9. Relation between the shift of output capacitance (∆ைௌௌ) and the oxide-trapped charge **Figure 9.** Relation between the shift of output capacitance (∆*COSS*) and the oxide-trapped charge (N_{ot}) of the devices after irradiation.

The on-state resistance is regulated by the channel reverse voltage ($V_{GS} - V_{TH}$), which is closely related to the *N*^{*ot*} [\[25](#page-11-20)[,35\]](#page-12-6). Because *V*^{*GS*} is much larger than the variation in *V*^{*TH*}, the variability of oxide trapped charges have no obvious effect on the variability of $R_{DS(ON)}$.

In general, the accumulation of trapped charges after irradiation magnifies the process differences of devices in the same batch and leads to differential variability in threshold voltage, subthreshold swing, maximum transconductance, output capacitance, and diode forward voltage. The correlations between the variations in electrical parameters and the trapped charges after irradiation are shown in Table [3.](#page-10-0) However, the variation in electrical parameters of devices in the same batch is a disadvantage to the stability and reliability of the spacecraft, which would lead to thermal failure, an unreasonable dead zone, or gate resonance problems in the circuit module. The differences in threshold voltage and output capacitance must be considered in the circuit design of space equipment, and the variability of on-state resistance in the same batch can be tolerated after irradiation.

Table 3. Correlation between the variation in electrical parameters and the trapped charges generated by irradiation.

5. Conclusions

Silicon-based VDMOS devices are important components of the power system of spacecraft. However, the VDMOS is sensitive to the TID effect. Moreover, the TID response is sensitive to process variation, behaving as within-batch TID response variability. The within-batch TID response variability on silicon-based VDMOS devices is investigated by the ⁶⁰Co gamma-ray irradiation experiment in this paper. Experimental results show that with the increase in total dose, the variability of the within-batch devices parameters changes. The variability of threshold voltage, subthreshold swing, output capacitance, and diode forward voltage increases after irradiation. Furthermore, the variability of maximum transconductance decreases after irradiation, and the variability of on-state resistance is basically unchanged before and after irradiation. By extracting *Not* and *Nit* induced by TID irradiation in the devices, the relationship between the parameters variation and trapped charges are established, and the reasons for within-batch TID response variability are clarified.

Among them, it should be noted that the variability of threshold voltage and output capacitance within-batch shows different functional trends with the increase in radiation dose. The differences in threshold voltage and output capacitance must be considered in some new spacecraft. The new generation of spacecraft requires higher reliability and better performance of electronic devices. The electrical parameter margins are very small in some circuits. Considering the variability of electrical parameters between the same batch of devices caused by TID can reduce the loss and protect the circuit more accurately. The variability of on-state resistance in the same batch can be tolerated after irradiation in the circuit design of space equipment. This study provides a foundation for the establishment of scientific and reasonable TID effect evaluation and screening methods on the within-batch devices so as to ensure the stability and reliability of the power system of spacecraft.

Author Contributions: Conceptualization, J.C. and Q.Z.; methodology, writing—original draft preparation X.L.; writing—review and editing, J.C.; supervision, Y.L. and Q.G.; data curation, X.C.; formal analysis, P.L. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported in part by the Youth Innovation Promotion Association CAS (2020430), the West Light Foundation of the Chinese Academy of Science under Grant No. 2019- XBQNXZ-A-003, the National Natural Science Foundation of China under Grant 12275352, and the project under Grant No. 2022D14003.

Data Availability Statement: The data presented in this study are available on reasonable request from the corresponding authors.

Conflicts of Interest: The authors declare no conflict of interest.

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