electronics

MDPI

Article

STATCOM Switching Technique Based on a Finite-State Machine †

César Contreras [1], Juan C. Quirós [2], Inmaculada Casaucao [2], Alicia Triviño [2,*], Eliseo Villagrasa [2] and José A. Aguado [2]

[1] Decanato de Investigación, Universidad Nacional Experimental del Táchira, San Cristóbal Sector 5001, Venezuela
[2] Departamento de Ingeniería Eléctrica, Universidad de Málaga, 29071 Málaga, Spain
* Correspondence: atc@uma.es
† This paper is an extended version of our paper published in IEEE.

Abstract: The Voltage Source Converter (VSC) is the basis of STATCOMs and other power systems. It is composed of a three-phase inverter in which the activation of the switching devices must be controlled to generate the intended signals. The control technique used to switch the power devices affects the performance of the converter in terms of harmonic distortion mainly. Although some complex modulation techniques have been proposed in the related literature, local controllers opt for simpler methods as they provide robustness and they ease the implementation. In this paper, we propose a simple but effective technique to switch the transistors of a three-phase inverter with a Space Vector Modulation (SVM) supported by a Finite-State Machine (FSM). With this model, the switching technique can be easily implemented in low-cost microcontrollers with reduced memory and computational resources if code optimisation is performed. With an electrical analysis, we have designed a low-pass band filter adequate for the proposed switching technique. In a laboratory prototype, the performance of this proposal is evaluated under static and dynamic conditions. When compared with other control techniques (classical SVM and PWM), we conclude that a similar harmonic distortion is achieved.

Keywords: voltage source converter; three-phase inverter; PWM; SVM; finite-state machine

Citation: Contreras, C.; Quirós, J.C.; Casaucao, I.; Triviño, A.; Villagrasa, E.; Aguado, J.A. STATCOM Switching Technique Based on a Finite-State Machine. *Electronics* **2023**, *12*, 1481. https://doi.org/10.3390/electronics12061481

Academic Editor: Sheldon Williamson

Received: 30 January 2023
Revised: 9 March 2023
Accepted: 17 March 2023
Published: 21 March 2023

1. Introduction

Power systems are evolving to a more sustainable production in which renewable energy sources are relevant assets. However, their intermittency poses new challenges to address. Voltage deviations and harmonic distortion are the main effects of uncontrolled integration of renewable energy sources into the grid. To overcome some of these problems, modern wind and photovoltaic (PV) farms incorporate a voltage and reactive power control system to regulate the voltage at the point of connection (POC) [1]. For this purpose, the integration of these plants is commonly supported by voltage compensators, such as the static synchronous compensator (STATCOM), in order to comply with the grid codes.

STATCOMs help in the voltage stabilisation and correction of the power factor. Its operating principle is based on the injection of controlled currents so that it can absorb or supply reactive power at the load connection point to the grid as demanded. Centralised or distributed algorithms decide the amount and features of the current that a set of STATCOMs must provide [2]. With this command, each STATCOM configures its internal components to reach the preset goal [3]. The basis of a STATCOM is a voltage source converter (VSC). A VSC can be defined as a power converter that transforms a DC voltage (e.g., from a photovoltaic plant or converted from a wind power plant) into three alternating signals with a 120º phase shifting with respect to each other. These output signals or phases are identified as $R - S - T$. In the case of a two-level three-phase inverter, the electronic circuit corresponds to that illustrated in Figure 1, where there is a DC voltage source (V_{DC}) and six switches in three parallel branches [4]. In this case, the IGBT symbol

has been selected to represent the switches, as they are common for the integration of renewable energy sources. The outputs are obtained from the connections with regard to the neutral point.

The variation of each output signal (between V_{DC} and $-V_{DC}$) is achieved by alternatively closing and opening the switches of each branch. The phase shift of the three signals is achieved by adjusting the activation sequence of the switches. In order to generate the VSC switching or control signals, a wide diversity of methods has been studied and applied. Differences in their mode of operation have been developed to achieve one or more of the following objectives: wide linear modulation range, reduced switching losses, lower total harmonic distortion (THD), easy implementation and shorter computation time [5–7].

Although inverters have been traditionally designed as analogue circuits, these converters are more often activated by microcontrollers nowadays [8,9]. Among the control methods applied by these microcontrollers, three different solutions can be highlighted: voltage input variation, pulse bandwidth variation, pulse width modulation (PWM), sine pulse width modulation (SPWM), or space vector modulation.

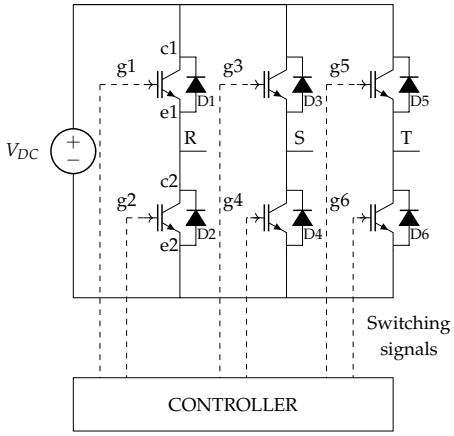


Figure 1. Schematic of a basic three-phase VSC.

Since the use of microcontrollers is common, SVM has become one of the most important methods for three-phase converters. In this case, the space vector concept is used to calculate the duty cycle of the switches. Generally, SVM involves the sequence of the following phases: (i) sector identification, (ii) calculation of switching times, (iii) determination of the switching vector and (iv) selection of the optimal switching sequence for the inverter voltage vectors. In Ref. [8], the authors describe an example of a modified approach to space vector modulation technique implemented on a low-cost PIC 18F4431 microcontroller. As stated by the authors, with this type of modulation it is digitally easy to implement the control of the switching devices.

Since the use of VSC is getting more widespread in applications such as renewable energy, high-voltage DC transmission (HVDC), the flexible AC transmission system (FACTS), and smart grids [10–12], it is important to provide effective, simple and robust mechanisms to correctly perform the switching operation. The aim of this work is to propose a switching technique based on a finite-state machine (FSM), which stands out as a simple mechanism to generate the inverter control signals. FSM is a conceptual machine used to model the behaviour of objects. This behaviour is defined in different states. The transition through the states is caused by the occurrence of some events. Due to this conceptualisation, FSMs are more in accordance with the discrete performance of a programmable device such as a microcontroller, making these types of controls easier to implement and monitor. Finite-state machines have already been used for the characterisation of power electronics devices. The switching operation of power devices is characterised with this type of model for SiC MOSFET [13] and for Si-SiC hybrid switches [14]. In Ref. [15], the authors propose a fault diagnosis method to detect multiple transistor open-circuit faults in a three-level T-type

inverter with the support of a finite-state machine. As for the control, the suitability of FSM has also been validated for DC–DC converters [16].

In Ref. [17], we identified the states and transitions to describe a FSM for the switching control of a VSC. The main advantage provided by this control technique is its capability to be implemented in low-cost microprocessors. This promotes the reduction in costs in low-power renewable installations, such as those oriented for self-consumption. The simplification also helps to reduce the complexity of converter-monitoring. In addition to the simplification that this method provides, the proposal is able to maintain similar harmonic distortion than conventional methods such as PWM and SVM. This paper extends our previous work with four main topics: (i) the analysis of the filter to be placed at the output of the VSC, (ii) a comprehensive and theoretical analysis of the performance provided by the proposed switching technique under static and dynamic conditions, (iii) design of an optimised coding for the proposed control, which is valid for low-cost microcontrollers, and (iv) lab-test evaluations with a proof-of-concept.

The main contributions of this work are:

- Proposing an effective and simple mechanism to proceed with VSC-switching based on SVM. The method is supported by a FSM, which enables the implementation of the method in current microcontrollers with computational and memory constraints.
- Analysing the effects of the low-pass band filter in the proposed method.
- Simulation-based study of the performance of the controller when there are changes on the grid's main features or on the commands of the STATCOM.
- Evaluating the proficiency of the proposed controller in comparison with PWM and conventional SVM. We observed similar harmonic distortion for the three switching techniques. The compliance with ANSI/IEEE-519 has also been verified.
- Defining an optimal coding of the control so that it can be executed in a low-cost microcontroller, widely available in the market.
- Evaluating the proposed control with a proof-of-concept implementation in our lab. There is good agreement between the simulated data and the measurements.

The rest of this paper is structured as follows. Section 2 presents the details of SVM vector space modulation. Then, Section 3 develops the proposed method, that is, SVM modulation based on a finite-state machine (SVM-FSM). Section 4 addresses the design of the LC filter at the inverter output. In Section 5, the performance of that proposed is evaluated with respect to PWM and SVM. The control implementation is described in Section 6, while the experimental results are shown in Section 7. Finally, in Section 8, the conclusions are presented.

2. Space Vector Modulation: Fundamentals

For a VSC, there are two types of switching sequences. The first type consists in forcing the conduction to 120° electrical. This implies that the excitation signals for each switch last 120° and are conducted two at a time ($g_1g_6 - g_1g_2 - g_2g_3 - g_3g_4 - g_4g_5 - g_5g_6$). The second option is based on the conduction to 180° electrical. In this case, three transistors are active at a time ($g_4g_6g_2 - g_1g_5g_6 - g_1g_2g_6 - g_1g_2g_3 - g_2g_3g_4 - g_3g_4g_5 - g_4g_5g_6 - g_1g_3g_5$) [18]. Imposing three switches to be active at the same time in this last approach allows higher power levels to be delivered to the load, so this is the most common option. However, short-circuits must be avoided [19].

A different way to represent the alternating signals generated by the inverter is the consideration of a reference frame that rotates at the fundamental frequency of signals, obtaining a plane of two $\alpha - \beta$ axes, known as vector representation. To calculate the vectors, the Clarke transform Equation (1) is used, obtaining the hexagon in Figure 2, with seven voltage vectors and two null vectors. Each of these vectors corresponds to a combination of switches in the active state. For a conduction of 180°, the vectors are 60°

apart, with a length of $\frac{2}{3}V_{DC}$. A more extensive description of the basic concepts of this transform can be found in Ref. [20].

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \quad (1)$$

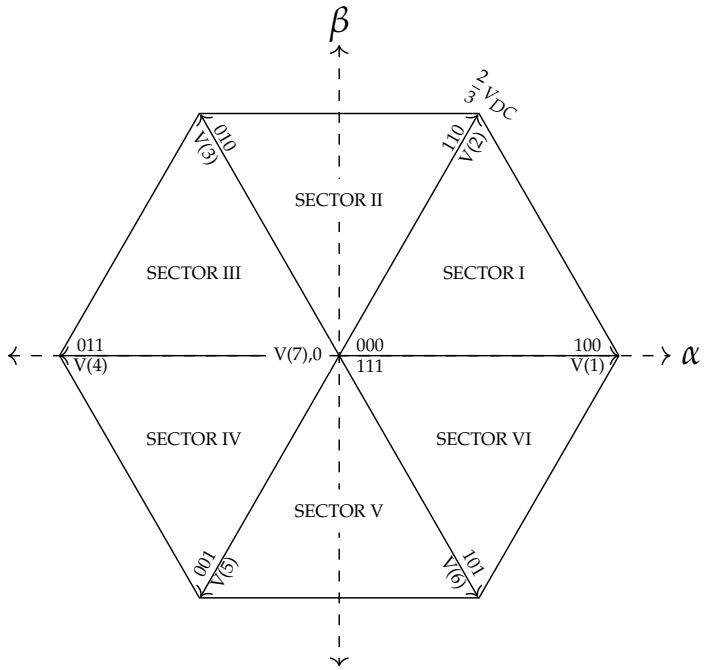


Figure 2. VSC vector diagram.

The voltages are listed in Table 1. Each state/voltage ($V(k)$) generated with the SVM is related to a group of three activation states (first column in Table 1). These variables model g_1, g_3 and g_5 control signals in the order as they are mentioned. The variables g_2, g_4 and g_6 are complementary to the previous signals.

Table 1. VSC-generated voltages.

g_1	g_3	g_5	$V(k)$	Voltage	Complex Voltage
Off	Off	Off	$V(0)$	0	$0\,e^{0j}$
On	Off	Off	$V(1)$	$\frac{2}{3}V_{DC}$	$\frac{2}{3}V_{DC}\,e^{0j}$
On	On	Off	$V(2)$	$\frac{1}{3}V_{DC} + j\frac{\sqrt{3}}{3}V_{DC}$	$\frac{2}{3}V_{DC}\,e^{\frac{\pi}{3}j}$
Off	On	Off	$V(3)$	$-\frac{1}{3}V_{DC} + j\frac{\sqrt{3}}{3}V_{DC}$	$\frac{2}{3}V_{DC}\,e^{\frac{2\pi}{3}j}$
Off	On	On	$V(4)$	$-\frac{2}{3}V_{DC}$	$\frac{2}{3}V_{DC}\,e^{\frac{3\pi}{3}j}$
Off	Off	On	$V(5)$	$-\frac{1}{3}V_{DC} - j\frac{\sqrt{3}}{3}V_{DC}$	$\frac{2}{3}V_{DC}\,e^{\frac{4\pi}{3}j}$
On	Off	On	$V(6)$	$\frac{1}{3}V_{DC} - j\frac{\sqrt{3}}{3}V_{DC}$	$\frac{2}{3}V_{DC}\,e^{\frac{5\pi}{3}j}$
On	On	On	$V(7)$	0	$\frac{2}{3}V_{DC}\,e^{0j}$

There is a variety of techniques used for the generation of switching trigger patterns. However, they can all be classified into sine modulation and the vector modulation technique. The latter consists of determining the linear combination of the virtual voltages (V_a, V_b and V_0) that conform the intended voltage (V_{ref}) during the interval (T_{sw}).

The generation of the three-phase voltages is related to the variation of the reference voltage in a clock-wise way. Thus, every time during a complete period, V_{ref} is in a specific position so that it must be modelled with a particular combination of the virtual voltages corresponding to the sector where it is placed. Thus, the modelling with the virtual voltages is time-dependent. The virtual voltages V_a and V_b depend on the sector on which

the voltage is located. Each reference vector is active only during a fraction of the complete period T_{sw}. Specifically, V_a contributes to the generation of V_{ref} during T_a, whereas V_b is used during T_b, being $T_a < T_{sw}$ and $T_b < T_{sw}$. In order to unify the concept to compare the PWM and SVM techniques with the proposed method, the switching frequency has been taken as $f_{sw} = \frac{1}{T_{sw}}$. To compute this combination, the following Equations (2) and (3) are used.

$$\begin{aligned} V_{ref} T_{sw} &= V_a T_a + V_b T_b + V_0 T_0 \\ T_{sw} &= T_a + T_b + T_0 \end{aligned} \tag{2}$$

Since $V_0 = 0$, then

$$V_{ref} T_{sw} = V_a T_a + V_b T_b \tag{3}$$

The goal of a SVM-based switching technique is to determine how long each vector must be maintained to get the virtual vector V_{ref}. It is said that it is necessary to determine the T_a, T_b and T_0 considering the vectors V_a and V_b in each sector. As previously mentioned, these vectors depend on the specific sector in which the reference voltage is. For illustrative purposes, Figure 3a shows the vectors V_a and V_b for Sectors I and II.

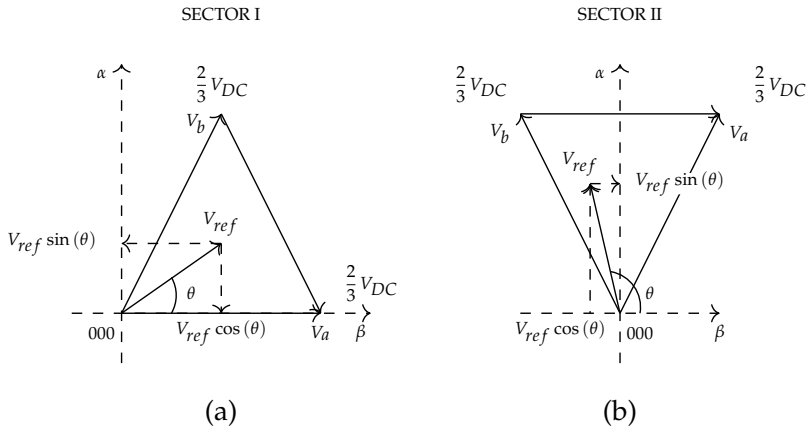


Figure 3. Virtual vectors in (**a**) Sector I and (**b**) Sector II.

Supported by a trigonometry analysis, it is possible to derive the equations of the times associated with each sector, as shown in Table 2. For a voltage value V_{ref} in Sector n with $n \in \{1, 2, 3, 4, 5, 6\}$, Equations (4)–(6) are general expressions to calculate T_a, T_b y T_0 times.

$$T_a = \sqrt{3}\frac{V_{ref}}{V_{DC}} T_{sw} \sin\left(n\,\frac{\pi}{3} - \theta\right) \tag{4}$$

$$T_b = \sqrt{3}\frac{V_{ref}}{V_{DC}} T_{sw} \sin\left(\theta - (n-1)\,\frac{\pi}{3}\right) \tag{5}$$

$$T_0 = T_{sw} - (T_a + T_b) \tag{6}$$

As the purpose of the inverter is to generate a three-phase periodic sine wave, then it is necessary to determine the electrical angle and sector by using a timer. Thus, the voltage V_{ref} varies and the times T_a, T_b and T_0 are accordingly computed. A dynamic determination of the sector must be accomplished. For a generic time instant t, the electric angle $\theta = wt$, where $w = 2\pi f$ is calculated. Then, the number of turns is determined, that is, how many times the value 2π is reached in wt, and that number is subtracted from wt to leave only the decimal part using the following formula: $wt -$ integer part$(wt/2\pi)$. In this way, only the angle between $0 - 2\pi$ is obtained. Moreover, since sectors are separated by 60° $(\pi/3)$,

then it is determined how many fractions of $\pi/3$ can be computed in the decimal part calculated above, using the Equation (7).

$$n = 1 + \frac{wt - \text{integer}\left(\frac{wt}{2\pi}\right)}{\frac{\pi}{3}} \tag{7}$$

Table 2. Equations for calculating times in each sector.

Sector I	Sector II	Sector III
$T_a = \frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\frac{\pi}{3} - \theta) T_{sw}$ $T_b = \frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta) T_{sw}$	$T_a = \frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta + \frac{\pi}{3}) T_{sw}$ $T_b = \frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta - \frac{\pi}{3}) T_{sw}$	$Ta = \frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta) T_{sw}$ $T_b = -\frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta + \frac{\pi}{3}) T_{sw}$
Sector IV	**Sector V**	**Sector VI**
$T_a = -\frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\frac{\pi}{3} - \theta) T_{sw}$ $T_b = -\frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta) T_{sw}$	$T_a = -\frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta + \frac{\pi}{3}) T_{sw}$ $T_b = -\frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta - \frac{\pi}{3}) T_{sw}$	$Ta = -\frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta) T_{sw}$ $T_b = \frac{3}{\sqrt{3}} \frac{V_{ref}}{V_{DC}} \sin(\theta + \frac{\pi}{3}) T_{sw}$

3. SVM Supported by a Finite-State Machine (SVM-FSM)

Once the method for determining the electric angle and the sector at time t is known, it is now possible to propose a finite-state machine-based space vector modulation methodology. The application of FSM to model the dynamics of the inverters is feasible due to the discrete nature of these power converters. Switching dynamics can be accurately modelled with a FSM, as mentioned in Ref. [21], for the control of a dual bridge converter, or in Ref. [22] for single-phase inverters. One of the advantages of using finite-state machines is that it makes their digital implementation more systematic and flexible. For example, it could be implemented in a programmable gate array, such as FPGAs, as in the case of Ref. [23]. There are also published results for a photovoltaic power plant [24], where the different operating states or operating modes of the PV plant are sub-models based on finite-state machines working cooperatively. The authors report that the approach seems suitable for simplifying the operating model for renewable energy sources and acceptable simulation runtimes.

As described above, to generate an alternating waveform, switches are closed and opened as follows: a closed switch is fed with a logic 1 and an open switch is fed with a logic 0. In this way, a three-bit code can be constructed with the activation signals of the three upper-level switches (since the three lower-level switches are complementary). Therefore, when the upper level switch is active, the lower level switch on the same branch is open. In Figure 4 the signals of the three upper level switches have been identified with g_1, g_3, g_5. It should be noted, as mentioned above, that in order to generate a virtual vector V_{ref}, V_a must last for a time T_a, V_b must remain for a time T_b, and a time T_0 for the null vector. The latter vector can be achieved with all the top-level switches g_1, g_3, g_5, closed 1 1 1 or open 0 0 0.

As it is recognised from digital techniques, it is important that the changes are one bit at a time. For example, if a reference vector within sector I has to be generated, combination 1 0 0 is used as vector V_a, combination 1 1 0 as vector V_b, and both 0 0 0 and 1 1 1 for null vector V_0. The sequence of these virtual vectors could be set out in multiple ways, but we will opt for that in which two successive virtual vectors used for the generation of V_{ref} differ in only one bit. In Figure 4, seven different combinations are generated for each sector. For the seven combinations, the intervals in which the signals g_1, g_3 and g_5 are constant have the same duration ($T_0/2$). Another detail that can be observed in all the time diagrams is that four pulses are interleaved. They are identified by colours in Figure 4, and can be distinguished by their own duration: the first one is yellow and has a duration of $T_1 = T_a + T_b + T_0/2$, the second one is red and it appears only in odd sectors, with a duration of $T_2 = T_b + T_0/2$, the third is blue and it appears only in even sectors with a

duration of $T_3 = T_a + T_0/2$. The last one is green, with a duration of $T_4 = T_0/2$. We use these patterns to model four finite-state machines associated to T_1, T_2, T_3 and T_4.

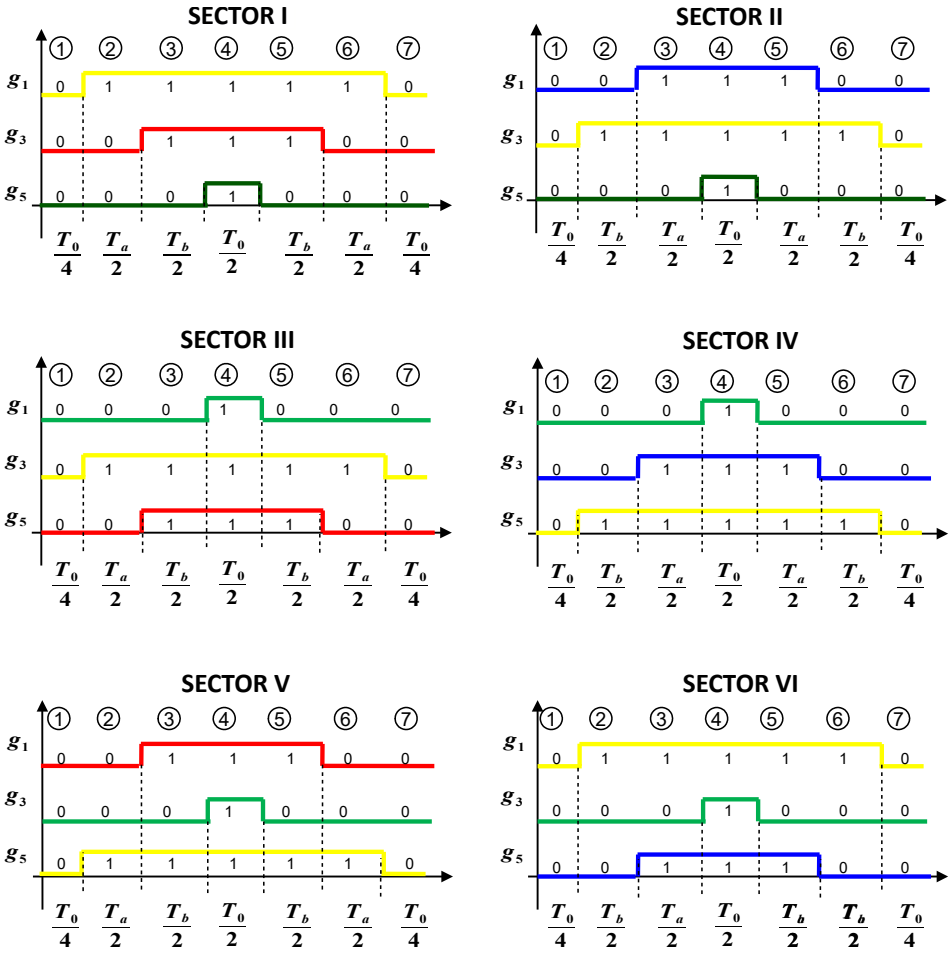


Figure 4. Time diagrams for each sector.

In addition, we also identify the fifth finite-state machine to assign to each gate the pattern corresponding to the sector in which V_{ref} is placed. Figure 5 shows the diagram of this FSM. We can observe the association of the gate and the time patterns and the sequence of the sectors in Figure 6.

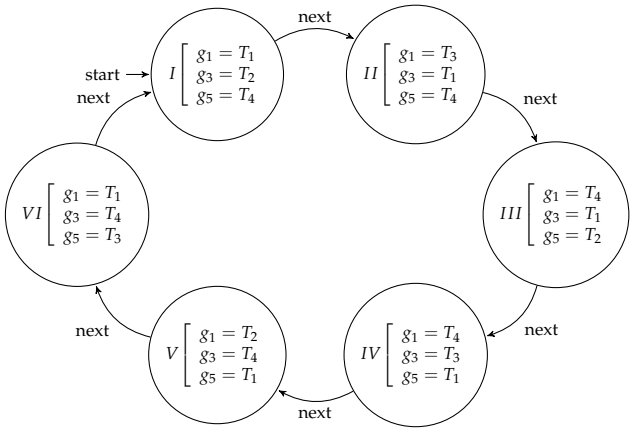


Figure 5. Machine states of the switching signals, depending on the sector.

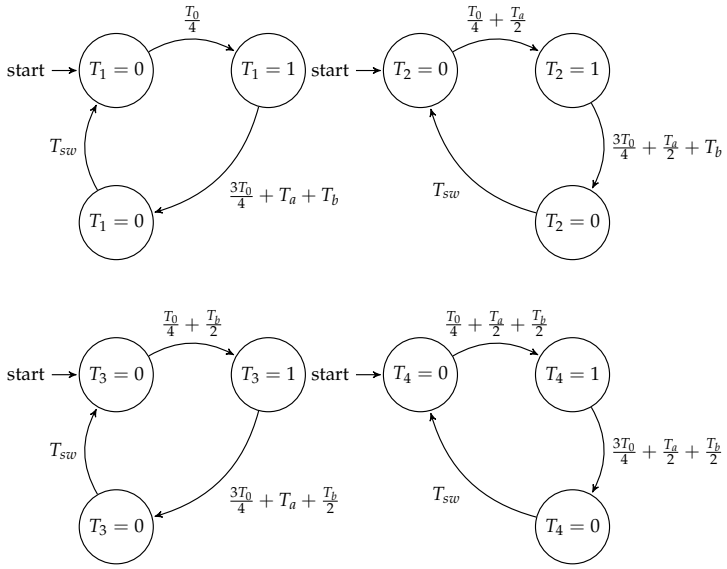


Figure 6. Finite-state machines that model the activation patterns.

4. Design of the LC Filter

The output of the inverter is a digital signal. To derive a sine-wave signal, a low-pass filter is necessary. The *LC* low-pass filter is used to attenuate the low-order harmonics of the output voltage in order to minimise distortion of both linear and non-linear loads.

Figure 7 shows the most simple schematics for this type of filter, which is widely used in inverters connected to the grid [25,26]. It is composed of a capacitor C and a coil with inductance L and parasitic resistance R_L. The resistance R_o corresponds to the output load. There are different criteria to design this type of filter. We will proceed with a specific design based on the behaviour of the VSC and its modelling on a FSM.

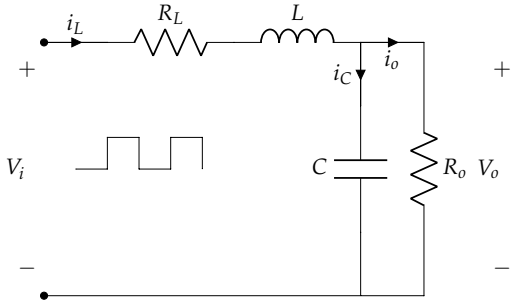


Figure 7. One-phase LC-filter for FSM-based control.

With a circuital analysis, we can derive that:

$$\frac{V_o}{V_i} = \frac{\frac{R_0}{R_0+R_L} w_0^2}{w^2 + 2 \cdot \varsigma \cdot w_0 \cdot w + w_0^2} \tag{8}$$

where the cut-off angular frequency is defined as:

$$w_0 = \sqrt{\frac{R_0 + R_L}{R_0 \cdot L \cdot C}} \tag{9}$$

and the damping factor is:

$$\varsigma = \frac{R_0 \cdot R_L \cdot C + L}{\sqrt{(R_0 + R_L) \cdot R_0 \cdot L \cdot C}} \tag{10}$$

In order to reduce the value of the inverter impedance, the capacitance must be increased and the inductance has to be minimised as a function of the filter cut-off frequency f_0. This allows the cost, volume, and therefore, weight of the inverter to be reduced. However, the increase in capacitance leads to an increase in the inverter power with the rise of reactive power. Therefore, there is a trade-off between these three inverter parameters.

From the definition of inductance, the inductor voltage is determined as follows:

$$V_L = L \cdot \frac{\Delta I_L}{\Delta T} \tag{11}$$

where $\Delta T = \delta T_{sw}$, and δ is the maximum duty cycle for the switching control of the VSC. In Figure 4, the maximum duty cycle is identified with the yellow signal, and its value corresponds to $\delta T_{sw} = \frac{T_0}{2} + T_a + T_b$.

To determine an approximate value for the duty cycle, the general expressions (4)–(6) are substituted into the Equation (11). The expression δ is determined by simplifying Equations (12) and (13) and is shown below Equation (14):

$$\delta T_{sw} = \frac{T_{sw} + \sqrt{3}\frac{V_{ref}}{V_{dc}} T_{sw} \sin\left(n\frac{\pi}{3} - \theta\right) + \sqrt{3}\frac{V_{ref}}{V_{DC}} T_{sw} \sin\left(\theta - (n-1)\frac{\pi}{3}\right)}{2} \tag{12}$$

Taking $n = 1$ (sector I) and considering that the rest of the sectors are calculated in the same way, then:

$$\delta = \frac{1 + \sqrt{3}\frac{V_{ref}}{V_{DC}} \sin\left(\frac{\pi}{3} + \theta\right)}{2} \tag{13}$$

In Equation (13), we replace $V_{ref} = \frac{V_{DC}}{3}$, a value with which the overmodulation is avoided. As we are looking for the maximum duty cycle, then we choose $\theta = \frac{\pi}{6}$, which is where it takes the maximum value, resulting in Equation (14).

$$\delta = \frac{1 + \frac{\sqrt{3}}{3}}{2} = 0.788 \approx 0.79 \tag{14}$$

This means that $\Delta T \approx 0.79 T_{sw}$. However, the standard requirements [27] consider a limit of 0.75, which corresponds with a $\delta = \frac{3}{4}$. Once the value of the duty cycle has been determined, an expression for the inductance L can be obtained. The modulus of the complex voltage at the output of the inverter according to Table 1 is $\frac{2}{3}V_{DC}$, which corresponds to the V_i of the filter, if the output V_0 of the filter is limited to $\frac{1}{2}V_{DC}$ and is considered to vary slowly with respect to the switching frequency. Then, the inductor voltage, which is given by $V_L = V_i - V_0$, leads to $V_L = \frac{1}{6}V_{DC}$. The value of the inductor L can be obtained from Equation (15).

$$L = \frac{V_{dc}}{8 \cdot \Delta I_L \cdot f_{sw}} \tag{15}$$

The standard requirements [27] also contemplate for the current variation Δ to be between 15–20% of the nominal current (I_n) of the inverter. The current variation can be determined from the inverter power (S_n) and line nominal voltage (V_n), as shown in Equation (16).

$$\Delta I_L = \Delta \cdot I_n = \Delta \cdot \frac{S_n}{\sqrt{3}V_n} \tag{16}$$

The SVM-FSM technique is going to be evaluated under the following conditions. The inverter feeds a load consuming a power of $S_n = 5$, kVA with a line nominal voltage $V_n(RMS) = 155$ V , where the fundamental frequency is $f = 60$ Hz. The switching frequency is $f_{sw} = 2000$ Hz, $V_{DC} = 400$ V, and the reference three-phase peak voltage value is $V_{ref} = 150$ V.

With these conditions, we apply the Equation (16). The first step is to obtain the maximum current value for the inductor $I_n = 18.62$ A. Considering a current variation or inductor ripple of 15%, we have a value of $\Delta I_L = 2.79$ A. To calculate the inductance, these values are replaced into Equation (15), with a result of $L = 8.90$ mH.

5. Analysis of the Proposed SVM-FSM Method

The evaluation of the proposed switching technique is performed in a simulation tool. Specifically, we have used Simulink/Matlab, which counts with the package Stateflow to model the finite-state machines [28]. As described before, a control that generates a correct firing sequence in the switches and, thus, generates a three-phase waveform is essential. Therefore, a stage that generates the three waves with a 120° phase shift is needed. The total implemented circuit consists of three stages: the control stage based on finite-state machines (since the gates of the switches must be controlled under a periodic sequence), the sine wave generation stage constituted by the set of switches, and the filtering stage based on the LC filter. The state machines designed in Section 3 have been implemented in Matlab Stateflow. Another important aspect to be taken into account with respect to the state machine is the clock signal that controls the changes of the sequence generating both the angle and the sector. With these data, the times are computed, and it helps to check the conditions that lead to the transitions of a state.

Pulse width modulation (PWM) and vector space modulation (SVM) generators have been implemented to qualitatively compare the designed SVM-FSM method and these two widely used generators. The inverter was implemented with the *LC* filter feeding a 155 V, 5 kVA load, as can be seen in Figure 8. The trigger pattern generator (controller) is located at the bottom, its outputs being the signals to activate/deactivate each switch. Figure 9 corresponds to the submodel of the generator SVM-FSM. We have modelled the following blocks: (i) one block to determine the times according to Equations (4)–(6) and (ii) the block to determine the sector, based on the Equation (7). Then the state machine in Figures 5 and 6 were also implemented in the block FSM.

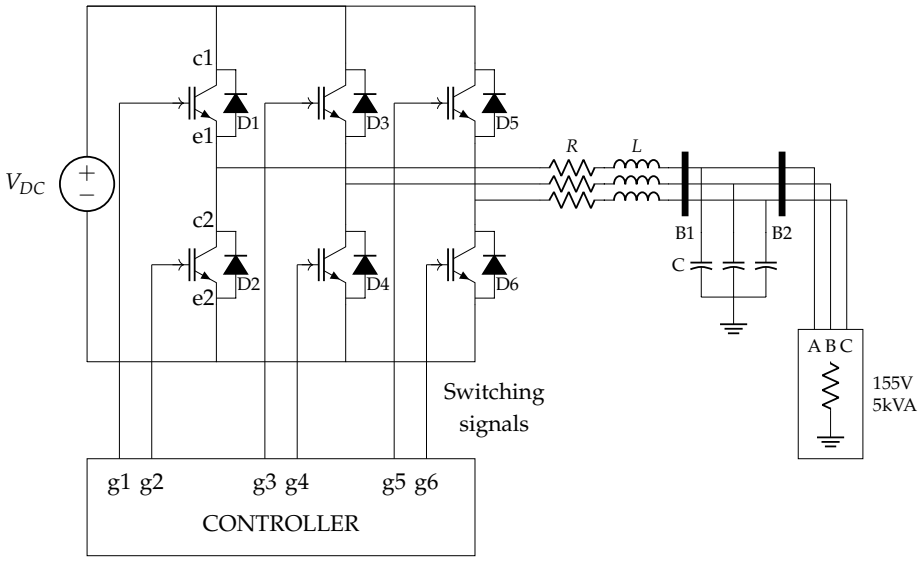


Figure 8. Modelling of the VSC in Matlab/Simulink.

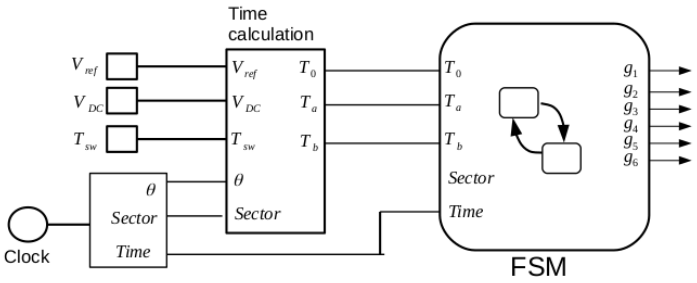


Figure 9. Switching control based on SVM-FSM.

The proposed control technique was evaluated with three types of tests. In the first one, the impact of the filter is analysed by varying the cut-off frequency. In the second one, the switching frequency is modified to see the effects on the performance of the finite-state machine. Finally, the load is varied to see the time response of the method. These three tests are described next.

The first test was performed to prove that the design of the low-pass band filter clearly impacts on the performance of these switching techniques, as the amount of harmonics and their amplitude depend on the features of this element. The first test consists of using the inductance $L = 8.90$ mH previously computed and applying the cut-off frequency equation. The three capacitance values for the three cut-off frequencies are shown in Table 3. The effective voltage (V_{RMS}) and the total harmonic distortion of the load voltage have been measured for each generator for a sampling time of $T_s = 1$ µs and a simulation time of $T = 0.5$ s. The results obtained for V_{RMS} and THD are shown in Figures 10 and 11, respectively, for each phase of the load output voltage (R, S, T). The distortion depends on the phase, as indicated in Figure 11. The phases are affected by the non-lineal performance of the switching technique in a non-equivalent way. This phenomenon is observed for SVM and SVM-FSM.

Table 3. Capacitor values depending on the cut-off frequency.

f_0 (Hz)	180	300	1000
C (µF)	87.36	31.45	2.83

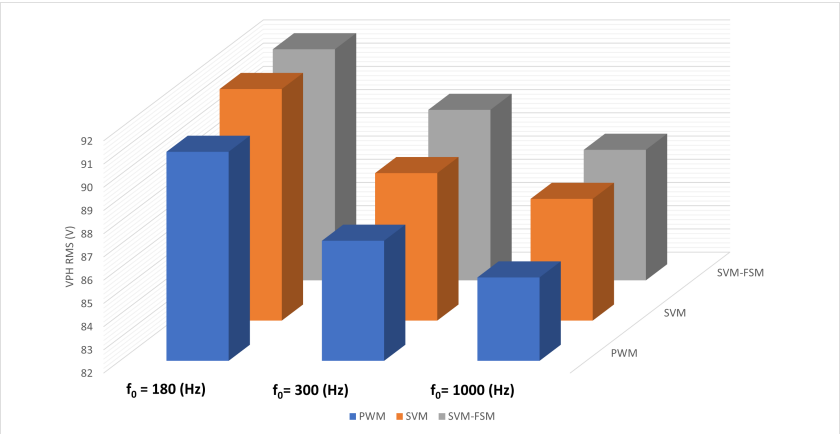


Figure 10. Effective voltage (RMS) depending on the cut-off frequency and modulation type.

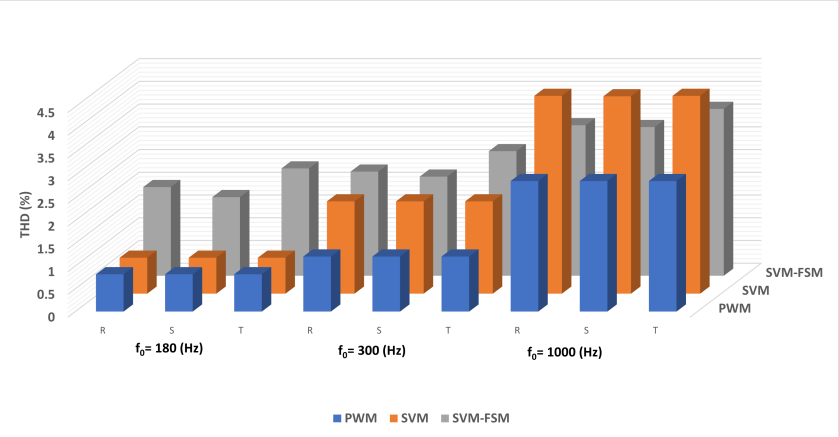


Figure 11. THD depending on the cut-off frequency and modulation type.

In Figure 10 it can be observed that the effective voltage decreases as the cut-off frequency increases for all the configurations. The RMS voltage value (V_{ph}) is similar in all three cases, with a maximum difference of 2 V localised between the PWM and SVM-FSM configuration for a cut-off frequency of 300 Hz.

Figures 12 and 13 show an analysis of the THD levels obtained in two different Harmonic Order (HO) ranges, according to IEEE Std 519 (2014). It can be observed that the limit indicated by the regulations is not exceeded in any case, being 2% for the range $3 \leq \text{HO} < 11$ and 1% for the range $11 \leq \text{HO} < 17$.

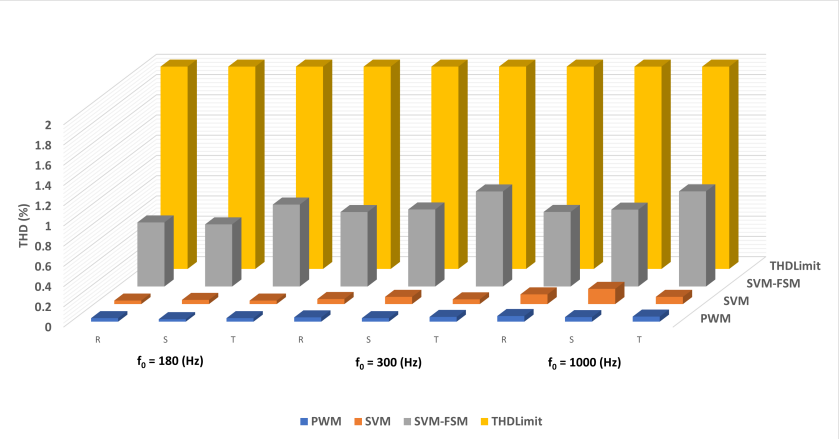


Figure 12. THD limits, according to IEEE Std 519 (2014) ($3 \leq \text{HO} < 11$).

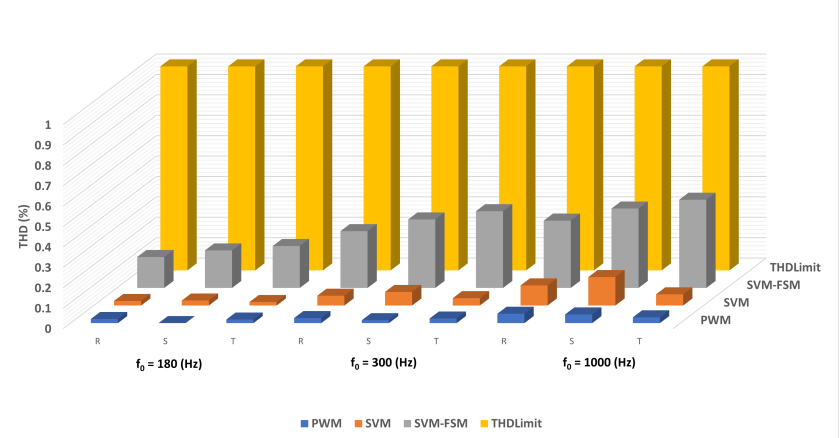


Figure 13. THD limits, according to IEEE Std 519 (2014) ($11 \leq \text{HO} < 17$).

The second test consisted of setting the filter cut-off frequency to $f_0 = 1000$ Hz, which, according to the previous results, shows the worst performance. We aim to evaluate the control technique and the effect of f_{sw} in the worst condition to expand the usability of our proposal. Therefore, we increase the inductor current ripple to $\Delta I_L = 20\%$ and $I_L = 3.72$ A. Then, we compute the inductance and capacitance for three switching frequencies $f_{sw} = 2000,\ 4000,\ 8000$ Hz. The details about the configuration of the filter for these switching frequencies are summarized in Table 4. In the same way, the (V_{RMS}) and THD of the load voltage were measured for the three generators with $T_s = 1$ µS and a simulation time of $T = 0.5$ s. The results obtained are in Figures 14 and 15.

Table 4. Inductor and capacitor values for a cut-off frequency of $f_0 = 1000$ Hz, depending on switching frequency (f_{sw}).

f_{sw} (Hz)	2000	4000	8000
L (mH)	6.7	3.4	1.7
C (µF)	3.77	7.5	15

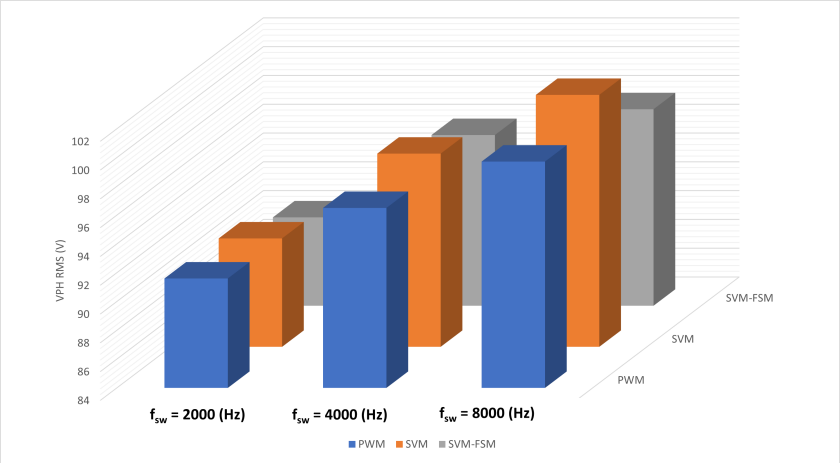


Figure 14. Effective voltage (RMS) depending on the switching frequencies and modulation type.

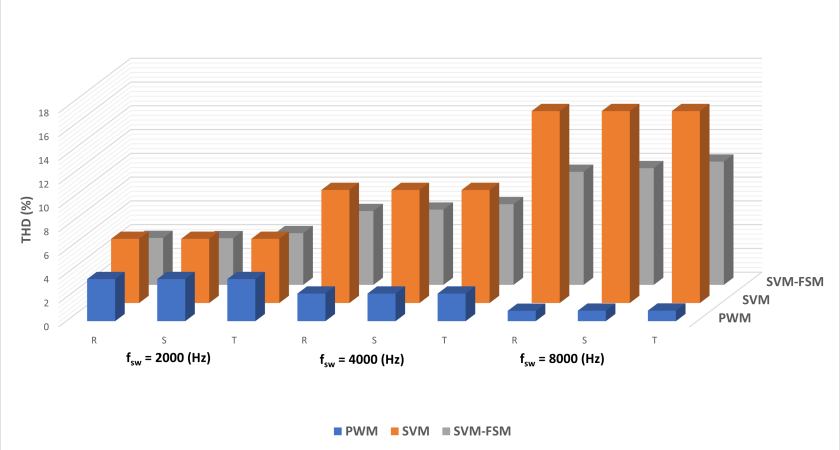
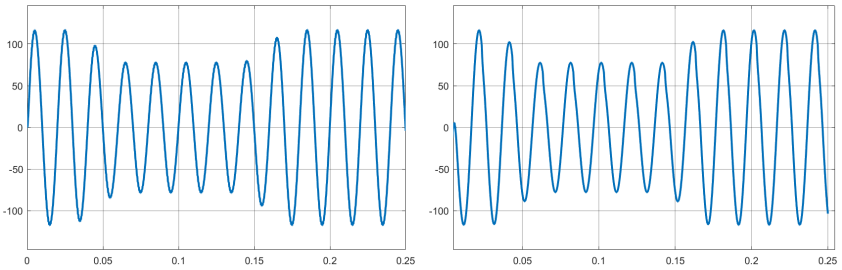


Figure 15. THD depending on the switching frequencies and modulation type.

Figure 14 shows a similar improvement for all three methods when we increase the switching frequency. For the proposed switching technique, there is an up to 9 V increase. In Figure 15, the THD increases when f_{sw} is higher. With this condition, T_{sw} decreases and, therefore, the switching time of the switches between inverter branches is shorter. Consequently, the effects of the non-linearity of the inverter are more notable. Our method

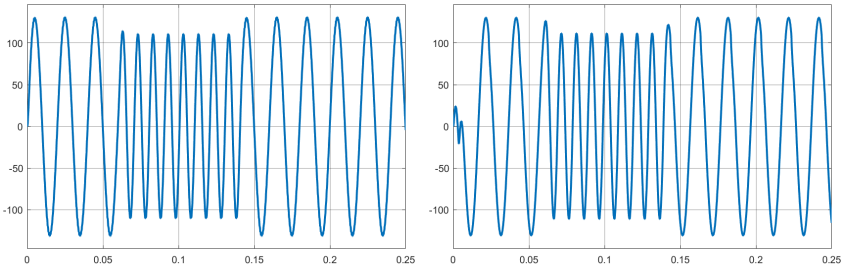
is robust since the lower the f_{sw}, the better the performance is achieved. The best results are obtained at $f_{sw} = 2000$ Hz, that is, more switching time and therefore less power losses due to the switching effects [29]. The complexity required for the microprocessor is also decreased as the operations can be executed in longer intervals.

Finally, the technique has been evaluated when there are changes on the goal or grid conditions. The parameters established in these experiments are: $f_0 = 180$ Hz, $\Delta = 15\%$ and $f_{sw} = 2000$ Hz, where the filter results in $C = 87.36$ µF and $L = 8.9$ mH. Specifically, we have tested how the control performs when (i) the reference voltage is variable from 150 V to 100 V and back to 150 V; (ii) the fundamental frequency abruptly changes from 50 Hz to 100 Hz and back to 50 Hz; and (iii) the fundamental frequency varies gradually (with a ramp), from 50 Hz to 100 Hz and back to 50 Hz. The waveforms are depicted in Figures 16–18.



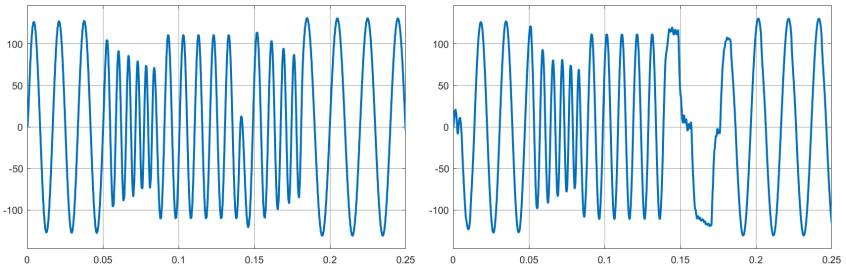
(**a**) (**b**)

Figure 16. Load voltage waveform with $f_0 = 180$ Hz, $\Delta = 15\%$ and $f_{sw} = 2000$ Hz, Variable reference voltage (**a**) SVM, (**b**) SVM-FSM.



(**a**) (**b**)

Figure 17. Load voltage waveform with $f_0 = 180$ Hz, $\Delta = 15\%$ and $f_{sw} = 2000$ Hz, instantaneous change of operating frequency (**a**) SVM, (**b**) SVM-FSM.



(**a**) (**b**)

Figure 18. Load voltage waveform with $f_0 = 180$ Hz, $\Delta = 15\%$ and $f_{sw} = 2000$ Hz, ramp-proportional change of the operating frequency (**a**) SVM, (**b**) SVM-FSM.

The simulation time was increased to 2.5 ms with the intention to observe the waveforms properly. As can be observed in Figures 16–18, SVM and SVM-FSM generators are compared. The results show that there is a response time that affects the synchronisation of

the proposed method. It should be noted that as SVM-FSM is a discrete generator, jumps in the signals are more noticeable than in the case of SVM.

The developmental steps, design, and performance evaluation of the proposed method showed that it is easy to implement, which is the greatest strength of the proposal. However, it presents a dependence on the switching frequency, since the method is based on event dynamics.

6. Control Implementation

One of the main goals of the control technique is to achieve an efficient and easy to implement method to switch the power devices. To do so, we carefully programmed ESP8266, a low-cost microprocessor available at most popular electronics dealers. The microcontroller has a L106 32 bit RISC microprocessor running at 160 MHz, with a 32 kB instruction RAM and 80 kB RAM of data. In addition, it has 17 general-purpose input/output pins and wifi, SPI, I2C and UART communication protocols. Considering these restrictions, the coding of the instructions must be well designed to allow the switching frequency intended in the application under study.

From straight-forward coding of the FSM, we identified the more time-consuming instructions in order to optimise their execution with alternative programming. In our coding, we needed to generate a 50 Hz signal with a switching frequency of 2 kHz. This implied that the changes on the V_{ref} must be performed every 500 µs. Thus, the following instructions needed to be optimised:

- Computation of the times T_a and T_b. As they require trigonometric operations, they are more time-consuming. In fact, after measurement, we found that they require almost 300 µs in the microcontroller considered for the application.
- Unnecessary loops which add extra time to the execution of the main programme. These loops are associated to the modelling of the time patterns T_1, T_2, T_3 and T_4 individually.
- Redundant computations that can be simplified. For instance, in the traditional coding of the SVM, the time is computed in each iteration, and from this, the sector in which V_{ref} is placed must be determined so that the correct operations are executed. This operation can be simplified as the position of V_{ref} in two consecutive iterations is in the same sector, or it has moved to the next sector. Most simple operations can be executed to check if the reference voltage has changed to the next sector.

To overcome the aforementioned limitations, we have proceeded with a code optimisation. This process has been achieved with the following steps:

- Memory preallocation of the times T_a and T_b with a precision of 1°.
- Memory preallocation of the sector S with a precision of 1°.
- Joint implementation of the four finite-state machines T_1, T_2, T_3 and T_4 in order to reduce the computational cost.

Once the key factors have been identified, we proceeded to code PWM and SVM so that the performance of the proposed switching method can be evaluated in an experimental setup. Results showed that the memory usage for these control techniques with the same microcontroller was 17,896 bytes, 18,296 bytes, and 19,688 bytes for PWM, SVM, and SVM-FSM, respectively. With this parameter, it can be observed that PWM is the most simple implementation. SVM requires some additional computations to determine the sector, which increases the memory usage. Finally, SVM-FSM makes use of a pre-allocated table, which results in an augmented memory usage.

Algorithms 1 and 2 shows the two pseudo-codes considered in this project. Algorithm 1 stands out for the direct implementation of the method with a simple sequence of phases. Algorithm 2 is the optimised version of the code with a memory preallocation of the times and sector and a joint implementation of the FSM related to the time patterns. The optimisation process was released in order to reduce computational costs and times as computations with a relevant time consumption were eliminated and replaced with a predefined array

of values depending of the current angle. With this optimisation, we aimed to reduce the execution time of a loop to 37.4 µs.

Algorithm 1: Simple implementation

```
1. while (1)
2.   Compute time
3.   Compute angle
4.   Compute Sector
5.   Compute Ta
6.   Compute Tb
7.   Compute T0
8.        States Machine T1
9.        States Machine T2
10.       States Machine T3
11.       States Machine T4
12.       States Machine Switching
13. end while
```

Algorithm 2: Optimised

```
1. Define Ta, Tb, T0 and S
2. while (1)
3.   Compute time
4.   Compute angle
5.   Prestored value of Ta, Tb, T0 and S
6.        States Machine T1, T2, T3, T4
7.        States Machine Switching
8. end while
```

7. Experimental Evaluation

In order to evaluate the effectiveness of the proposed switching technique, we implemented it and two other well-known methods in a real laboratory setup. We illustrate the lab setup in Figure 19. The setup consists of a set of IGBT modules which can be used for a three-phase inverter. These modules have all the necessary security elements, such as short-circuit and over-voltage protections. In addition, these modules also have the necessary drivers to activate the IGBTs.

Simulated and experimental results have been compared. The experiments were implemented for the three different control systems: PWM, SVM and SVM-FSM. Two different switching frequencies have been considered: $f_{sw} = 2000$ Hz and $f_{sw} = 1500$ Hz. Due to the nature of the FSM-SVM algorithm, there are 80 changes from 0 to 1 and 1 to 0 in the IGBTs per AC cycle (for 2000 kHz of carrier signal). In a period of 0.02 s (50 Hz), the IGBTs switch 40 times. The same performance was perceived with PWM and SVM implementations where the carrier was also implemented at 2000 Hz. For an implementation of 1500 Hz, the switching cycles change from 40 to 30, due to its larger period.

VSCs are usually operated with higher input voltages, but due to the laboratory constraints, the maximum input voltage we could test was 50 V. Tables 5 and 6 show a comparison between the simulated and experimental values for the load phase voltage. The experimental results show the same trend as the simulation results. Slight variations can be observed in the experimental results due to the effect of the losses produced in the power converters that have not been considered in the simulation. Comparing the different methods, it can be seen that the RMS voltage values achieved with SVM-FSM are, in most cases, moderately higher than those of the other methods for the same input conditions. It

should be noted that, when the switching frequency was varied from 2000 Hz to 1500 Hz, no significant changes in the RMS voltage value were observed.

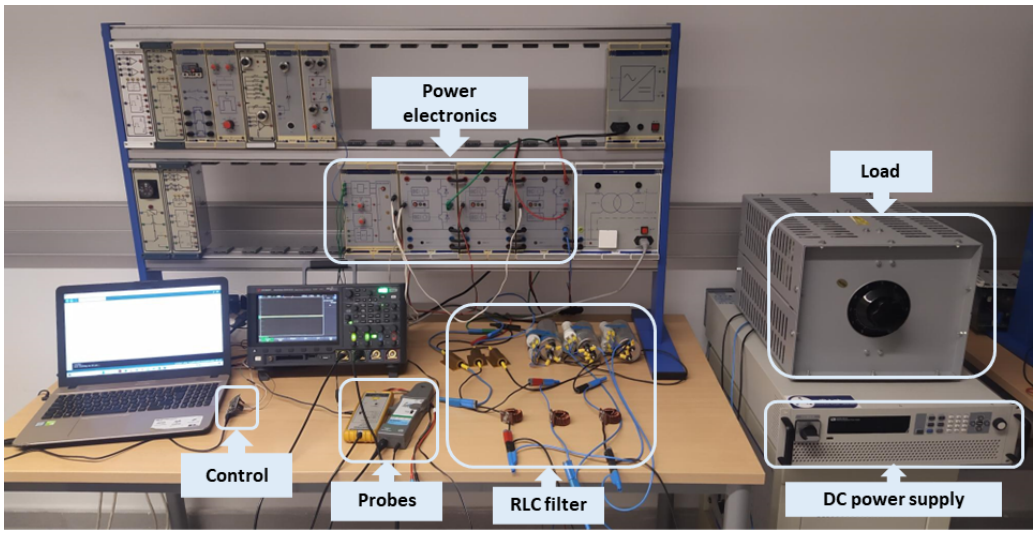


Figure 19. Laboratory setup.

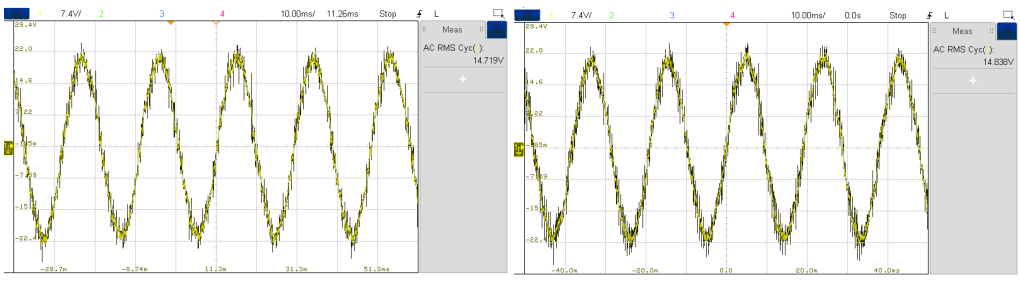
Table 5. Vrms (V), f_{sw} = 2000 Hz.

	SIMULATION			EXPERIMENTAL		
	R	**S**	**T**	**R**	**S**	**T**
PWM	14.23	13.98	14	11.297	12.035	12.693
SVM	16.78	16.49	17.01	13.18	14.002	14.719
SVM-FSM	16.51	16.94	16.59	14.838	15.03	16.289

Table 6. Vrms (V), f_{sw} = 1500 Hz.

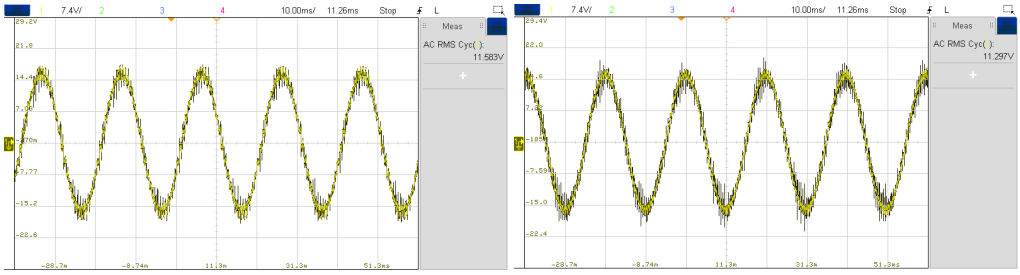
	SIMULATION			EXPERIMENTAL		
	R	**S**	**T**	**R**	**S**	**T**
PWM	14.02	13.86	14.34	11.583	12.271	12.921
SVM	16.81	16.7	16.78	13.344	14.119	14.837
SVM-FSM	16.41	17.13	16.49	14.719	15.546	16.365

Figures 20–22 show the filtered phase R for the SV-FSM, PWM and SVM techniques. The RLC filter was implemented as described in the previous section. The cutoff frequency was established in 180 Hz with $R_L = 1\,\Omega$, $L = 8.9\,\text{mH}$ and $C = 87.63\,\mu\text{F}$. The sinusoidal wave with some added harmonics could be observed, which was a common feature in the three methods tested.



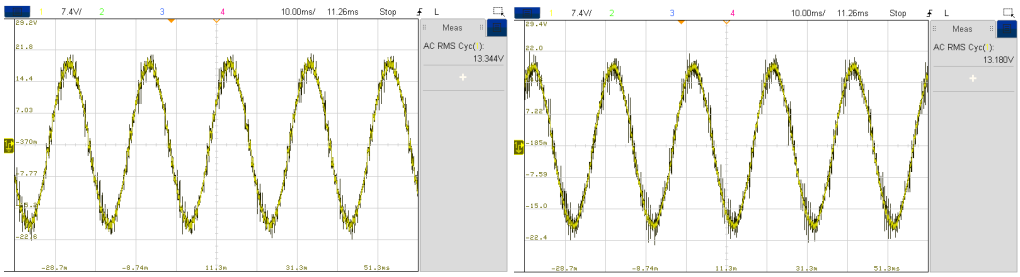
(**a**) f_{sw} = 1500 Hz (**b**) f_{sw} = 2000 Hz

Figure 20. Phase Voltage SVM-FSM.



(**a**) f_{sw} = 1500 Hz (**b**) f_{sw} = 2000 Hz

Figure 21. Phase Voltage SVM.



(**a**) f_{sw} = 1500 Hz (**b**) f_{sw} = 2000 Hz

Figure 22. Phase voltage SVM-FSM.

In addition to the comparison in terms of RMS voltage, an analysis of the THD was performed to each f_{sw} to ensure that the proposed method is compliant with the standard IEEE Std 519 for each technique, both in the simulated and experimental cases. In Tables 7 and 8, the obtained results can be observed. As stated, the divergence between simulated and experimental results is not very significant. These differences may be due to the non-ideality of the filter for the experimental case, which can lead to slight variations in the characterisation of the components. Passive components can also have parasitic parameters that have not been considered in the simulation. Additionally, it has been observed that the differences found between the cases $f_{sw} = 2000$ Hz and $f_{sw} = 1500$ Hz are not remarkable, but also indicates a strong correlation between non-linearities and the frequency of the case of study, resulting in an inferior THD when the frequency is lower. The non-linear performance is not equivalent for the three phases, due to the fact that the processing times in the microcontroller do not affect each phase in a uniform way (the angle at which there are some deformations on the sinusoidal wave is different for each phase). This could explain the differences on the THD for each phase, as it has already been identified in Refs. [30,31]. Moreover, these effects are strongly dependent on the switching frequency and on non-perfectly balanced loads. A deep analysis should be performed to avoid this effect, which was present in the three switching techniques tested. The work in Ref. [32] argues that the modulation index should be carefully set to avoid some of these effects.

Table 7. THD (%), f_{sw} = 2000 Hz.

	SIMULATION			**EXPERIMENTAL**		
	R	**S**	**T**	**R**	**S**	**T**
PWM	0.39	0.39	0.39	0.795	0.891	0.846
SVM	0.49	0.48	0.49	1.92	2	2.14
SVM-FSM	3	2.55	2	2.79	1.29	2.27

Table 8. THD (%), f_{sw} = 1500 Hz.

	SIMULATION			EXPERIMENTAL		
	R	**S**	**T**	**R**	**S**	**T**
PWM	0.68	0.68	0.68	0.74	1.01	0.68
SVM	0.49	0.48	0.49	1.3	1.31	1.37
SVM-FSM	3	2.55	2	2.06	2.27	1.63

Table 9 shows the efficiency results obtained in the laboratory implementations. As can be observed, SV-FSM has the highest efficiency compared with SVM and PWM. The efficiency levels are relatively low due the fact that our experimental setup was implemented with low power transfer. Under these conditions, the losses of the switches and other non-ideal components may be comparable to the levels of the power transfer, which derives from low efficiencies.

Table 9. Efficiency (%).

f_{sw} **(Hz)**	**PWM**	**SVM**	**SVM-FSM**
2000	32.97	37.81	37.95
1500	26.45	32.51	34.46

8. Conclusions

VSCs are one of the most commonly used components in electrical power systems. The performance of this type of system is highly influenced by the switching technique used. In this paper, a SVM based on a finite-state machine (SVM-FSM) has been proposed. The determination of the vectors through the modulation of time is based on simple concepts which are easy to understand and implement in current microcontrollers once a code optimisation is accomplished. The use of these devices provides the possibility of using this technique widely at a low cost. The proposed control technique fulfills two of the objectives of the study of the operation modes: lower THD and simplicity of implementation, that is, less computational time and memory required. In addition, a comparison between different techniques, such as PWM or SVM, was carried out to study the performance of each of them. The comparison entails simulation and experimental results. In this comparison, variables such as the load effective voltage and the harmonic distortion found in each solution have been analysed. In order to verify the feasibility of the proposed design, an analysis was carried out to ensure that the THD values found were within the range of values established as maximum values in the IEEE Std 519, with satisfactory results. The performance with changes on the grid features and goals has also been analysed. We could observe some transient effects of the non-linearity of our proposed method.

As future work, we will evaluate the feasibility of implementing this system in a renewable energy plant with an optimised coding that ensures equivalent performance parameters (mainly THD) for the three phases.

Author Contributions: Conceptualization, C.C.; methodology, C.C. and A.T.; software, C.C., I.C. and J.C.Q.; validation, A.T., J.C.Q., E.V. and J.A.A.; formal analysis, C.C. and A.T.; investigation, C.C. and A.T.; resources, I.C.; data curation, I.C.; writing—original draft preparation, C.C.; writing—review and editing, I.C., A.T., E.V. and J.A.A.; visualization, J.A.A.; supervision, J.A.A.; project administration, J.A.A.; funding acquisition, A.T. All authors have read and agreed to the published version of the manuscript.

Funding: Funding for this project was partially provided by the Spanish Ministerio de Ciencia e Innovacion (MICINN) project PID2019-110531-RA-I00/AEI/10.13039/501100011033 from the "Proyectos de I+D+i—RTI Tipo A" programme. This work was also partially supported by Junta de Andalucia (Spain) Project Ref: P20 01164.

Data Availability Statement: The data presented in this study are available on request from the corresponding author. The data are not publicly available due to privacy reasons.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

VSC	Voltage Source Converter
SVM	Space Vector Modulation
FSM	finite-state Machine
PWM	Pulse Width Modulation
THD	Total Harmonic Distortion

References

1. Lou, H.; Wang, X.; Sun, Y.; Mao, C.; Wang, D.; Dai, Y. Optimal Pulse Width Modulated STATCOMs in Photovoltaic Power Plants. In Proceedings of the 2020 IEEE Sustainable Power and Energy Conference (iSPEC), Chengdu, China, 23–25 November 2020; pp. 1899–1906. [CrossRef]
2. Contreras, C.; Triviño, A.; Aguado, J.A. Distributed Model Predictive Control for voltage coordination of large-scale wind power plants. *Int. J. Electr. Power Energy Syst.* **2022**, *143*, 108436. [CrossRef]
3. Azbe, V.; Mihalic, R. STATCOM control strategies in energy-function-based methods for the globally optimal control of renewable sources during transients. *Int. J. Electr. Power Energy Syst.* **2022**, *141*, 108145. [CrossRef]
4. Rashid, M.H. *Power Electronics: Devices Circuits and Applications*, 4th ed.; Pearson: New York, NY, USA, 2014.
5. Arranz-Gimon, A.; Zorita-Lamadrid, A.; Morinigo-Sotelo, D.; Duque-Perez, O. A Review of Total Harmonic Distortion Factors for the Measurement of Harmonic and Interharmonic Pollution in Modern Power Systems. *Energies* **2021**, *14*, 6467. [CrossRef]
6. Khalid, S.; Dwivedi, B. Power quality issues, problems, standards & their effects in industry with corrective means. *Int. J. Adv. Eng. Technol.* **2011**, *1*, 2231–19631.
7. Kazmierkowski, M.; Malinowski, M.; Bech, M. Pulse Width Modulation Techniques for Three-Phase Voltage Source Converters. In *Control in Power Electronics: Selected Problems*; Kazmierkowski, M.P., Krishnan, R., Blaabjerg, F., Eds.; Academic Press Series in Engineering; Academic Press: Cambridge, MA, USA, 2002.
8. Gaballah, M.M. Design and Implementation of Space Vector PWM Inverter Based on a Low Cost Microcontroller. *Arab. J. Sci. Eng.* **2012**, *38*, 3059–3070. [CrossRef]
9. Ghanmare, R.U.; Palpankar, P.M.; Dutta, A.A.; Damle, N.S. Microcontroller Based PWM Controlled Four Switch Three Phase Inverter Fed Induction Motor Drive. *Int. J. Recent Innov. Trends Comput. Commun.* **2015**, *3*, 195–204.
10. Dai, N.Y.; Lam, C.S.; Zhang, W. Multifunctional Voltage Source Inverter for Renewable Energy Integration and Power Quality Conditioning. *Sci. World J.* **2014**, *2014*, 421628. [CrossRef] [PubMed]
11. Jing, T.; Maklakov, A.S. A Review of Voltage Source Converters for Energy Applications. In Proceedings of the 2018 International Ural Conference on Green Energy (UralCon), Chelyabinsk, Russia, 4–6 October 2018; pp. 275–281. [CrossRef]
12. Tahir, S.; Wang, J.; Baloch, M.; Kaloi, G. Digital Control Techniques Based on Voltage Source Inverters in Renewable Energy Applications: A Review. *Electronics* **2018**, *7*, 18. [CrossRef]
13. Wu, Y.; Yin, S.; Li, H. Analytical Modeling of Switching Characteristics of the SiC MOSFET Based on finite-state Machine. In Proceedings of the 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, 15–19 March 2020; pp. 1956–1963. [CrossRef]
14. Wang, B.; Yu, J.; Yu, H.; Zhang, C.; Li, Z.; Yin, X.; Yan, H.; Shao, L.; Sun, X.; Wang, J. A Modeling Method for Si/SiC Hybrid Switch Based on finite-state Machine. In Proceedings of the 2021 IEEE 1st International Power Electronics and Application Symposium (PEAS), Shanghai, China, 13–15 November 2021; pp. 1–5. [CrossRef]
15. Wang, B.; Li, Z.; Bai, Z.; Krein, P.T.; Ma, H. Real-time diagnosis of multiple transistor open-circuit faults in a T-type inverter based on finite-state machine model. *CPSS Trans. Power Electron. Appl.* **2020**, *5*, 74–85. [CrossRef]
16. Mirebrahimi, S.N.; Merrikh-Bayat, F.; Taheri, A. Voltage-mode robust controller design for DC–DC boost converter at the presence of wide load and input voltage variations based on finite-state-machine model. *IET Power Electron.* **2018**, *11*, 866–875.
17. Contreras, C.; Triviño, A.; Aguado, J.A. Simpler STATCOM operation based on PWM with a finite-state machine. In Proceedings of the 2022 IEEE International Conference on Environment and Electrical Engineering and 2022 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I & CPS Europe), Salamanca, Spain, 5–7 September 2022; pp. 1–6. [CrossRef]
18. Torres, P.C.A.; Murillo, Y.D.; Restrepo Patiño, C. Diseño y construcción de un inversor trifásico. *Sci. Tech.* **2008**, *14*, 37–42.
19. Arun Shankar, V.; Umashankar, S.; Paramasivam, S.; Venkatesh, Y.; Venkatesh, K.; Dileep Sailesh, K. Mathematical modelling and investigation of reduced order induction motor drive system. In Proceedings of the 2017 Innovations in Power and Advanced Computing Technologies (i-PACT), Vellore, India, 21–22 April 2017; pp. 1–8. [CrossRef]
20. Tobar, A.N.S.J. Estudio del Inversor Multinivel Híbrido Simétrico como STACOM. Capítulo 3: Estrategia de Control. Bachelor's Thesis, Pontifia Universidad Católica de Valparaíso, Escuela de Ingeniería Eléctrica, Valparaíso, Chile, 2012.

21. Duan, R.; Yuan, L.; Gu, Q.; Zhao, Z. Finite-state-machine model of boundary control for dual-active-bridge converter. In Proceedings of the 2017 20th International Conference on Electrical Machines and Systems (ICEMS), Sydney, Australia, 11–14 August 2017; pp. 1–6. [CrossRef]
22. Pokharel, M.; Hildebrandt, N.; Ho, C.N.M.; He, Y. A Fast-Dynamic Unipolar Switching Control Scheme for Single-Phase Inverters in DC Microgrids. *IEEE Trans. Power Electron.* **2019**, *34*, 916–927. [CrossRef]
23. Noorsal, E.; Rongi, A.; Darus, R.; Kho, D.; Setumin, S. Design of FPGA-Based SHE and SPWM Digital Switching Controllers for 21-Level Cascaded H-Bridge Multilevel Inverter Model. *Micromachines* **2022**, *13*, 179. [CrossRef] [PubMed]
24. Bracinik, P.; Latkova, M. Modelling of a photovoltaic power plant with finite-state Machines. In Proceedings of the 2016 IEEE International Energy Conference (ENERGYCON), Leuven, Belgium, 4–8 April 2016; pp. 1–5. [CrossRef]
25. Pan, D.; Wang, X.; Liu, F.; Shi, R. Transient Stability of Voltage-Source Converters with Grid-Forming Control: A Design-Oriented Study. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 1019–1033. [CrossRef]
26. Xiao, D.; Alam, K.S.; Rahman, M.F. Predictive Duty Cycle Control for Four-Leg Inverters with *LC* Output Filter. *IEEE Trans. Ind. Electron.* **2021**, *68*, 4259–4268. [CrossRef]
27. Transmission and Distribution Committee of the IEEE Power Engineering Society and Static Power Converter Committee of the IEEE Industry Applications Society. *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*; IEEE: New York, NY, USA, 1993.
28. MATLAB. *MATLAB and Stateflow Model and Simulate Decision Logic Using State Machines and Flow Charts, Release 2022b*; The MathWorks Inc.: Natick, MA, USA, 2022.
29. González-González, J.M.; Triviño-Cabrera, A.; Aguado, J.A. Assessment of the Power Losses in a SAE J2954-Compliant Wireless Charger. *IEEE Access* **2022**, *10*, 54474–54483. [CrossRef]
30. Flota-Bañuelos, M.; Miranda-Vidales, H.; Fernández, B.; Ricalde, L.J.; Basam, A.; Medina, J. Harmonic Compensation via Grid-Tied Three-Phase Inverter with Variable Structure I&I Observer-Based Control Scheme. *Energies* **2022**, *15*, 6419. [CrossRef]
31. Hasan, I.J.; Salih, N.A.J.; Abdulkhaleq, N.I. Three-phase photovoltaic grid inverter system design based on PIC24FJ256GB110 for distributed generation. *Int. J. Power Electron. Drive Syst. (IJPEDS)* **2019**, *10*, 1215. [CrossRef]
32. Busacca, A.; Di Tommaso, A.O.; Miceli, R.; Nevoloso, C.; Schettino, G.; Scaglione, G.; Viola, F.; Colak, I. Switching Frequency Effects on the Efficiency and Harmonic Distortion in a Three-Phase Five-Level CHBMI Prototype with Multicarrier PWM Schemes: Experimental Analysis. *Energies* **2022**, *15*, 586. [CrossRef]